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Date : April 01, 2005

DESIGN OF AN INTERNAL CLOCK, A COINCIDENCE AND A SYNCHRONIZATION CIRCUIT

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This Report Is Submitted In Partial Fulfillment Of The Requirements For The Bachelor Degree of Electronic Engineering (Industrial Electronic)

Fakulti Kejuruteraan Elektronik dan Kejuruteraan Komputer
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"I hereby verify that this paper work is done on my own except for the references I made which I have stated the sources clearly on the specified section."

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Date : 1/4/2005

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ABSTRACT

The internal clock, coincidence and synchronization circuit will be combined together with other set of project to make into a main project known as 'Versatile Pulse Programmer' which produce the pulse sequence and a 'saturation burst' sequence which useful in the measurement of long relaxation time in solid. The internal clock will produce a symmetric square wave and impendence matcher to the other circuit which need it such as decade divider and synchronization circuit. It contains a 1MHz crystal oscillator, a Schmidt trigger with coupling and a emitter follower. The 1MHz crystal oscillator used to convert the DC input voltage to AC voltage and produce a stable output signal. This circuit also will converting sine wave signal which was produced from the oscillator circuit into square wave signal. The Schmidt trigger circuit will switches the negative output when the input passes upward through a positive reference voltage. At last emitter follower circuit will produce impendence matching to the remaining circuit. The coincidence circuit will be used to select the position of each of the three delayed pulses required ; W, the carr-purcell reset ; the delayed pulse in two pulse sequence ; and R, the reset pulse determining the repetition rate for all pulse sequence. The synchronization circuit will be used to remove timing errors that accumulated in the preceding circuitry The output 90 and 180 pulses are synchronized with time base clock.

ABSTRAK

Litar internal clock, litar coincidence dan litar synchronization akan digabungkan dengan satu set projek untuk dijadikan projek utama yang dikenali sebagai "Versatile Pulse Programmer" yang akan menghasilkan turutan denyut dan turutan 'saturation burst' yang digunakan dalam mengukur masa rehat yang panjang dan kukuh. Internal clock akan menghasilkan sebuah gelombang simetrik segi empat dan galangan (impendence) kepada litar yang memerlukannya seperti litar 'decade divider' dan litar 'synchronization'. Ia mengandungi pengayun kristal (1MHz), Picuan Schmidt dengan penjodoh serta pemancar sepunya. Pengayun krystal (1MHz) digunakan untuk mengubah voltan masukan AT kepada voltan AU dimana ia menghasilkan isyarat keluaran yang stabil. Litar ini juga akan menukar gelombang sinusoidal yang dihasilkan daripada litar pengayun kepada isyarat denyut. Litar picuan Schmidt akan menghasilkan keluaran negatif bila isyarat masukan merentasi voltan rujukan positif. Akhirnya litar pemancar sepunya akan menghasilkan galangan kepada litar seterusnya. Litar coincidence digunakan untuk memilih kedudukan 3 jenis denyutan 'delay' yang dikehendaki ; W, reset bagi carr-purcell ; denyutan 'delay' dalam dua turutan denyutan dan R, denyut reset yang menentukan pengulangan turutan denyut. Litar synchronization digunakan untuk menyingkirkan ralat masa yang dikumpul di dalam litar yang mendahului dengan output denyut 90° dan 180°. Seterusnya ia akan di 'synchronied' dengan berasaskan pada masa clock.

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CHAPTER I

INTRODUCTION

1.1 INTRODUCTION

It is about to design an internal clock, a coincidence and synchronization circuit. These circuits will be combined together with another set of project to make into a main project known as "Versatile Pulse Programmer for Pulsed Nuclear Magnetic Resonance Spectroscopy". For an internal clock, its use a 1MHz crystal oscillator, some resistors and transistor (2N2369 – medium speed TTL) to produce a symmetric square wave and impendence matching to the remaining circuit. A coincidence circuit used to select the position of the delayed pulses. It can be constructed with two NOR gates and one NAND gate. A synchronization circuit is used to remove timing error that will accumulate in the preceding circuitry the output 90^{o} and 180^{o} pulses. Later it will be synchronized with the time base circuit.

1.2 OBJECTIVES OF THE PROJECT

- To design an internal clock, a coincidence circuit and a synchronization circuit.
- To design an internal clock which produces a square wave and impendence matcher
- To design a coincidence circuit which use to select the position of delay pulse.
- To design a synchronization circuit which use to remove the timing error.

1.3 SCOPES OF THE PROJECT

- To design an internal clock to produce a square wave and impedance matching to the remaining circuit.
- To design a coincidence circuit to produce a selector of the position of delayed pulse.
- To design a synchronization circuit to produce a remover for the timing error.
- To combine all the 3 circuit with other circuit to build into a large system of pulse programmer.

1.4 OVERALL VIEW

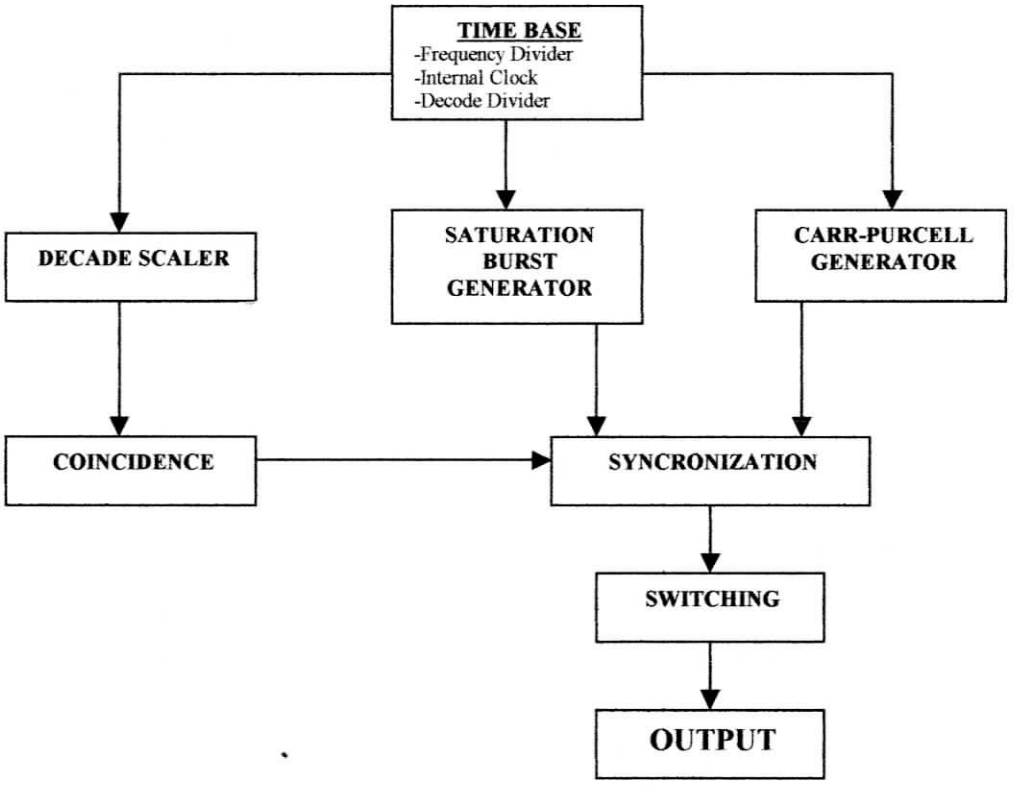

Figure 1.1 : Overall Diagram

Refer to the Figure 1.1 of the digital pulse programmer above, the time base separated into 3 groups which is Frequency Divider, Internal Clock and Decode Divider. The frequency divider will take appropriate division of the oscillator frequency of a coherent spectrometer to provide phase locking to the pulse programmer. The Frequency Divider can be substituted with an internal clock which produces a square wave and impendence matcher. The Decade Divider will receive the impendence matcher from the Internal Clock and provides frequency at decade interval from 1MHz to 1Hz to be separated to 3 different circuits. The circuits are Decade Scaler, Saturation burst and Car-Purcell. The Decade Scaler will provide 4 digit precision for each three delay pulse to the Coincidence Circuit which then used to select the position of each three delay pulse. The frequency from the Decade

Divider will be use in Saturation burst to produce a sequence of pulse to provide a pseudo-90° and in Carr-Purcell to produce carr-purcell sequence of 90° – t – 180° - 2t – 180° – 2t – 180°.....180° pulses. The output signal from the Coincidence, Saturation burst and Carr-Purcell will be produce to the Synchronization circuit to remove the timing error in each circuit. At last the digital pulse programmer will produce the standard pulse sequence and 'saturation burst' sequence required for pulsed nuclear magnetic resonance spectroscopy.

1.5 OVERVIEW OF THE REPORT

In the following subsequent chapters, a Versatile Pulse Programmer for pulsed nuclear magnetic resonance spectroscopy will be discussed in detail in Chapter 2. Chapter 3 deals of the methodology, in which a wide coverage will be given on hardware and software process while Chapter 4 will explain about the analysis and result that I get from this project. Finally Chapter 5 will explain about the conclusion of the overall project.

CHAPTER II

A VERSATILE PULSE PROGRAMMER

2.1 INTRODUCTION

The pulse programmer is capable of producing the standard pulse sequences required for pulsed nuclear magnetic resonance spectroscopy and may easily be modified to produce more specialized pulse sequences. Those provided are ; the two pulse sequences for 90°-90° or 180°-90° spin-lattice relaxation time T1 measurements with a 'saturation burst' sequence for measurements of long T1 in solids ; two pulse sequences for rotating frame spin-lattice relaxation time measurements ; and two pulse and multiple pulse sequences for spin-spin relaxation time T2 measurements.

An internal oscillator or a RF source of a coherent spectrometer (with suitable frequency division) can be use as a time base. Medium speed TTL integrated circuits (Table 2.1) are used throughout and the circuitry is fully synchronous with the time base, producing maximum pulse jitter of the order of 3 ns so that the programmer can be phase locked to the RF source. The output may be either positive or negative markers of 1μs duration and 4 V amplitude to provide triggers for the pulse length controls of the spectrometer.

Table 2.1 : Integrated Circuit used in Pulse Programmer

Type	Description
SN7402N	Quad 2-input positive NOR gate
SN7440N	Dual 4-input positive NAND gate
SN7441N	BCD-to-decimal decoder / driver
SN7442N	4-line to 10-line decoder
SN7474N	Dual D-type edge-triggered flip-flop
SN7409N	Decade counter

2.2 CIRCUIT DESCRIPTION

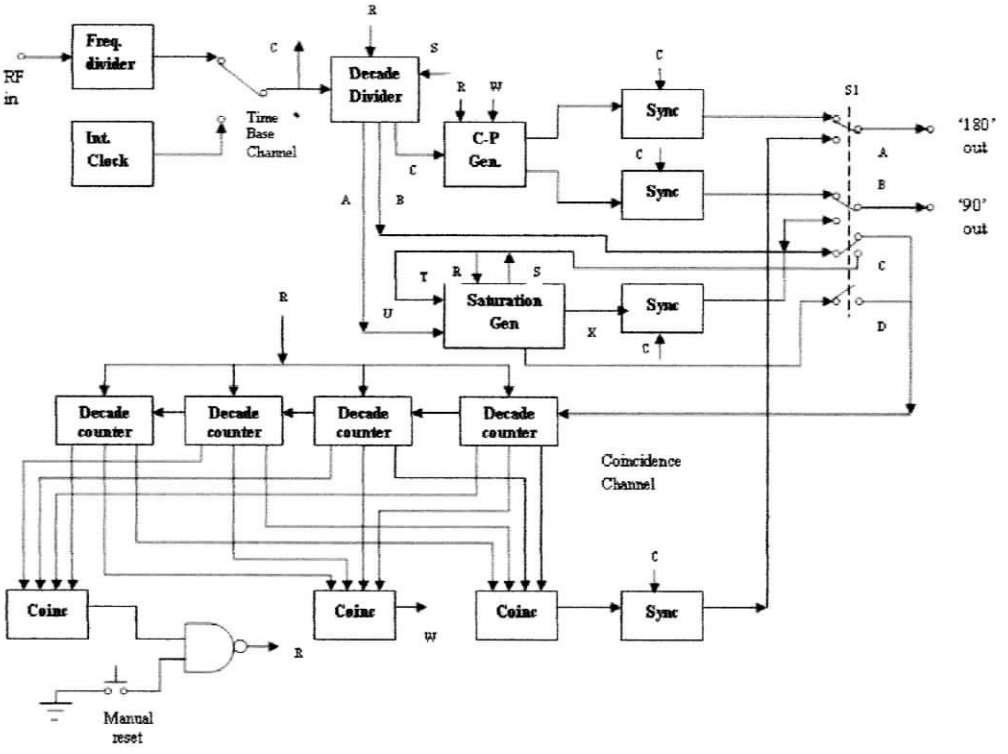

Figure 2.1 : Block diagram of the pulse programmer

The block diagram of the pulse programmer shown in (Figure 2.1) described and represent separate logical grouping of components as a guide to construction. This circuitry of the pulse programmer will be discussed in four segments; time base, four digit decade scaler, burst generators for the special pulse sequences, and coincidence and synchronization circuits.

2.2.1 Time Base

The time base consists of a frequency standard and a decade divider. The frequency standard may be taken as some appropriate division of the oscillator frequency of a coherent spectrometer to provide phase locking to the pulse programmer or an internal clock can be used.

The internal clock (Figure 2.2) contains a 1MHz crystal oscillator and a Schmidt trigger with coupling and divider resistors to produce a symmetric square wave. An emitter follower output circuit to provide the impendence matching to the remaining circuitry.

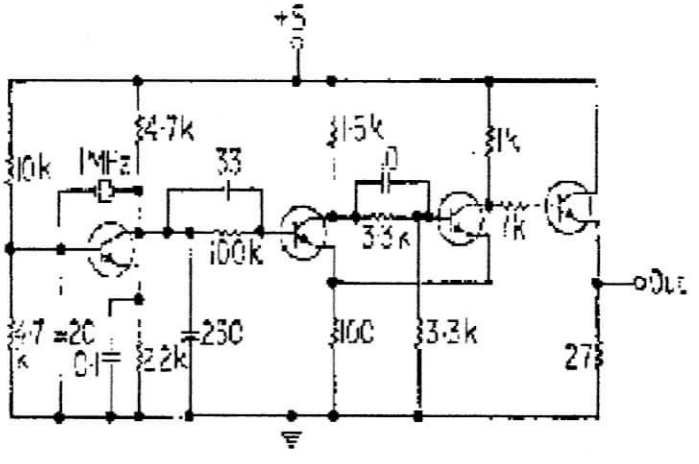

Figure 2.2 : Schematic diagram of the internal clock

Six SN7409N decade counters (Figure 2.3) wired as symmetric divide-by-ten counters and three independent switched outputs labeled, 'time base channel A, B and C', provide frequencies at decade intervals from 1MHz to 1Hz, inclusive. The decade divider is automatically reset to zero by coincidence circuit set to provide the desired repetition rate for the pulse sequence (input R) and by the saturation burst generator (input S) following a series of 90° pulses.

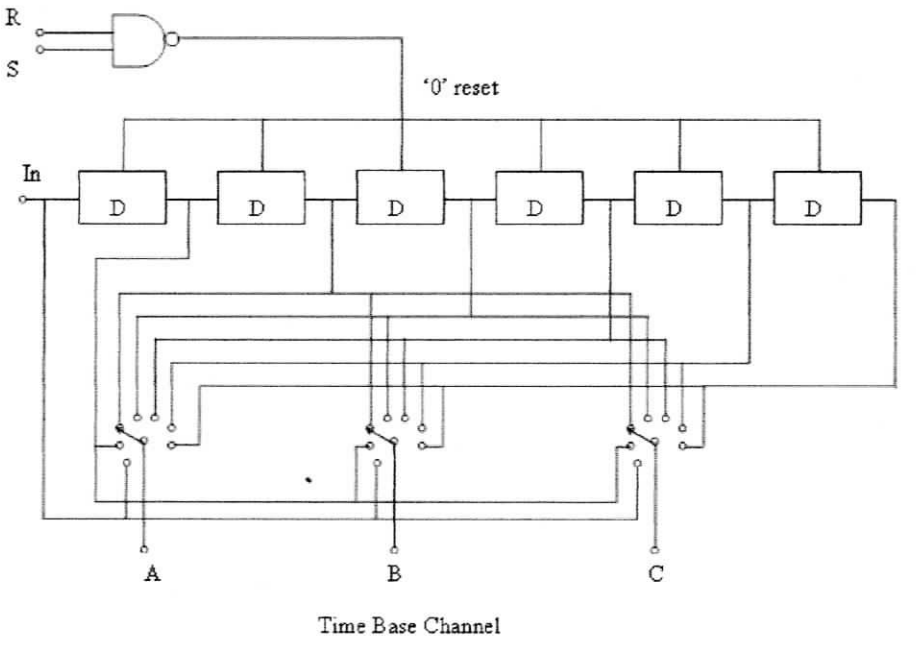

Figure 2.3 : Logic diagram of the decade divider

2.2.2 Decade Scaler

The decade scaler (Figure 2.4) contains four of the synchronous decade counters. An SN7490N decade counter wired as a binary coded decimal (BCD) counter is decoded to decimal output by an SN7442N four-line to 10-line decoder.

Visual display is provided by a Burroughs B5540 display tube driven by an SN7441AN decoder. The carry output of each decade counter is synchronized with its count input to minimize accumulated delays and allow independent resetting (input R) of the counters.

The leading edge of a negative-going output from the (BCD) decade decoder coincides with a trailing edge of the count input, as shown in Figure 2.9(c). The '9' output is inverted (Figure 2.9(d)) and applied to the D-input of an SN7474N edge triggered flip-flop. This flip-flop is clocked by the inverted count input (Figure 2.9(b)) to produce a carry pulse (Figure 2.9(e)) whose negative leading edge is synchronous with the trailing edge of the count input.

Independently adjustable delayed pulses are produced when coincidence occurs between the switch selected decimal outputs of each decade counter. Three such coincidence channels provide pulses for: resetting time base and decade scaler (coincidence channel A, output R in Figure 2.1) to enable selection of a variable repetition rate for the various pulse sequences; termination of the Carr-Purcell sequence (coincidence channel B, output W); and delayed pulse in two-pulse sequences (coincidence channel C). Four-digit ganged switches were used for each of the three coincidence channels for compact construction and ease of operation.

The use of four decade counters in the decade scaler provides four-digit precision for each of the three delayed pulses. The precision may be increased or decreased by using more or fewer decade counters.

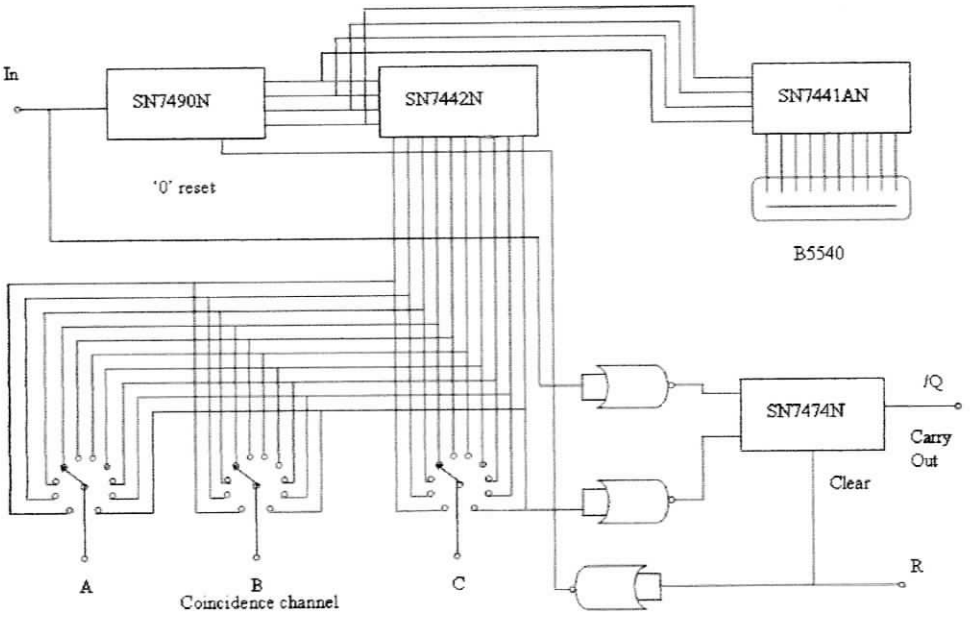

Figure 2.4 : Logic diagram of the decade counter

2.2.3 Burst Generators

2.2.3.1 Saturation burst generator

The saturation burst generator (Figure 2.5) produces a sequence of pulses to provide a pseudo-90° pulse useful for the measurement of long relaxation times in solids. This sequence consists of 1-9 pulses of equal separation t such that $T2 < t << T1$. During this sequence the input to the decade scaler is interrupted, and the time base is reset on the last pulse in the sequence. In this way, all delayed pulses following the pseudo-90° pulse occur at times measured from the beginning of the final pulse in the saturation burst, and no corrections for the finite extent of the sequence are required.

The pulse separation of the burst can be selected as a multiple of time base channel A which is input to U (Figures 2.1 and 2.6). This input frequency is divided by an SN7490N (BCD) counter and SN7442N decoder. Switch S2 determines the frequency division by resetting the counter when the desired divisor has been reached. The wiper of S2 also provides the pulses for the 90° saturation burst pulses at X and is input to a second (BCD) counter and decoder. When the number of 90° pulses selected on S3 has been reached the second counter resets, and the sequence is terminated. During this sequence, the time base (time base channel B) selected for the decade scaler is interrupted by an AND gate. This gate is formed with three NOR gates and is controlled by the $\bar{Q}$ output of an SN7474N flip-flop. When a reset pulse R resulting from the initiation of a new pulse sequence is applied to the preset input of the flip-flop, $\bar{Q}$ goes to a low level (0), and the decade scaler time base input at T is interrupted. When the last pulse in the sequence is detected at S and on the clear input of the flip-flop, $\bar{Q}$ is set to a high level (1), and the signal at T is passed to P and to the input of the decade scaler. The pulse at S also serves to reset the decade divider to zero, so that all subsequent delays are measured from the beginning of the final pulse in the saturation burst.

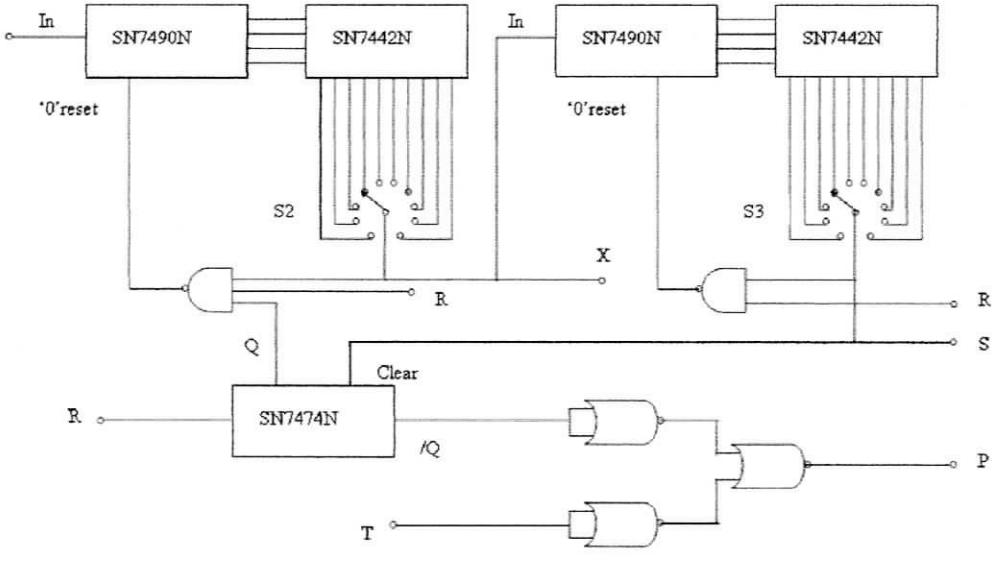

Figure 2.5 : Logic diagram of saturation burst generator