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VEHICLE PRE- EMPTIVE SYSTEM

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NOVEMBER 2005

NAD

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VEHICLE PRE-EMPTIVE SYSTEM


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**This Report Is Submitted In Partial Fulfillment of Requirements For
The Degree of Bachelor in Electrical Engineering (Industrial Power)**

**Faculty of Electrical Engineering
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November 2005

"I hereby declared that this report is a result of my own work except for the excerpts that have been cited clearly in the references."

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ABSTRAK

Teknologi hari ini memberikan kepelbagaian terhadap pelbagai jenis dan pilihan terhadap penghantar isyarat yang mampu untuk menghantar pelbagai bentuk isyarat. Tujuan utama adalah untuk mengaktifkan isyarat awal dan kemudiannya mengalami proses modulasi di dalam bentuk atau format yang betul. Walau bagaimanapun, terdapat spesifikasi spektrum frekuensi yang dibenarkan oleh Telekom Malaysia dalam merealisasikan projek ini. Sebaik sahaja frekuensi dikenalpasti, isyarat akan dijana pada tahap yang betul dan akan mengenyahkan segala bendasing yang tidak diperlukan dalam penghantaran isyarat. Pada tangga keluaran juga terdapat litar penyesuaian untuk memastikan terdapat galangan yang bersesuaian diantara pengawal lampu isyarat dan penghantar isyarat. Kemudian, kuasa maksimum akan berpindah. Sementara itu, penerima isyarat pula akan memainkan 2 fungsi utama. Operasi pertama akan menyingkirkan modulasi dari frekuensi isyarat radio. Selepas isyarat dikesan, maklumat dihantar kepada pengawal lampu isyarat dan system akan beroperasi dimana sedikit gangguan dan perubahan kecil berlaku terhadap aliran trafik. Kesimpulannya, apapun kegunaan terhadap penghantar isyarat ataupun penerima isyarat, konsep asas adalah sama. Bentuk blok serta spesifikasi yang sama digunakan. Oleh kerana faktor kesedaran, telah menjadi pendorong projek ini dijalankan. Dengan itu, projek yang dicadangkan ini diberi nama **Vehicle pre-emptive system**. Sistem ini menggunakan arahan microprocessor 68k untuk mengumpul data, memproses dan mengeluarkan hasil keluaran data. Keluarannya boleh dilihat pada perubahan system lampu isyarat. Kesimpulannya, projek ini memberi pelbagai impak berguna dan membantu dalam penyelesaian masalah trafik kepada semua pengguna jalan raya.

ABSTRACT

Nowadays, there is an enormous variety of different type of transmitters used to generate the signals that can be found in the radio spectrum. The purpose is to generate the basic signal or carrier and then superimpose the modulation onto it in the correct format. However, there are specifications of frequency spectrum that allowed by Telecom Malaysia. Once this is done, the signal is then amplified to the correct level and filtered to remove any spurious products that are outside the required band. The output stage may also include a simple conditioning circuit to ensure there is an accurate impedance matching between the traffic light controller and transmitter. Then, the maximum power transfer will happen. While that, for the receiver, it performs two mains functions. The first operation will remove the modulation from the radio frequency signal. After detection, it gives a signal and will interrupt the traffic light controller at frequencies that can be amplified by an audio frequency amplifier. The other thing is to provide selectivity. In this function is not performed well than a number of different stations will be received at one time making it very difficult to copy any of them. Whatever the use of transmitter or receiver, the fundamental concepts are the same and the same building blocks are use and the same specifications are applied. Carelessness is a main important point that leads to the creation of this project. To overcome this problem, a vehicle pre-emptive system is proposed. The system uses microprocessor 68k as a tool to collect input data, process and release output data. Otherwise the microprocessor will have an interfacing with the transmitter and also the receiver. As the result, the desired action will be done in the sequence of traffic light. This method is considered effective because it gives several benefits to the consumer. Overall, this project will resolve to be the solution to many problems occurred and could give convenient to the handicapped person.

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CHAPTER 1

INTRODUCTION

The integration of technology to the control system and wireless communication field continues to revolutionize the expectation of scientist as well as researches. Many developments had been carried out in the engineering industry in order to improve their way into current control system and wireless communication. This is a true phenomenon of current outcome in wireless communication.

With the ongoing consolidation of technology, there is an increasing desire of users to manage the operation of their appliances from a central location. The system would comprise a set of lights and a software package to configure them. Reliability and built in safety features would be a big issue to be examined. The central control console can be of particular use to those that are handicapped in their mobility. In addition, the dial in feature allows those far from the traffic light to control the lights sequence. Everyone is familiar with the concept of using a remote control for the TV. Now imagine a remote control that can also control lights, the temperature, drapes, the front door lock and in fact, virtually anything electrical. And further, imagine that this system is so easy to install and would not take too much long. Additionally this

system could be integrated to the traffic controller to transmit data to control the traffic sequence. With this remote control it can now interrupt the sequence of traffic lights to let the special vehicle to pass through the road during the congestive traffic situation. It produces many benefits to the consumer, including the person on duty such as policeman, the patient and others. It is very easy and more reliable.

From the phenomenon, we can clearly understand how the system goes actually. When a traffic light goes emergency usually an ambulance is stationed at the intersection of traffic jammed. Often in such cases the traffic flow will not be as smooth as a carefully thought-out robot system. One solution to the problem would be to have a portable set of traffic lights. The ambulance would have a remote system to interrupt the traffic light sequence based on the program setting on the traffic light. The portable lights would be changed from normal sequence to the emergency sequence. The portable lights could be configured to emulate the normal timing pattern for the intersection. Such a system would improve traffic flow and improve ambulance and other selective car personnel safety. The system could also be used to experiment with traffic flow and in situations where emergency is happened.

Traffic Signal Pre-emption is not a new idea. The technology was spawned several years ago in recognition of the increasing traffic congestion on roadways, particularly at intersections in metropolitan areas and busy thoroughfares in mid-sized and even smaller communities. The concept of Vehicle Pre-emptive system plays an important role in the planning of future traffic flow. In other country they have used this type of system where three means of signal preemption from emergency vehicles which is mobile radio, siren sensor, and modulated strobe light. Most of the systems operate with small transmitters that send *radio* waves or *infrared* signals that are received by other devices on or near the traffic lights. An additional signal light is placed nearby to warn motorists that an oncoming vehicle is preempting the signals.

1.1 OBJECTIVES OF THE PROJECT

This project focuses on the following six objectives:

1. To develop a program that can be a system to interrupt the traffic light sequence and control the light to give a priority to selective vehicle pass through.
2. To understand the traffic light sequence controller.
3. To study the schematic and function of microprocessor and how to apply into this project.
4. To interface the pre-emptive system with the existing traffic light controller.
5. To test the functional of the whole system.
6. To demonstrate the process running in the system built and the output result.

1.2 SCOPE OF THE PROJECT

1. Built a circuit for:
 - a. Condition circuit for interfacing part
2. Develop program for microprocessor (68000)
3. Simulate the program
4. Using the transmitter to transmit the signal
5. Demonstrate the output of project to the model.

1.3 Flight 68000 overview

This project uses the package of Flight Electronics Flight 68k. This package is designed to provide the perfect introduction to the world of 16/32 bit microprocessors by way of the very popular Motorola MC68000. The FLIGHT 68k is so simple and efficient design and very easy to use. It will enable the newcomer to the 68000 to quickly get to grips with the subject, leading him along in a clear and precise manner.

The FLIGHT 68K includes two serial ports and several 8-bit digital I/O ports and can grow still further and expand. This is ensured by the on board memory expansion capabilities and the external expansion bus. On board expansion consists of two free 32-pin sockets to which virtually any type of static byte wide memory may be fitted. "Careful attention has been paid to future trends in memory design to ensure that the FLIGHT 68K can take advantage of current and future memory technology [2]".

"Auxiliary RAM's can expand the RAM program capability of the system from 16k bytes to 512k bytes [2]". "An expansion bus expands all the 68000 signals to the outside world via a 64 way connector, allowing the user to easily expand the system, to peripherals of his own design [2]". This also makes the Flight 68K the ideal choice for a turnkey data acquisition or industrial process control system, with all the power of the 68000 available.

1.4 Hardware and Firmware features

The FLIGHT 68K is based around the full 16-bit bus version of the 68000 and contains two devices from the 68000 peripheral families. The MC68681 Dual Universal Asynchronous Receiver / Transmitter provides two RS232 compatible serial ports, one for communication with a PC/terminal, and the other for communication with either a host computer, or a printer for producing assembler listings or hard copy printout of debug sessions and others.

A 64k byte firmware package is provided with the FLIGHT 68K making on the board into a mini development system. It comprises comprehensive monitor, line by line assembler and disassembler. Demonstration programs for use with the Flight Multi-Applications Board and Test programs to ensure the board is fully functional.

The monitor program provided with the Flight 68k has been made as simple as possible to use. Each of the 53 different commands available is invoked by a simple two letter code, no further information has to be provided on the command invocation line. The monitor responds by asking for any further information that is required, in a clear and verbose manner. The monitor is used friendly and easy to use, and does not require many hours of learning before constructive use of the board can begin.

The line by line assembler will be invaluable to the user with just the FLIGHT 68k and a PC / terminal and no host development system. It accepts 68000 assembler language instructions and assembles them a line at a time, making program entry simple and quick. For demonstration and test programs it will even be found faster and more convenient than using a host computer will full cross software facilities. Using the assembler, 68000 machine code maybe disassembled from anywhere in memory. The assembler source code may be displayed, or printed out if a printer is connected.

1.5 Microprocessor – Flight 68K

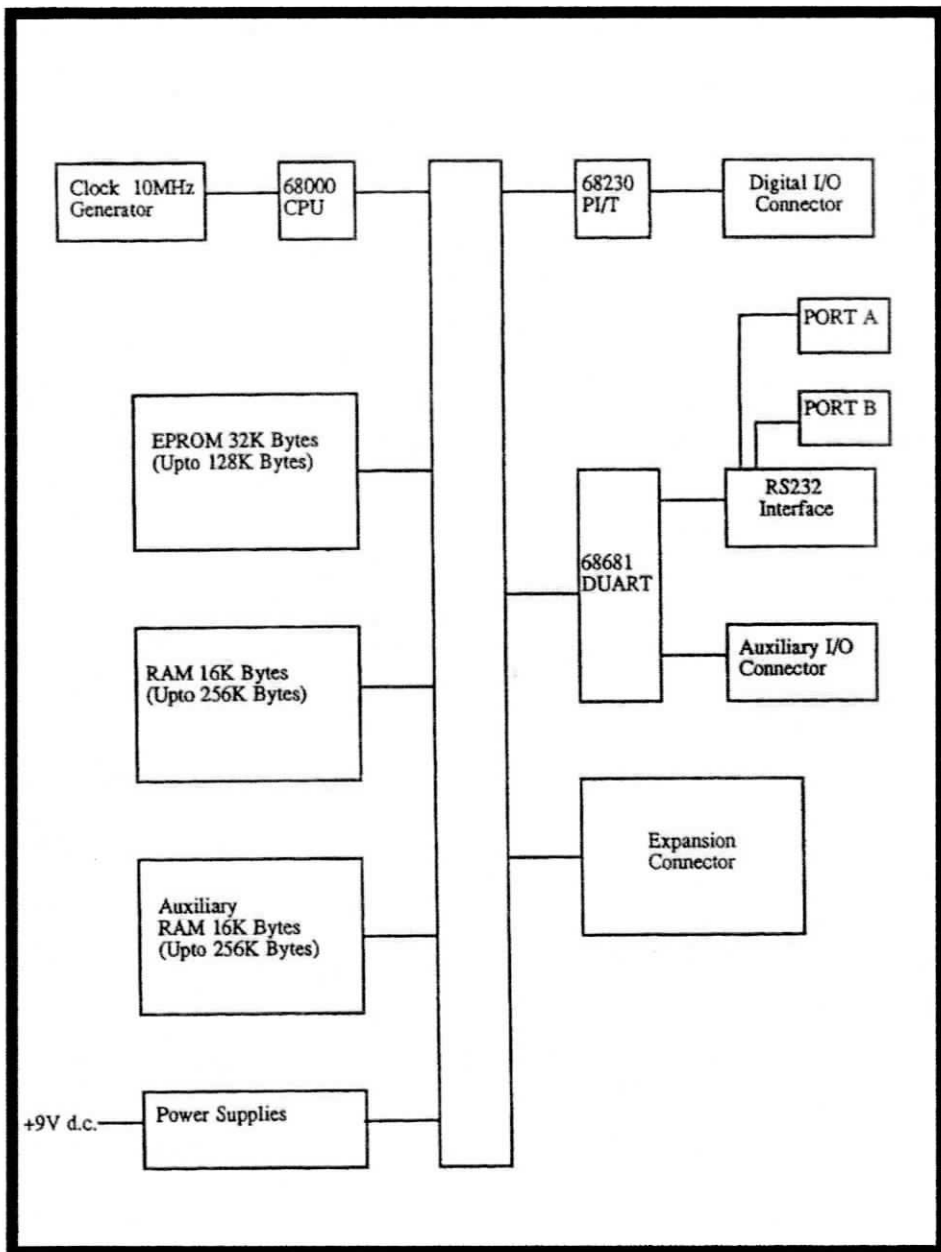


Figure 1.1: Block Diagram of the Flight 68K

“This part sets out to briefly describe the various elements which go to make up the Flight 68K board, what facilities are available, and what alterations can be made to suit a particular user’s needs [2]”.

What will be dealt with here are the various link areas on his board, denoted LK1 through to LK7 and how they altered, if required by the user. This part is very important in this project where the project point begin here. Let's see the details description for each block.

They are:

1. **68000 CPU:**

The heart of Flight 68k is the Motorola MC68000 Central Processing Unit. This unit has a 16 bit data bus and a 24 bit address bus which is capable of accessing a linear address space of 16 megabytes. As mention in the MK II manual, it is driven by a 10 MHz clock generated by a CMOS oscillator. A number of other TTL/CMOS chips surround the CPU to provide the necessary address decoding and other functions necessary to 'glue' the elements of the board together. The processor is reset automatically at power up, and may be subsequently be reset by pressing switch SW1. The MC 68000 processor is fitted as standard, but the MC 68010 which is pin compatible may also be fitted.

2. **EPROM Memory:**

The Flight 68K is fitted with two 27256 32k byte EPROM's which contain the 64k byte monitor firmware. These sockets can accept 27256 (32k) and 27512 (64k) EPROM's if the appropriate link is made on LK5.

3. **RAM Memory:**

Two 8k byte RAM memories are fitted to these sockets as delivered, giving a total of 16k bytes. The bottom 1k byte is used by the monitor firmware, but the rest is available to the user. This memory may be extended up to a total of 256k bytes. If further RAM memory is needed this may be fitted to the Auxiliary Memory sockets, the positions in the memory map being adjacent so that the two blocks of memory are contiguous.

APPENDIX B FLIGHT-68K MEMORY MAP	
Unused (Illegal Address)	FFFFFF
Ambiguous area DUART	A80000
	A7FFFF
DUART	A00020
	A0001F
Unused (Illegal Address)	A00000
	9FFFFFFF
Ambiguous area PI/T	880000
	87FFFF
PI/T	800040
	80003F
	800000
Unused (Illegal Address)	7FFFFFFF
	480000
Auxiliary Memory	47FFFF - 128K
	44FFFF - 32K
	443FFF - 8K
	device
RAM	440000
	43FFFF - 128K
	40FFFF - 32K
	403FFF - 8K
-----	400400
Reserved for Monitor	
Unused (Illegal Address)	400000
	3FFFFFFF
Ambiguous area EPROM	080000
	07FFFF
EPROM	020000
	01FFFF - 27512
	00FFFF - 27256
	007FFF - 27128
	device
	000000

Figure 1.2: Flight 68k Memory Map

4. Auxiliary Memory:

“These two sockets are blank when the Flight 68k is delivered and are for the user to expand the memory as desired [2]”. These sockets will accept static RAM. Link LK7 must be set to accommodate the particular size of memory it is desired to use.

5. **68230 Peripheral Interface / Timer (PI/T):**

From the FLT 68k manual, this LSI integrated circuit provides digital input / output interfacing as well as a timer functions. No functions on it are used by the monitor firmware, so it is freely available for the user. *All the I / O lines are brought out to connector P5, and the unit may be made to produce vectored interrupts to the processor by making the appropriate links on LK4.*

6. **68681 Dual Synchronous Receiver / Transmitter (DUART):**

As 68230, is another member of the 68000 peripherals family. *"It provides two serial interfaces, which are used by the monitor firmware for the two serial interfaces of the Flight 68 k, Port A (P2) and Port B (P3) [2]". "There are also a number of auxiliary input / output lines which are available to the user, brought out to connector P4, along with a counter / timer facility [2]". "This device too may generate vectored interrupts to the processor if linked in on LK4 [2]".* An on-chip clock controlled by a 3.6864 MHz crystal is used to derive the various baud rates available for the serial ports.

7. **Bus Expansion:**

As state in the manual, all 64 pins (with the exception of + 5v) of the 68000 CPU are extended via P1 to the outside world for the users convenience, either to monitor signals, or for connecting additional memory or peripherals, designed by the user.

8. **Power Supplies:**

The Flight 68k only requires a single 9 volt unregulated supply to operate, which normally be provided by the mains adaptor supplied with the board. The board itself requires voltage of +5v, +12v, and -12v. These are all derived from the 9 volt input. The +5v being obtained by regulating the input supply, and the 12v supplies, which are only used for the RS232 serial ports are then derived internally within the RS232 driver devices. The +5v supply can also be used externally via P7, to power a peripheral card but the 12v supplies are not available to power the bus.

9. **Memory Map:**

As in figure 1.2, each of the address elements on the board is assigned a 2M byte block in the map. This is far greater than is required by any device, except expanded memory but makes for simple address decoding circuitry and ensures there is no limit as far as the address decoding circuitry is concerned to the size of memory that can be fitted. Memory is further broken down into 512K blocks, to aid the addition of external memory without conflict.

10. **Link Areas:**

There are seven link areas on the Flight 68k board which allow certain configurations of the board to be altered. None of these needs to be attended to in order to get the board working, where links are necessary then they are made at time of manufacture with push on jumpers. Only when a user is confident enough to be involved with more advanced applications is it likely that alterations of some of these link areas may be necessary.

11. **LK 5, 6, 7 – Memory Type Configuration:**

- a) LK 5 – allows different types of memory to fit to the EPROM sockets.
- b) LK 6 – allows different types of memory to be fitted to the main RAM sockets.
- c) LK 7 – allows different types of memory to be fitted to the auxiliary RAM sockets.

At the time of manufacture links are fitted for

IC 2 / IC 3 EPROM 32k x 8 (27256)

IC 4 / IC 5 RAM 8k x 8 (6264)

IC 6 / IC 7 RAM 8k x 8 (6264)

This may be altered if desired by repositioning the push on jumpers as appropriate on LK 5, LK 6 and LK 7. Table 1.1 tabulates all the various memory types that may be fitted and the appropriate links to be made. With time of course new devices become available which may not be listed here, but reference to the Flight 68k circuit diagram and the device manufacture's data sheet should resolve how to connect in

the new device. All memory device fitted to the board must have a cycle time of 200nS or less.

Table 1.1: Link Area – LK 5, LK 6 and LK 7

	IC2/3 Monitor EPROM LINK 5	IC4/5 System/User RAM LINK 6	IC6/7 Auxiliary RAM LINK 7
RAMS			
6264 (8k)	-----	2-3	2-3
62256 (32k)	-----	2-1	2-1
551001 (128k)	-----	2-1	2-1
EPROMS			
27128 (16k)	2-3	-----	-----
27256 (32k)	2-3	-----	-----
27512 (64k)	2-1	-----	-----

12. LK 2, LK 3 – Serial Port Configuration:

The two serial port link areas, LK 2 for Port A and LK 3 for Port B are preset with track links. The RS232 ports on the Flight 68k have patching areas, LK2 for the terminal and LK3 for the host computer / printer. These are there to accommodate the various versions of RS232 interconnection that exist, but track links across LK2 and LK3 set the board at manufacture to work with most common terminals

13. LK 4 – Interrupt Selection:

This link area is used to direct interrupts and their respective acknowledge signal (IACK x) from/to the PI/T or DUART, or for use externally to the board. There are no preset links on this link area, and so if interrupts are required, then the appropriate links must be made. For instance, to enable interrupt INT1* from the peripheral side of the PI/T, connect LK 4 pin 18 (PC5/PIRQ) to pin & (INT1*) to direct interrupt, and connect pin 19 (PC6/PIACK) to pin 14 (IACK1*) to direct the acknowledge signal.