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Lot testing scheduling system for infineon / Lew Mei Yee.

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JUDUL: **LOT TESTING SCHEDULING SYSTEM FOR INFINEON**

SESI PENGAJIAN: **2006**

Saya LEW MEI YEE
(HURUF BESAR)

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^ Tesis dimaksudkan sebagai Laporan Projek Sarjana Muda (PSM)

LOT TESTING SCHEDULING SYSTEM FOR INFINEON

LEW MEI YEE

**This report is submitted in partial fulfillment of the requirement for the
Bachelor of Computer Science (Software Development)**

**FACULTY OF INFORMATION AND COMMUNICATIONS TECHNOLOGY
KOLEJ UNIVERSITI TEKNIKAL KEBANGSAAN MALAYSIA
2006**

ADMISSION

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(LEW MEI YEE)

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(ZERATUL IZZAH BINTI MOHD YUSOH)

DEDICATION

Specially dedicated to

My beloved Dad, Mum, brothers and sisters who have encourage, guided, helped and inspired me throughout the journey of success.

ACKNOWLEDGEMENT

The completion of this Projek Sarjana Muda (PSM) report is successfully done as a result of the contribution of many parties. Here I would like to express my greatest gratitude to those who had helped me, directly or indirectly, in accomplishing this report.

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Last but not least I wish to thank all my course mate and friends from KUTKM and also others that may not have been mentioned here. Without any of these supports, I would not have completed my final project successfully.

ABSTRACT

The project is known as Lot Testing Scheduling System for Infineon (LTSS). This software project is purposely developed to help Module Assembly and Test department of Qimonda, Infineon for schedule testing lot of production line. LTSS assists APT production line to work productively. The testing lot will moved to APT after completed Advantest, so LTSS responsible to plan the start lot time and cluster (tester) will used for testing. Firstly, LTSS can estimate the expected finish time of active lot at APT. Secondly, LTSS calculate the expected start time and expected finish time of waiting lot. At the same time, LTSS plan appropriate cluster for the waiting lots. In doing these modules, the measurements such as operation, module type, number of mother boards, and testing flow need to be count on. This software project is developed by using MS Visual Basic version 6 and MS Access for database. The methodology being applied in the system is Rational Unified Process (RUP). The reasons for the proven framework RUP being chosen because needs to work with the users of Infineon to explore their requirements and refining these through many versions until an adequate system has been developed.

ABSTRAK

Projek ini dikenali sebagai *Lot Testing Scheduling System for Infineon (LTSS)*. Projek ini dibangunkan bertujuan untuk membantu *Module Test and Assembly Department* di *Qimonda, Infineon* menjadualkan lot ujian di baris pengeluaran. *LTSS* dapat membantu baris pengeluaran iaitu *Application Test (APT)* untuk meningkatkan produktiviti. Lot diuji akan dipindahkan ke *APT* apabila lot tersebut sudah habis diuji di *Advantest*, oleh itu *LTSS* bertanggungjawab untuk menjadualkan masa bermula dan perkakas ujian yang akan diguna. Pertama, *LTSS* boleh menjangka masa tamat uji untuk lot yang aktif di *APT*. Kedua, *LTSS* juga menjangka masa mula dan masa tamat bagi lot yang sedang menunggu di *APT*. Pada masa yang sama, *LTSS* merancang perkakas ujian untuk lot yang sedang menunggu di *APT*. Dalam membuat modul-modul tersebut, ukuran-ukuran untuk proses pengujian seperti operasi, jenis modul, bilangan *motherboard* dan juga cara pengujian perlu diambil kira. Projek perisian ini dibangunkan dengan menggunakan *MS Visual Basic Version 6* dan kombinasi *MS Access* untuk pangkalan data. Metodologi yang digunakan dalam sistem ini ialah *Rational Unified Process (RUP)*. *RUP* dipilih disebabkan sistem ini perlu bekerja dengan pihak pengguna Infineon sepanjang masa sistem dibangunkan untuk mendedah permintaan pengguna bersama dan seterusnya menghasilkan sistem sehingga versi yang sesuai.

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LIST OF ABBREVIATIONS

PSM	Project Sarjana Muda.
LTSS	Lot Testing Scheduling System for Infineon
VB6	Microsoft Visual Basic version 6
APT	Application Test
RAM	Random Access Memory
GUI	Graphical User Interface
OOAD	Object-oriented Analysis and Design
RUP	Rational Unified Process
FIFO	First Come First Out
LIFO	Last In First Out
TCP/ IP	Transfer Control Protocol/ Internet Protocol
SQL	Structure Query Language
KUTKM	Kolej Universiti Teknikal Kebangsaan Malaysia
UT	Unit test
MT	Module test
SIT	System Integration Test
V1.0	Version 1.0
UML	Unified Modeling Language

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CHAPTER I

INTRODUCTION

1.1 Project Background

Infineon Technologies (Malaysia) Sdn. Bhd. is one of the largest semiconductor manufacturers in Melaka. Their products are DRAM, Small Signal Devices, Power Products and Logic Products. Qimonda is one of the main companies of Infineon Technologies, it focused on the production of memory products such as DRAM and SDRAM chips. Module Test and Assembly Department is the testing department for Qimonda, it responsible to test the memory RAM before delivery.

The proposed system is developed for Module Test and Assembly Department. The system is known as Lot Testing Scheduling System for Infineon (LTSS). It is a scheduling system that enables to assist production planner to assign starting time and machine to test the memory product.

The memory RAM which tested in production line is called modules. Advantest is a production line for writing data into modules by machines. Once the modules completed Advantest, the modules is collected and placed as a lot. The lot of modules waits to send to Application Test (APT) production line for test a module whether is in good or defective condition. The waiting lot is in status "Wait for APT".

When a lot moved to APT, production planner needs to assign a lot test at appropriate tester which called cluster. Cluster is formed by four racks of mother boards, there are 60 of mother boards for one cluster.

There are 20 clusters at APT which controlled by servers. Different clusters support different of module types of modules. There are many module types of modules, a module type can has more than one supported cluster. So production planner needs a scheduling system to assist them to predict what lot can be moved at a time, what time a lot can be finished and what time a lot can be moved.

1.2 Problem Statements

A few problems found at production line APT during lot movement and scheduling activities (equipment or time) as mention as following.

In manufacturing, there is wide variety of products, process and production levels, it is very hard for production planner to coordinate and schedule production activities. Therefore, production planner takes time for decision making especially for new employees. New employee needs to undergo training and learn to work tightly with another production line.

Another problem is resource allocation is not productive since it is a complicated task at production line. Production planner needs to assign resources (equipment or time) to job, count on prioritizing jobs that require same resource and determine when a job should be started based on their experience and knowledge.

The testing process will be delayed if production planner takes long time to assign lot "Wait for APT". "Wait for APT" is status where the lot is waiting to be assigned a machine for testing.

1.3 Objectives

Several objectives were set to be achieved for the successful implementation of LTSS. These objectives were summarized as following:

- To produce auto scheduling time table to assist production planner.
- To smooth whole process of lot movement.
- To help production planner in decision making.
- To increase productivity and to reduce operating time.

1.4 Scope

Before the construction of the system commence, the scope of the project has to be determine in order to create the boundary of the system. This will keep the development of the system within a manageable scope. The scope is divided into 3 parts, which are functions, users and platform.

The LTSS consists of several main functions that make up the solutions for production planners. These functions are as described as following:

- i. Define supported testers (cluster) for each module type of memory product.
- ii. Calculate expected finish time of active lot at APT.
- iii. Calculate expected start time and expected finish time of lot at Wait for APT.
- iv. Plan tester (cluster) for each lot of Wait for APT before testing.

The target users for LTSS are the administrator, engineers and production planners of Module Test and Assembly Department, Qimonda, Infineon Technology. LTSS mainly assist APT for purpose schedule lot testing.

While the platform used is Window, Window MS Window 2000 Professional and MS Windows XP Professional are recommended. This is because current