DESIGN AND CHARACTERIZATION OF VERTICAL MOSFET

NUR ASIMA BINTI MOHAMMAD NASIR

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ZUL ATFYI FAUZAN BIN MOHAMMED NAPIAH
Lecturer
Faculty of Electronic and Computer Engineering,
Universiti Teknikal Malaysia Melaka,
Hang Tuah Jaya,
76100 Durian Tunggal, Melaka

Tarikh: 15th JUNE 2012 Tarikh: 15th JUNE 2012

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Author : NUR ASIMA BINTI MOHAMMAD NASIR

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Supervisor's Name : ZUL ATFYI FAUZAN BIN MOHAMMED NAPIAH

Date : 15th JUNE 2012

Dedicated to my beloved family

To my father and mother

To my respected lecturer/supervisor

And to all my friends

For their support, advice, patience and understanding.

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ABSTRACT

Vertical MOSFET is a device structure that considered overcoming the Short Channel Effects (SCEs) in nanometer scale device structure. In this research, the comparison between Drain-On-Top (DOT) and Source-On-Top (SOT) of Double Gate Vertical MOSFET were developed by using the SILVACO TCAD tools for several channel length (L_g) of 50, 70, 90, 130, and 180 nm respectively. The performance of the Double Gate Vertical MOSFET was analyzed by using process and device simulation which are DevEdit, ATHENA and ATLAS tools respectively. The electrical characteristics for proposed devices have been analyzed based on different channel length and the results are as shown in the I-V curve. The physical parameters extracted from the I-V curve are the threshold voltage (V_T), leakage current (I_{OFF}), active current (I_{ON}), Drain Induced Barrier Lowering (DIBL) and sub-threshold swing. From the analysis, Drain-On-Top structure is more practically better compared to Source-On-Top due to their electrical characteristic.

ABSTRAK

MOSFET Menegak adalah satu struktur peranti elektronik yang dipertimbangkan untuk mengatasi Kesan Saluran Pendek (SCEs) dalam struktur peranti berskala nanometer. Dalam kajian ini, perbandingan antara Saliran-Di-Atas (DOT) dan Sumber-Di-Atas (SOT) bagi MOSFET Menegak Get Duaan dilakukan dengan menggunakan perisian SILVACO TCAD untuk beberapa panjang saluran (L_g) iaitu 50, 70, 90, 130, dan 180 nm masing-masing. Prestasi MOSFET Menegak Get Duaan telah dianalisa dengan menggunakan simulasi proses dan peranti iaitu DevEdit, ATHENA dan ATLAS masing-masing. Ciri-ciri elektrikal untuk peranti yang diusulkan telah dikaji berdasarkan panjang saluran yang berbeza dan hasil kajian adalah seperti yang ditunjukkan di dalam graf arus-voltan. Parameter fizikal yang diekstrak dari graf arus-voltan ambang (V_T), arus bocor (I_{OFF}), arus aktif (I_{ON}), *Drain Induced Barrier Lowering* (DIBL) dan ayunan separa ambang. Daripada semua analisa yang telah dilakukan, struktur Saliran-Di-Atas terbukti lebih praktikal jika dibandingkan dengan struktur Sumber-Di-Atas berdasarkan ciri-ciri elektrikal kedua-dua peranti.

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LIST OF ABBREVIATIONS

AC	-	Alternating Current
DC	-	Direct Current
DIBL	-	Drain Induced Barrier Lowering
DOT	-	Drain-On-Top
FET	-	Field Effect Transistor
IC	-	Integrated Circuit
I_D	-	Drain Current
I_{OFF}	-	Leakage Current
I_{ON}	-	Active Current
L_g	-	Channel Length
MOSFET	-	Metal-Oxide Semiconductor Field Effect Transistor
N_{sub}	-	Substrate Thickness
SCEs	-	Short Channel Effects
SOT	-	Source-On-Top
TCAD	-	Technology Computer Aided Design
t_{ox}	-	Oxide Thickness
V_{DS}	-	Drain-Source Voltage
V_{GS}	-	Gate-Source Voltage
V_T	-	Threshold Voltage
VWF	-	Virtual Wafer Fab

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CHAPTER 1

INTRODUCTION

1.1 Background

The Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET) is largely regarded as a popular device and is extensively used in digital circuits, microprocessors, memory circuit, and other logic applications of many kinds. This is due to the MOSFET ability to act as an efficient switch that practically consumes no current at the gate and the channel conductivity dependents only on the potentials at the gate. The relatively small size of the MOSFET causes thousands of devices that can be fabricated into a single integrated circuit design is another advantage to the electronic industry [1].

It is impossible to be engaged in the semiconductor industry without encountering frequent references to Moore's Law. In 1965, Gordon Moore, co-founder and chairman Emeritus of Intel Corporation, made the observation that the number of transistors per integrated circuit (IC) were growing at an exponential rate and predicted that this trend would continue. Since that time, the industry has an accomplished the exceptional feat of producing semiconductor devices with twice as many transistors as the prior generation every 18-24 months. Consumers and businesses alike have reaped tremendous benefits from the electronics technology, and semiconductors is the heart of it all [4].

Nowadays, research is focused on obtaining higher speeds, low power consumption, and low cost devices. Marketing leaders are very keen on inventing a new generation of MOSFET technologies to continue their dominating position [4]. Due to physical device fabrication limitations and short channel effects, the future of MOSFET relies on the evaluation of new techniques like Vertical MOSFET and Double Gate MOSFET.

1.2 Problem Statement

An integrated circuit (IC) is a minuscule electronic circuit that consists of active and passive components as well as interconnection. These components include transistor, diode, capacitor, and resistor. The IC is based mainly on the transistor. The transistor, a semiconductor device was developed as an alternative to the old vacuum tube.

Since the transistor could be made much smaller, it was much more convenient to use. As a result, the transistor became the main amplifying device in

almost all electronic equipment. The recent development of MOSFET has reached the progress that the channel length goes shorter into nanometer scale.

While the MOSFET undergoes scaling down of the size in order to improve integrated circuit performance such as speed, power consumption and packing density, a number of challenges need to be overcome.

1.3 Objectives

The objectives of this project are:

(i) To be familiarize with SILVACO TCAD tools.
(ii) To design and characterize the Vertical MOSFET (Metal-Oxide-Semiconductor Field Effect Transistor).
(iii) To compare the performance of Vertical MOSFET and other relevant device structure.

1.4 Scope of Project

The scope of this project presents an overview of the performances on Double Gate Vertical MOSFET by using process and device simulation using DevEdit, ATHENA and ATLAS tools respectively. The proposed device structures were designed by using DevEdit and ATHENA tools.

1.4.1 Introduction to TCAD

TCAD stands for Technology Computer Aided Design, which is not that self-explanatory. What it really refers to is computer programs able to simulate either the workings of a semiconductor device (device simulation) or the fabrication process of a semiconductor device (process simulation). Often the result of a process simulation, which is called a "mesh" or "grid", is fed into a device simulator to evaluate the performance or the behavior of the device that has been "virtually fabricated". Simulations are very inexpensive and fast compared to actual prototype fabrication. They are also an excellent tool to understand semiconductor physics.

1.4.1 DevEdit

DevEdit can be used to either create a device from scratch or to re-mesh or edit an existing device. DevEdit creates standard SILVACO structures that are easily integrated into SILVACO 2D or 3D simulators and other support tools.

1.4.2 ATHENA

ATHENA provides a convenient platform for simulating processes used in semiconductor industry such as ion implantation, diffusion, oxidation, physical etching and deposition, lithography, stress formation and silicidation.

1.4.3 ATLAS

ATLAS enables device technology engineers to simulate the electrical, optical and thermal behavior of semiconductor devices. ATLAS provides a physics-

based, easy to use, modular and extensible platform to analyze DC, AC and time domain responses for all semiconductor based technologies in 2 and 3 dimensions.

1.5 Methodology

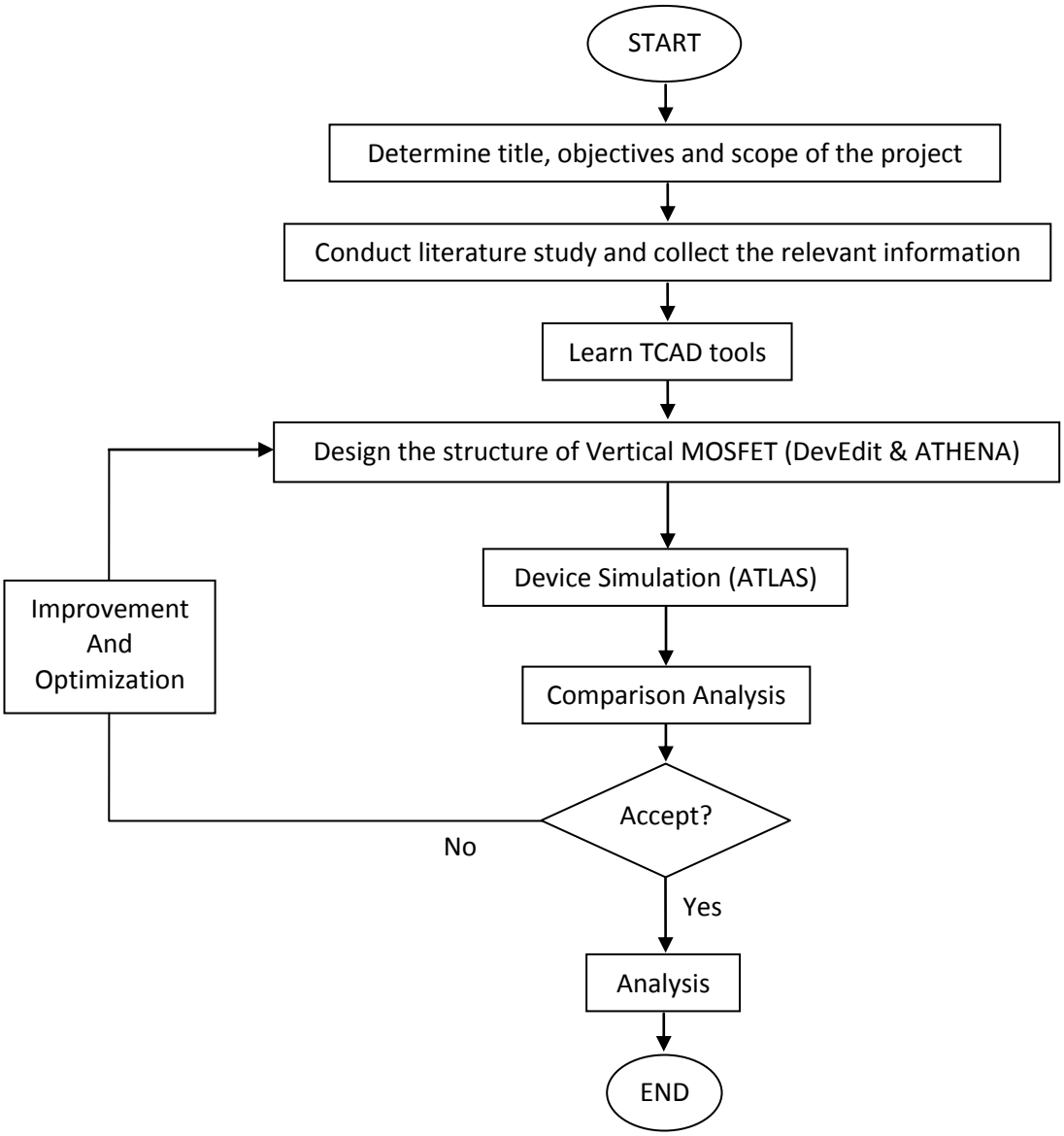

Figure 1.1: Flow Chart of the Project

1.6 Project Structure Overview

This thesis consists of five chapters. The first chapter provides an introduction to this project. This includes the objectives and importance of this project. The second chapter contains theories and information about other relevant researchers conducted by research institutes and universities around the world.

The research activities and methods employed in this project will be discussed in detail in Chapter 3. This chapter shows the flow of this project from the very beginning of the data collection until the acceptable results. It also introduced the TCAD tools used in this project. Step by step explanations on the development of the Vertical MOSFET are provided for extra information and knowledge.

Chapter four will discuss about the result obtained from the process simulation using ATLAS tools. The data and results from the process are analyzed and discussed in this chapter. The effect of the tested parameters is discussed and opinions are brought forward in this chapter. Comparison between the Drain-On-Top (DOT) and Source-On-Top (SOT) structure are also discussed.

Finally, the last chapter will be the conclusion and incorporates the overview of the results and recommendation for this project. This chapter compares the results analysis with the objectives of this research in order to determine the achievement of this research.

CHAPTER 2

LITERATURE REVIEW

This chapter provides an introduction to MOSFET inclusive of an overall view of the past and current technology revolving around it. Backgrounds of the planar MOSFET to the novel device of Double Gate Vertical MOSFET were illustrated in this chapter. The previous research paper that had been selected to be the key papers was also discussed in this chapter.

2.1 Planar MOSFET

The conventional MOSFET or as known as the normal planar MOSFET has a source and a drain area divided by the channel area as shown in Figure 2.1. Its contacts are symmetric [3].