

**THE DESIGN AND IMPLEMENTATION OF VGA CONTROLLER ON FPGA**

**WOON WOEI KEAT**

**This Report is Submitted in Partial Fulfillment of Requirements for the Bachelor  
Degree of Electronic Engineering (Computer Engineering)**

**Fakulti Kejuruteraan Elektronik dan Kejuruteraan Komputer  
Universiti Teknikal Malaysia Melaka**

**June 2012**



UNIVERSITI TEKNIKAL MALAYSIA MELAKA  
FAKULTI KEJURUTERAAN ELEKTRONIK DAN KEJURUTERAAN KOMPUTER

BORANG PENGESAHAN STATUS LAPORAN  
PROJEK SARJANA MUDA II

Tajuk Projek : THE DESIGN AND IMPLEMENTATION OF VGA CONTROLLER ON FPGA

Sesi Pengajian : 

1	1	/	1	2
---	---	---	---	---

Saya ..... WOON WOEI KEAT  
(HURUF BESAR)

mengaku membenarkan Laporan Projek Sarjana Muda ini disimpan di Perpustakaan dengan syarat-syarat kegunaan seperti berikut:

1. Laporan adalah hakmilik Universiti Teknikal Malaysia Melaka.
2. Perpustakaan dibenarkan membuat salinan untuk tujuan pengajian sahaja.
3. Perpustakaan dibenarkan membuat salinan laporan ini sebagai bahan pertukaran antara institusi pengajian tinggi.
4. Sila tandakan (  $\checkmark$  ) :

SULIT\*

\*(Mengandungi maklumat yang berdarjah keselamatan atau kepentingan Malaysia seperti yang termaktub di dalam AKTA RAHSIA RASMI 1972)

TERHAD\*\*

\*\* (Mengandungi maklumat terhad yang telah ditentukan oleh organisasi/badan di mana penyelidikan dijalankan)

TIDAK TERHAD

Disahkan oleh:

(TANDATANGAN PENULIS)

(COP DAN TANDATANGAN PENYELIA)


**Razi Husin Bin Ramlee**  
Pensyarah

Fakulti Kejuruteraan Elektronik Dan Kejuruteraan Komputer  
Universiti Teknikal Malaysia Melaka (UTeM)  
Hang Tuah Jaya, 76100 Durian Tunggal, Melaka

Tarikh: 15.06.2012

Tarikh: 15/6/2012


“Saya akui laporan ini adalah hasil kerja saya sendiri kecuali ringkasan dan petikan yang tiap-tiap satunya telah saya jelaskan sumbernya.”

Tandatangan :  .....

Nama Penulis : WOON WOEI KEAT .....

Tarikh : 14.06.2012 .....

“Saya/kami akui bahawa saya telah membaca karya ini pada pandangan saya/kami karya ini adalah memadai dari skop dan kualiti untuk tujuan penganugerahan Ijazah Sarjana Muda Kejuruteraan Elektronik (Kejuruteraan Komputer).”

Tandatangan :   
Nama Penyelia : Razi Hussin Ramlee  
Tarikh : 15/6/2012

## ACKNOWLEDGEMENT

First, I would like to thank Mr. Radi Husin Bin Ramlee who was giving me a chance to be a final year project student of him; guiding me within the whole flow of my final year project; and sharing knowledge those are very useful for helping me to solve the problems faced within period of doing the project. The experiences and knowledge gained will also be a very useful references and tools in my future studies or work. I really appreciate all the things that I had learnt in this whole year on my final year project, the writing skills practiced on writing thesis of project and experiences gained by doing lots of surveys and problem solving with other Verilog HDL teammates.

Also, I would like to thank Universiti Teknikal Malaysia Melaka (UTeM) that giving me a chance to study in with the course Bachelor of Electronic Engineering (major in Computer Engineering), and also a chance to choose on this project, The Design and Implementation of VGA Controller on FPGA, under guidance from Mr. Radi Husin Bin Ramlee. It is the best time to understand the advantages of using FPGA and Verilog HDL and practice the skills on using FPGA and Verilog HDL as a good lesson before further study or work in future. I really appreciate all the efforts done by UTeM on designing learning techniques for courses, observing and examining students for future generation. Thank you.

## ABSTRACT

Industrial production machines of today must be highly flexible in order to competitively account for dynamic and unforeseen changes in the product demands. Field-programmable gate arrays (FPGAs) are especially suited to fulfill these requirements; FPGAs are very powerful, relatively inexpensive, and adaptable, since their configuration is specified in an abstract hardware description language. Thus, in order to design and implement VGA Controller on FPGA, Verilog Hardware Description Language (Verilog HDL) is used. Verilog HDL is used to describe and program the gates and counters in FPGA blocks in order to construct an internal logic circuit in FPGA. The main purpose of this project is to design and implement VGA Controller on FPGA. Therefore, the block diagram for VGA Controller is designed and the VGA Controller program is written based on the block diagram using Verilog HDL. Also, functions required for VGA Controller are included in the Verilog code and test bench is created to test the functions written to ensure the FPGA VGA Controller works correctly and accurately without errors. Finally, the completed program is implemented on FPGAs chip of Altera DE2-115 Development and Educational Board.

## ABSTRAK

Pengeluaran mesin dalam industri pada hari ini mesti fleksibel dengan mengambil kira perubahan dinamik dan permintaan produk di luar jangkaan. Field-Programmable Gate Arrays (FPGAs) sangat sesuai untuk memenuhi permintaan ini; FPGAs sangat berguna, murah, dan fleksibel kerana konfigurasinya dibentuk dalam Hardware Description Language. Oleh itu, untuk mereka bentuk dan mengaplikasikan VGA Controller pada FPGA, Verilog Hardware Description Language (Verilog HDL) digunakan. Verilog HDL digunakan untuk menggambarkan dan program “gates” dan kaunter dalam blok FPGA dalam usaha untuk membina litar logik dalaman dalam FPGA. Tujuan utama projek ini adalah untuk mereka bentuk dan mengaplikasikan VGA Controller pada FPGA. Oleh itu, gambarajah blok bagi VGA Controller direka dan program bagi VGA Controller ditulis berdasarkan gambarajah blok tersebut dengan menggunakan Verilog HDL. Selain itu, fungsi-fungsi VGA Controller yang diperlukan juga dimasukkan ke dalam kod Verilog dan bangku ujian dicipta untuk menguji fungsi-fungsi yang ditulis untuk memastikan ketepatan dan efisiensi VGA Controller FPGA tanpa kesilapan. Akhirnya, program yang lengkap tanpa sebarang kesilapan diaplikasikan pada cip FPGAs Altera DE2-115 Development and Educational Board.

## CONTENT

<b>CHAPTER</b>	<b>TITLE</b>	<b>PAGE</b>
	<b>ABSTRACT</b>	<b>vi</b>
	<b>ABSTRAK</b>	<b>vii</b>
	<b>CONTENTS</b>	<b>viii</b>
	<b>LIST OF FIGURE</b>	<b>xi</b>
	<b>LIST OF TABLE</b>	<b>xiv</b>
	<b>LIST OF APPENDIX</b>	<b>xv</b>
	<b>LIST OF ABBREVIATION</b>	<b>xvi</b>
 <b>I</b>	 <b>INTRODUCTION</b>	 <b>1</b>
	1.1 Objectives	2
	1.2 Problem Statement	3
	1.3 Scope of Work	3
	1.4 Methodology	4
	1.5 Summaries of Chapter	4
 <b>II</b>	 <b>LITERATURE REVIEW</b>	 <b>6</b>
	2.1 Field-Programmable Gate Arrays (FPGAs)	6
	2.1.1 FPGAs vs. Programmable Logic Devices (PLDs)	7
	2.1.2 FPGAs vs. Application-Specific Integrated Circuits (ASICs)	7



2.2	Altera DE2-115 Development and Education Board	8
2.3	Video Graphics Array (VGA) Controller	10
2.3.1	VGA Specifications	10
2.3.2	Pixel on Screen	12
2.3.3	Five Control Signal	13
2.3.4	Sync Timing	14
2.3.5	Counting Clock Cycle	15
2.4	Verilog Hardware Description Language	17
2.4.1	Capabilities of Verilog HDL	18
2.5	Altera Quartus II Compiler Software	18
2.5.1	Quartus II Web Edition	19
2.5.2	Quartus II Subscription Edition	20
<b>III</b>	<b>METHODOLOGY</b>	<b>21</b>
3.1	Project Planning	21
3.2	Literature Review	22
3.3	Study the Programming Language	22
3.4	Familiarize the FPGAs	22
3.5	Troubleshooting	23
3.6	Implementation	23
3.7	Flow Chart Diagram	24
<b>IV</b>	<b>RESULT AND DISCUSSION</b>	<b>26</b>
4.1	Expected Results	26
4.2	Result and Discussion	28
4.2.1	Block Diagram	28
4.2.2	Flow Chart	30

	4.2.2.1 VGA Synchronization	30
	4.2.2.2 VGA Controller	36
4.2.3	Waveform	37
	4.2.3.1 VGA Synchronization	37
	4.2.3.2 VGA Controller	39
4.2.4	Synthesis Process	39
	4.2.4.1 Design Summary in Altera Quartus II Compiler Software	39
	4.2.4.2 Pin Planner in Altera Quartus II Compiler Software	41
	4.2.4.3 Register Transfer Level (RTL) Viewer	43
	4.2.4.4 VGA Controller on Altera DE2-115 Development and Education Board	45
4.2.5	VGA Controller Verilog HDL Coding	46
<b>V</b>	<b>CONCLUSION AND SUGGESTIONS</b>	<b>54</b>
	5.1 Project Limitation	54
	5.2 Future Works	54
	5.3 Conclusion	55
<b>VI</b>	<b>REFERENCES</b>	<b>56</b>
<b>VII</b>	<b>APPENDICES</b>	<b>57</b>

## LIST OF FIGURE

NO	TITLE	PAGE
1.2.1	The use of paper as poster at cinema and menu at restaurant	3
2.2.1	Altera DE2-115 Development and Education Board	8
2.3.1.1	Female port and male port on VGA Connector	11
2.3.2.1	Scanning pattern of VGA Controller	13
2.3.4.1	The horizontal and vertical synchronization signal-timing diagram	15
2.5.1	Interface of Quartus II 11.1sp2 Web Edition (32-Bit)	19
3.7.1	Flow Chart diagram of the design and implementation of VGA Controller on FPGA (i)	24
3.7.2	Flow Chart diagram of the design and implementation of VGA Controller on FPGA (ii)	25
4.1.1	Conversion of VGA picture in bmp format to MIF file	27
4.1.2	Expected result	27
4.2.1.1	Block diagram of VGA controller	28
4.2.2.1.1	Flow chart for vga_sync module (i)	30
4.2.2.1.2	Flow chart for vga_sync module (ii)	31

4.2.2.1.3	Flow chart for vga_sync module (iii)	32
4.2.2.1.4	Flow chart for vga_sync module (iv)	33
4.2.2.1.5	Flow chart for vga_sync module (v)	34
4.2.2.1.6	Flow chart for vga_sync module (vi)	35
4.2.2.2.1	Flow chart for vga_controller module	36
4.2.3.1.1	Waveform obtained from vga_sync module	37
4.2.3.1.2	Waveform obtained from vga_sync module (zoom in)	38
4.2.3.2.1	Waveform obtained from vga_controller module	39
4.2.4.2.1	Top view of Cyclone IV E – EP4CE115F29C7	42
4.2.4.2.2	I/O pins location for VGA controller project on Altera DE2-115 Development and Education board	42
4.2.4.3.1	RTL Viewer of the VGA Controller Project	44
4.2.4.4.1	Final product of VGA controller project in Altera Quartus II compiler software	45
4.2.4.4.2	VGA controller on Altera DE2-115 Development and Education board and LCD screen	46
4.2.5.1	Example of “img_data.mif” file (left) and “img_index.mif” file (right)	47
4.2.5.2	Interface of MegaWizard Plug-in Manager (i)	48
4.2.5.3	Interface of MegaWizard Plug-in Manager (ii)	48
4.2.5.4	Interface of MegaWizard Plug-in Manager (iii)	49
4.2.5.5	Interface of MegaWizard Plug-in Manager (iv)	50
4.2.5.6	Interface of MegaWizard Plug-in Manager (v)	51
4.2.5.7	Interface of MegaWizard Plug-in Manager (vi)	52

4.2.5.8	Interface of MegaWizard Plug-in Manager (vii)	53
---------	---	----

**LIST OF TABLE**

<b>NO</b>	<b>TITLE</b>	<b>PAGE</b>
2.2.1	DE2-115 Board Information	9
2.3.1.1	VGA Connector pins name	11
2.3.5.1	Number of cycles required by the four regions in the horizontal sync signal	16
2.3.5.2	Number of cycles required by the four regions in the vertical sync signal	17
4.2.4.1.1	VGA controller project status	40

**LIST OF APPENDICES**

<b>NO</b>	<b>TITLE</b>	<b>PAGE</b>
A1	Verilog HDL Code of vga_sync module	57
A2	Verilog HDL Code of vga_sync module	58
B1	Verilog HDL Code of vga_controller module	59
B2	Verilog HDL Code of vga_controller module	60
C1	Verilog HDL Code of img_data module	61
C2	Verilog HDL Code of img_data module	62
C3	Verilog HDL Code of img_data module	63
C4	Verilog HDL Code of img_data module	64
D1	Verilog HDL Code of img_index module	65
D2	Verilog HDL Code of img_index module	66
D3	Verilog HDL Code of img_index module	67
D4	Verilog HDL Code of img_index module	68
E	DE2-115_User_Manual	69

## LIST OF ABBREVIATION

ASIC	-	Application Specific Integrated Circuit
ATM	-	Automated Teller Machine
DAC	-	Digital-to-Analog Converter
FPGA	-	Field-Programmable Gate Array
IC	-	Integrated Circuit
LCD	-	Liquid Crystal Display
LE	-	Logic Element
LED	-	Light Emitting Diode
NTSC	-	National Television System Committee
PAL	-	Phase Alternating Line
PC	-	Personal Computer
PDA	-	Personal Digital Assistant
PLD	-	Programmable Logic Device
PLI	-	Programming Language Interface
RAM	-	Random Access Memory
RGB	-	Red, Green, Blue
RTL	-	Register Transfer Level
SDRAM	-	Synchronous Dynamic Random Access Memory
SMA	-	Sub Miniature version A
SRAM	-	Static Random Access Memory
USB	-	Universal Serial Bus
VGA	-	Video Graphics Array



## CHAPTER I

### INTRODUCTION

Field-Programmable Gate Arrays (FPGAs) are digital integrated circuits (ICs) that contain configurable blocks of logic along with configurable interconnects between these blocks [1]. Specifically, an FPGA contains programmable logic components called logic elements (LEs) and a hierarchy of reconfigurable interconnects that allow the LEs to be physically connected. LEs can be configured to perform complex combinational functions, or merely simple logic gates like AND and XOR. In most FPGAs, the logic blocks also include memory elements, which may be simple flip-flops or more complete blocks of memory [2].

VGA (video graphics array) is a video display standard. It provides a simple method to connect a system with a monitor for showing information or images. As a standard display interface, VGA has been widely used. There is more and more need in displaying the result of the process in real time as the fast development of embedded system, especially the development of high speed image processing [3]. Apart from that, display will be replacing paper for future. Words of wisdom; seeing is believing and picture telling thousand words, display can give correct information about something. Display is used when people present something. Pictures or texts at display catch more

attention than verbal voice when people are doing presentation. When people do that kind of presentation, there must be some device involved in control the display.

Verilog Hardware Description Language (Verilog HDL) is a popular and standard hardware description language which is now extensively used by engineers and scientists on digital hardware designs. Verilog HDL offers many useful features for digital hardware design, that is, Verilog HDL is a general-purpose hardware description language that is easy to learn and easy to use. It is similar in syntax to the C programming language. Verilog HDL allows different levels of abstraction to be mixed in the same model [4]. Thus, a hardware model can be defined in terms of switches, gates, RTL, or behavioral code. Also, most popular logic synthesis tools support Verilog HDL. This makes it the language of choice for designers [4].

The purpose of this project is to design a VGA Controller using Verilog HDL and implement it on FPGA. First and foremost, RGB data are abstracted from an image file in bitmap format using MATLAB and rearranged using Microsoft Excel. The arranged data are then stored in a MIF file created by using Altera Quartus II compiler software. After that, a VGA Controller program is written in Verilog HDL using Altera Quartus II compiler software, which will compile, run and simulate the written program. Once the simulation is succeeded, the program will be burnt into Altera DE2-115 Board, which will process the VGA Controller program and display the image on LCD screen.

## **1.1 Objectives**

The objectives that must be met to ensure the successful of this project are to abstract RGB data from an image file in bitmap format and store in a MIF file, to design and write a VGA Controller program in Verilog HDL and implement it on FPGA.

## 1.2 Problem Statement

Existing advertisement methods use many papers as shown in Figure 1.2.1. This project can be used as advertisement device since the color will catch the attention of people eyes. Furthermore, there is no need to chop tree to make paper, this VGA Controller only needs new data to change to other design display. Thus, indirectly the environment can be saved.



Figure 1.2.1: The use of paper as poster at cinema and menu at restaurant.

Apart from that, power consumption, weight, price and easy maintenance are main issues in display. PC is heavy to be lift here and there. Therefore, it is not suitable for display. Even though laptop, tablet PC or PDA can be a solution for weigh issues, prices become the next issues. Other than that, PC based device need software and software need license such as operating system. License for software add more cost. So, PC based is not suitable for standalone device that can display at monitor.

## 1.3 Scope of Work

The scope of work for this project are design a VGA Controller using Verilog HDL on Altera Quartus II software, implement the VGA Controller program into Altera

DE2-115 Development and Education Board to generate images on LCD screen, and establish an interconnection between a LCD screen and Altera DE2-115 Development and Education Board to display image.

#### **1.4 Methodology**

To design VGA Controller on Verilog compiler software, the block diagram for VGA Controller is created. To implement VGA Controller program into FPGA, the designed VGA Controller is compiled, ran and simulated. If everything goes in the right path, the VGA Controller program will be burned into Altera DE2-115 Development and Education Board. A VGA cable is used to establish an interconnection between a LCD screen and Altera DE2-115 Development and Education Board. One end of the cable is connected to VGA port on Altera DE2-115 Development and Education Board and the other end is connected to VGA port on LCD screen. More detail explanation and flow chart for the design and implementation of VGA Controller on FPGA will be discussed in Chapter III, Methodology.

#### **1.5 Summaries of Chapters**

This report is documentary delivering the ideas generated, concepts applied, activities done, and finally the product of the project itself. It consists of five chapters. Following is a chapter-by-chapter description of information in this report.

Chapter 1 gives reader a basic introduction to how the idea of this project generated. This chapter contains introduction of the project, objective, problem statement, scope of work, methodology and report structure.

Chapter 2 is a literature review on theoretical concepts applied in this project. This chapter will be discussing the background study of Field-Programmable Gate Arrays (FPGAs), Altera DE2 Development and Education Board, Video Graphics Array (VGA) Controller and Verilog HDL. The theory and concept are explained in this chapter.

Chapter 3 introduces the methodology of the project. This chapter contains flow chart which explains the overall method taken along the project carry out.

Chapter 4 will be covered all the simulation, result, and collection of the data and analysis.

Chapter 5 will be conclusion of this final year project. This chapter includes the conclusion and recommendation that can be implemented in the future.

## CHAPTER II

### LITERATURE REVIEW

This chapter is a literature review on theoretical concepts applied in this project. As this project involved FPGAs, Altera DE2-115 Development and Education Board, VGA Controller, Verilog HDL, and Altera Quartus II Compiler Software information on the basic of the above mentioned has to be studied.

#### 2.1 Field-Programmable Gate Arrays (FPGAs)

FPGAs are a semiconductor device containing programmable logic components called "logic blocks", and programmable interconnects. Logic blocks can be programmed to perform the function of basic logic gates such as AND, and XOR, or more complex combinational functions such as decoders or simple mathematical functions. FPGAs are also known as reconfigurable devices. These reconfigurable FPGAs are generally favored in prototype building because the device does not need to be thrown away every time a change is made. This allows one piece of hardware to perform several different functions. Of course, those functions cannot be performed at the same time. Besides that, FPGAs are

standard parts, they are not designed for any particular function but are programmed by the customer for a particular purpose [5].

FPGAs have compensating advantages, largely due to the fact that they are standard parts. There is no wait from completing the design to obtaining a working chip. The design can be programmed into the FPGA and tested immediately. Apart from that, FPGAs are excellent prototyping vehicles. When the FPGA is used in the final design, the jump from prototype to product is much smaller and easier to negotiate. Also, the same FPGA can be used in several different designs, reducing inventory costs [5].

### **2.1.1 FPGAs vs. Programmable Logic Devices (PLDs)**

In comparison between FPGAs and PLDs, PLDs contain a relatively limited number of logic gates, and the functions they can be used to implement are much smaller and simpler. Moreover, PLDs use fixed interconnect and simply change the logic functions attached to the wires. FPGAs, in contrast, require programming logic blocks and connecting them together in order to implement functions.

### **2.1.2 FPGAs vs. Application-specific Integrated Circuits (ASICs)**

In comparison between FPGAs and ASICs, the final design for ASICs is “frozen in silicon”, which means it cannot be modified without creating a new version of device. On the other way round, FPGAs can be configured by engineers in the field to perform variety of different function. Furthermore, designing and building ASIC is an extremely time-consuming and expensive process, time to market for FPGAs is much faster.

## 2.2 Altera DE2-115 Development and Education Board

The Altera DE2-115 Development and Education board was designed by professors, for professors. It is an ideal vehicle for learning about digital logic, computer organization, and FPGAs. Featuring an Altera Cyclone® IV 4CE115 FPGA, the DE2-115 board is designed for university and college laboratory use. It is suitable for a wide range of exercises in courses on digital logic and computer organization, from simple tasks that illustrate fundamental concepts to advanced designs [6].



Figure 2.2.1: Altera DE2-115 Development and Education Board