

raf

TK2796 .M72 2005



0000016354

Design and implementation of a pulse-width modulation (PWM) for modular structured multilevel inverter / Mohd Saifulizan Omar.

**DESIGN AND IMPLEMENTATION OF A PULSE-WIDTH
MODULATION (PWM) FOR MODULAR STRUCTURED
MULTILEVEL INVERTER**

MOHD SAIFULIZAN BIN OMAR

NOVEMBER 2005

“I admit that I have read this literature work through my observation which has fulfilled the scope and quality in order to be qualified for the conferment the degree of Bachelor in Electrical Engineering (Industrial Power).”

Signature :
Supervisor's Name : Encik Azziddin Mohamad Razali
Date :

DESIGN AND IMPLEMENTATION OF A PULSE-WIDTH MODULATION
(PWM) FOR MODULAR STRUCTURED MULTILEVEL INVERTER


MOHD SAIFULIZAN BIN OMAR

This Report Is Submitted In Partial Fulfillment of Requirements for the Degree of
Bachelor in Electrical Engineering (Industrial Power)

Fakulti Kejuruteraan Elektrik
Kolej Universiti Teknikal Kebangsaan Malaysia

November 2005

"I admitted that this thesis is written by me and is my own effort except as cited in references."

Signature : 

Author's name : Mohd Saifulizan Bin Omar

Date : 21/4/05

To my dearest mother
For continuous love, motivation, support and encouragement.

ACKNOWLEDGEMENT

Alhamdulillah, thanks a lot to the Almighty with His permission finally I have finished my Projek Sarjana Muda 2 in a whole semester. First of all, I would like to express my deepest gratitude to my supervisor, Encik Azziddin Mohamad Razali, for his advice, guidance, help, encouragement and motivation throughout the progress of completing this project.

I also would like to thank to Encik Auzani Jidin who assist and guide me a lot in executing my project, and also to all my colleagues from KUTKM, my house mate especially Ashrol Sharif who help me a lot and also others that may not have been mentioned here. Without any of these supports, I would not have completed my project successfully.

ABSTRACT

Modular structured multilevel inverter is very attractive in high voltage and high power applications. The general function of this multilevel inverter is used to produce a desired sinusoidal voltage from several separate DC sources (SDCS). This inverter has a few advantages. First, by using a multilevel structure, the stress on each switching device can be reduced proportional to the number of levels of the multilevel inverter, thus the inverter can handle higher voltage without using an expensive and bulky step-up transformer in various application. Second, as the number of inverter output voltage levels is increased, harmonics content will be low enough to avoid the need of bulky filters. This project applied Alternative Phase Opposition Disposition (APOD) technique as a PWM switching strategy. A Cascaded-Inverter with Separated DC Sources (CISDCS) is selected as a topology for this multilevel inverter hardware implementation. This inverter generally use PWM switching control signals for producing an AC output voltage and generated by analogue circuit of PWM generator. The multilevel inverter is being analyzed by using MATLAB simulation software.

ABSTRAK

Struktur modular penyongsang pelbagai paras (*multilevel inverter*), amat sesuai untuk kegunaan dan aplikasi voltan dan kuasa tinggi. Secara amnya, penggunaan penyongsang ini adalah untuk menghasilkan voltan keluaran *sinusoidal* daripada sebilangan punca arus terus (DC) yang diasingkan (SDCS). Penyongsang jenis ini mempunyai kelebihan tertentu. Pertamanya, dengan penggunaan struktur *multilevel*, tekanan ke atas setiap perkakasan pensuisan dapat dikurangkan sekadar dengan bilangan paras penyongsang. Oleh itu, penyongsang boleh mengendalikan voltan pada kadar yang tinggi tanpa memerlukan pengubah penaik yang besar dan mahal bagi pelbagai aplikasi. Keduanya, kandungan harmonik akan menjadi rendah sejajar dengan peningkatan bilangan paras penyongsang tanpa memerlukan penapis yang besar. Pelaksanaan projek ini akan mengaplikasikan teknik *Alternative Phase Opposition Disposition (APOD)* sebagai strategi pensuisan pemodulatan lebar denyut (PWM). Selain itu, pembinaan penyongsang ini juga akan menggunakan topologi *Cascaded Inverter with separated DC Sources (CISDCS)*. Umumnya, penghasilan voltan keluaran arus ulang-alik (AC) menggunakan kaedah PWM sebagai isyarat kawalan untuk pensuisan. Manakala, isyarat PWM ini pula dijana oleh litar analog yang dikenali sebagai penjana PWM (*PWM generator*). Perisian simulasi MATLAB digunakan untuk menganalisis penyongsang pelbagai paras ini.

TABLE OF CONTENTS

CHAPTER	TOPICS	PAGE
	TITLE PAGE	i
	DECLARATION	ii
	DEDICATION	iii
	ACKNOWLEDGEMENT	iv
	ABSTRACT	v
	ABSTRAK	vi
	TABLE OF CONTENTS	vii
	LIST OF TABLES	x
	LIST OF FIGURES	xi
	LIST OF ABBREVIATIONS	xiii
	LIST OF APPENDICES	xiv
1	INTRODUCTION	1
	1.1 Introduction	1
	1.2 Objective of the project	2
	1.3 Scope of the project	3
	1.4 Problem statement	3
2	LITERATURE REVIEW	4
	2.1 Multilevel inverter	4
	2.2 Topology of multilevel inverter	5
	2.2.1 Diode-Clamped Multilevel Inverter (DCMI)	5
	2.2.2 Flying-Capacitor Multilevel Inverter (FCMI)	6

2.2.3	Cascaded Inverter with Separated DC Sources (CISDCS)	7
2.2.4	Comparison among three multilevel Inverter in application aspects	8
2.3	PWM voltage control of single-phase inverters	9
2.3.1	Sinusoidal Pulse-Width Modulation (SPWM)	10
2.3.1.1	Sinusoidal Pulse-Width Modulation technique	11
3	METHODOLOGY	13
4	PRELIMINARY ANALYSIS	16
4.1	Simulation	16
4.2	Simulation result	19
5	DESIGN AND IMPLEMENTATION OF HARDWARE	23
5.1	PWM Generator	24
5.1.1	Summing Circuit	25
5.1.2	Comparator Circuit	28
5.2	Gate Drive	29
5.2.1	Dead time circuit	29
5.2.2	DC Isolation supply circuit	32
5.2.3	Signal Isolation	33
5.3	H-Bridge	33
5.3.1	Inverter operation	34
5.3.2	Power Switching Devices	34
5.4	Result	36
5.4.1	Output waveform from PWM Generator circuit	36
5.4.2	Output waveform from gate Drive circuit	38

6	CONCLUSION AND RECOMMENDATION	42
6.1	Conclusion	42
6.2	Recommendation	43
	REFERENCES	44
	APPENDICES	46

LIST OF TABLES

NO	TITLE	PAGE
2-1	Comparison of power component requirement	9
5-1	Absolute maximum rating of MOSFET	35

LIST OF FIGURES

NO	TITLE	PAGE
1-1	General block diagram of inverter	2
2-1	A three phase five-level diode-clamped inverter	5
2-2	A three phase five-level flying-capacitor inverter	6
2-3	A single-phase five-level CISDCS	7
2-4	Sinusoidal pulse-width modulation (SPWM)	11
2-5	SPWM strategy	12
	(a) APOD	12
	(b) POD	12
	(c) PD	12
3-1	Step of progress	15
4-1	Simulation block diagram for five-level inverter	17
4-2	Simulation block diagram for three-level inverter	18
4-3	(a) Five-level input waveform	19
	(b) Three-level input waveform	19
4-4	(a) Five-level switch signal cascaded inverter	20
	(b) Three-level switch signal cascaded inverter	20
4-5	Five-level inverter output voltage waveform	22
4-6	Three-level inverter output voltage waveform	22
5-1	Block diagram of multilevel inverter	23
5-2	Photograph of three-level inverter system overall	24
5-3	Summing circuit	24
5-4	Comparator circuit	25
5-5	(a) Original input triangle wave	27
	(b) Shift up triangle wave	27
	(c) Inverting triangle wave	27

5-6	(a) LM 339 comparator block diagram	28
	(b) Operation of one LM 339 comparator circuit	28
5-7	(a) Dead time gate drive circuit	30
	(b) DC isolation supply gate drive	31
	(c) Signal isolation gate drive	32
5-8	Blanking time generation signals	32
5-9	An H-bridge cell	33
5-10	Switching signals and the output voltage of inverter	34
5-11	MOSFET H-bridge	35
5-12	Original modulation and carrier signal waveform	36
5-13	PWM output 1 waveform	37
5-14	PWM output 2 waveform	37
5-15	PWM waveform	38
5-16	(a) Upper leg PWM waveform from gate drive 1	38
	(b) Lower leg PWM waveform from gate drive 1	39
	(c) Upper leg PWM waveform from gate drive 2	39
	(d) Lower leg PWM waveform from gate drive 2	40
5-17	(a) Photograph of PWM generator circuit board	40
	(b) Photograph of gate drive circuit board	41
	(c) Photograph of MOSFET H-bridge circuit board	41
A-1	PCB layout top layer	46
A-2	PCB layout bottom layer	46

LIST OF ABBREVIATIONS

AC	Alternating Current
APOD	Alternative Phase Opposition Disposition
CISDCS	Cascaded Inverter with Separated DC Sources
CMI	Cascaded Multilevel Inverter
DC	Direct Current
DCMI	Diode Clamped Multilevel Inverter
FCMI	Flying Capacitor Multilevel Inverter
IC	Integrated Circuit
IGBT	Insulated Gate Bipolar Transistor
MOSFET	Metal Oxide Silicon Field Effect Transistor
Op-amp	Operational Amplifier
PCB	Printed Circuit Board
PD	Phase Disposition
PIC	Programmable Interrupt Control
POD	Phase Opposition Disposition
PWM	Pulse Width Modulation
SPWM	Sinusoidal Pulse Width Modulation
UPS	Uninterruptible Power Supply

LIST OF APPENDICES

APPENDIX	TITLE	PAGE
A	Printed Circuit Board (PCB) Layout	46
B	LM 741 Operational Amplifier (Op-amp) Datasheet	47
C	LM 339 Operational Amplifier (Op-amp) Datasheet	55
D	IRFZ34N Power MOSFET Datasheet	66

CHAPTER 1

INTRODUCTION

1.1 Introduction

Inverter is used to convert DC to AC voltage. General block diagram for inverter is shown in Figure 1-1. In the other words, the function of an inverter is to change a DC input voltage to a symmetric AC output voltage of desired magnitude and frequency [1]. Inverters are widely used in industrial application such as, variable-speed AC motor drives, induction heating, standby power supplies, AC appliances run from an automobile battery, and uninterruptible power supply (UPS) [1]. The input may be a battery, fuel cell, solar cell or other DC source.

A variable output voltage can be obtained by varying the input of DC voltage and maintaining the gain of the inverter constant. If the input of inverter is fixed and it is not controllable, a variable output voltage can be obtained by varying the gain of the inverter. The gain can be controlled by pulse-width modulation (PWM) control within the inverter. This inverter gain may be defined as the ratio of the AC output voltage to DC input voltage.

The output voltage waveforms of an ideal inverter should be sinusoidal [2]. However, the waveforms of practical inverters are non-sinusoidal and certainly contain harmonics. Therefore, to obtain a quality output voltage waveform with a minimum amount of ripple or harmonic content, we required high-switching frequency along with various pulse-width modulation (PWM) strategies. In the other word, we need a modular structured of multilevel inverter.

The multilevel inverters have drawn tremendous interest in the power industry. Modular structured multilevel inverter is very attractive in high voltage and high power application. It may easier to produce a high voltage, high power inverter with the multilevel structure because of the way in which device voltage stresses are controlled in the structure. By using multilevel structure, the stress on each switching device can be reduced proportional to the number of levels of the multilevel inverter. Thus, the inverter can handle higher voltage without using an expensive and bulky step-up transformer in various applications. As the number of inverter output voltage levels is increased, harmonics content of the output voltage waveform decreases significantly enough to avoid the need of bulky filters [1].

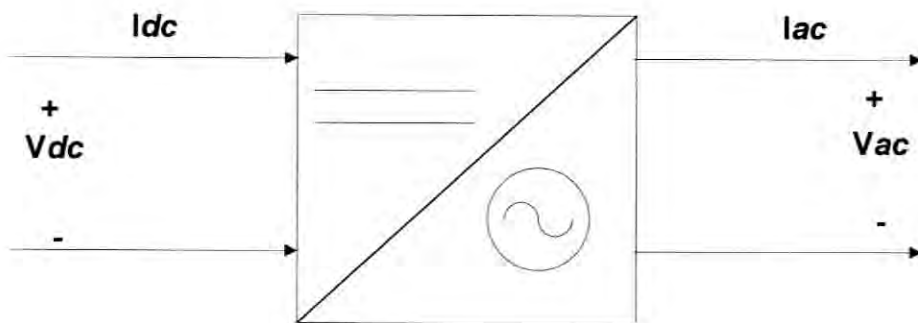


Figure 1-1: General block diagram of inverter

1.2 Objective Of The Project

The objective of this project is to design and implement an attractive multilevel inverter in high voltage and high power application suitable for current scenario in implementation of multilevel inverter and achieve the following:

1. Design a five-level single-phase inverter circuit using MATLAB software.
2. Design and implement a three-level single-phase inverter.
3. This multilevel inverter can produce a desired sinusoidal output voltage waveform with low harmonic content.
4. This multilevel inverter can be applied to improve the performance of other types of multilevel inverter.

5. This multilevel inverter use topology which required the least number of components, among all multilevel inverters, to achieve the same number of voltage levels.

1.3 Scope Of The Project

The work scopes for this project are highlighted as follows:

1. Simulation using MATLAB simulation software.
2. Design and implement a PWM generator circuit using summing operational amplifiers (op-amp) and quad comparator op-amp.
3. Design and implement gate drive circuit.
4. Construct H-bridge inverter using three-level single-phase cascaded full-bridge inverter.

1.4 Problem Statement

Currently, the development of multilevel inverter is usually implemented in various types of application. However, others type of multilevel inverter such as diode-clamped multilevel inverter (DCMI), and flying-capacitors multilevel inverter (FCMI) has major disadvantages. Firstly, high-switching frequency and various PWM required obtaining a quality output voltage waveform. It is also limited operation in high-power and high-voltage application.

Excessive clamping diodes and a number of storage capacitor are required when the number of level is high. High-level inverters are more difficult to pack with the bulky power capacitor and are more expensive to implement. Another disadvantage is the inverter control can be very complicated or difficult to control the real power flow and the output voltage waveform are non-sinusoidal and certainly contain a harmonics [1, 4].

CHAPTER 2

LITERATURE REVIEW

2.1 Multilevel Inverter

The multilevel inverter has drawn tremendous interest in the power industry. This inverter is very attractive in high-voltage and high-power applications. This inverter has a few advantages. It may be easier to produce a high-power and high-voltage inverter with the multilevel structure because of the way in which device voltage stresses are controlled in the structure. Increasing the number of voltage levels in the inverter without requiring higher ratings on individual devices can increase the power rating.

The stress on each switching device can be reduced proportional to the number of levels of the multilevel inverter, thus the inverter can handle higher voltage without using an expensive and bulky step-up transformer in various applications. As the number of voltage levels increases, the harmonic content of the output voltage waveform decreases significantly enough to avoid the need of bulky filters [1, 5, 6].

The topological structure of multilevel inverter must have less switching devices as far as possible, be capable of withstanding very high input voltage for high-power applications and have lower switching frequency for each switching device.

2.2 Topology Of Multilevel Inverter

The topology of multilevel inverter can be classified into three types [3].

- Diode-clamped multilevel inverter (DCMI).
- Flying-capacitor multilevel inverter (FCMI).
- Cascaded multilevel inverter with separated DC sources (CISDCS).

2.2.1 Diode-Clamped Multilevel Inverter (DCMI)

The diode-clamped multilevel inverter (DCMI) uses capacitors in series to divide up the DC bus voltage into a set of voltage levels. A sample of three-phase five-level DCMI is shown in Figure 2-1.

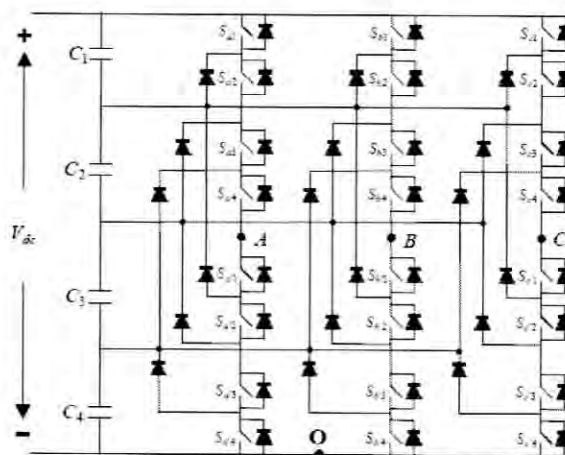


Figure 2-1: A three phase five-level diode-clamped inverter

The major advantages of the DCMI can be summarized as follow [1]:

- When the number of levels is high enough, the harmonic content is low enough to avoid the need for filters.
- Inverter efficiency is high because all devices are switched at the fundamental frequency.
- The control method is simple.

However, the DCMI also has few disadvantages [1]:

1. Excessive clamping diodes are required when the number of levels is high.
2. Difficult to control the real power flow of the individual converter in multilevel converter systems.

2.2.2 Flying-Capacitor Multilevel Inverter (FCMI)

Figure 2-2 shows a sample three-phase five-level converter based on a flying-capacitor multilevel inverter (FCMI). The size of the voltage increment between two capacitors determines the size of the voltage levels in the output waveform.

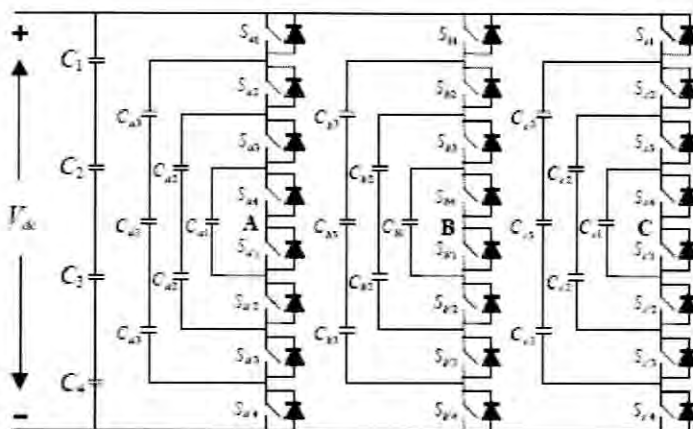


Figure 2-2: A three phase five-level flying-capacitor inverter

The major advantages of the FCMI can be summarized as follow [1]:

1. Large amount of storage capacitors can provide capabilities during power outages.
2. These inverters provide switch combination redundancy for balancing different voltage levels.
3. Like the DCMI with more levels, the harmonic content is low enough to avoid the need of filters.
4. Both real and reactive power flow can be controlled.

The major disadvantages of the FCMI [1]:

1. An excessive number of storage capacitors is required when the number of levels is high. High-level inverters are more difficult to package with the bulky power capacitors and are more expensive too.
2. The inverter control can be very complicated, and the switching frequency and switching losses are high for real power transmission.

2.2.3 Cascaded Inverter With Separated DC Sources (CISDCS)

A cascaded multilevel inverter (CMI) which uses cascaded inverters with separated DC sources (CISDCS) consists of a series of H-bridge (single-phase, full-bridge) inverter units [1]. To avoid short circuit of DC sources, the separated DC source configuration is applied to the multilevel inverter using cascaded-inverter [4]. The general function of this multilevel inverter is the same as that of the other two previous inverters. This CISDCS synthesizes a desired voltage from several independent sources of DC voltages, which may be obtained from batteries, fuel cells, or solar cells.

This configuration recently becomes very popular in AC power supply and adjustable speed drive applications. This new inverter can avoid any voltage-clamping diodes or voltage-balancing capacitors [4]. A single-phase five-level configuration of such an inverter as illustrated in Figure 2-3.

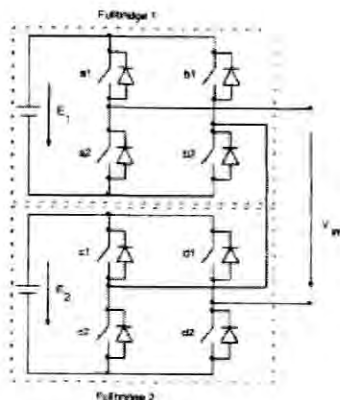


Figure 2-3: A single-phase five-level CISDCS

Each separated DC sources (SDCS) is associated with a single-phase full-bridge inverter. The AC terminal voltages of different level inverters are connected in series. The AC output of each of the different level of full-bridge inverters are connected in series such that the synthesized voltage waveform is the sum of the inverter outputs. In this topology, the number of output phase voltage levels is defined by $m = 2s+1$, where s is the number of DC sources.

The major advantages of the CISDCS can be summarized as follows [1]:

1. Compared with the DCMI and FCMI, it requires the least number of components to achieve the same number of voltage levels.
2. Optimized circuit layout and packaging are possible because each level has the same structure and there are no extra clamping diodes or voltage-balancing capacitors.
3. Soft-switching techniques can be used to reduce switching losses and device stresses.

The disadvantages of the CISDCS are:

1. Needs separate DC source for real power conversions, thereby limiting its applications.

2.2.4 Comparison Among Three Multilevel Inverters In Application Aspects

Table 2-1 compares the power component requirements per phase leg among the three multilevel voltage source inverter. Table 2-1 explains that the number of main switches and main diodes, needed by the inverters to achieve the same number of voltage levels, is the same. Clamping diodes do not need in flying-capacitor and cascaded-inverter configuration, while balancing capacitors do not need in diode-clamp and cascaded-inverter configuration. Implicitly, the multilevel converter using cascaded inverters requires the least number of components.