"I / We admit that to have read this report and it has followed the scope and quality in partial fulfillment of requirements for The Bachelor Degree of Electronic Engineering (Computer Engineering)."

Signature : 

Supervisor Name : En. Nor Zaidi Bin Haron

Date : 5/5/2006

DESIGN OF FINITE STATE MACHINE MEMORY BUILT-IN SELF TEST

SITI AISAH BINTI MAT JUNOS @ YUNUS

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Kolej Universiti Teknikal Kebangsaan Malaysia

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"Hereby the author declares that all the material presented in this thesis to be the effort of the author herself. Any kind of materials that is not the effort of the author has been stated clearly in the references."

Signature : _____

Author Name : Siti Aisah Binti Mat Junos @ Yunus

Date : 05/05/2006

Dedicated to:

Mak, Ayah, Adik Ya, Kak Ba, Kak Da, Kak Yah, Abang, family and my beloved friends for giving me unconditional love and caring……

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ABSTRACT

This project is designing a Design for Test (DfT) technique to test embedded memory called Finite State Machine (FSM) Memory Built–In Self Test (MBIST). The design is written using Very High Speed Integrated Circuit Hardware Design Language, (VHDL) based on the FSM architecture. The architecture will be modelled using Register Transfer Level (RTL) abstraction. A simulation on two testing algorithms is implemented on this architecture. Evaluation on area and testing time of these algorithms are carried out. The area is referring to number of logic gates used to build the circuit. While, the testing time is the completion time for testing the embedded Memory. Lastly, a comparison to Microcode Memory Built–In Self Test (MBIST) architecture evaluation is performed.

ABSTRAK

Projek ini ialah merekabentuk satu Teknik Reka Bentuk untuk Pengujian, (DfT) bagi menguji memori yang terbenam yang dikenali sebagai Terbina dalam Pengujian Sendiri Memori dengan Mesin Keadaan Terhingga (Finite State Machine Memory Built-In Self Test). Rekabentuk ini ditulis menggunakan pembangunan perisian melalui perisian Very High Speed Integrated Circuit Hardware Design Language, (VHDL) berdasarkan senibina Mesin Keadaan Terhingga, (FSM). Senibina projek ini akan dimodelkan menggunakan Peniskalaan Peringkat Pemindahan Daftar, (Register Transfer Level). Dua algoritma pengujian yang diimplementasikan ke atas senibina tersebut adalah untuk proses simulasi. Penilaian ke atas kawasan dan masa pengujian bagi algoritma tersebut akan dilakukan. Kawasan pengujian merujuk kepada bilangan logik get yang digunakan dalam membina litar tersebut. Sementara bagi masa pengujian adalah masa yang diperlukan untuk menyiapkan pengujian memori yang terbenam. Akhirnya, satu penilaian di laksanakan bagi menunjukkan perbezaan dengan teknik senibina Mikrokod bagi Terbina dalam Pengujian Sendiri Memori, (MBIST).

CONTENTS

II LITERATURE REVIEW

III METHODOLOGY

IV RESULTS AND ANALYSIS

LIST OF TABLES

LIST OF FIGURES

LIST OF ABBREVIATIONS

ATE	-	Automatic Test Equipment
BIST	-	Built-In Self Test
CE	-	Chip Enable
CF	-	Coupling Faults
CUT	-	Circuit Under Test
DfT	-	Design for Test
DRF	-	Data Retention Faults
FPGA	-	Field Programmable Gate Array
FSM	-	Finite State Machine
HDL	-	Hardware Description Language
IC	-	Integrated Circuit
LFSR	-	Linear Feedback Shift Register
MBIST	-	Memory Built-In Self Test
MUT	-	Memory Under Test
MUX	-	Multiplexer
OE	-	Read Enable
PCB	-	Printed Circuit Board
RAM	-	Random Access Memory
ROM	-	Read Only Memory
RTL	-	Register Transfer Level
SAF	-	Stuck At Faults
SoC	-	System on Chip
SRAM	-	Static Random Access Memory

TF	-	Transition Faults
VHDL	-	Very High Speed Integrated Circuit Hardware Description Language
WE	-	Write Enable

CHAPTER I

INTRODUCTION

Chapter 1 starts with the background of the project. It is followed by objectives and scope of the project. The overview method of project is presented in fourth part and lastly summary of the thesis is described.

1.1 BACKGROUND OF PROJECT

Design for Test, (DfT) is a philosophy to overcome the complete product testing problem. Built-In Self Test, (BIST) is the one of technique used in this philosophy. According to the Memory Built-In Self Test, (MBIST) technique, the embedded memories becoming a major part in System on Chip (SoC). The density of this component is bigger and larger to due the number of data to be stored. However, the increase in circuit complexity was because the embedded memories testing more challenging. Among the problem encountered while testing the memories are:

i) Controllability of the logic elements problem. The Controllability is to produce any desired values on the internal signal of the circuit by applying an appropriate test vector input combination to the primary inputs.

ii) Observability of the logic elements problem. The observability is any internal signal can be propagated to a primary output for comparison with an expected value by the application of an appropriate primary input combination.

iii) Insufficient fault coverage in the embedded memory testing.

iv) The increasing testing data to be stored and analysed.

v) New sophisticated and expensive testers are needed to test the embedded memory.

vi) Tomorrow's memories cannot be tested by today's testers. New version of memories one invented everyday. The tester cannot cope with the new fault that might be occurred.

1.1.1 Design for Test, (DfT) Techniques

Design for Test is a design philosophy which suggests that the problem of testing complex circuit can be improved. DfT technique range from a simple set of guide lines to a formal set of design rules [1]. The objective of developing DfT methods are to facilitate the testing of complex sequential circuits. The purpose of testing is to ensure before fabrication, the circuit behavior satisfies the intent of the designer which is free from functional or logical design errors and to detect faulty devices after fabrication. It is also can improve the IC testability in terms of controllability, observability and predictability of signal values on nodes inside the circuit [6]. The evolutions of test methods for embedded memories are:

i) Bed-of Nails and In-Circuit Testing

ii) Scan Method

iii) Built-In Self Test, (BIST) Technique

1.1.1.1 Bed-of Nails and In-Circuit Testing

Digital circuits that are fabricated on a single PCB, observability is obtained by using every pin of every IC as a test point. This is achieved by building a special test fixture that matches the layout of the PCB and contains a spring-loaded pin (nail) at each IC-pin position. The PCB is placed on this bed of nails, and the nails are connected to an automatic tester that can monitor each pin as required by a test program. Disadvantage of this technique are [7]:

i) The rise of high density surface mount packaging has made Bed-of Nails Testing more difficult. Components may be mounted on both sides of the PCB; a special test fixture called a clamp shell may be needed to connect nails to both sides of the PCB.

ii) The pins of many surface mount devices are so small and their spacing is so tight (25 mils or less), that it may be impossible to reliably land a test pin on them.

1.1.1.2 Scan Method

A scan method attempts to control and observe the internal signals of a circuit using only a small number of test points [7]. It is consider as any digital circuit to be a collection of flip-flops or other storage elements interconnected by combinational logic and is concerned with controlling and observing the state of the storage elements. It does this by providing two operation modes: a normal mode and a scan mode in which all of storage elements are reorganized into a giant shift register. In scan mode, the state of the circuit and storage elements can be read out by *n* shifts (observability), and a new state can be loaded at the same time (controllability). Figure 1.1 illustrates this scan method circuitry.

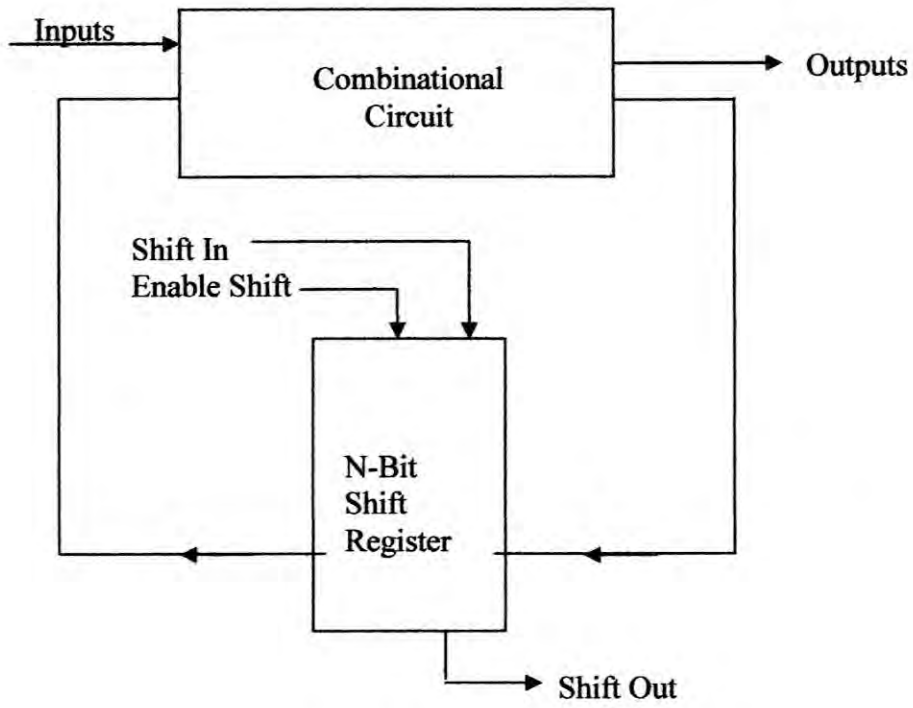

Figure 1.1: Scan Path Principle [simplified from 7].

1.1.1.3 Built-In Self Test, (BIST) Technique

Built-In Self Test, or BIST, is the technique of integrate the functionality of an automatic test system onto a chip. BIST is a design for testability Design for Test, (DfT) technique in which testing (test generation and test application) is accomplished through built in hardware features [5].

The general BIST architecture is a BIST test controller which controls the BIST circuit, test generator which generates the test address sequence, response verification as a comparator which compares the memory output response with the expected correct data and Circuit Under Test (CUT) as shown in Figure 1.2.

The BIST controller can be implemented by either hardwired logic in the form of a Finite State Machine (FSM), microcode controller or processor-based.

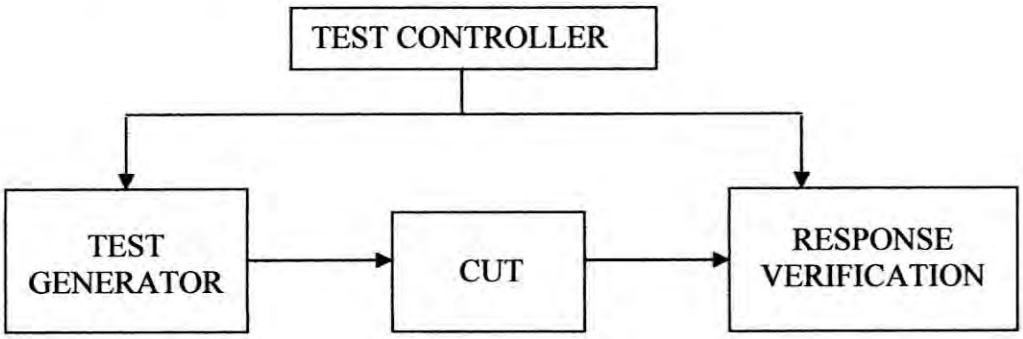

Figure 1.2: General BIST Architecture [simplified from 5].

1.1.2 Motivation of BIST versus ATE

There are two main approaches for testing embedded memories: external test by direct access using Automatic Test Equipment, (ATE) and internal testing using Built-In Self Test (BIST). When external testing is employed, the input test vectors and correct response data are stored in the ATE memory. For external testing, the comparison is carried out on the tester.

ATE limitations make BIST technology an attractive alternative to external test for complex chips. BIST is a Design for Test (DfT) method where part of the circuit is used to test the circuit itself where the test vectors are generated and test responses are analyzed on-chip.

ATE, as well as very long testing time since tester channels are timeshared by different memories under test. On the other hand, BIST provides at-speed and high-bandwidth access to the embedded memory cores and it only needs a low cost to initialize the test sessions and to inspect the final results either status bits pass or fail. However, although BIST is may induce excessive power, in addition to performance and area overhead [3].

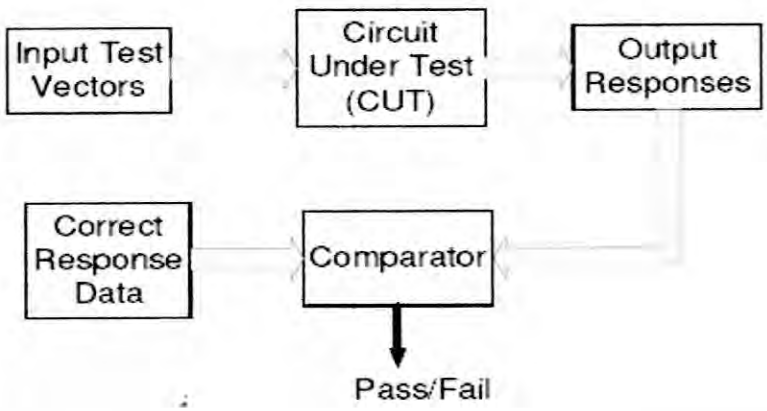

Figure 1.3: Basic Principle of Testing [3].

The advantages of the BIST compared to ATE are:

i) Provides efficient testing of the embedded components and interconnections.
ii) Permit circuits to be tested at speed.
iii) Reduce the test time and cost the large size of embedded memory.
iv) Reduce the volume of test data.
v) Better fault coverage, special test structures can be incorporated onto the chips.
vi) Produce an alternative to costly Automatic Test Equipment, (ATE).
vii) Well designed testing, the same hardware can test chips, boards and system.

1.2 OBJECTIVE OF PROJECT

The objectives of the project are:

i) To Study Design for Test (DfT) techniques to test embedded memory.
ii) Learn the way to design a logic circuit using Very High Speed Integrated Circuit Hardware Description Language (VHDL) software.
iii) To Design Finite State Machine (FSM) Memory Built–In Self Test (MBIST) using VHDL.
iv) To simulate, synthesis and verify the design.
v) To evaluate the area and time based on the implementation of the algorithms.

1.3 SCOPE OF PROJECT

There are the scopes of the project:

i) Software-based project which is to design FSM Memory BIST architecture for testing embedded memory.
ii) Implementation of two memory testing algorithms as FSM Memory controller.
iii) Evaluation the area and time based on the implementation of the algorithms.
iv) Target completion is simulation on fault SRAM Memory.

1.4 METHOD OF PROJECT

Several steps are gone through in completing this design. Firstly, make some study is made understood the overall specification of the project. Reading on the past journals and books is done to gain the knowledge for achieving the objectives.

By referring the information and data obtained through the study, the overall functional block diagram of the Finite State Machine controller is sketched using the top-down level design. This is a design technique that starts with the highest level of an idea to block diagram and works its way down the single component in block diagram. From that, the state diagram of the algorithms FSM controller is derived and translated in VHDL programming. The VHDL program is checked it syntax to ensure error free.

After that, the program is simulated by testing fault SRAM Memory to verify the functionality of the design. Lastly, the designs are synthesised its area and time testing