


“I / We admit that I / We have read this literature work through my/our observation which has fulfilled the scope and quality in order to be qualified for the conferment of Bachelor Degree in Electronic Engineering (Computer Engineering).”

Signature :  .....

Supervisor's name: Mrs. Anis Suhaila Bt. Mohd Zain

Date : 5 Mei 2006 .....

**STUDY OF AN ATM SWITCH WITH SUPPORT FOR TIME  
DETERMINISTIC COMMUNICATION**


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**May 2006**

**“I admit that this report is done by myself except the discussion and extracts taken from other sources that clearly stated in the sources of reference”**

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**I dedicate my respect and thankful to my beloved mom, Pn. Rahimah Bt. Dol, family and myBeaR. All the joy and difficulties that we had faced together is a priceless gift that I could never forget...**

## **ACKNOWLEDGEMENT**

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## ABSTRACT

In a multiprocessor or distributed real time system, a need to know the temporal behavior of the system is sometimes of major concern, mainly in the sense of guaranteeing a maximum upper limit on delivery times for messages sent from one endpoint to another. This project makes a survey of current methods for time deterministic delivery of messages in a multiprocessor or distributed hard real-time environment and concurrently tries to adopt a suitable architecture for an ATM (Asynchronous Transfer Mode) switch that supports these methods of communication. The switch architecture's most prominent feature is intended to be a low implement cost. In order to build large networks of computational units, running distributed applications, the cost of the total implementation can grow very large. Therefore, a smaller architecture than traditional ATM will be processed that still is able to relay ATM traffic, in a time deterministic manner.

## ABSTRAK

Projek ini bertujuan untuk membuat tinjauan terhadap kaedah yang sedia ada bagi penghantaran data dengan masa yang dapat ditentukan dalam pelbagai pemprosesan untuk disebarkan dalam persekitaran masa nyata keras. Selaras dengan itu, rekabentuk yang bersesuaian cuba dikaji bagi suis ATM (mod penghantaran tak segerak) yang dapat menampung kaedah komunikasi tersebut. Rekabentuk suis mestilah mempunyai ciri yang menonjol dengan kos pelaksanaan yang rendah. Untuk membina sistem rangkaian yang besar dengan aplikasi penyebaran data yang luas, kos pelaksanaan akan meningkat dengan tinggi. Oleh yang demikian, rekabentuk suis yang lebih kecil dan dapat menggantikan trafik ATM dalam kaedah penghantaran data dengan masa yang dapat ditentukan akan dihasilkan.

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**LIST OF ABBREVIATION**

<b>AAL</b>	ATM Adaptation Layer
<b>ATM</b>	Asynchronous Transfer Mode
<b>B-ISDN</b>	Broadband Integrated Services Digital Network
<b>EDF</b>	Earliest Deadline First
<b>FCFS</b>	First Come First Served
<b>ITU</b>	International Telecommunications Union
<b>LAN</b>	Local Area Network
<b>OSI</b>	Open System Interconnection
<b>PGPS</b>	Packet-by-packet Generalized Processor Sharing
<b>SONET</b>	Synchronous Optical NETwork
<b>TDC</b>	Time Deterministic Communication
<b>VPI</b>	Virtual Path Identifier
<b>WAN</b>	Wide Area Network
<b>WRR</b>	Weighted Round Robin

## **CHAPTER I**

### **INTRODUCTION**

#### **1.1 INTRODUCTION OF THE PROJECT**

To overcome the increasing need for computational power, parallel multiprocessor architectures seem to be a possible solution. This approach provides the way for distributing partial computations on several cheap processing nodes in parallel network architecture. Applications that run in real-time, such as industrial automation, signal processing, critical control systems and power generation is under evaluation in this context. The requirements laid upon real-time systems are change. Often a best-effort scheme is sufficient, but in other applications, stronger constraints are imposed on the system. For example, these constraints could be of a timely nature. It is meaning that not just the fact that an event took place, but when it took place is of importance. Also, a desire to predict the upper bound on communication latency between two endpoints in the system, forces some kind of scheduling and admission control of the traffic in the network. Methods for calculating maximum message latency in multiple host network architectures will be covered, in the second part of this project. Their purpose is to provide an application developer with deterministic knowledge of the architecture, so that requirements laid upon the system in the sense of real-time demands can be met.

## 1.2 OBJECTIVES OF PROJECT

Generally, this project and investigation is standing for the requirement to complete this bachelor degree course. Thus, the objectives to finish this project are just to apply all the knowledge that has been gained during this course study. As technical objectives, all the project aims and scopes are stated below:

- To study of an Asynchronous Transfer Mode (ATM) switch based on its structure, functionality and standardization.
- To study of Time Deterministic Communication (TDC) and other methods and make a comparison of each methods.
- ATM switches architecture will be proposed that contains enough support for time deterministic traffic relay.

## 1.3 SCOPE OF PROJECT

This project is basically based on the ATM switch and real time communication and not out of the works border. For myself, since the scope of ATM switch and real time communication is wide, I faced a problem to limit the scope for this project. After a discussion with the supervisor of this project, I decide to limit the scopes of work as listed below:

- Study of Asynchronous Transfer Mode (ATM) switch's functionality, structure, standardization and recommendations.
- Study of Time Deterministic Communication (TDC) and other methods such as First Come First Served (FCFS), Weighted Round Robin (WRR), Earliest Deadline First (EDF) and Packet-by-Packet Generalized Processor Sharing

(PGPS) for guaranteeing communication delays in parallel network architectures. Also to find the advantages and disadvantages of each methods.

- Evaluation of the ability of these methods to accommodate real time traffic in an ATM type of network and the implementation complexity in relation to the various methods.
- Present a proposal for an ATM switch architecture that contains enough support to allow for TDC to be used as a run time scheduling method and also the implication on the different layers of the ATM reference model and the solution of this problem.

#### **1.4 METHODOLOGY OF PROJECT**

- Get information of Asynchronous Transfer Mode (ATM) switch from reference books, Internet and other sources.
- Study of ATM switch: functionality, structure, standardization and recommendations.
- Study of Time Deterministic Communication (TDC) and other methods and make a comparison.
- Investigate the problem of implementation the TDC methods into ATM switch architecture.
- Propose ATM switches architecture suitable for TDC.

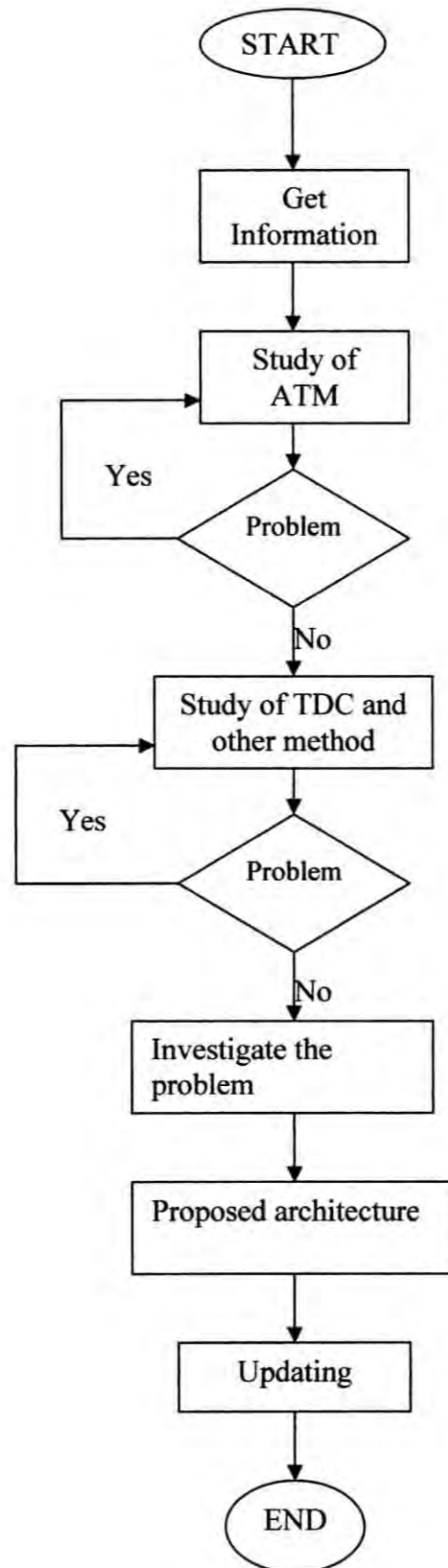


Figure 1.1: Flowchart of Methodology Project



## **CHAPTER II**

### **LITERATURE STUDY**

#### **2.1 GENERAL REVIEW**

In this chapter, the literature review is discussing to provide insight into the previous study of this project. On the other hand, any related finding during doing this project will be implemented to improve the previous result.

## 2.2 ATM

### 2.2.1 ATM History

Before there were computers that needed to be linked together to share resources and communicate, telephone companies built an international network to carry telephone calls. These Wide Area Networks (WAN) were optimized to carry multiple telephone calls from one person to another, primarily using copper cable. As time passed, the bandwidth limitations of copper cable became apparent, and these WAN carriers began looking into upgrading their copper cable to fiber cable.

Because of its potential for almost unlimited bandwidth, carriers saw fibers as an essential part of their future. However, other limitations of the voice network still existed. Even though WAN carriers were upgrading to fiber, there were still no agreed upon standards that allowed equipment from different vendors' fiber-based equipment to be integrated together. The short-term solution to this problem was to upgrade to fiber; however, this was costly and time consuming. In addition, the lack of sophisticated network management in these WANs made them difficult to maintain.

Around the same time, computers were becoming more prevalent in the office. Networking these computers together was desirable and beneficial. When linking these computers over a long distance, the existing voice-optimized WANs were used. Because computers send data instead of voice, and data has different characteristics, these WANs did not send computer data very efficiently. Therefore, separate WANs were sometimes built specifically to carry data traffic. Also, a network that could carry voice, data and video had been envisioned-something needed to be done.

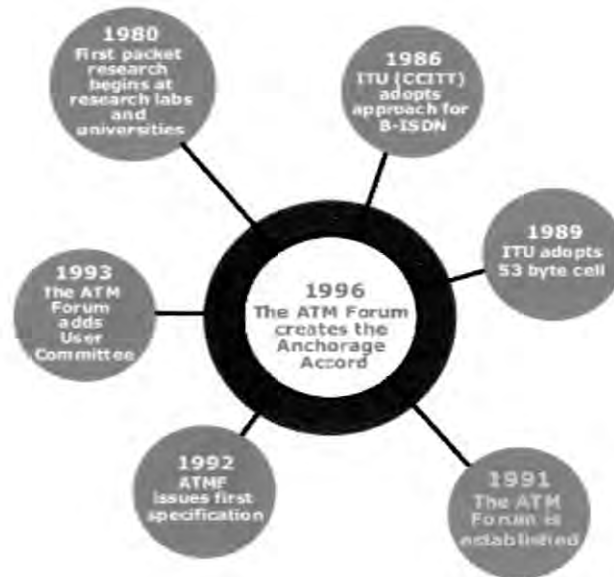


Figure 2.1: ATM History

To address these concerns, ITU-T (formerly CCITT) and other standards groups started work in the 1980s to establish a series of recommendations for the transmission, switching, signaling and control techniques required to implement an intelligent fiber-based network that could solve current limitations and would allow networks to be able to efficiently carry services of the future. This network was termed Broadband Integrated Services Digital Network (B-ISDN). By 1990, decisions had been made to base B-ISDN on SONET/SDH (Synchronous Optical Network/Synchronous Digital Hierarchy) and ATM. SONET only describes the transmission and multiplexing of information. It can operate with nearly all-emerging switching technologies. For B-ISDN, two types of switching were considered by the ITU-T: Synchronous and Asynchronous. An intelligent switching fabric with the ability to switch all forms of traffic at extremely high speeds, while maximizing the use of bandwidth, was needed to optimize the potential of B-ISDN. Ideally, maximum bandwidth should be accessible to all applications and users, and should be allocated on demand. ATM was chosen as the standard for B-ISDN that will ultimately satisfy these stringent requirements. Even though ATM was initially considered part of the solution for WANs, local area network (LAN) architects and

equipment vendors saw ATM as a solution to many of their network limitations, and cable TV operators looked at ATM as a possible addition to their existing networks.

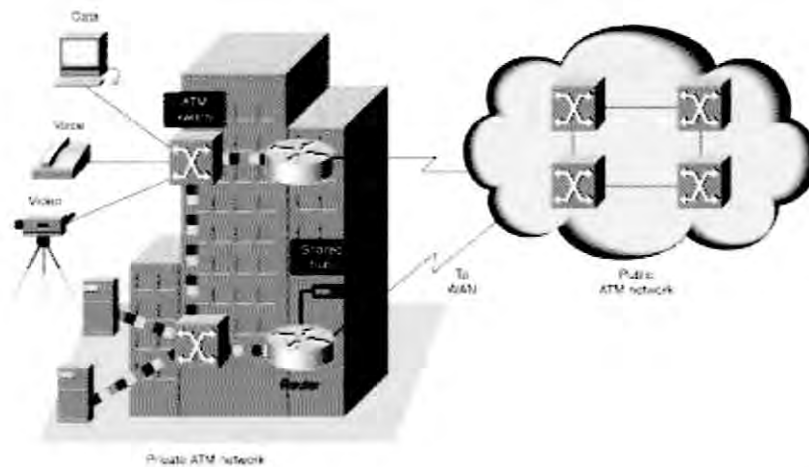


Figure 2.2: A Private ATM Network and a Public ATM Network Both Can Carry Voice, Video, and Data Traffic

The ATM Forum was established in October 1991 and issued its first specifications eight months later. The ATM Forum was formed to accelerate the user of ATM product and services through a rapid convergence of interoperability specifications. In addition, the Forum promotes industry cooperation and market awareness.

By 1996 The ATM Forum presented the Anchorage Accord objective. Fundamentally, the message is that the set of specifications needed for the development of multi-service ATM networks is available. These specifications were complete to implement and manage an ATM infrastructure, and ensure backward compatibility.

Entering the new millennium, ATM services are still in demand. The global market for ATM is in the billions of US dollars. Even with emerging technologies, ATM technology is still the only technology that can guarantee a certain and predefined quality of service. The growth of the Internet, need for broadband access and content, e-commerce and more are spurring the need for a reliable, efficient transport system - ATM Technology. For voice, video, data and images together, the next generation network depends on ATM.

### **2.2.2 ATM Standardization**

ATM is based on the efforts of the ITU-T Broadband Integrated Services Digital Network (B-ISDN) standard. It was originally conceived as a high-speed transfer technology for voice, video, and data over public networks. The ATM Forum extended the ITU-T's vision of ATM for use over public and private networks. The ATM Forum has released work on the following specifications:

- User-to-Network Interface (UNI) 2.0
- UNI 3.0
- UNI 3.1
- UNI 4.0
- Public-Network Node Interface (P-NNI)
- LAN Emulation (LANE)
- Multi-protocol over ATM

### 2.2.3 ATM Reference Model

The ATM architecture uses a logical model to describe the functionality that it supports. ATM functionality corresponds to the physical layer and part of the data link layer of the OSI reference model.

The ATM reference model is composed of the following ATM layers:

- **Physical Layer**—Analogous to the physical layer of the OSI reference model, the ATM physical layer manages the medium-dependent transmission.
- **ATM Layer**—Combined with the ATM adaptation layer, the ATM layer is roughly analogous to the data link layer of the OSI reference model. The ATM layer is responsible for the simultaneous sharing of virtual circuits over a physical link (cell multiplexing) and passing cells through the ATM network (cell relay). To do this, it uses the VPI and VCI information in the header of each ATM cell.
- **ATM Adaptation Layer (AAL)**—Combined with the ATM layer, the AAL is roughly analogous to the data link layer of the OSI model. The AAL is responsible for isolating higher-layer protocols from the details of the ATM processes. The adaptation layer prepares user data for conversion into cells and segments the data into 48-byte cell payloads.

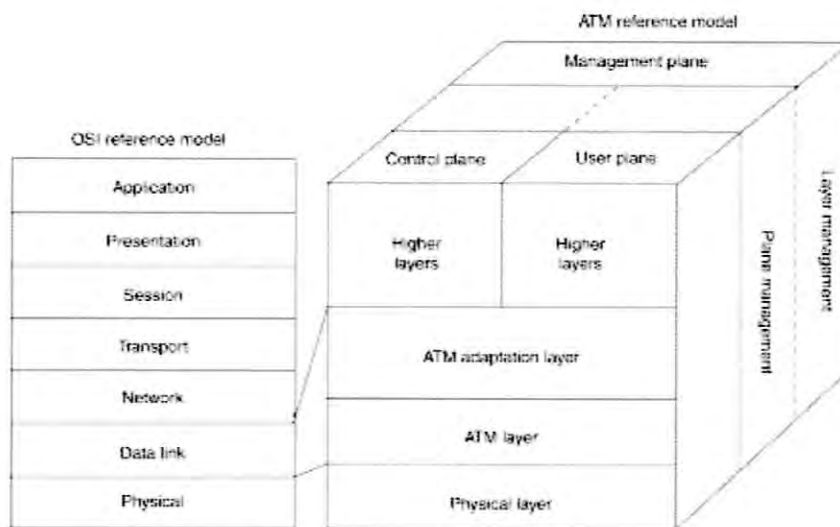


Figure 2.3: The ATM Reference Model Relates To the Lowest Two Layers of the OSI Reference Model

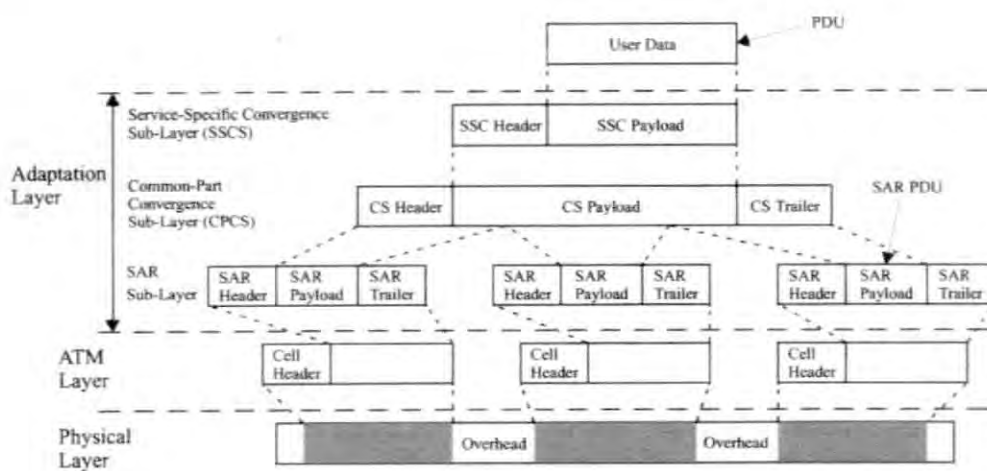


Figure 2.4: ATM Layer Structure

## 2.2.4 Switchboards

The core unit of any ATM switch is the switching fabric, or switchboard. This control component performs the actual transfer of data from an input link to an output link. It also performs timing with respect to message boundaries and resolving functions regarding contention that can arise inside a switch.

Basically the switching fabric consists of some sort of interconnect with which it is possible to create a path from every input link/port to every output link/port. To accommodate features such as speed and scalability, simple structures are encouraged, although many different solutions exist to realize a high-speed switchboard.

### 2.2.4.1 Shifter

Easy to understand, low implementation-cost switch. An input link is connected to a proper output link through a shifter/rotator that interchanges the different links an appropriate amount of steps. Has a disadvantage in that it has to perform some arithmetic operations in order to derive the amount of steps to shift every message period. The shifter switch is highly scalable and compact in its design. It is also a switch with high-speed capabilities, if the derivation of the amount of steps to rotate can be automated, i.e. the switch self-routed.

Without major alterations, more ports can be added to a shifter switch. As always, the buffer implications will limit the switch size. Since only one cell can be routed through the switch simultaneously, as the numbers of links grow, the per-link latency will increase.