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DESIGN OF MICROCODE MEMORY BUILT-IN SELF TEST

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This Report Is Submitted In Partial Fulfillment of Requirements for the Bachelor Degree of Electronic Engineering (Electronic Industry)

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"Hereby the author declares that all the material presented in this thesis to be the effort of the author himself. Any kind of materials that is not the effort of the author has been state clearly in the references."

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Dedicated to:

Ma, Abah, Abang, Kakak, Adik-adik, and my beloved friends for giving me the support .

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ABSTRACT

This project is designing a Design for Test (DfT) technique to test embedded memory called Microcode Built–In Self Test (MBIST). The design is written using Very High Speed Integrated Circuit Hardware Design Language, (VHDL) based on the Microcode architecture. The architecture will be modelled using Register Transfer Level (RTL) abstraction. A simulation on two testing algorithms is implemented on this architecture. Evaluation on area and testing time of these algorithms are carried out. The area is referring to number of logic gates used to build the circuit. While, the testing time is the completion time for testing the embedded Memory. Besides that a comparison to Finite State Machine Memory Built–In Self Test (FSMBIST) architecture evaluation is performed. Lastly, The advantages of Microcode Built–In Self Test (MBIST) will be presented in another chapter below.

ABSTRAK

Projek ini ialah merekabentuk satu Teknik Reka Bentuk untuk Pengujian, (DfT) bagi menguji memori yang terbenam yang dikenali sebagai teknik senibina Mikrokod bagi Terbina dalam Pengujian Sendiri Memori, (MBIST). Rekabentuk ini ditulis menggunakan pembangunan perisian melalui perisian Very High Speed Integrated Circuit Hardware Design Language, (VHDL) berdasarkan senibina Mikrokod bagi Terbina dalam Pengujian Sendiri Memori, (MBIST). Senibina projek ini akan dimodelkan menggunakan Peniskalaan Peringkat Pemindahan Daftar, (Register Transfer Level). Dua algoritma pengujian yang diimplementasikan ke atas senibina tersebut adalah untuk proses simulasi. Penilaian ke atas kawasan dan masa pengujian bagi algoritma tersebut akan dilakukan. Kawasan pengujian merujuk kepada bilangan logik get yang digunakan dalam membina litar tersebut. Sementara bagi masa pengujian adalah masa yang diperlukan untuk menyiapkan pengujian memori yang terbenam. Di samping itu satu penilaian di laksanakan bagi menunjukkan perbezaan dengan teknik Terbina dalam Pengujian Sendiri Memori dengan Mesin Keadaan Terhingga (Finite State Machine Memory Built-In Self Test). Akhirnya, Kelebihan Mikrokod bagi Terbina dalam Pengujian Sendiri Memori, (MBIST) dibentangkan di bahagian seterusnya

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LIST OF ABBREVIATIONS

A

ATE	-	Automatic Test Equipment

B

BIST	-	Built-In Self Test

C

CE	-	Chip Enable
CF	-	Coupling Faults
CUT	-	Circuit Under Test

D

DfT	-	Design for Test
DRF	-	Data Retention Faults

F

FPGA	-	Field Programmable Gate Array
FSM	-	Finite State Machine

H

HDL	-	Hardware Description Language

L

LFSR	-	Linear Feedback Shift Register

M

MBIST	-	Memory Built-In Self Test
MUT	-	Memory Under Test
MUX	-	Multiplexer

O

OE	-	Read Enable

P

PCB	-	Printed Circuit Board

R

RAM	-	Random Access Memory
ROM	-	Read Only Memory
RTL	-	Register Transfer Level

S

SAF	-	Stuck At Faults
SoC	-	System on Chip
SRAM	-	Static Random Access Memory

T

TF	-	Transition Faults
TPG	-	Test Pattern Generator

V

VHDL	-	Very High Speed Integrated Circuit Hardware Description Language

W

WE	-	Write Enable

CHAPTER I

INTRODUCTION

1.1 BACKGROUND OF PROJECT

Design for Test, (DfT) is a philosophy to overcome the complete product testing problem. Built-In Self Test (BIST) is the one of technique used in this philosophy. Built-in self-test (BIST) techniques enable an integrated circuit (IC) to test itself. BIST reduces test and maintenance costs for an IC by eliminating the need for expensive test equipment and by allowing fast location of failed ICs in a system. BIST also allows an IC to be tested at its normal operating speed which is very important for detecting timing faults. Despite all of these advantages, BIST has seen limited use in industry because of area and performance overhead and increased design time.

According to the Memory Built-In Self Test, (MBIST) technique, the embedded memories becoming a major part in System on Chip (SoC). The density of this component is bigger and larger to due the number of data to be stored. However, the increase in circuit complexity is cause the embedded memories testing more challenging. Among the problem encountered while testing the memories are:

i) Controllability of the logic elements problem. The Controllability is to produce any desired values on the internal signal of the circuit by applying an appropriate test vector input combination to the primary inputs.

ii) Observability of the logic elements problem. The observability is any internal signal can be propagated to a primary output for comparison with an expected value by the application of an appropriate primary input combination.

iii) Insufficient fault coverage in the embedded memory testing.

iv) The increasing testing data to be stored and analysed.

v) New sophisticated and expensive testers are needed to test the embedded memory.

vi) Tomorrow's memories cannot be tested by today's testers. New version of memories one invented everyday. The tester cannot cope with the new fault that might be occurred.

1.2 OBJECTIVE OF PROJECT

The objectives of the project are:

i) To Study Design for Test (DfT) techniques to test embedded memory.

ii) To know the latest techniques to gain knowledge.

iii) Learn the way to design a logic circuit using Very High Speed Integrated Circuit Hardware Description Language (VHDL) software.

iv) To Design a MMBIST "*Microcode Memory Built in Self Test*" using VHDL.

v) To simulate, synthesis and verify the design.

vi) To evaluate the area and time based on the implementation of the algorithms.

1.3 SCOPE OF PROJECT

There are the scopes of the project:

i) Software-based project which is to design *Microcode Memory Built in Self Test* (MMBIST) architecture for testing embedded memory.

ii) Implementation of two memory testing algorithms as *Microcode Memory Built in Self Test* (MMBIST) controller.

iii) Evaluation the area and time based on the implementation of the algorithms.

iv) Target completion is simulation on fault SRAM Memory.

v) This result will be compared with student which done the title "*Design of Finite State Machine Memory Built-in Self Test*(FSM BIST)"

1.4 METHOD OF PROJECT

The first what we done is we find a title of project which this project will be given from my supervisor En.Noor Zaidi bin Haron. Then we will find and read also understand the literature of this project which we find journal website *IEEE,* the latest and newest technique to test embedded memory.

Several steps are gone through in completing this design. Firstly, make some study is made understood the overall specification of the project. Reading on the past journals and books is done to gain the knowledge for achieving the objectives.

By referring the information and data obtained through the study, the overall functional block diagram of the *Microcode Built in Self Test* controller is sketched using the top-down level design. This is a design technique that starts with the highest level of an idea to block diagram and works its way down the single component in block diagram. From that, the state diagram of the algorithms MBIST controller is derived and translated in VHDL programming. The VHDL program is checked it syntax to ensure error free.

After that, the program is simulated by testing fault SRAM Memory to verify the functionality of the design. Lastly, the designs are synthesized its area and time testing for each algorithms is used. Note that, some iteration processes are performed during VHDL programming, syntax checking, simulation and synthesized in meeting the task.

1.5 SUMMARY OF THESIS

This thesis consists of five chapters what describes in detail and clearly about this project. Chapter one is an introduction of the entire of the project. They are including with importance of this project and motivation of the projects. Besides, the problem statement, objective, scope and overview method of project are discussed in this chapter.

Chapter two will discuss the study and all the information that are related to this project. Each the fact and data are gathered through the different source of references in order to choose the best algorithm to implement in this project.

Chapter three will be explaining the methodology of implemented in this project in detail. Introduction to Xilinx ISE 7.1i and ModelSim XE III 6.0a are presented in this chapter.

The results obtained on this project are given in chapter four. Analysis all the test bench also described. In this chapter I also include all the waveform simulation that I have done.

Last chapter in this thesis, which conclude the project and some suggestion are given. Besides that, I have included the knowledge which I have learnt and have understood in this project.

CHAPTER II

LITERATURE REVIEW

2.1 INTRODUCTION

In this chapter, explains about theory and concept of the entire project. Literature review on past journals is done to understand the memory fault models and memory test pattern algorithms which are presented first in this chapter. Design techniques will be presented in this chapter. Two MBIST architectures are also briefly explained in following section. The architectures are Microcode MBIST and Finite State Machine are commonly has their own characteristics. After that, comparison will carry out from both of MBIST architectures.