DESIGN AND CHARACTERIZATION OF BIAXIAL STRAINED SILICON N-CHANNEL METAL-OXIDE-SEMICONDUCTOR FIELD-EFFECT TRANSISTOR (MOSFET)

NORAZIAN BINTI MD SUKARDI

UNIVERSITI TEKNIKAL MALAYSIA MELAKA (UTeM)

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NORAZIAN BINTI MD SUKARDI

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This thesis is dedicated to

My family for their supports
and guide me throughout my academic career

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ABSTRACT

For the high demand of faster and smaller electronic devices, the researchers and semiconductor manufacturers are putting a lot of effort to face the difficulties and challenges of improving of the performance of the semiconductor devices from the conventional one. One of the solutions is to apply strained silicon alternative to the conventional devices so that the structure of the MOSFET is not totally changed but the device performances are improved. In order to increase the mobility and the speed of the electronic devices, semiconductor technology researchers face the limitations such as short channel effect in MOSFET device as it is unavoidable in scaling. The aim of this project is to conduct research on the biaxial strained silicon NMOS. Technology Computer Aided Design (TCAD) tool from Silvaco's International® was used to simulate the structure designed in this project. Silvaco's DevEdit software will be used to design a structure of MOSFET according to the steps, ATHENA software will virtually fabricate the MOSFET according to the steps and commands given, while Silvaco's ATLAS software was used to obtain its characteristics. The characteristics and result analysis such as transfer characteristics (I_d - V_{gs}), subthreshold curves (log I_d - V_{gs}), output characteristics (I_d - V_{ds}) and the variation of SiGe thickness analysis in biaxial strained silicon NMOS were done to compare with the conventional NMOS. Results analyzed in this project show the biaxial strained silicon NMOS give better electrical performance compared to the conventional NMOS in term of enhance mobility, lower resistance and power consumption.

ABSTRAK

Bagi memenuhi permintaan tinggi terhadap peranti elektronik yang cepat dan kecil, para penyelidik dan pengilang semikonduktor berusaha untuk menghadapi cabaran ini. Hal ini disebabkan peningkatan prestasi peranti semikonduktor daripada yang konvensional merupakan satu tugasan yang sukar. Salah satu penyelesaian bagi masalah ini adalah dengan menambah satu lapisan silikon tegang ke dalam MOSFET konvensional supaya struktur MOSFET tidak berubah dengan sepenuhnya, tetapi prestasi elektriknya bertambah baik. Selain itu, kajian terhadap peningkatan dalam mobiliti dan kepantasan peranti elektronik telah dilaksanakan oleh penyelidik teknologi semikonduktor kini bagi melepasi batasan dalam MOSFET, contohnya, kesan saluran pendek yang tidak boleh dielakkan semasa penskalaan. Tujuan projek ini adalah untuk mengkaji dwipaksi silikon tegang NMOS. *Technology Computer Aided Design* (TCAD) dari *Silvaco's International*® digunakan dalam projek ini untuk mensimulasi struktur yang dibina. Perisian *Silvaco's DevEdit* digunakan untuk membuat lakaran struktur MOSFET sebelum strukutur sebenar dibuat, *ATHENA* pula digunakan untuk fabrikasi MOSFET berdasarkan langkah dan arahan yang diberi, manakala perisian *ATLAS* digunakan untuk mendapat pencirian elektriknya. Pencirian dan analisis keputusan seperti pencirian pemindahan (I_d - V_{gs}), lengkungan subthreshold (log I_d - V_{gs}), pencirian keluaran (I_d - V_{ds}) dan analisis saiz SiGe mengikut ketebalan di dalam NMOS tegangan silikon dwipaksi dilakukan untuk membandingkannya dengan NMOS konvensional. Analisis keputusan yang diperolehi NMOS tegangan silikon dwipaksi mempunyai prestasi yang lebih baik berbanding dengan NMOS konvensional dari segi peningkatan mobiliti, pertahanan yang lebih rendah dan juga kurang pengambilan kuasanya.

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LIST OF ABBREVIATIONS

CMOS	-	Complementary Metal Oxide Semiconductor
Ge	-	Germanium
MOSFET	-	Metal-Oxide-Semiconductor Field Effect Transistor
nm	-	nanometer
NMOS	-	N-channel MOSFET
PMOS	-	P-channel MOSFET
SiGe	-	Silicon-Germanium
DIBL	-	Drain-Induced Barrier Lowering
SiGe	-	Silicon-Germanium
SOI	-	Silicon On Insulator
SSOI	-	Strained Silicon-On-Insulator
TCAD	-	Technology Computer Aided Design
VLSI	-	Very Large Scale Integrated Circuits
C-V	-	Capacitance Voltage
DC	-	Direct Current

LIST OF SYMBOLS

I_d	-	Drain Current
V_{ds}	-	Drain-To-Source Voltage
V_{gs}	-	Gate-To-Source Voltage
V_t	-	Threshold Voltage
Leff	-	Effective Channel Length
S	-	Subthreshold Curves
W	-	Width Of Transistor
C	-	Capacitance

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CHAPTER I

INTRODUCTION

This project use SILVACO TCAD tools to design MOSFET structure process and device simulation. The background of the study is thoroughly elaborated. This chapter also outlined on the objectives and scope of the research.

1.1 Background

More than 30 years, the MOSFET have continually been scale down in size in channel length from micrometers to sub - micrometers and then to sub - micrometers range following Moore's Law. The channel length of MOSFET is reduced from 100 nm to 45 nm. The size reduction of the device makes great improvement to MOSFET operation.

Nowadays, many researchers have been done to improve the performance of the device in obtaining higher speed, low power consumption, low cost and smaller device. There a new techniques that are study in the present time to improve the MOSFET such as double gate MOSFET, vertical MOSFET, silicon on insulator and many more.

The Metal–Oxide–Semiconductor Field-Effect Transistor (MOSFET) is a voltage controlled device used to amplify electronic signals or acted as a switch. The MOSFET includes a channel of n-type or p-type semiconductor material and is accordingly called an NMOSFET or a PMOSFET (also commonly NMOS or PMOS). It is one of the most common transistors used in both analog and mixed-signal circuits for advanced integrated circuit (IC) design. MOSFET has the advantages which the switching time is about 10 times faster than a bipolar transistor, very much smaller switching current, and less affected by temperature when compared to bipolar transistor [1].

Silicon-Germanium or SiGe is a general term for the alloy Si1-xGex which consists of any molar ratio of silicon and germanium. It is commonly used as a semiconductor material in integrated circuits (ICs) for hetero junction bipolar transistors or as a strain-inducing layer for CMOS transistors. Strained SiGe MOSFET extends the fundamental scaling limit which causes short channel effect. The 4.2% lattice mismatch between Si and SiGe layer are used to create strained layer to enhance the carrier transport in the MOSFET's channel [2]. Strained silicon MOSFET has been known for increasing speed, mobility and reducing power consumption of traditional MOSFET [3]. In this project, biaxial strained silicon n-channel MOSFET has been selected to be studied. N-type transistor is more significant in biaxial tensile strain compared to uniaxial tensile strain and conventional MOSFET (as control device) [4]. Thus, this supports the studies of this project to be done on biaxial strained silicon NMOS.

1.2 Problem Statement

The phenomenon of obtaining high demand for faster and smaller MOSFET devices in semiconductor technology has led to develop strained silicon in the conventional MOSFET. As the MOSFET technology is approaching nano scaling, short channel effect becomes more considerable as the channel length is reduced. Thus, the strained silicon layer is introduced into conventional MOSFET to improve the performance of the device without reducing the channel length.

Besides, the cost to obtain optimized semiconductor device through fabrication process to perform experimental analysis is quite high due to the repeating process. The cost is also involving the purchase of expensive electrical fabricating and testing equipment. Therefore, Technology Computer Aided Design (TCAD) software is used for the process and device simulations of the devices in this project (e.g. DEVEDIT, Silvaco's International ATHENA and ATLAS simulation software).

1.3 Objectives

The general and specific objectives of this project can be summarized as below:

(i) To conduct literature research on the differences between uniaxial and biaxial strained silicon NMOS.
(ii) To design and fabricate biaxial strained silicon NMOS using ATHENA.
(iii) To obtain the characteristics of the biaxial strained silicon NMOS designed and compare with the conventional MOSFET.
(iv) To conclude the characteristics of biaxial strained silicon NMOS by including the theoretical statements and mathematical calculations.

1.4 Scope

This project studied the characteristics of biaxial strained silicon NMOS that is modified from conventional MOSFET. Design and fabrication of biaxial strained silicon NMOS was done using Silvaco's ATHENA software while device simulation (characterization) was done using ATLAS software.

From the project, the required parameters of every fabrication steps and the order of fabrication steps are very important to ensure a proper MOSFET device was fabricated. On the other hand, it also highlighted some MOSFET characteristics that need to be studied before entering the circuit design level, such as transfer

characteristics (I_d - V_{gs}), subthreshold curves (log I_d - V_{gs}) and output characteristics (I_d - V_{ds}).

1.5 Summary of Work

This project will be carried out in two semesters. The first part of the project is done in the first semester where the understandings of literature review and methodology that will use are done. Gathering information is needed in order to understanding the concept of this research and the process to design it. Most of the information is obtained from articles and journal that can be downloading from the Institute of Electrical and Electronic Engineering (IEEE) website. Next, for second semester the research continues with design the structure, fabricated and simulates the devices and analyzes the result.

1.6 Thesis Outline

This thesis consists of six chapter. The first chapter provides an introduction for this project to readers. This includes the background, problem statement, objectives, scope and summary of work. The second chapter contains literature review, theory and information about strain silicon MOSFET and other relevant researches conducted by research institutes and universities around the world.

The research activities and methods employed in this project will be discussed in detail in Chapter III. This chapter explain the flow of this project from the very beginning of the data collection until the acceptable results. It also introduces the TCAD tools to readers which is DevEdit, ATENA and ATLAS software.

Chapters IV discuss the step by step explanations on the development of the strained silicon NMOS using DevEdit and fabrication process using ATHENA. The characterization of biaxial strained silicon NMOS employed in detail in Chapter V. Chapter V shows the results that obtained from the process simulation of the device

structure using the ATLAS tools. The data and results are analyzed and discussed in this chapter. Analysis from transfer characteristics, subthreshold curves and output characteristics are also discussed in this chapter.

Finally, Chapter VI is the conclusion and suggestions for this project. More importantly, this chapter compares the results analysis with the objectives of this project in order to determine the achievements of this project.