LAYOUT DESIGN AND SIMULATION OF COMPLEMENTARY METAL – OXIDE – SEMICONDUCTOR (CMOS) OPERATION AMPLIFIER

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A thesis submitted in partial fulfillment of the requirements for the award of the degree of Bachelor of Electronic Engineering (Computer Engineering)

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To my beloved parents, sisters, and friends, who have encouraged me throughout my journey of education. A warm thanks to all.

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Alhamdulillah, thank you to Allah S.W.T because of His blessing, I finally complete and finish my final year project successfully.

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ABSTRACT

Today's atmosphere and demands continue to drive operating voltages down, especially for widely used components such as the operational amplifier. Some of the motivations driving the market are integration, battery operated components, and biomedical instrumentation. The increased packaging densities in integrated circuits require reduction in feature size that, in turn, reduces breakdown voltages thereby limiting the power supply. In order to as certain low voltage and smaller in size operational amplifier, CMOS operational amplifier is preferred. In this project, the design and simulation of low power, moderate gain, and fast settling time CMOS operational amplifier consisting of two stages is implemented. The design was implemented using SILVACO EDA tool. Gateway tool will be used to draw the schematic for this design, while Expert tool will be used for design the layout.

ABSTRAK

Dewasa ini permintaan dan keperluan bagi komponen-komponen elektronik yang beroperasi dalam voltan rendah semakin meningkat terutamanya bagi komponen yang banyak digunakan seperti penguat operasi. Beberapa motivasi yang menggalakkan pasaran ialah integrasi, komponen yang menggunakan bateri dan peralatan bio-perubatan. Peringkat kepadatan bungkusan bagi litar bersepadu memerlukan komponen yang bersaiz tetapi dapat menghadkan sumber kuasa. Alternatif yang paling berkesan dalam memenuhi keperluan ini adalah dengan beralih kepada CMOS (*Complementary Metal-Oxide-Semiconductor*) yang menawarkan komponen dengan keperluan kuasa yang rendah dan kecil dari segi saiz. Dalam projek ini, rekabentuk dan simulasi penguat operasi CMOS yang mempunyai ciri-ciri kuasa yang rendah dan gandaan yang sederhana serta terdiri daripada dua peringkat telah diimplikasikan. Rekabentuk ini dilaksanakan menggunakan dalam perisian SILVACO EDA. Pekakasan yang digunakan bagi lakaran skematik adalah *Gateway*, manakala untuk melakar *layout* menggunakan perisian *Expert*.

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K	-	Transconductance parameter (in saturation)
Γ	-	Bulk threshold parameter
VT	-	Threshold voltage
λ	-	Channel length modulation parameter.
Gm	-	Tranconductance
Fu	-	Unity gain frequency
VDSAT	-	Saturation voltage
VGS	-	Gate to source voltage.
GBW	-	Gain bandwidth
W	-	Width
L	-	Length
DRC	-	Design rule check.
LVS l	-	Layout versus schematic.
S/D	-	Source/Drain

LIST OF APPENDICES

CHAPTER I

INTRODUCTION

This project uses software SILVATO EDA tools for design and simulate for layout. The background of the study is thoroughly elaborated. This chapter also outlined on the objective and scope of the research.

1.1 Historical Background

The Metal–Oxide–Semiconductor Field-Effect Transistor (MOSFET) is a voltage controlled device used to amplify electronic signals or acted as a switch. The MOSFET includes a channel of n-type or p-type semiconductor material and is accordingly called an NMOSFET or a PMOSFET (also commonly NMOS or PMOS). It is one of the most common transistors used in both analog and mixed-signal circuits for advanced integrated circuit (IC) design. MOSFET has the advantages which the switching time is about 10 times faster than a bipolar transistor, very much smaller switching current, and less affected by temperature when compared to bipolar transistor.

Complementary Metal-Oxide-Semiconductor (CMOS) technology is circuit implementation using both PMOS and NMOS transistors on the same silicon chip. CMOS designs typically offer high gain and speed at low power consumption. In addition, CMOS scales well to smaller devices without drastic changes in performance.

The operational amplifier often referred to informally as an op amp, is a circuit that provides extremely high-gain amplification of the difference in voltage between two inputs. One input is known as the inverting input and the other is known as the non-inverting input. There is only a single output. The input impedance of the inverting and non-inverting inputs is extremely high. The output impedance of the op amp is very low.

The primary requirement of an op amp is to have an open loop gain that is sufficiently large to implement the negative feedback concept. Most of the amplifiers do not have a large enough gain. Consequently, CMOS op amps use two or more stages of gain. One of the most popular op-amp is a two stage op amp. The first is because it is simple yet robust implementation of an op amp and second it can be used as the starting point for the development of other types of op amp.

1.2 Problem Statement

There are two problems. First, while the voltage gain is high, it is not predictable. Second, in order for the circuit to function properly, the transistors used in differential amplifiers must be matched exactly. The first problem can be corrected by using negative feedback to control the gain. CMOS is use because they made from the same block of silicon and it easier to match.

1.3 Objectives

The objectives of this project can be summarized as below:

(i) To understand the use of SILVACO EDA tool.

(ii) To design layout of Complementary Metal Oxide Semiconductor operational amplifier.

(iii) To validate the layout and schematic of the amplifier

1.4 Scope

This project is based on analog electronic devices and advanced integrated circuit design fundamentals. It involves 2 basic concepts, design and verification using SILVACO EDA tool software.

(i) Gateway supports flat or hierarchical designs of any technology. Gateway readily accepts legacy designs from other schematic editors (PSPICE, OrCAD, Composer, etc) through EDIF 200 standard. Gateway can be used by large design teams through global preferences and handles multiple designs and technologies with specific workspaces [1].

(ii) Expert is a high performance hierarchical IC layout editor with full editing features, large capacity and fast layout viewing. Expert provides high level of design assistance with Netlist Driven Layout and parameterized cells (Pcells) [1].

1.5 Project Outline

This project is organized into five chapters as follows:

Chapter 1 clarifies the background of the study for this project. This chapter also outlined on the objective and scope of the research.

Chapter 2 discusses the literature survey on the theories of an ideal operational amplifier and its performance characteristics. This chapter also details the two stages operational amplifier design technique consist of differential gain stage and common source gain stage.

Chapter 3 presents the methodology for the two stages CMOS operational amplifier design. The transistor sizes then calculated according to schematic.

Chapter 4 present results and discussion of CMOS operational amplifier generated using SILVACO EDA tool. The discussion is about the finding and observation from layout design performance.

Chapter 5 outlines the conclusion and suggestion for this work. Conclusion for the overall project findings especially on the CMOS operational amplifier circuit is done and the suggestion for the future works is also stated.

CHAPTER II

LITERATURE REVIEW

In this chapter, the basic theories of MOSFET transistors and the characteristics of an ideal operational amplifier will be reviewed. The important relationships of two stages CMOS operational amplifier is reviewed.

2.1 MOSFET (Metal – Oxide - Semiconductor Field Effect Transistor)

The metal – oxide - semiconductor field effect transistor (MOSFET, MOS-FET, or MOS FET), is by far the most common field effect transistor in both digital and analog circuits. Figure 2.1 shows the structure of MOSFET.

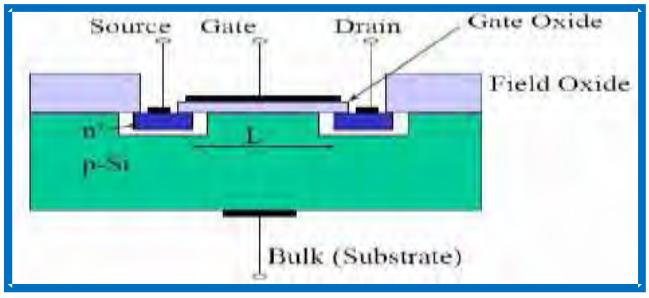

Figure 2.1: MOSFET Structure