# OPTIMAL SIZING OF TRANSISTOR'S PARAMETER USING GENETIC ALGORITHM

YAP YUNG LIN

A project report submitted in partial fulfillment of the requirements for the award of Bachelor Degree of Electronic & Computer Engineering with Honour.

Faculty of Electronic and Computer Engineering Universiti Teknikal Malaysia Melaka

April 2010

C Universiti Teknikal Malaysia Melaka

AN AVER AN AVER	UNIN FAKULTI KEJURU	/ <b>ERSTI TEKNIK</b> JTERAAN ELEKTR <b>BORANG PENGESA</b>	<b>AL MALAYSIA MELAKA</b> ONIK DAN KEJURUTERAAN KOMPUTER <b>HAN STATUS LAPORAN</b>
		PROJEK SA	RJANA MUDA II
Tajuk Projek 💠	Optimal Sizing o	of Transistor's Par	rameter using Genetic Algorithm
Sesi Pengajian 🗄	2009/2010		
Saya		YAP YUNG	LIN
<ul> <li>mengaku membenarkan Laporan Projek Sarjana Muda ini disimpan di Perpustakaan dengan syarat-syarat kegunaan seperti berikut: <ol> <li>Laporan adalah hakmilik Universiti Teknikal Malaysia Melaka.</li> <li>Perpustakaan dibenarkan membuat salinan untuk tujuan pengajian sahaja.</li> <li>Perpustakaan dibenarkan membuat salinan laporan ini sebagai bahan pertukaran antara institusi pengajian tinggi.</li> <li>Sila tandakan (√):</li> </ol> </li> <li>SULIT* <ol> <li>(Mengandungi maklumat yang berdarjah keselamatan atau kepentingan Malaysia seperti yang termaktub di dalam AKTA RAHSIA RASMI 1972)</li> </ol> </li> </ul>			
тп	DAK TERHAD		
			Disahkan oleh:
(TAND/	ATANGAN PENULIS)	(	COP DAN TANDATANGAN PENYELIA)
Alamat Tetap: No 22	2, Jln 3/5, Tmn Sg Besi I	ndah,	
4330	0, Seri Kembangan, Sela	angor.	
Tarikh:		1	`arikh:

I hereby declare that I have read this project report and in my opinion this project report is sufficient in terms of scope and quality for the award of the Bachelor Degree Honour of Electronic & Computer Engineering.

Signature	:
Name of Supervisor	: Madam. Wong Yan Chiew
Date	: 23 April 2010

iii

I declare that this project report entitled "Optimal Sizing of Transistor's Parameters using Genetic Algorithm" is the result of my own research except as cited in the references. The project report has not been accepted for any degree and is not concurrently submitted in candidature of any other degree.

Signature	:
Name	: Yap Yung Lin
Date	: <u>23 April 2010</u>

Specially... To my beloved parents To my kind brothers and sisters And not forgetting to all friends For their Love, Sacrifice, Encouragements, and Best Wishes

#### ACKNOWLEDGEMENTS

First of all, I would like to admire and express my thankfulness to our God because I can finish this 40 weeks or two semester long period final year project at Universiti Teknikal Malaysia Melaka (UTeM) and the report is submitted exact on time. Base on that, I already fulfill the requirement of the BENU4583 and BENU4983.

Next, I would like to state my gratitude to all people that have assist and guide me in this final year project or Project Saujana Muda (PSM). My PSM supervisor, Madam Wong Yan Chiew does help me a lot to scheduling mile stone and increasing my spirit strange to accomplish the work. She is brilliant who color the PSM group under her guidance, which consists of 6 students in the same course.

Madam Wong had patiently guides me to the actual way to finish this project. She is the person who masters the knowledge of Genetic Algorithm, which bring and provide us a lot of extra knowledge. Moreover, I am also indebted to UTeM for their encouragement and facilities support during my research. Not forgetting to all fellow postgraduate students and friends for their moral support and helping me during this entire two semesters. Without their continued support and interest, this project would not have been realized.

Last but not least, my gratitude also goes to all my family members for their continuous encouragement and financial support. Thanks you all.

#### ABSTRACT

This project report presents the design and development of genetic circuit optimizer. Initially, genetic circuit optimizer is based on the Simple Genetic Algorithm (SGA) to perform the optimization function. Genetic algorithm is the programming concept that mimics the mutation concept of biological evolution. Genetic circuit optimizer tends to use the transistor width and length in the selected circuit to tune circuit performance near to optimal. Genetic Circuit Optimizer developed by using Pspice and Matlab. SGA was written in Matlab environment to perform the optimization task. The random transistor width and length named chromosome are generated in Matlab by uing SGA. Chromosomes are decoded into format that recognized by PC Simulation Program with Integrated Circuit Emphasis (PSpice) to simulating corresponding output. Interfacing part is essential part of the project. The output with the transistor's width and length are encoded into chromosome to perform genetic operation. Genetic operation performed to optimal the chromosome. Previous research had concluded the GA optimization process. Moreover, researcher had found the way to decode and encode the transistor sizing into chromosome. Improved Non-dominate Sorting Genetic Algorithm was used to upgrade the Genetic Circuit optimizer. Hence, the Genetic Circuit Optimizer manages to optimization more circuit parameters. The capabilities of Genetic Circuit Optimizer are proved by optimizing the inverter circuit, four stage amplifier circuit and Operational Transconductance Amplifier circuit. Furthermore, the speed and accuracy of Genetic Circuit Optimizer are improved by changing the simulator into Disk Operation Mode (Dos) and using Hspice respectively. Finally, verification and validation of Genetic Circuit Optimizer are statistically showed and studied.

#### ABSTRAK

Project ini membincangkan pendekatan dan ciptaan Pengoptimasi Litar Genetik. Pada permulaan, Pengoptimasi Litar Genetik terdiri daripada Mudah Litar Pengotimasi Genetic untuk optimasikan parameter yang ditujukan. Genetic algorithm adalah konsep pengaturcaraan yang meniru konsep mutasi evolusi biologi. Pengoptimasi litar genetik cenderung menggunakan transistor lebar dan panjang di litar yang dipilih untuk prestasi tune litar berdekatan ke tahap optimum. Pengoptimasi Genetik dikembangkan dengan Pspice dan Matlab. Litar Pengotimasi Genetic ditulis di dalam Matlab untuk melaksanakan tugas pengoptimuman. Lebar dan panjang transistor dinamakan kromosom dihasil dalam Matlab oleh Mudah Pengoptimasi Genetic secara rawak. Kumpulan data yang dihasilkan dipanggil kromosom. Kromosom diperihal dalam format Komputer peribadi Program Simulasi Penekanan dengan litar bersepadu untuk mensimulasikan keluaran yang sesuai. merupakan bahagian penting dalam projek ini untuk menunjukkan Interaksi menukaran and penghantaran data. Seterusnya, keluaran dengan lebar dan panjang transistor dikodekan menjadi kromosom untuk melakukan operasi genetik. Operasi genetik akan mengoptimumkan kromosom. Kajian dahulu telah menyimpulkan proses optimasi GA. Selain itu, Ahli pengkajian telah menyediakan cara untuk membaca kata laluan dan menyandi saiz transistor sebagai kromosom. Peningkatan Non-mendominasi Sortasi Algoritma Genetik digunakan untuk meningkatkan optimasi Genetik Circuit. Oleh itu, Genetik Circuit Pengoptimal berjaya pengoptimumkan lebih parameter litar yang ditujukan. Kemampuan Pengoptimal Genetic Litar terbukti dengan mengoptimumkan rangkaian inverter, empat tahap penguat litar and litar transkonduktansi operasi penguat. Selanjutnya, kelajuan dan ketepatan Genetic Litar Pengoptimal ditingkatkan dengan menukarkan simulator ke Mode Operasi Disk and menggunakan Hspice. Akhirnya, pengesahan and validasi Genetic Litar Pengoptimal secara statistic dituniuk dan dipelajari.

## TABLE OF CONTENT

### CHAPTER TITLE

# PAGE

PROJECT TITLE	i
PROJECT STATUS FORM	ii
DECLARATION	iii
DEDICATION	V
ACKNOWLEDGEMENTS	vi
ABSTRACT	vii
ABSTRAK	viii
TABLE OF CONTENTS	ix
LIST OF TABLE	xiii
LIST OF FIGURES	xiv
LIST OF ABBREVIATIONS	xviii
LIST OF SYMBOLS	xix
LIST OF APPENDICES	XX

# I INTRODUCTION

1.1	Background	1
1.2	Problem Statement	3
1.3	Objective	4
1.4	Scope	5
1.5	Significant Of Study	7
1.6	Organization	8

## II LITERATURE REVIEW

2.1	Genetic Algorithm Overview	10
2.2	Genetic Algorithm For Circuit Modeling	12
2.3	Transistor's Size Optimization	13
2.4	Fitting Transistor Sizing Parameter	14
2.5	GA Flow In Transistor Sizing	16
2.6	Chromosome Representation	
2.7	Multi Objective Optimization	17
	2.7.1 Improved Non-dominate Sorting Genetic Algorithm	18
2.8	Simulation Program with Integrated Circuit Emphasis	19
	2.8.1 Transistor Scaling	19
2.9	Summary	19

# III METHODOLOGY

3.1	Optimization System Of The Transistor size		20
3.2	Evolutionary Development		21
	3.2.1	Modeling Analysis (Pspice + Matlab)	22
	3.2.2	Construction Of Coding	23
	3.2.3	Deployment Deliver Feedback, Testing and Collect	24
		Result	
	3.2.4	Analyze Data And Approach	25
3.3	Simpl	e GA Optimization Flow Chart	26
3.4	NSGA	_2 Optimization flow Chart	27
3.5	Summ	ary	28

# IV GENETIC CIRCUIT OPTIMIZER DEVELOPMENT

4.1	A Pspice Simple Circuit	29
4.2	Schematic Netlist	31

4.3	Interfacing Pspice With Matlab	
4.4	Data Extraction From Pspice To Matlab	
4.5	Relation Between Transistor Width And Length To Output	
	Current, <i>I</i> <sub>D</sub>	
4.6	Chromosome Encryption	36
4.7	Fitness Function To Measure Output Variable	
4.8	GA Optimization	
	4.81 MOSFET Inverter Circuit.	41
	4.82 Simple Operation Amplifier	43
4.9	Summary	46

### V ENHANCEMENT OF GENETIC CIRCUIT OPTIMIZER

5.1	Circui	it Under Testing	47
	5.1.1	Operational Transconductance Amplifier	49
		5.1.1.1 Selected Circuit Parameter	50
		5.1.1.2 MOS Transistor Model	51
	5.1.2	Fitness Function	51
	5.1.3	Result	52
5.2	Accuracy And Precision Simulator		55
	5.2.1	Inaccuracy	55
	5.2.2	Hpsice	56
	5.2.3	Interface Of Hspice To Matlab	56
		5.2.3.1 Interfacing	57
	5.2.4	Results	58
5.3	Summ	nary	60

# VI ANALYSIS

6.1	Statistical Analysis		
	6.1.1	Pspice In Window And Dos Mode	62

	6.1.2 Hspice And Pspice	68
6.2	Summary	75

## VII CONCLUSION

7.1	Troubleshoot	76
7.2	Conclusion	78
7.3	Future work	79

REFERENCE	80

83
86
87
88
89
90
98
99
102
103
104
107
108
112
113
119

### LIST OF TABLE

NO	TITLE	PAGES
1.1	Scope of study fields	5
4.1	Different set of length and width of transistor in the	35
	circuit	
4.2	Last generation of optimized width and length of	42
	transistors	
4.3	First generation of width and length of transistors	42
4.4	Last generations for 13 set chromosome data.	45
4.5	First generation for 13 set chromosome data.	45
5.1	Optimization parameters of OTA	50
5.2	Transistor's width and length range	51
5.3	Time consumed	53
6.11	Quantiles of first generation's power objective	63
6.12	Means and Std Deviations of first generation's power	63
	objective	
6.21	Quantiles of first generation's width objective	64
6.22	Means and Std Deviations of first generation's width	64
	objective	
6.31	Quantiles of first generation's output gain objective	64
6.32	Means and Std Deviations of first generation's output	65
	gain objective	
6.41	Quantiles of 100 generation's power objective	65
6.42	Means and Std Deviations of 100 generation's power	65
	objective	

6.51	Quantiles of 100 generation's width objective	66
6.52	Means and Std Deviations of 100 generation's width	66
	objective	
6.61	Quantiles of 100 generation's output gain objective	67
6.62	Means and Std Deviations of 100 generation's output gain	67
	objective	
6.7	Details of data between Pspice in Dos and window	68
	optimization	
6.81	Quantiles of first generation's power objective	69
6.82	Means and Std Deviations of first generation's power	69
	objective	
6.91	Quantiles of first generation's width objective	70
6.92	Means and Std Deviations of first generation's width	70
	objective	
6.101	Quantiles of first generation's output gain objective	71
6.102	Means and Std Deviations of first generation's output	71
	gain objective	
6.111	Quantiles of 200 generation's power objective	72
6.112	Means and Std Deviations of 200 generation's power	72
	objective	
6.121	Quantiles of 200 generation's width objective	73
6.122	Means and Std Deviations of 200 generation's width	73
	objective	
6.131	Quantiles of 200 generation's output gain objective	74
6.132	Means and Std Deviations of 200 generation's output gain	74
	objective	
6.14	Worst, mean and best value in last generation between	75
	Hspice and Pspice	

### LIST OF FIGURE

NO	TITLE	PAGES
2.1	Fundamental pseudo-code of GA	11
2.2	Fitting Op-Amp transistor parameters in chromosome	15
2.3	Genetic Algorithm flow for Transistor's size optimization	16
2.4	Encoding for a transistor width as $10^4 \text{ x } 22$ and using	17
	binary encoding technique.	
3.1	Process Stages of the System	21
3.2	Evolution cycle of the system development	22
3.3	SGA of the system	24
3.4	NSGA_2 optimization path	27
4.1	Schematic of a circuit in Pspice. Output current to be	31
	analyzed at resistor, R2	
4.2	Netlist of the schematic at Figure 4.1.	30
4.3	Matlab will interface with Pspice to do circuit simulation.	31
4.4	Data of circuit loaded into parsedData matrix. These data	32
	are waiting to be analyzed.	
4.5	Extract data from the log file into Matlab, and prepare to	33
	send to chromosome and evaluate its fitness value.	
4.6	Graph of output current, $I_{\text{DS}}$ versus sweeping voltage, $V_{\text{GS}}$	33
	and set of parameter used state in Table 1.	
4.7	Eight chromosome and total of nine variables in one	35
	chromosome before PSPICE simulation.	
4.8	Ninth variable corresponding to eight sets of random	36
	generated data point after analyzed by PSPICE at last	

iteration.

4.9	Fitness function to evaluate output current, $I_D$	37
4.10	Initial setup for GA to optimize circuit at Figure 4.1	38
4.11	Decode of chromosome parameter and evaluate fitness	38
	value	
4.12	Best individual will be evaluated and plot on the graph.	39
4.13	Generation loop in GA optimization system	40
4.14	GA fitness calculation which show the best fitness 1.1794	41
4.15	An op-amp circuit with 8 MOSFET will be optimizing by	43
	GA optimization system.	
4.16	Netlist contents of op-amp schematic	44
4.17	50 generation create by GA optimization system to	45
	evaluate 8 MOSFET width and length	
5.1	Algorithm for interfacing Matlab with Pspice in Dos	48
	mode	
5.2	Algorithm for interfacing Matlab with Pspice in window	48
	mode.	
5.3	Overall genetic circuit optimizer process	48
5.4	Schematic of OTA	49
5.5	Netlist of OTA circuit.	50
5.6	The fitness function	52
5.7	Parameters of circuit optimized by GA in Dos mode.	54
5.8	Parameters of circuit optimized by GA in window mode	54
5.9	Optimization process flow	57
5.10	interfacing path of Hspice	58
5.11	Parameters optimized by NSGA_2 by using Hspice	59
	simulator	
5.12	Parameters optimized by NSGA_2 by using Pspice	59
	simulator	
6.11	First generation of chromosome between Pspice in Dos	62
	and window for power consumption objective.	
6.12	First generation of chromosome between Pspice in Dos	63
	and window for total width objective.	

6.13	First generation of chromosome between Pspice in Dos	64
	and window for circuit gain objective.	
6.21	Last generation of chromosome between Pspice in Dos	65
	and window for power consumption objective.	
6.22	Last generation of chromosome between Pspice in Dos	66
	and window for total width objective.	
6.23	Last generation of chromosome between Pspice in Dos	67
	and window for circuit gain objective.	
6.31	First generation of chromosome between Hspice and	69
	Pspice for the power objective.	
6.32	First generation of chromosome between Hspice and	70
	Pspice for the Total width objective.	
6.33	First generation of chromosome between Hspice and	71
	Pspice for the output gain objective.	
6.41	Last generation of chromosome between Hspice and	72
	Pspice for the power objective.	
6.42	Last generation of chromosome between Hspice and	73
	Pspice for the Total width objective.	
6.43	Last generation of chromosome between Hspice and	74
	Pspice for the output gain objective.	
7.1	Error occurs when ran the software to optimizing	77
	electronic circuit.	
7.2	Real time debugging from Visual Basic.	77

## LIST OF ABBREVIATIONS

GA	-	Genetic Algorithm
AI	-	Artificial Intelligent
SPICE	-	Simulation Program with Integrated Circuit Emphasis
SGA	-	Simple Genetic Algorithm
NSGA_2	-	Improved Non-dominate Sorting Genetic Algorithm
MOS	-	Metal-Oxide-Semiconductor
CMOS	-	Complementary Metal-Oxide-Semiconductor
GUI	-	Graphic User Interface
NAND	-	Number of Individual
MAXGEN	-	Maximum generation
NVAR	-	Number of variable
PRECI	-	Precision of variables
GGAP	-	Generation gap
SBX	-	Simulated Binary Crossover
DC	-	Direct Current
MOSFET	-	Metal Oxide Semiconductor Field Effect transistor
DOS	-	Disk Operation System
ΟΤΑ	-	Operational Transconductance Amplifier
IBM	-	International Business Machine
LM	-	Levenberg – Marguardt

## LIST OF SYMBOLS

$g_m$	-	Gain
<i>w</i> <sub>c</sub>	-	Gain bandwidth
ǿ	-	Phase margin
L	-	Length
W	-	width
Ι.	-	Input current
$K_n$	-	Transistor ratio constant
V <sub>GS</sub>	-	Voltage between Gate and Source
$V_{\text{TN}}$	-	Threshold voltage
В	-	<i>W/L</i> ratio
$U_T$	-	thermal voltage
$C_{max}$	-	Maximum Width allowed by technology
$C_{min}$	-	Minimum Width allowed by technology
W <sub>max</sub>	-	Maximum Width chosen by user
$W_{min}$	-	Minimum Width chosen by user
$k_{1,} k_{2}$	-	Conversion constant
т	-	Number of objective
$\mu_{n}$	-	Surface mobility of electrons
Cax	-	Thickness of the oxide

# LIST OF APPENDICES

APPENDIX TITLE

#### PAGES

А	Main Algorithm	83
В	Initial Variables	86
С	Write	87
D	Interface	88
E	ParseData1	89
F	Readpower	90
G	Evaluate Objective	98
Н	Non-dominate Sort Modified	99
Ι	Crowding Distance	102
J	Tournament Selection	103
K	Genetic Operator	104
Ι	Replace Chromosome	103
М	Graphic User Interface algorithm	107
N	Graphic User Interface	108
0	Journal Under Review	112
Р	Genetic Circuit Optimizer	119

#### **CHAPTER I**

#### INTRODUCTION

Chapter one states the objectives of optimal sizing of transistor parameter by using Genetic Algorithm (GA). A roughly background in this research field will be introduced. Next, scopes of thesis listed in this chapter will layout related topic and literature excluded. Problem statement will clarify problem faced in this field. Lastly, organization of thesis describes structure of all seven chapters.

#### 1.1 Background

Nowadays, many designers struggle in optimizing the transistor's width and length. Usually, optimization process is done by trial and error technique. Therefore, fast and reliable artificial intelligent (AI) tools have become a pressing demand for analog designers.

Transistor size will determine the speed of circuit, energy consumption, total area of circuit, and the delay constraints. So, analog designers are tasked with taking large and small signal models of transistor, and in order to fulfill certain performance requirements, changing the transistors input parameters in accordance with output

constraints. A given output performance measurements like gain,  $g_m$ , unity gain bandwidth,  $w_c$ , phase margin,  $\phi$ , they must correspondingly produce the input MOSFET parameters such as the length, L, and width, W and the input current, I. circuit sizing is the process to translating these parameters into performance measurement. In a modern analog design process, designers need to specify between 10 to 100 input parameters in order to achieve up to 20 output performance measurements.

Automated and manual methods for circuit sizing are in practice. The manual method of circuit sizing will be more time consume. It involves a designer using his or her own accumulated knowledge of circuit behavior to iteratively adjust the component parameters such that they satisfy a set of first order transistor models, and then test the accuracy of these models.

GA programming uses the length and width variables of MOSFET to optimize the size of transistors. From the optimal transistor's size, obtain the optimal output. An algorithm by using GA optimization for transistors sizing was created. Hence, a fast and productive automated circuit analyze and optimization tool help circuit designer to obtain optimal parameters of transistor in the shortest time. Ability of GA, one of the AI will help in automate the optimization. It automatically inserts the input parameter to the respective circuit and generates the corresponding output. From the Input and output generated, circuit parameters are optimized.

Besides, analog design optimization encompasses a large set of specifications. The design mostly relies on the solution from equation of the system. However, thousand of solution may exist when tons of objectives included in the system. The designer will assess which solution fits better according to the relative importance of each objective. Hence, a new strategic formulated by GA to tackle multi-objective optimization [1].

#### **1.2 Problem Statement**

Transistor's size optimization will involve numbers of transistors and single transistor's width and length. GA will randomly generate data set and optimal it base on output response from Pspice. So, a large search space will be need for GA to optimal large set of parameters. Limitation of the search space and narrow it up to a direction will be an important task. Search space always the main problem for optimal large set of parameter. If the direction of the searching technique wrong, then GA will never found the best parameter. It took time to search for the best solution.

Next, encoding technique for chromosome will be the main consideration. Binary encryption is produce precise data, decoding will be easy and process of genetic evolution more reliable. Disadvantage of binary encryption is data too precise and lead to large mutation rate. There are three more encryption techniques such as floating point encryption, gray code encryption and symbol encryption. Different data set or application will use different encryption method and it highly influences optimization result. Choosing these techniques to encode data in chromosome will be a huge problem to create GA optimization system. Reduction of selection error in GA analysis is the second priority problem. The accuracy of GA in selecting proper data set to create best chromosome need to be investigated. When selection and guide GA select better individual to perform evolution. These are the problem faced when the genetic algorithm is developed. Accuracy of output and precision of GA in analyzing data to produce output will be focus in the developed algorithm as well.

There are few circuit performance need to be optimized. Hence, this project will discuss the multi-objective optimization technique. Relationship between two or three objective function are created. Some of the optimal parameter will toward maximum while some will go to minimum. So, intermediate function is created to relate all the parameters to ensure the GA heading toward right direction. Time consumed in the optimization process is one of the concerns of algorithm developed.

3

#### **1.3 Objective**

Main objective of this thesis is to study the artificial intelligent (AI) technology to transistor size optimization. GA will be the main AI technology to be study here. Basic concept of GA will be understood and elements of GA are investigated. Genetic evolution process of GA which contains the basic element of selection, crossover, and mutation are concerned. Suitable technique for encrypt data into chromosome will concentrated also. Different encryption technique produces different optimization quality.

Secondly, after understood GA well, a GA optimization system will be created base on the study. This system wills optimal transistor's width and length in a specific circuit. GA optimization system consists of three stages. There are collect input stage, interface between software stage and optimization stage. GA will first analyze different set of transistor's parameter corresponding to different output by using Pspice simulator. Results from Pspice will feedback to GA to evaluate it fitness value. Fitness value will decide optimal parameter set.

Thirdly, automated and interfacing between Pspice and Matlab will be apriority task. In GA optimization system, interfacing between software are essential. Matlab which contain GA need output data from Pspice. Pspice is one of the accurate circuit simulators which can provide significant output result due to changing of transistor's parameter. Circuit output need to feedback to Matlab in order to continue GA execution. So, a lot of step need in this process. In order to make GA optimization system fast, automate interfacing will be an important task.

Fourth, develop multiple objective optimization algorithm are needed to optimal few specific circuit parameter. There are few outputs of the circuit will be optimized instance of one. In this study, multiple parameters selected are circuit total width, power and output gain. Matlab will be the core system of GA. Hence, different set of Matlab coding need to understand and explore. Matrix presentation, interfacing between data point and mathematic calculation will be use in GA.