FPGA BASED SURVEILLANCE SYSTEM

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To my beloved parents, sisters and brothers and also
my best friends, Rahi and Faizal.

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ABSTRACT

Surveillance system nowadays is no more an option. Many people think surveillance system becomes one of the important things for security reason. In this project, a real-time smart surveillance system will be introduced. With this project, user can monitor surrounding without human supervision because this smart system can detect any movement in the designated area. Everytime the system detected any movement in the area, it will trigger the alarm. This is to overcome the problems by conventional surveillance system which is inflexible and expensive. The old system also needs regular upgrades and modification which leads to higher demand in operator time for viewing and monitoring activities. Based on these problems, several objectives were approach such as designing this system using Field Programmable Gate Array and implementing the algorithms using Xilinx System Generator. This system will integrates detect motion algorithms to perform its function. Spartan 3e FPGA Board will be used as a hardware part and interface for this system. Matlab Simulink and Xilinx System Generator will be a platform to design and testing the algorithms. This project mainly focuses on supervising the environment which may have a potential of trespassing or danger such as museum, bank counter, safe deposit room, shopping complex or car park. The focal point for this project is on implementation issue and not on the algorithms issues. A sophisticated system but low in cost is also the aim of this project.

ABSTRAK

Sistem pegawasan keselamatan bukan sesuatu yang luar biasa pada masa kini. Masyarakat kini menganggap sistem pengawasan adalah satu keperluan untuk tujuan keselamatan. Di dalam projek ini, satu sistem pengawasan pintar masa nyata akan diperkenalkan. Dengan projek ini, pengguna boleh memantau kawasan persekitaran tanpa pengawasan manusia kerana sistem pintar ini akan mengenalpasti sebarang pergerakan di dalam kawasan yang telah ditentukan. Setiap kali sistem mengesan pergerakan, ia akan menghantar isyarat kepada penggera dan penggera akan berbunyi. Ini adalah untuk mengatasi kekurangan yang terdapat pada sistem pengawasan terdahulu dimana ianya tidak fleksibel dan juga mahal. Selain itu, ia juga memerlukan pengubahsuaian dan penambahbaikkan yang kerap dimana ia memerlukan penambahan tenaga kerja bagi tujuan pengawasan dan pemerhatian. Berdasarkan masalah ini, beberapa objektif telah dikenalpasti sebagai panduan dalam menjayakan projek ini seperti penggunaan 'Field Programmable Gate Array' atau FPGA dan juga implementasi 'Xilinx System Generator' sebagai platform bagi algoritma. Sistem ini akan menggunakan algoritma pengesan pergerakan untuk menjalankan fungsinya. Papan 'Spartan 3e FPGA' akan digunakan sebagai perkakasan dan antaramuka. 'Matlab Simulink' dan 'Xilinx System Generator' akan digunakan sebagai platform untuk merekabentuk dan menguji algoritma. Fokus utama penggunaan projek ini adalah pada tempat-tempat yang mungkin dicerobohi dan terdedah pada bahaya seperti muzium, kaunter bank, bilik simpanan deposit, pusat membeli-belah dan tempat letak kereta. Projek ini menekankan aspek penggunaan sistem dan bukan pada aspek pembinaan algoritma. Sistem yang canggih tetapi murah dari segi kos juga adalah isu yang turut ditekankan di dalam projek ini.

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INTRODUCTION

Systems surveillance is the process of monitoring the behavior of people, objects or processes within systems for conformity to expected or desired norms in trusted systems for security or social control. Surveillance in many modern cities and buildings often uses closed-circuit television cameras[1]. It becomes a 'must' for people nowadays to have a surveillance system which work effectively for a security reason. There are many approaches done by researchers since few years ago about surveillance system.

1.1 Objectives

This project objectives were identified after all the possible problems were listed down. Based on these problems, the aim of this project is to design a surveillance system using Field Programmable Gate Array (FPGA). FPGA which has advantages in terms of architecture allow flexibility in implementation. This makes it as a suitable 'candidates' for designing the surveillance system. Besides that, this project has a focus on designing the algorithms using Matlab Simulink and Xilinx System Generator. Matlab Simulink which has appropriate and latest algorithms becomes a fit platform to implement the algorithms. For the System Generator, it is a quick way to convert the Simulink Block Set into the FPGA compatible Block Set. Lastly, the aim of this project is to design a smart surveillance system which can detect human motion in real time.

1.2 Problem Statement

For the past 20 years, the monitoring and surveillance applications have been served by analog technology. CCTV has traditionally been recorded to VCRs (video cassette recorders), and because of its perceived ease of use and manageable price point, analog was probably the right choice at the time of purchase. However, the rise of digital has laid bare analog's many shortcomings. Analog CCTV systems are generally maintenance intensive, offer no remote accessibility, and are notoriously difficult to integrate with other systems. This weaknesses lead to the inflexible and expensive system. In addition, changing security makes regular system upgrades and modification essentials. Conventional surveillance system also demands a lot of operator time for viewing insignificant activities, compared with the very small fraction of their time that is spent viewing those of real importance. An analog system also face a problem with data storage which using the VCR. This type of data storage may lead to a poor recording or data loss. Besides that, capacity of storage and data safety is also an issue when using VCR.

1.3 Scope of Work

In this project, the system specification can be divide into hardware and software part. As for hardware part, FPGA chip will be used as a data processing. The main reason of the appliance is faster data processing compared to the other Digital Signal Processing chip. Besides that, this project will be implemented the Xilinx Spartan 3e FPGA board. This board allows high volume application, reduce die size and cost and easily migrate to different densities. For the software part, Matlab Simulink will be the first platform to generate the Block Set. This Block Set then, will be converting into FPGA compatible Block Set using Xilinx System Generator. Though there are many other applications can be used to implement and generate the algorithms, this system will using Matlab Simulink because it has wider scope in video image processing and latest algorithms about motion detection. And for System Generator, it can convert the

algorithms in Matlab directly to FPGA compatible Block Set. This surveillance system will detect human motion in real-time environment.

1.4 Methodology

Procedures or process for this project will be initiate from acquiring the algorithm from internet or book resources. In this project, the algorithms from Matlab Simulink will be used for detect motion in real-time background. This algorithm is modified in terms of input pixels or data format. After that, it will be combined together and tested to see the performance. Once the integration is successful, it will be converted to the FPGA compatible Block Set using System Generator. Output will be downloading into Spartan 3e FPGA Board for testing. Any problems occurred during testing will be troubleshoot before implement it at the real situation.

1.5 Outline

In this report, it was divided into five chapters; introduction, literature review, methodology, results and discussion and lastly conclusion and suggestions. In chapter one, overview about the project such as introduction to FPGA, scopes, objectives and brief review about methodology were stated.

In the literature review, all the past years project and research which related to the project was discussed. After that, all the information and data gathered were compared to the FPGA Based Surveillance System project to identify the strengths of this project.

For methodology, all the methods, hardware and software used in this project were verified. For this project, Spartan 3E FPGA Board is used as a hardware, while for software, Matlab Simulink, Xilinx System Generator and iMPACT were used. Matlab Simulink acts as a platform to modify the algorithm, while System Generator is used to

generate the .xsf file which is compatible file for the board. iMPACT is used to download the program into the board.

In chapter 4, all the results were discussed to justify any problems throughout the process of developing the system. In the last chapter, overall findings in this project are concluded and any suggestions for future expansion were verified. These suggestions can be used for references and also as an improvement for anyone who wishes to develop a sophisticated surveillance system.

BAB 2

Literature Review

Surveillance system becomes a system which started to become a higher demand by user. Since there are so many unlawful and illegal activities happen nowadays, people become unsecured and search something that can improve their safety and security. There are a lot of brand and manufacturer that produced surveillance system since 20 years ago. As a user, we should know either the system we used giving the most reliable and efficiency system or not.

2.1 Surveillance system

Several typical high-level design issues for commercial CCTV surveillance systems, along with how they affect system design are shown in Table 2.1. Key among these is the size of the area to be put under surveillance and the number of security personnel available to do the job. The larger the area, the more cameras, cabling, and recording equipment are needed[2].

Table 2.1: CCTV Surveillance System Design Issues

System Issue	Impact on System Design
How large is the total area to be monitored and how many surveillance personnel are available for monitoring?	Impacts number of camera, need for camera pan, zoom, and tilt features, number of manned surveillance stations, and degree of automation.

System Issue	Impact on System Design
How critical is the area to be monitored, and how continuous must be the surveillance?	Impacts the degree to which cameras can be multiplexed into a single recording device.
Will video be monitored locally, remotely or both?	Remote monitoring may require video transmission capability.
What is the environment of the area to be monitored (e.g: indoor or outdoor, day or night)?	Impacts camera light sensitivity, area lighting requirements, system false alarm rates.
How often must recorded video be archived video retained?	Influences type, capacity, and physical size of recording and/or archival media and archive physical storage requirements.
How will recorded video be used (e.g: for legal prosecutions)?	Influences minimally acceptable levels of video quality and resolution.
What other types of activity must be monitored along with video (e.g: audio, door openings and closings)?	Impacts event time and location stamping; should be possible to correlate video with other recorded activities.

In addition, since security personnel are usually highly limited in number, it is important that the system incorporates features that make them as efficient as possible. Such features include automated camera control & multiplexing, video motion alarm detection, and high-resolution, multi-camera video display.

2.1.1 Analog Surveillance System

A typical commercial CCTV surveillance system today is based largely on analog signal technology. An audio/video multiplexed selects the analog audio and/or video output from one of multiple cameras. The cameras may be either color or monochrome, although monochrome is still the most prevalent. The cameras may also have remotely controlled pan, zoom, and tilt (PZT) capabilities, as well as built-in microphones.

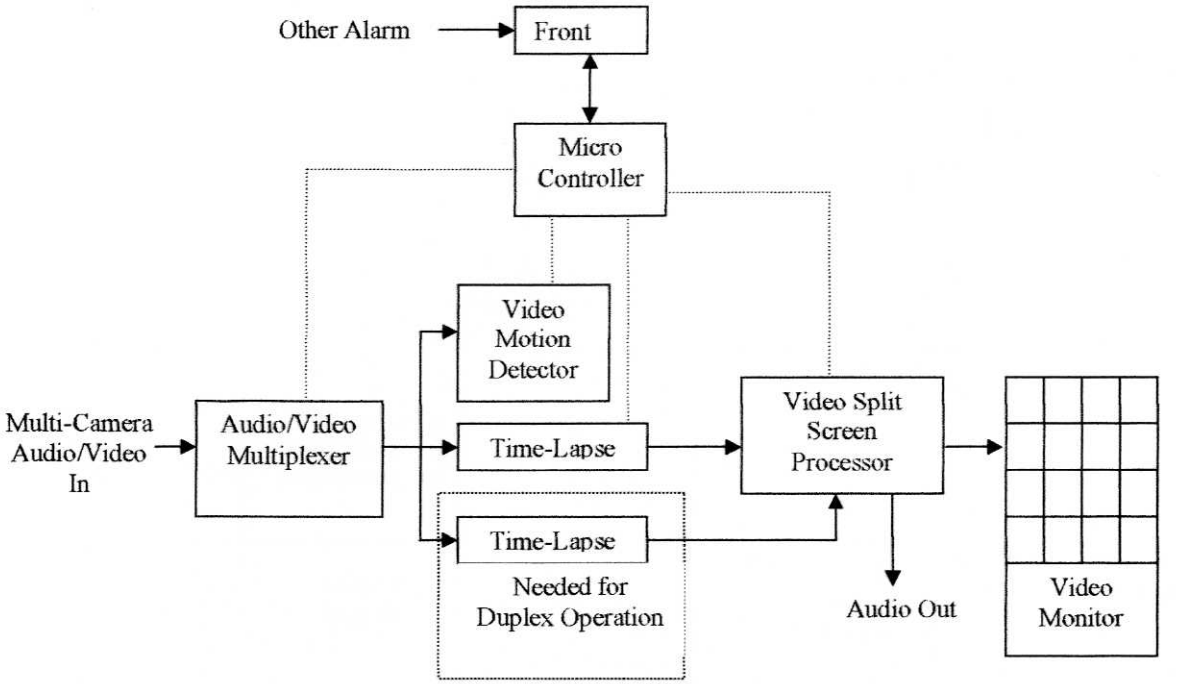

Figure 2.1: Typical CCTV Surveillance System Based on Analog Technology

Figure 2.1 shows the typical surveillance system which using the analog technology. The multiplexer is a key system component because it allows the cameras to share the other surveillance system components, thereby making the system economically feasible. As shown in Figure 2.1, the video output from the multiplexer feeds one or more time-lapse VCRs that record and play back the video[2].

This video can be recorded or played in frames, fields, or continuously, to and from a videotape, a video motion detector, and a video split screen processor which displays the video on a video monitor. Some time-lapse VCRs can also digitally tag recorded frames with the ID numbers of the cameras they were captured from. Some systems also support simultaneous video recording and playback through the use of two VCRs[2].

2.1.2 Digital Surveillance System

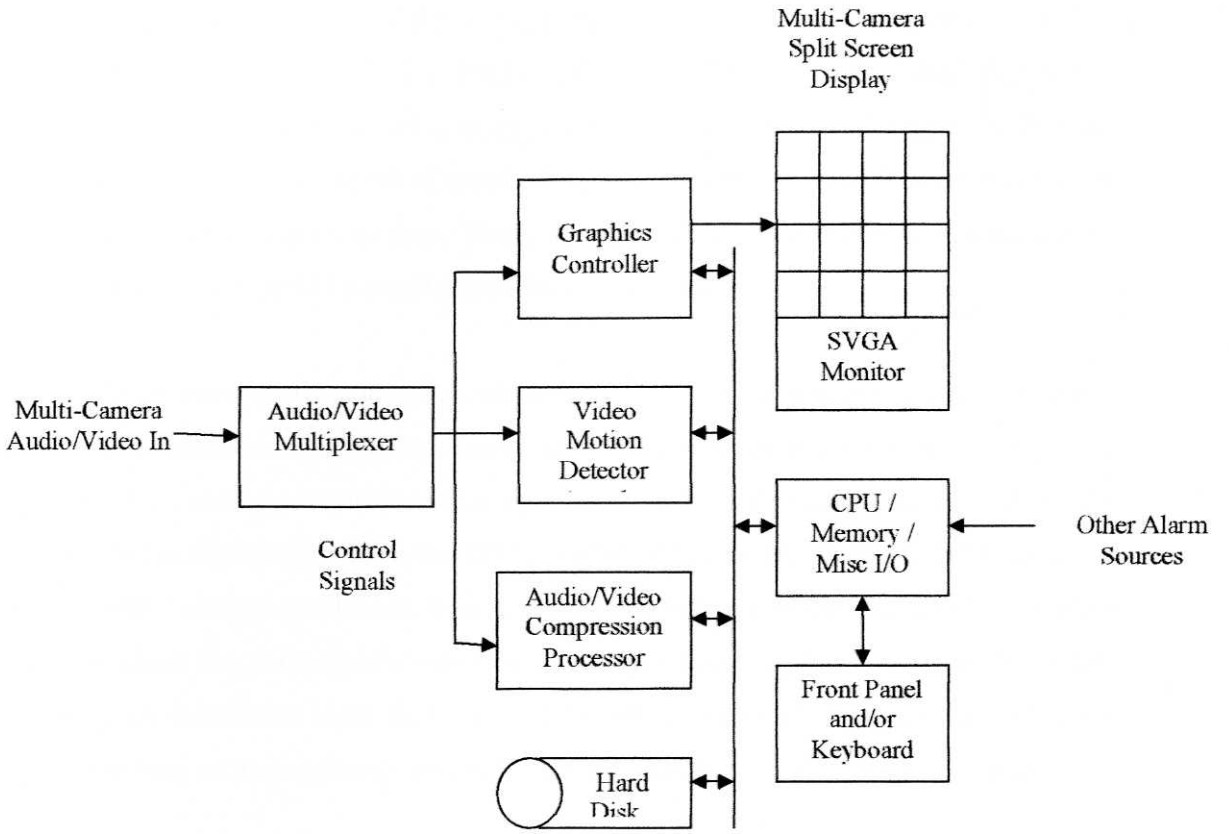

Figure 2.2: Typical CCTV Surveillance System Based on Digital Technology

Video compression is generally accomplished in two stages. The first stage, which is optional, reduces the resolution of the digitized input video. In some cases, customer requirements do not permit this; however, in many cases, a reduction from full to one-quarter resolution (e.g. 352 x 240, also known as "SIF") is acceptable. Also, video images consist of both luminance and chrominance components, with the image bytes being evenly split between them; this is referred to as 4:2:2 chrominance sampling.

In many cases, the resolution of the chrominance component can be reduced by twice as much as the corresponding luminance component with few visual side effects. For example, in a SIF resolution image with so-called 4:2:0 chrominance sampling, only one-third of the bytes corresponds to the chrominance component[2].

The next stage applies a compression algorithm to the resolution-reduced digital video. Many different algorithms have been used for this purpose, including international standards such as JPEG, MPEG, H.261/263 and other proprietary algorithms such as wavelets and customized derivatives of JPEG. Compared with users of proprietary algorithms, users of standardized algorithms generally have a much wider range of industry sources to draw from. In many cases, decompression software for algorithms such as MPEG is available at little or no cost.

Since most real-world video sequences exhibit high degrees of frame-to-frame correlation, interframe algorithms such as MPEG and H.261 have the capacity to dramatically reduce bandwidth and storage requirements over intraframe algorithms like JPEG. This is especially true in the case of surveillance video, where in most cases; the video doesn't change much over time, especially in the case of stationary cameras. Even in cases where the surveillance video scene changes fairly regularly, say, due to camera panning, an interframe algorithm can still deliver exceptional compression with good quality as long as it can effectively track scene motion from one frame to the next[2].

This motion tracking function, called motion estimation, is probably the single largest contributor to the effectiveness of the MPEG and H.261 compression algorithms, but not all implementations of these algorithms pay it the same respect due its high computational requirements. Note also that motion estimation is distinct from the video motion detection function common to both analog and digital surveillance systems, although they do have computational similarities.

2.2 Detect Motion Algorithm

Detection of a human based only on motion may, at first, seem far-fetched. Do the motions of the limbs contain enough information to infer the presence of a human? Experiments which carried out by Johansson in the 1970's demonstrated the answer to be 'Yes'. Johansson filmed moving humans in a pitch-black room, the only visual

indicator being a white point of light attached to each limb. He showed that a viewer watching the film could easily identify human motion, despite the absence of visual cues such as shape, texture, brightness, and color.

An example of these Johansson points is shown in Figure 2.3. It has been further demonstrated that specific individuals or genders can be recognized in the same manner. Given that the human brain can effortlessly recognize this motion, it is conceivable that a computer algorithm could do the same. In addition, single points of motion as used in the Johansson experiment can be efficiently represented on a computer. Unlike pure image processing, which must deal with large numbers of pixels at each time step, this Johansson motion can be specified by a handful of points, each represented by a 2-D position and a 2-D velocity at any given time. This gives us hope that a simple, effective algorithm is achievable[3].

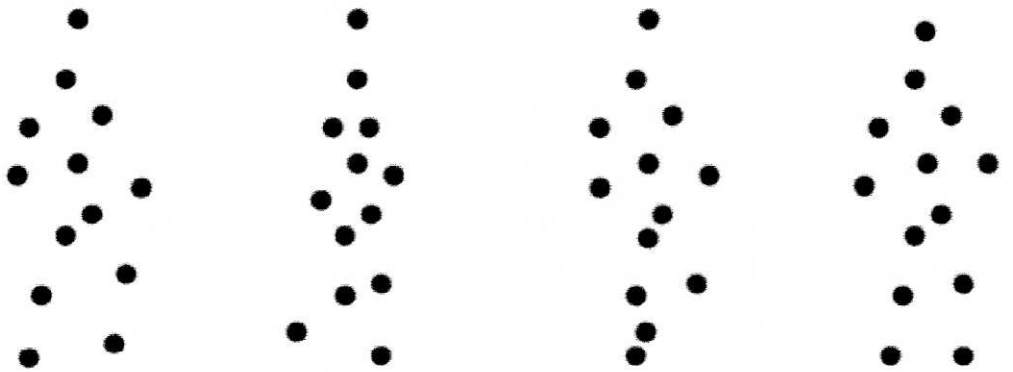

Figure 2.3: An image of Johansson point display the image of human waking

2.3 FPGA versus DSP

Due to advances in semiconductor technology, we are seeing ever more complex Digital Signal Processing (DSP) algorithms, protocols, and applications become realizable. This, in turn, is rapidly increasing the complexity of these systems and products. As the complexity of systems increase, system reliability is no longer solely

defined by the hardware platform reliability, typically quantified in MTBF (mean time between failure) calculations. Today, system reliability is being increasingly determined by hardware and software architectures, development and verification processes, and the level of design maintainability[4].

One of the fundamental architecture issues is the type of DSP platform. Digital signal processing functions are commonly implemented on two types of programmable platforms; DSPs and Field Programmable Gate Arrays (FPGAs). DSPs are a specialized form of microprocessor, while the FPGA is a form of highly configurable hardware. It has generally come to be expected that all software, (DSP code is considered a type of software) will contain some bugs and that the best one can do is to minimize them. By comparison, FPGA designs tend to be much less frequently updated, and it is generally a rather unusual event to for a manufacturer to issue a field upgrade for an FPGA configuration file. The reason is that reliability and maintainability is much better in FPGA implementations compared to those using a DSP[4].

The engineering development process for DSPs and FPGAs are dramatically different. There is a fundamental challenge in developing complex software for any type of processor. In essence, the DSP is basically a specialized processing engine being constantly reconfigured for many different tasks, some digital signal processing, others more control or protocol oriented tasks. Resources such as processor core registers, internal and external memory, DMA engines, and IO peripherals are shared by all tasks, often referred to as "threads" like shown in Figure 2.4.

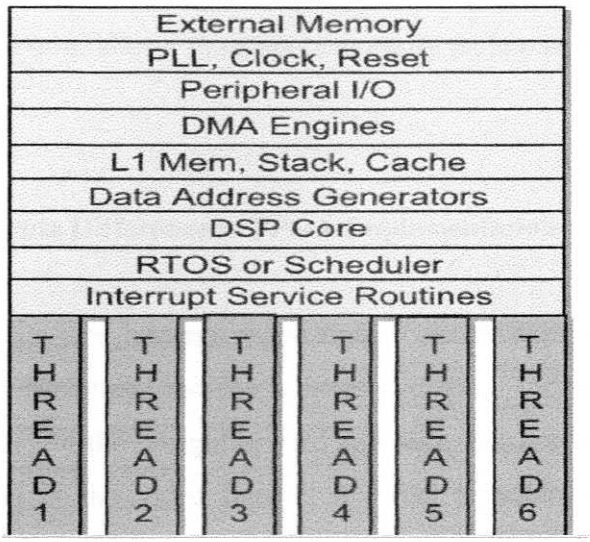

Figure 2.4: The architecture of DSP

This creates ample opportunities for the design or modification of one task to interact with another, often in unexpected or non-obvious ways. In addition, most DSP algorithms must run in "real-time", so even unanticipated delays or latencies can cause system failures.

An FPGA is a more native implementation for most digital signal processing algorithms. Each task is allocated its own resources and runs independently. This intuitively makes more sense, to process an often continuously streaming signal in an assembly-line like process, with dedicated resources for each step. As the FPGA is inherently a parallel implementation, it offers much higher digital signal processing rates in nearly all applications[4].

FPGA resources assigned can be tailored to the requirement of the task. The tasks can be broken up along logical partitions. This usually makes for a well defined interface between tasks, and largely eliminates unexpected interaction between tasks. Because each task can run continuously, the memory required is often much less than in a DSP, which must buffer the data and process in a batch fashion. As FPGAs distribute memory throughout the device, each task is most likely permanently allocated the necessary dedicated memory. This achieves a high degree of isolation between tasks.