ANALOG VERY LARGE SCALED OF INTEGRATION (VLSI) TESTING AND ANALYSIS OF COMBINATIONAL CIRCUITS USING COMPUTER-AIDED DESIGN (CAD) TOOLS

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To my beloved mom and dad.

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ABSTRACT

This project is to perform Analog Very Large Scaled of Integration (VLSI) testing and the analysis of combinational circuits using Computer-Aided Design (CAD) tools. The primary objective is to analyze the outputs of the combinational circuits to their inputs by using analog concept in order to study the effects of the parametric variation of the circuits to their performance. The circuits used in the project are simple circuits (NOT, AND, OR, NOR and NAND gates) and complex circuits (half-adder and 2-to-4 decoder). The project can be used to detect the defective analog VLSI devices with the analysis perform. The simulation on the combinational circuits is implemented in Multisim using fault model based testing while the analysis is performed using Matlab. The fault free output waveform of the analog combinational circuits is compared with the faulty circuit. With the simulation results and the waveform plotted on the Matlab graphical user interface (GUI), the circuits are analyzed to explain the reasons of obtaining faulty outputs. Besides that, the GUI is used as interface for users to explore and understand the analog combinational circuit testing.

ABSTRAK

Projek ini bertujuan untuk menjalankan ujikaji Integrasi Skala Sangat Besar (VLSI) dan analisis menggunakan alat Reka Bentuk Komputer (CAD). Objektif utama projek ini adalah untuk menganalisis keluaran litar gabungan kepada pemasukan litar dengan menggunakan konsep analog. Tujuannya adalah untuk mengkaji kesan perubahan parameter-parameter ke atas prestasi litar tersebut. Litar yang digunakan dalam projek termasuk litar mudah (pintu NOT, AND, OR, NAND dan NOR) dan litar kompleks (pertambah separuh dan alat pembaca sandi 2-kepada-4). Projek ini boleh digunakan untuk mengesan kecacatan alat VLSI analog. Simulasi ke atas litar gabungan dilaksanakan dalam Multisim dengan meggunakan ujikaji berdasarkan model kecacatan manakala analisis dijalankan dengan meggunakan Matlab. Gelombang keluaran tanpa kecacatan litar gabungan analog dibandingkan dengan gelombang litar yang mempunyai kecacatan. Litar dianalisis untuk menjelaskan sebab keluaran yang mempunyai kecacatan diperolehi berdasarkan keputusan simulasi dan gelombang yang dilukis dengan perantaramuka pengguna grafik (GUI) Matlab. Selain itu, GUI digunakan sebagai perantaramuka untuk pengguna mengkaji dan memahami ujikaji litar gabungan analog.

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LIST OF ABBREVIATION AND SYMBOL

A_{ol}	-	Open loop DC gain
B	-	base
BJT	-	bipolar junction transistor
C	-	collector
CAD	-	Computer-Aided Design
CMRR	-	Common mode rejection ratio
dB	-	decibels
Demux	-	demultiplexer
E	-	emitter
GBW	-	Gain bandwidth product
GUI	-	Graphical User Interface
GUIDE	-	graphical user interface development environment
I_B	-	Input bias current
IC	-	integrated circuit
m	-	milli
Matlab	-	MATrix LABoratory
MOSFET	-	Metal Oxide Semiconductor Field Effect Transistor
Mux	-	Multiplexer
n	-	nano
Op-amp	-	operational amplifier
PSRR	-	Power supply rejection ratio
SR	-	Slew rate
UTeM	-	Universiti Teknikal Malaysia Melaka

Vos	-	Input offset voltage
SPICE	-	Simulation Program with Integrated Circuit Emphasis
Vin	-	input voltage
VLSI	-	Very Large Scaled of Integration
Vout	-	output voltage
µ	-	micro

LIST OF APPENDIX

CHAPTER I

INTRODUCTION

This chapter introduces this project in which the project is Very Large Scaled of Integration (VLSI) based. The circuits use in the project is combinational circuit and software involves are Multisim and MATrix LABoratory (Matlab). Besides that, the objectives, problem statements and scopes of project are described in this chapter. Next, the methodology shows the implementation of the project and the contents of each chapter are introduced in thesis outline.

1.1 Introduction

This project is conducted based on the principle of VLSI technology. In order to achieve successful analog device testing and modeling, the characteristics of the circuit need to study. The combinational circuit is implemented at the transistor level instead of logic gate level to observe the effects of parametric variation to the performance of the circuit. In this project, Computer-Aided Design (CAD) tools are used where the circuit simulation is performed in Multisim and the analysis of the results from circuit simulation is implemented in Matlab. At the end of the project, a Graphical User Interface (GUI) is created to provide an interface to explore and analyze the analog circuit testing.

1.2 Objective

There are five objectives to be achieved in this project:

- To characterize combinational circuits.
- To study the effects of circuit's parameters to its performance.
- To perform the analog testing.
- To analysis the result of testing.
- To create a GUI to provide users a media to explore and analyze the analog circuit testing.

1.3 Problem Statement

Nowadays, in VLSI technology in electronics field, it is possible to produce a die with millions of transistors on it so that a total system can be produced on a single chip. The chips are developed with decreasing physical dimensions of the transistors. The reduction in physical dimensions of the transistors will then increases the probability of manufacturing defect in the integrated circuit (IC) and hence results in a faulty chip. The entire chip might not properly function even though only a transistor is defected. For instance, the chip will not function at the required operating frequency due to only one faulty transistor in a chip. Hence, testing is required to guarantee fault free products as the defect chips are disallowed during the manufacturing process.

1.4 Scope

The project is focused primarily on the characterization of combinational circuits, the effects of the parameters of the circuits to its performance, analog testing and the analysis of the results of the testing. The project is software-based where the Multisim is used to conduct the circuit simulation and Matlab is used to perform circuit analysis. The circuit analysis is implemented in Matlab environment which is

graphical user interface (GUI). Besides that, the GUI is functioned as a user interface to explore and analyze analog circuit testing through it.

1.5 Methodology

The project is started with the literature review on the VLSI testing and the combinational circuit. After that, several combinational circuits are chosen and constructed in Multisim. The circuits are simulated using appropriate VLSI testing. The circuit simulation is started with the simple circuits which are basic logic gates and some others logic gates and following by more complex circuits. The circuits are simulated for fault free and also with their resistors opened and shorted. The simulation results are then collected for used in Matlab GUI.

The next step is to come out a GUI using Matlab. The GUI is created and designed by using the combination of GUI layout design editor as well as source code editor. From the GUI, it shows the waveforms of the testing results after the button of the desired circuit is being selected. From the waveforms, the testing results are analyzed. Also, the testing results of the fault free circuits are compared with their circuits with parametric variation.

1.6 Thesis Outline

This thesis is wrote to provide information about the final year project perform by final year student of Universiti Teknikal Malaysia Melaka (UTeM). There are five chapters contains in this thesis.

Chapter 1 gives the introduction and the objectives of the project. Besides that, there is also the problem statement, the scope of the project and the short description of the methodology as well as the thesis outline includes in this chapter.

Chapter 2 covers the literature review of the project. Combinational circuits and several examples of this category of circuit are mentioned here. Also, analog VLSI testing and its types are discussed in this chapter. Another topic to be covered here is the CAD tools used in the project.

Chapter 3 provides the methodology of the project and the reason for choosing these methods. Also, the project flow is shown in this chapter.

Chapter 4 delivers the results of the project which included the simulation results and the analysis on it. Besides that, the discussion included problems faced, results from circuit simulation and analysis are presented in this chapter.

The last chapter is the conclusion of the project. Other than that, there are some suggestions for future development of the project.

1.7 Conclusion

This chapter has covered the introduction, objectives and also problem statement of this project. Besides that, the scope of this project is clearly defined and a brief description of the methodology has added in this section. The literature review of this project will be presented in the next chapter.

CHAPTER II

LITERATURE REVIEW

This chapter explains the literature review of the project which including the introduction of several combinational circuits, several test methods of the VLSI testing and the CAD tools use to implement the project. A number of circuits discussed in this chapter are chosen for simulation and analysis. In addition, the test methods are compared in order to choose the one that is more applicable for the circuits.

2.1 Combinational Circuit

Generally, there are two basic categories of circuits in electronics field which are combinational circuit and sequential circuit. Different from sequential circuit where the outputs is depend on the current and past inputs, combinational circuit using only the current inputs to produce outputs [3]. The inputs are combined in someway to produce the outputs [3].

Combinational circuits are build from the basic AND, OR and NOT gates as well as some others logic gates included NAND, NOR, XOR and XNOR gates by combining these gates in a huge variety of ways. Table 2.1 is the truth tables of the logic gates.

From Table 2.1, it shows that the OR gate will gives high output when at least one of the inputs is high. However, it is different for AND gate. AND gate produces high output only when all of the inputs are high. NOT gate is also known as inverter. Same as its name, NOT gate always gives the output which is the inversion of its input. For NOR gate, it inverts the output of OR gate. It produces high output only when all of the inputs are low. NAND gate shows low output when all of the inputs are high. When both of the inputs are same, XOR gate will shows low output. On the other hand, XNOR gate will gives high output as both of the inputs are same.

Table 2.1 Truth Tables of Logic Gates

Logic Gate	Truth Table		
	Input		Output
OR	0	0	0
	0	1	1
	1	0	1
	1	1	1
AND	0	0	0
	0	1	0
	1	0	0
	1	1	1
NOT	0		1
	1		0
NOR	0	0	1
	0	1	0
	1	0	0
	1	1	0
NAND	0	0	1
	0	1	1
	1	0	1

	1	1	0
XOR	0	0	0
	0	1	1
	1	0	1
	1	1	0
XNOR	0	0	1
	0	1	0
	1	0	0
	1	1	1

The logic gates in gate level and their corresponding transistor level are implemented in Table 2.2. NOT gate and single transistor NOR gate use only a transistor whereas double transistor NOR gate, OR, AND and NAND gates use two transistor in their circuit.

Table 2.2 Logic Gates

Logic Gate	Gate Level	Transistor Level
OR