A STUDY ON ISOLATION PERFORMANCE OF PIN DIODE WITH DEFECTED GROUND STRUCTURE (DGS) FOR RF SWITCH

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Faculty of Electronic and Computer Engineering
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FAKULTI KEJURUTERAAN ELEKTRONIK DAN KEJURUTERAAN KOMPUTER

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Sesi Pengajian : 2010/2011

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Date : 3 May 2011

Especially for

My beloved mom and dad

My family

My supervisor
Mr Noor Azwan bin Shairi

All beloved friends

Thanks for everything...

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ABSTRACT

This project aims to study the performance of isolation with DGS under PIN Diode for SPST switch design. This project involves with the studies of the background of Defected Ground Structure (DGS), PIN diode and the isolation issue in RF switch. There has been an isolation issue occurs in RF switch. The PIN diode with parasitic capacitance is causing degradation of isolation performance in RF switch and DGS (Defected Ground Structure) has a potential to remove the parasitic capacitance. Nowadays, there has been an increasing interest in studying microstrip lines that prohibit wave propagation in certain frequency bands using defected ground structure (DGS). DGS is implemented by modifying guided wave where it changes the propagation characteristic. DGS is realized by etching only a few areas on the ground plane under the microstrip line. Advanced Design Software (ADS) software will be used for PIN Diode and DGS circuit and layout modeling and then will be fabricated on the FR4 board. Once the prototype has been finish, the measurement parameter will be tested which then measured the isolation performance.

ABSTRAK

Projek ini bertujuan untuk mempelajari persembahan sisihan dengan Defected Ground Stucture(DGS) yang diletakkan di bawah PIN diod dalam reka bentuk suis SPST. Projek ini merangkumi kajian kerja untuk latar belakang Defected Ground Structure (DGS), PIN diod dan isu sisihan dalam suis RF. PIN diod yang mengandungi kapasitan parasitik menyebabkan penurunan dalam persembahan sisihan dalam suis RF dan Defected Ground Structure(DGS) mempunyai keupayaan untuk menyingkirkan kapasitan parasitik ini. Pada masa kini, pembelajaran garis mikrostrip yang menghalang perambatan gelombang dalam lingkaran frekuensi tertentu dengan menggunakan DGS kian meningkat. DGS dilaksanakan dengan mengubahsuai panduan gelombang di mana ia mengubah ciri-ciri perambatan. DGS direalisasikan dengan mengores beberapa tempat yang tertentu di permukaan dasar rata di bawah garis mikrostrip. Advanced Design Software (ADS) akan digunakan untuk membuat simulasi litar dan susun atur PIN diod dan DGS dan kemudiannya akan direalisasikan di atas papan litar bercetak FR4. Akhir sekali, ujian akan dilakukan ke atas prototaip yang telah disiap cetak di atas papan FR4 untuk memperolehi hasil sebelum persembahan penyisihan dianalisa.

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LIST OF ABBREVIATIONS

ADS	Advanced Design Software
DGS	Defected Ground Structure
SPST	Single Pole Single Throw
DC	Direct Current
FET	Field Effect Transistor
RF	Radio Frequency
PCB	Printed Circuit Board
SMA	SubMiniature version A
UV	Ultra- Violet

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CHAPTER I

INTRODUCTION

1.1 Project Background

There has been an increasing interest in studying microstrip lines that prohibit wave propagation in certain frequency bands using defected ground structure (DGS). DGS is implemented by modifying guided wave where it changes the propagation characteristic. DGS is realized by etching only a few areas on the ground plane under the microstrip line. This project will study the performance of isolation based with dumbbell shaped DGS under PIN Diode for SPST switch design.

1.2 Problem Statement

There are has been an isolation issue occurs in RF switch. The PIN diode with a parasitic capacitance is causing degradation of isolation performance in RF Switch based with dumbbell shaped DGS (Defected Ground Structure) has a potential to remove the parasitic capacitance.

1.3 Project Objective

This project will study the isolation performance based with dumbbell shaped Defected ground structure (DGS) under PIN diode for SPST switch design.

1.4 Project Scope

The scope of this project:

i. To study the background of Defected Ground Structure (DGS), PIN diode and the isolation issue in RF switch.
ii. Get familiar with the Advanced Design System Software (ADS).
iii. PIN diode and Defected Ground Structure (DGS) modeling.
iv. A simulation and analysis on PIN Diode with Defected Ground Structure (DGS) will be done by using Advanced Design System Software (ADS).

1.5 Thesis Outline

Chapter 1 is about project background for this paper, project statement, objectives, and scope of works. Chapter 2 defines the information and theory relates to this project and also the overview of the component involved. Chapter 3 will explain on the project implementation. It will discuss details on the tools and steps involved during performance of the projects. First and the most important to make this project flow smoothly is the project flow chart.

Chapter 4 will present all the project results regarding the experiments and test that have been done. There are three topologies that had been compared which SPST switch PIN diode that was connected with the dumbbell- shaped defected ground structure of dimensions 8mm, 12 mm, and 14mm with and without gap. This chapter also discusses which topologies is the best to design the RF switch. Chapter 5 is about to make a conclusion and recommendation for future works related to this study.

CHAPTER II

LITERATURE REVIEW

2.1 PIN Diode

The most important property of the PIN diode is the fact that it can, under certain circumstances, behave as an almost pure resistance at RF frequencies, with a resistance value that can be varied over a range of approximately 1Ω to 10 kΩ through the use of a DC or low frequency control current. When the control current is varied continuously, the PIN diode is useful for leveling and amplitude modulating an RF signal. When the control current is switched "on" and "off" or in the discrete steps, the device is useful for switching, pulse modulating, attenuating, and phase shifting of an RF signal [6].

2.1.1 Characteristics of the PIN diode

A PIN diode structure got its name from the device construction that consists of a heavily doped p-region and a heavily doped n-region separated by a thin layer of a high resistivity material that is nearly intrinsic. The nearly intrinsic layer is called π-type or v-type depending on whether the conductivity is p-type or n-type, respectively. The thickness of the high-resistivity layer, which is usually of v-type, is 10-200 μm. At zero bias, two separate space-charge regions are formed at the p-I and i-n junctions of a PIN diode just inside the highly doped p and n regions due to the diffusion of holes and electrons across the junction. In the case of an ideal diode, the intrinsic layer has no impurities; that is, it is totally depleted of mobile charge carriers. When a reverse bias is applied, (n electrode positive and p electrode negative) the space-charge regions in the p and n layers become wider and the diode gives rise to very high impedance in this state [6].

When a forward bias is applied to the diode, carrier injection takes place into the intrinsic layer. Electrons are injected into the intrinsic v or π layer from the n-layer and holes are injected from the p-layer. If the intrinsic thickness is less than the diffusion lengths or carrier life times of the injected mobile carriers, the injected carries have uniform distribution and both electrons and holes have equal concentrations. In this conditions, the resistivity of the intrinsic layer drops as the forward bias is increased [2].

The diffusion of carriers reduces the resistivity of the intrinsic layer and it drops further with the increasing forward bias voltage and the diode offers very low impedance in this state. Thus a PIN diode works as a switching device, open circuited in the reverse-biased state and short circuited in the forward-biased state. To achieve a low impedance state of PIN diodes, it is essential that the lifetime of mobile carriers in the intrinsic layer be greater than the time period of the operating frequency [6].

Simplified lumped element equivalent circuits of a packaged PIN diode in reverse- and forward-bias conditions are shown in Figure. L_s and C_p represent the series inductance and shunt capacitance of the package, R_s is the ohmic contact series resistance, and C_j is the junction capacitance of the diode. Under forward bias condition

R_f is the total diode resistance consisting of intrinsic layer resistance and ohmic contact resistances. Typical equivalent circuit model parameters of a package PIN diode are $L_s \cong 0.3$ nH, $C_p \cong 0.3$ pF, $R_s \cong 0.2\Omega$, $C_j \cong 0.02$ pF, and $R_f = 1\Omega$. The forward bias current is about 10 mA and reverse breakdown voltage at 10 μA is about 50V.

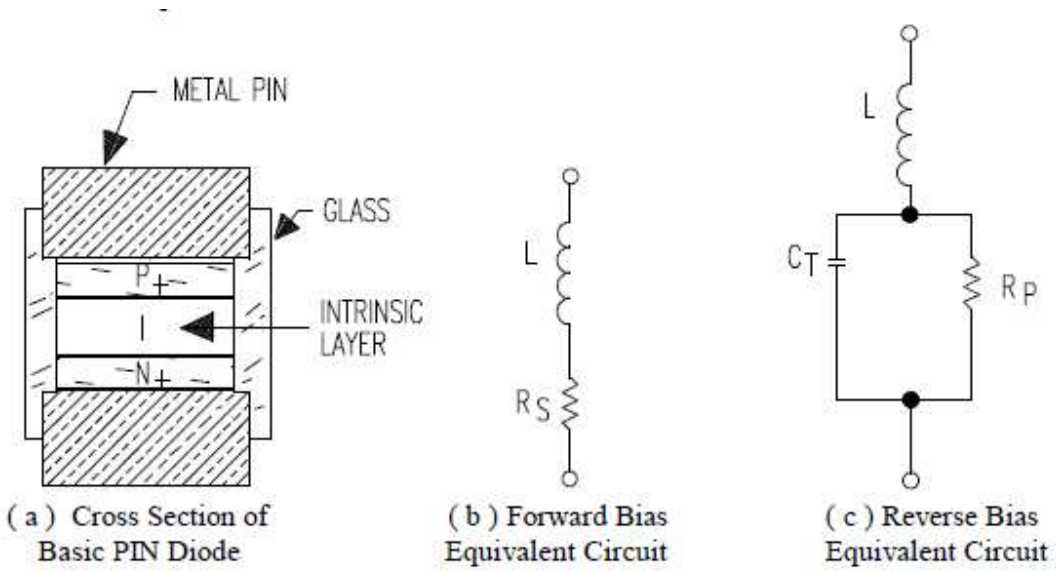

Figure 2.0: PIN diode and Corresponding Equivalent Circuit [6]

2.1.2 PIN Diode Applications as switches

PIN diodes are commonly used as switching elements to control RF signals. In these applications, the PIN diode can be biased to either a high or low impedance device state, depending on the level of stored charge on the I region. A simple unturned single-pole single throw (SPST) switch may be design using either a single series or shunt connected PIN diode, as shown in Figure 2.1 and Figure 2.2[6]. The series connected diode switch is commonly used when minimum insertion loss is required over a broad frequency range. This design is also easier to physically realize using printed circuit techniques, since no through holes are required in the circuit board. A single shunt mounted diode will, on the other hand, produce higher isolation values across a wider

frequency range and will result in a design capable of handling more power since it is easier to heat sink the diode.

Isolation is defined as the ratio of the power delivered to the load for an ideal switch in the ON state to the power delivered to the load when the switch is in the "OFF" state [4]. This also is expressed in Decibels and is a positive quantity. There are several techniques one can improve the isolation in switches, including using low OFF state capacitance FETs, distributed with tuning inductors, and realizing band-rejection filter in the operating frequency range. Basically, in these schemes either the OFF state capacitance of the switching devices is tuned out or their effect is minimized. In all these schemes, the insertion loss of the switches more or less remains the same. Most switches circuits designed at RF and low end of the microwave frequency band generally do not use any matching or tuning elements. They work down to DC, however as the frequency increases, the insertion loss increases and the isolation decreases due to finite value of the capacitance of the switching device in the OFF state [4].

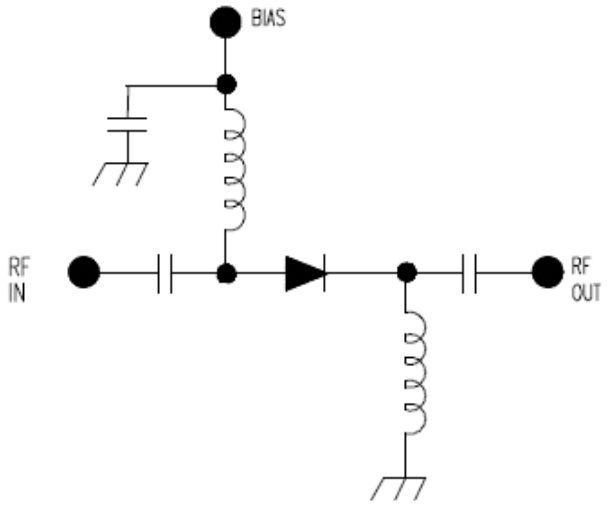

Figure 2.1: Series SPST Switch [6]