

DESIGN AND CHARACTERIZATION OF SILICON-ON-INSULATOR (SOI)  
METAL – OXIDE -- SEMICONDUCTOR FIELD EFFECT TRANSISTOR  
(MOSFET)

NURASMA ANSARI BINTI MOHD NAIM

UNIVERSITI TEKNIKAL MALAYSIA MELAKA (UTeM)

DESIGN AND CHARACTERIZATION OF SILICON-ON-INSULATOR (SOI)  
METAL – OXIDE -- SEMICONDUCTOR FIELD EFFECT TRANSISTOR  
(MOSFET)

NURASMA ANSARI BINTI MOHD NAIM

A thesis submitted in partial fulfillment of the requirements for the award of the  
degree of Bachelor of Electronic Engineering (Computer Engineering)

Faculty of Electronic and Computer Engineering  
Universiti Teknikal Malaysia Melaka

MAY 2011



UNIVERSITI TEKNIKAL MALAYSIA MELAKA  
FAKULTI KEJURUTERAAN ELEKTRONIK DAN KEJURUTERAAN KOMPUTER

BORANG PENGESAHAN STATUS LAPORAN  
PROJEK SARJANA MUDA II

Tajuk Projek : .....

Sevi Pengajian : .....

Saya .....  
(HURUF BESAR)

mengaku membenarkan laporan Sarjana Muda ini disimpan di Perpustakaan dengan syarat-syarat kegunaan seperti berikut:

1. Laporan adalah hakmilik Universiti Teknikal Malaysia Melaka.
2. Perpustakaan dibenarkan membuat salinan untuk tujuan pengajian sahaja.
3. Perpustakaan dibenarkan membuat salinan laporan ini sebagai bahan pertukaran antara institusi pengajian tinggi.
4. Sila tandakan (  ) -

SULIT\*

(Mengandungi maklumat yang berdarjah keselamatan atau kepentingan Malaysia seperti yang termaktub di dalam AKTA RAHSIA RASMI 1972)

TERHAD\*

(Mengandungi maklumat terhad yang telah ditentukan oleh organisasi/badan di mana penyelidikan dijangka)

TIDAK TERHAD

Disahkan oleh:

.....  
(TANDATANGAN PENULIS)

.....  
(COP DAN TANDATANGAN PENYELIA)

Alamat Tetap: .....

Tarikh: .....

Tarikh: .....

\*CATATAN : Jika laporan ini SULIT atau TERHAD, sila lampirkan surat daripada pihak berkuasa/organisasi berkenaan dengan menyatakan sekali tempoh laporan ini perlu dikelaskan sebagai SULIT atau TERHAD.

I declare that this thesis entitled “Design and Characterization of Silicon – On – Insulator (SOI) Metal – Oxide – Semiconductor Field Effect Transistor (MOSFET)” is the result of my own research except as cited in the references.

Signature : .....

Name : NURASMA ANSARI BT MOHD NAIM

Date : 2<sup>nd</sup> MAY 2011

I declare that I have been reading this paper in view of our work is sufficient from the scope and quality for the award of Bachelor of Electronic Engineering (Computer Engineering).

Signature : .....

Supervisor's Name : EN. ZUL ATFYI FAUZAN B. MOHAMMED NAPIAH

Date : .....

Special dedicated to my beloved father, mother,  
sisters and little brother

## ACKNOWLEDGEMENT

Firstly, „In the name of Allah, most gracious, most merciful“. Alhamdulillah, I would like to extend my deep gratitude towards the almighty Allah S.W.T because of His mercy and kindness, I was able to complete my Final Year Project and thesis in a given time frame without having any difficult problems.

I would like to express profound gratitude to my Final Year Project supervisor, En. Zul Atfyi Fauzan B. Mohammed Napiah for his invaluable support, encouragement, supervision and useful knowledge throughout this duration of my project.

I am also like to thank my parents, for their love and support me all time throughout my life, give me the spirit and pray for my success in carrying out the task. Thanks for their encouragement that they had given to me.

Nevertheless, my great appreciation dedicated to my best friends Nur Hidayah Binti Mansor, Fauziah Binti Osman and Norazian Binti Md Sukardi who had share their opinion and knowledge directly or indirectly with this project.

Thank you so much.

## ABSTRACT

The design of low cost Silicon – On – Insulator (SOI) MOSFET technology has brought about a need to develop specific characterization techniques. This project mainly focus on creating an initial SOI MOSFET device design, characterization and simulations of SOI devices and technology. SOI MOSFET has specific effects and characteristics which make SOI MOSFET different from conventional MOSFET such as NMOS. It can be obtained by using three simulation methods which are DEVEDIT, ATHENA and ATLAS from Silvaco TCAD simulation tools. For conventional MOSFET, there are a few problems in device performance such as switching which came from higher leakage current ( $I_{OFF}$ ), high power and low speed characteristic. To achieve the ultimate goal of SOI device and circuit design, its performance has to optimize while minimizing undesirable effects. From the analysis, SOI MOSFET shows good electrical characteristic when reducing the thickness of silicon and shrinking the channel length to 40 nm.



## ABSTRAK

Rekabentuk teknologi MOSFET Silikon – Atas – Penebat (SOI) yang murah telah membawa kepada keperluan untuk mengembangkan teknik perincian yang tertentu. Projek ini berfokuskan kepada merekabentuk peranti awal SOI MOSFET, perincian yang terdapat pada SOI MOSFET dan simulasi peranti SOI dan teknologinya. SOI MOSFET mempunyai kesan yang khusus dan ciri-ciri yang membuatkan SOI berbeza dari MOSFET biasa seperti diperolehi dengan menggunakan tiga kaedah simulasi iaitu DEVEDIT, ATHENA dan ATLAS dari simulasi dengan menggunakan perisian Silvaco TCAD. Bagi MOSFET biasa, terdapat beberapa masalah prestasi peranti seperti pensuisan di mana ia berpunca daripada kebocoran arus ( $I_{OFF}$ ) yang tinggi, memerlukan kuasa yang tinggi dan ciri-ciri kelajuan yang rendah. Untuk mencapai matlamat bagi peranti SOI dan rekabentuk litarnya, prestasi SOI harus dioptimumkan sementara itu meminimumkan kesan yang tidak diinginkan. Daripada analisis, SOI MOSFET menunjukkan pencirian elektrik yang baik apabila ketebalan silicon dikurangkan dan panjang saluran dikecilkan kepada 40 nm.

## TABLE OF CONTENTS

CHAPTER TITLE	PAGE
PROJECT TITLE	i
DECLARATION	iii
SUPERVISOR DECLARATION	iv
DEDICATION	v
ACKNOWLEDGEMENT	vi
ABSTRACT	vii
ABSTRAK	viii
TABLE OF CONTENTS	xi
LIST OF FIGURES	xiv
LIST OF ABBREVIATIONS	xv
LIST OF SYMBOLS	xvi
LIST OF APPENDICES	xvii
I INTRODUCTION	
1.0 Introduction	1
1.1 Objectives	4
1.2 Problem Statement	4
1.3 Scope	5
1.3.1 Introduction to TCAD Tools	7
1.3.2 DEVEDIT	7

	1.3.3 ATHENA	
	1.3.4 ATLAST	
1.4	Methodology	
1.5	Project Outlined	

## II LITERATURE REVIEW

2.1	Mosfet (Metal-Oxide- Semiconductor Field Effect Transistor)	8
2.2	Silicon - On - Insulator Mosfet Design	7
2.3	Theory	15
	2.3.2 Sub-Threshold Swing Current, SS	15
	2.3.3 Current Ratio, $\frac{I_{ON}}{I_{OFF}}$	16
	2.3.4 Threshold Voltage, $V_{TH}$	16
	2.3.5 Kink Effect	18
	2.3.6 Steep Subthreshold Slope	19
	2.3.7 Dynamic Floating Body Effect	19
	2.3.8 Short-Channel effects	21

## III METHODOLOGY

3.1	Summary of Project Flows	24
3.2	Create a SOI MOSFET Structure Using DEVEDIT	26
3.3	Create an SOI-MOSFET Device Using ATHENA	40
3.4	SOI-MOSFET Device Simulation Using ATLAS	46

IV	RESULTS AND DISCUSSION	
4.1	Electrical Characteristics	53
4.1.2	Different Gate Lengths Comparison	54
4.1.3	Comparison of SOI Structures with Different Silicon Thickness	57
4.1.4	Different Electrode Comparison	60
4.1.5	Comparison of SOI Structures with Different Doping	61
4.1.6	Comparison SOI MOSFET and Conventional MOSFET	63
V	CONCLUSSION AND RECOMMENDATIONS	
5.1	Conclusions	64
5.2	Recommendations	66
	REFERENCEES	67
	APPENDIXS	
	APPENDIX A	69
	APPENDIX B	71
	APPENDIX C	73
	APPENDIX D	74

## LIST OF FIGURES

FIGURE	TITLE	PAGE
1.0	The basic structure of MOSFET device	2
1.1	Physical structure of basic SOI device	4
2.0	Physical structure of the enhancement-type	9
2.1	The enhancement-type NMOS transistor with a positive voltage applied to the gate.	10
2.2	The drain current $I_D$ versus the drain-to-source voltage $V_{DS}$ for an enhancement-type NMOS transistor operated with $V_{GS} > V_{TH}$	11
2.3	Bulk and SOI structure comparison	12
2.4	Partially – depleted devices structure	13
2.5	Fully – depleted devices structure	15
2.6	An Inversion Layer at Threshold Voltage	17
2.7	The overall affect of the process parameters on the threshold voltage and transconductance	17
2.8	$V_G$ is Low- High [8]	20
2.9	$V_G$ is High- Low	20
2.10	Definition of coordinate system in a multiple-gate device. Gate-induced fields are in the x and z-directions. Drain penetration field is in the y-direction.	22
2.11	SOI MOSFET family tree.	23
3.0	Methodology of project	25

3.1	Firing DEVEDIT	26
3.2	Resize Work Area	27
3.3	Add Region Interface	27
3.4	Top Oxide Region	28
3.5	Details The Changes To The Silicon Region	29
3.6	Silicon Region Base Doping	29
3.7	Bottom Oxide Region	30
3.8	Front Gate Electrode	31
3.9	Back Gate Electrode	31
3.10	Add Impurity Interface	32
3.11	Drain Impurity	33
3.12	Source Impurity	33
3.13	Doping Concentrations	34
3.14	Mesh Constraints Interface	35
3.15	First Mesh	35
3.16	First Fix Box Constraint	36
3.17	Second Mesh	36
3.18	Second Fixed Box Constraint	37
3.19	Third Mesh	37
3.20	Fourth Mesh	38
3.21	Fourth Fix Box Constraint	39
3.22	Final Mesh	39
3.23	Substrate Layer	40
3.24	BOX Layer	40
3.25	Silicon - On - Insulator layer	41
3.26	Aluminium Deposition	42
3.27	Poly Deposition and Dry Oxygen	43
3.28	Polysilicon Oxidation	44
3.29	Final SOI Structure	45
3.30	Doping Concentration	46
3.31	Firing DECKBUILD	47

3.32	Open file	47
3.33	DECKBUILD With Command File Loaded	48
3.34	Edited code.	48
3.35	File I/O Window	49
3.36	Edited Code	49
3.37	Edited Code	50
3.38	Test Window With Initial Biasing	50
3.39	Edited Code	51
3.40	Edited Code	51
3.41	$I_D - V_{GS}$ curve	52
4.0	$I_D - V_D$ curves of SOI at 40 nm and 120 nm gate lengths for $V_{GS} = 1V, 2V$ and $3V$	54
4.1	$I_D - V_G$ curves of different channel lengths for SOI MOSFET	55
4.2	Log $I_D - V_{GS}$ curves of different channel length for SOI MOSFET	56
4.3	$I_D - V_D$ curves of different thickness for SOI MOSFET	57
4.4	$I_D - V_{GS}$ curves of different thickness SOI MOSFET	58
4.5	$I_D - V_{GS}$ Log Curves of Different Thickness	59
4.6	$I_D - V_{GS}$ Curve for SOI Structure with Different Electrode	60
4.7	$I_D - V_{GS}$ curve for SOI Structure with Different P-Type Doping	61
4.8	$I_D - V_{GS}$ curve for SOI Structure with Different N-Type Doping	62
4.9	Comparison of SOI Structures with Conventional Structure	63

## LIST OF ABBREVIATIONS

BOX	-	Buried Oxide
C	-	Capacitance
CMOS	-	Complementary MOSFET
DIBL	-	Drain Induced Barrier Lowering
FD	-	Fully Depleted
I	-	Current
I-V	-	Current-Voltage
MOSFET	-	Metal Oxide Semiconductor Field Effect Transistor
MPU	-	Microprocessor Unit
nm	-	Nano metre
op-amp	-	Operational Amplifier
PD	-	Partially Depleted
SCE	-	Short Channel Effect
SIMOX	-	Separation by Implantation of Oxide into Silicon
SOI	-	Silicon-On-Insulator
SOS	-	Silicon-on-Sapphire
TCAD	-	Technology Computer Aided Design
V	-	Voltage
VLSI	-	Very Large Scale Integration
SOS	-	Silicon-on-Sapphire



## LIST OF SYMBOLS

sf	-	Channel Surface Potential
Al	-	Aluminum
Ar	-	Argon
H <sub>2</sub>	-	Hydrogen molecule
k	-	Boltzmann Constant
Si	-	Silicon
SiO <sub>2</sub>	-	Silicon Dioxide
O <sup>+</sup>	-	Positive Oxygen Ion
q	-	Charge of Electron
x <sub>dv</sub>	-	Maximum Depletion Width
C	-	Conduction Band
D	-	Drain
G	-	Gate
O <sub>X</sub>	-	Oxide
S	-	Source
TH	-	Threshold
V	-	Voltage

## LIST OF APPENDICES

NO.	TITLE	PAGE
A	SOI MOSFET, $L_g = 40\text{nm}$	66
B	IDVD Curves	70
C	IDVG Curves	72
D	NMOS Structure	73

## CHAPTER I

### INTRODUCTION

#### 1.0 Introduction

The Metal - Oxide - Semiconductor Field Effect Transistor (MOSFET) is largely known as popular device and is extensively used in digital circuits, microprocessors, memory circuit, and other logic applications. The device is used to amplify or switch electronic signals. The relative small size of MOSFET causes thousands of devices that can be fabricate into single integrated circuit design is other advantage to the electronic industry [1].

First and foremost a basic understanding of the fabrication, operation, advantages, and applications of each device was needed before any simulations or optimizations could commence. This understanding of the devices was gained through extensive research conducted on each device. Various sources were consulted and the resultant understanding of the devices was key in the creation of optimized device configurations.

MOSFET technology is an industry standard. This technology has been around for many years, and the fabrication methods are continually improving, yet they are well established. There has been a consistent gain in the performance of these devices every few years since their creation.

The cost and size are main advantages of MOSFET devices. Since the technology is well established, fabrication methods have become relatively inexpensive. Also, the device itself is physically smaller than other technologies, allowing for the placement of more devices on a silicon wafer during fabrication. MOSFET devices are mainly used in the creation of CMOS logic chips, which are at the heart of every computer. An enhancement-type NMOS transistor was used during the course of this project [1].

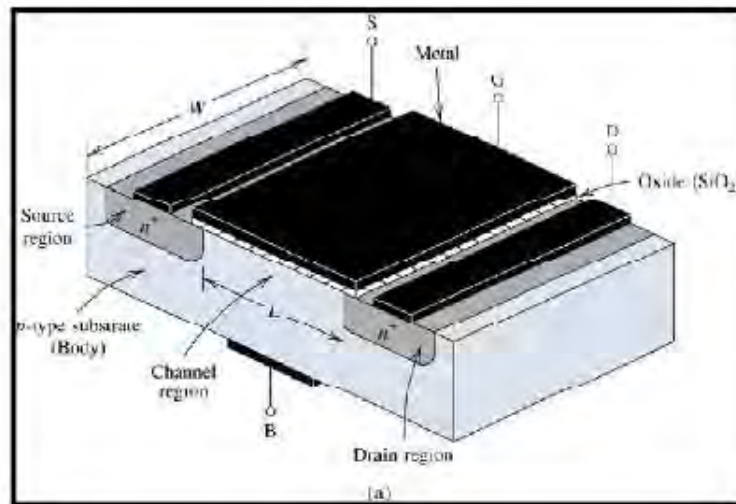


Figure1.0: The basic structure of MOSFET device [1]

Silicon - On - Insulator (SOI) devices are a relatively new technology. Although the technology has been around since the 1960's, SOI devices are only recently becoming commercially viable, due to the expense associated in producing the devices [2]. SOI devices are an advancement of standard MOSFET technology. The main difference between SOI and MOSFET technology is the inclusion of an insulating layer. SOI devices are created from a thin layer of silicon placed on top of a layer of insulating.

The purpose of this project is to design and analysis characteristic of Silicon - On - Insulator (SOI) Metal - Oxide - Semiconductor Field Effect Transistor (MOSFET) performance using semiconductor Technology Computer Aided Design (TCAD) tools. Semiconductor TCAD tools is computer programs which allow for the creation, fabrication, and simulation of semiconductor devices. These tools are used to design semiconductor devices for various applications. Silicon - On - Insulator (SOI) device is silicon-based device built upon an insulating substrate.

Substrate materials can range from unusual materials such as ruby, diamond and sapphire, to common materials such as silicon dioxide. The SOI device design in this project was for an SOI MOSFET, using Silicon Dioxide for the insulator. The structure of the device is very similar to that of a standard MOSFET device, but the presence of a thick layer of insulating material under the depletion region gives some changes of the device characteristics.

During the course of this project, these programs were used to create simulations of the devices being worked on. These simulations provided an opportunity to study the effect of different device parameters on the overall device performance. Throughout the year, the devices were simulated and gradually the performance of each one was improved, until an optimal device configuration was created for the particular applications[1].

SOI performance advantage over conventional bulk CMOS is mainly from lower average threshold-voltage due to transient floating-body (FB) operation and lower junction capacitance. The partial depleted (PD) instead of fully depleted (FD) SOI has become the desirable choice for mainstream digital applications, due to the easy of manufacturing, better control of short channel effects, larger design window for the threshold voltage, and lower self-heating effect [1].

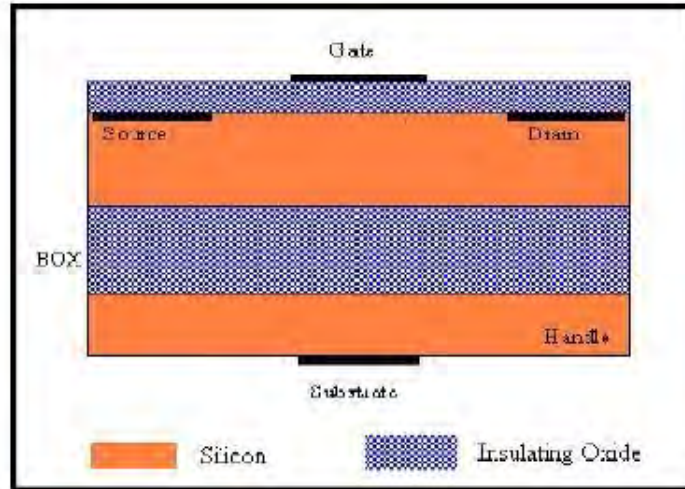


Figure1.1: Physical structure of basic SOI device [1]

## 1.1 Objectives

There are three main objectives of this project are:

- (i) To understand the use of Silvaco's TCAD software
- (ii) To create an initial SOI-MOSFET device design
- (iii) To vary device parameters and study resulting effects upon performance

## 1.2 Problem Statement

In the real world, the SILVACO TCAD tools (virtually fabrication tools) will be used to design the MOSFET device before proceeds to the fabrication process for more effective cost.

There is physical limitation which is short channel effects found in conventional MOSFET as the gate length is further downsizing. In conventional MOSFET, there are a few problems in device performance such as switching which came from higher leakage current ( $I_{OFF}$ ). Besides that, high-power and low speed characteristic for the conventional MOSFET must be improved to a new structure.

Hence, the new device concept of Silicon - On - Insulator (SOI) MOSFET is introduced to prove that it is able to compete with the conventional MOSFET in performances.

### 1.3 Scope

This project is focused on designing the device structure and determined the characterization of Silicon - On - Insulator (SOI) MOSFET. Besides that, this project was conducted by using Silvaco TCAD simulation tools. The Silvaco's TCAD Simulation tool is computer simulation software and used to design the proposed device structures. Silvaco's TCAD Tool consists of DEVEDIT, ATHENA and ATLAS.

#### 1.3.1 Introduction to TCAD Tools

Technology Computer Aided Design (TCAD) simulation tools is a virtual software fabrication and operation simulation of semiconductor devices. This TCAD simulation tools is used to plan, design and test the device structure such as MOSFET before the actual fabrication process. This test is important in order to assist researcher in designing device structures (DEVEDIT) and investigating the overall device performances based on device characteristics that have been extracted from the device simulation (ATLAS) results. Besides that, TCAD simulation tools also can reduce time constrained and save cost compare to actual fabrication process. There are varieties of TCAD simulation tools in industry but this project is used Silvaco TCAD simulation tools which are DEVEDIT, ATHENA and ATLAS.

#### 1.3.2 DEVEDIT

DEVEDIT is a device structure editor that used to create and design the SOI device structure or edit existing device to the straight forward graphical. It was easy to vary parameters such as gate length and doping by using this tool. In addition, this

tool consists of all device design process for example adding silicon base regions, adding gate, adding contact regions, adding substrate contact, adding some doping and creating a mesh. The device structure is designed using DEVEDIT and it is extracted by using ATLAS in order to carry out its electrical characteristics.

### 1.3.3 ATHENA

ATHENA is used to integrate several smaller programs into a more complete process simulation tool. It is a modular program that combines one and two-dimensional simulations into a more complete package allowing for the simulation of a wide range of semiconductor fabrication processes.

### 1.3.4 ATLAST

ATLAS is used to simulate the SOI device and to extract the data. The framework of ATLAS combines several one, two and three-dimensional simulation tools into one comprehensive device simulation package. All the electrical characteristics which are I – V (Current – Voltage) and C – V (Capacitance – Voltage) curves can be obtained by this tool. Then the performance can be determined by the parameter extraction from both curves.