DESIGN AND CHARACTERIZATION OF SILICON-ON-INSULATOR (SOI) METAL – OXIDE -- SEMICONDUCTOR FIELD EFFECT TRANSISTOR (MOSFET)

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A thesis submitted in partial fulfillment of the requirements for the award of the degree of Bachelor of Electronic Engineering (Computer Engineering)

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Special dedicated to my beloved father, mother,

sisters and little brother

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ABSTRACT

The design of low cost Silicon – On – Insulator (SOI) MOSFET technology has brought about a need to develop specific characterization techniques. This project mainly focus on creating an initial SOI MOSFET device design, characterization and simulations of SOI devices and technology. SOI MOSFET has specific effects and characteristics which make SOI MOSFET different from conventional MOSFET such as NMOS. It can be obtained by using three simulation methods which are DEVEDIT, ATHENA and ATLAS from Silvaco TCAD simulation tools. For conventional MOSFET, there are a few problems in device performance such as switching which came from higher leakage current (I_{OFF}), high power and low speed characteristic. To achieve the ultimate goal of SOI device and circuit design, its performance has to optimize while minimizing undesirable effects. From the analysis, SOI MOSFET shows good electrical characteristic when reducing the thickness of silicon and shrinking the channel length to 40 nm.

ABSTRAK

Rekabentuk teknologi MOSFET Silikon – Atas – Penebat (SOI) yang murah telah membawa kepada keperluan untuk mengembangkan teknik perincian yang tertentu. Projek ini berfokuskan kepada merekabentuk peranti awal SOI MOSFET, perincian yang terdapat pada SOI MOSFET dan simulasi peranti SOI dan teknologinya. SOI MOSFET mempunyai kesan yang khusus dan ciri-ciri yang membuatkan SOI berbeza dari MOSFET biasa seperti diperolehi dengan menggunakan tiga kaedah simulasi iaitu DEVEDIT, ATHENA dan ATLAS dari simulasi dengan menggunakan perisian Silvaco TCAD. Bagi MOSFET biasa, terdapat beberapa masalah prestasi peranti seperti pensuisan di mana ia berpunca daripada kebocoran arus (I_{OFF}) yang tinggi, memerlukan kuasa yang tinggi dan ciri-ciri kelajuan yang rendah. Untuk mencapai matlamat bagi peranti SOI dan rekabentuk litarnya, prestasi SOI harus dioptimumkan sementara itu meminimumkan kesan yang tidak diingini. Daripada analisis, SOI MOSFET menunjukkan pencirian elektrik yang baik apabila ketebalan silicon dikurangkan dan panjang saluran dikecilkan kepada 40 nm.

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LIST OF ABBREVIATIONS

BOX	-	Buried Oxide
C	-	Capacitance
CMOS	-	Complementary MOSFET
DIBL	-	Drain Induced Barrier Lowering
FD	-	Fully Depleted
I	-	Current
I-V	-	Current-Voltage
MOSFET	-	Metal Oxide Semiconductor Field Effect Transistor
MPU	-	Microprocessor Unit
nm	-	Nano metre
op-amp	-	Operational Amplifier
PD	-	Partially Depleted
SCE	-	Short Channel Effect
SIMOX	-	Separation by Implantation of Oxide into Silicon
SOI	-	Silicon-On-Insulator
SOS	-	Silicon-on-Sapphire
TCAD	-	Technology Computer Aided Design
V	-	Voltage
VLSI	-	Very Large Scale Integration
SOS	-	Silicon-on-Sapphire

LIST OF SYMBOLS

sf	-	Channel Surface Potential
Al	-	Aluminum
Ar	-	Argon
H2	-	Hydrogen molecule
k	-	Boltzmann Constant
Si	-	Silicon
SiO2	-	Silicon Dioxide
O+	-	Positive Oxygen Ion
q	-	Charge of Electron
xdv	-	Maximum Depletion Width
C	-	Conduction Band
D	-	Drain
G	-	Gate
OX	-	Oxide
S	-	Source
TH	-	Threshold
V	-	Voltage

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CHAPTER I

INTRODUCTION

1.0 Introduction

The Metal - Oxide - Semiconductor Field Effect Transistor (MOSFET) is largely known as popular device and is extensively used in digital circuits, microprocessors, memory circuit, and other logic applications. The device is used to amplify or switch electronic signals. The relative small size of MOSFET causes thousands of devices that can be fabricate into single integrated circuit design is other advantage to the electronic industry [1].

First and foremost a basic understanding of the fabrication, operation, advantages, and applications of each device was needed before any simulations or optimizations could commence. This understanding of the devices was gained through extensive research conducted on each device. Various sources were consulted and the resultant understanding of the devices was key in the creation of optimized device configurations.

MOSFET technology is an industry standard. This technology has been around for many years, and the fabrication methods are continually improving, yet they are well established. There has been a consistent gain in the performance of these devices every few years since their creation.

The cost and size are main advantages of MOSFET devices. Since the technology is well established, fabrication methods have become relatively inexpensive. Also, the device itself is physically smaller than other technologies, allowing for the placement of more devices on a silicon wafer during fabrication. MOSFET devices are mainly used in the creation of CMOS logic chips, which are at the heart of every computer. An enhancement-type NMOS transistor was used during the course of this project [1].

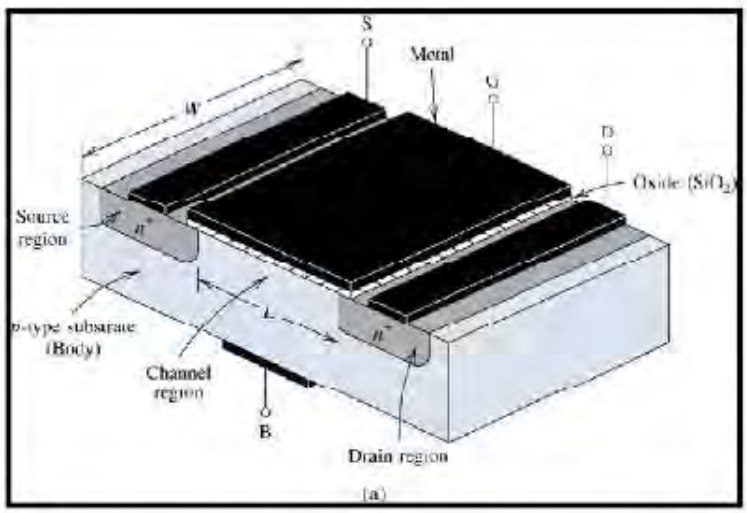

Figure1.0: The basic structure of MOSFET device [1]

Silicon - On - Insulator (SOI) devices are a relatively new technology. Although the technology has been around since the 1960"s, SOI devices are only recently becoming commercially viable, due to the expense associated in producing the devices [2]. SOI devices are an advancement of standard MOSFET technology. The main difference between SOI and MOSFET technology is the inclusion of an insulating layer. SOI devices are created from a thin layer of silicon placed on top of a layer of insulating.

The purpose of this project is to design and analysis characteristic of Silicon - On - Insulator (SOI) Metal - Oxide - Semiconductor Field Effect Transistor (MOSFET) performance using semiconductor Technology Computer Aided Design (TCAD) tools. Semiconductor TCAD tools is computer programs which allow for the creation, fabrication, and simulation of semiconductor devices. These tools are used to design semiconductor devices for various applications. Silicon - On - Insulator (SOI) device is silicon-based device built upon an insulating substrate.

Substrate materials can range from unusual materials such as ruby, diamond and sapphire, to common materials such as silicon dioxide. The SOI device design in this project was for an SOI MOSFET, using Silicon Dioxide for the insulator. The structure of the device is very similar to that of a standard MOSFET device, but the presence of a thick layer of insulating material under the depletion region gives some changes of the device characteristics.

During the course of this project, these programs were used to create simulations of the devices being worked on. These simulations provided an opportunity to study the effect of different device parameters on the overall device performance. Throughout the year, the devices were simulated and gradually the performance of each one was improved, until an optimal device configuration was created for the particular applications[1].

SOI performance advantage over conventional bulk CMOS is mainly from lower average threshold-voltage due to transient floating-body (FB) operation and lower junction capacitance. The partial depleted (PD) instead of fully depleted (FD) SOI has become the desirable choice for mainstream digital applications, due to the easy of manufacturing, better control of short channel effects, larger design window for the threshold voltage, and lower self-heating effect [1].

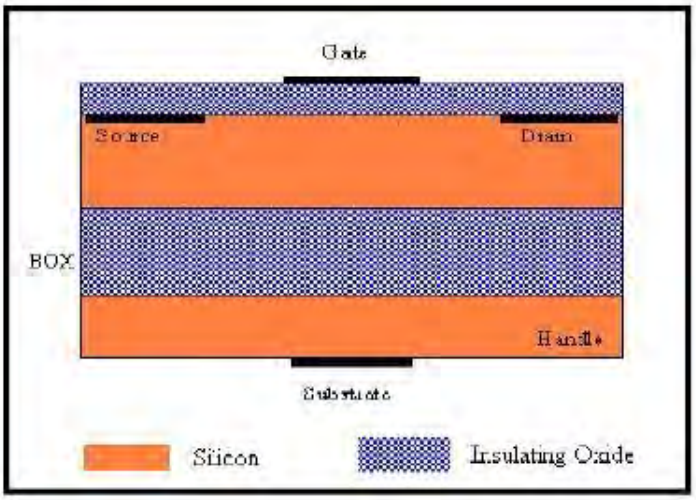

Figure1.1: Physical structure of basic SOI device [1]

1.1 Objectives

There are three main objectives of this project are:

(i) To understand the use of Silvaco's TCAD software

(ii) To create an initial SOI-MOSFET device design

(iii) To vary device parameters and study resulting effects upon performance

1.2 Problem Statement

In the real world, the SILVACO TCAD tools (virtually fabrication tools) will be used to design the MOSFET device before proceeds to the fabrication process for more effective cost.

There is physical limitation which is short channel effects found in conventional MOSFET as the gate length is further downsizing. In conventional MOSFET, there are a few problems in device performance such as switching which came from higher leakage current (I_{OFF}). Besides that, high-power and low speed characteristic for the conventional MOSFET must be improved to a new structure.

Hence, the new device concept of Silicon - On - Insulator (SOI) MOSFET is introduced to prove that it is able to compete with the conventional MOSFET in performances.

1.3 Scope

This project is focused on designing the device structure and determined the characterization of Silicon - On - Insulator (SOI) MOSFET. Besides that, this project was conducted by using Silvaco TCAD simulation tools. The Silvaco"s TCAD Simulation tool is computer simulation software and used to design the proposed device structures. Silvaco's TCAD Tool consists of DEVEDIT, ATHENA and ATLAS.

1.3.1 Introduction to TCAD Tools

Technology Computer Aided Design (TCAD) simulation tools is a virtual software fabrication and operation simulation of semiconductor devices. This TCAD simulation tools is used to plan, design and test the device structure such as MOSFET before the actual fabrication process. This test is important in order to assist researcher in designing device structures (DEVEDIT) and investigating the overall device performances based on device characteristics that have been extracted from the device simulation (ATLAS) results. Besides that, TCAD simulation tools also can reduce time constrained and save cost compare to actual fabrication process. There are varieties of TCAD simulation tools in industry but this project is used Silvaco TCAD simulation tools which are DEVEDIT, ATHENA and ATLAS.

1.3.2 DEVEDIT

DEVEDIT is a device structure editor that used to create and design the SOI device structure or edit existing device to the straight forward graphical. It was easy to vary parameters such as gate length and doping by using this tool. In addition, this

tool consists of all device design process for example adding silicon base regions, adding gate, adding contact regions, adding substrate contact, adding some doping and creating a mesh. The device structure is designed using DEVEDIT and it is extracted by using ATLAS in order to carry out its electrical characteristics.

1.3.3 ATHENA

ATHENA is used to integrate several smaller programs into a more complete process simulation tool. It is a modular program that combines one and two-dimensional simulations into a more complete package allowing for the simulation of a wide range of semiconductor fabrication processes.

1.3.4 ATLAST

ATLAS is used to simulate the SOI device and to extract the data. The framework of ATLAS combines several one, two and three-dimensional simulation tools into one comprehensive device simulation package. All the electrical characteristics which are I – V (Current – Voltage) and C – V (Capacitance – Voltage) curves can be obtained by this tool. Then the performance can be determined by the parameter extraction from both curves.