SOLAR POWERED LIGHTING SYSTEM VIA FIELD PROGRAMMABLE GATE ARRAY

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THIS REPORT IS SUBMITTED IN PARTIAL FULFILMENT OF THE REQUIREMENTS FOR THE DEGREE OF BACHELOR OF ELECTRONIC ENGINEERING WITH HONOURS

FACULTY OF ELECTRONIC AND COMPUTER ENGINEERING
UNIVERSITI TEKNIKAL MALAYSIA MELAKA

JULY 2021

DECLARATION

I declare that this report entitled "Solar Powered Lighting System via Field Programmable Gate Array" is the result of my own work except for quotes as cited in the references.

Signature : .....

Author : CHAN YAN YI

Date : 22 June 2021

APPROVAL

I hereby declare that I have read this thesis and in my opinion this thesis is sufficient in terms of scope and quality for the award of Bachelor of Electronic Engineering with Honours.

Signature : .....

Supervisor Name : IR TS ANUAR BIN JAAFAR

Date : 22 June 2021

DEDICATION

Special thanks to my family, supervisor, and friends who supported and helped me complete the final year project.

ABSTRACT

Nowadays, electricity has become one of the essential needs to carry out people's daily routines. One of the applications of electricity is to provide electrical power to our home lighting system at night. However, most of the electricity is generated by burning fossil fuels. Fossil fuel is a non-renewable and finite resource, which causes pollution to the environment. Instead of burning fossil fuels, the renewable resource solar energy could be a great solution. The solar panel generates electrical power from solar energy stored in the lead-acid battery through the charging and discharging process. The solar-powered lighting system is controlled by the Xilinx Spartan 6 FPGA Development board. Field Programmable Gate Array is an integrated circuit containing programmable logic blocks and interconnection circuits. It is used as a system controller that is programmed by uses Verilog HDL according to different requirements. The output of this project is the lead-acid battery provides power to light on the LED when the Light Dependent Resistor detects darkness and the lead-acid battery in a fully-charged situation. Also, the lead-acid battery will change the state from discharging to the charging stage when low voltage is detected. This project involves developing a solar-powered lighting system via Field Programmable Gate Array and the analysis of the number of battery cycle life based on the different Depth of Discharge (DOD).

ABSTRAK

Pada masa kini, elektrik telah menjadi salah satu keperluan yang penting untuk menjalankan rutin harian masyarakat. Salah satu aplikasi elektrik adalah memberi tenaga elektrik ke sistem pencahayaan rumah kita pada waktu malam. Selain itu, elektrik juga memberi tenaga kepada peralatan elektrik, tetapi sebahagian besar tenaga elektrik dihasilkan dengan membakar bahan bakar fosil. Bahan bakar fosil adalah sumber yang tidak boleh diperbaharui dan terhad yang menyebabkan pencemaran kepada alam sekitar. Daripada membakar bahan bakar fosil, tenaga suria sumber yang boleh diperbaharui ialah satu penyelesaian yang baik. Panel solar menghasilkan tenaga elektrik dari tenaga suria yang tersimpan di dalam bateri asid plumbum melalui proses pengisian dan pengosongan. Sistem pencahayaan bertenaga suria dikendalikan oleh papan Xilinx Spartan 6 Field Programmable Gate Array. Field Programmable Gate Array adalah litar bersepadu yang mengandungi blok logik dan litar interkoneksi yang dapat diprogramkan. Ia digunakan sebagai pengawal sistem yang diprogramkan dengan menggunakan Verilog HDL mengikut keperluan yang berbeza. Hasilan dari projek ini adalah bateri asid plumbum yang memberikan kuasa untuk menyalakan LED apabila Perintang Bergantung Cahaya mengesan kegelapan dan bateri asid plumbm dalam keadaan yang diisi penuh. Juga, bateri asid plumbum akan mengubah keadaan dari tahap pelepasan bateri ke tahap pengecasan bateri apabila voltan rendah dikesan. Projek ini melibatkan pengembangan sistem pencahayaan bertenaga suria

melalui Field Programmable Gate Array dan analisis jumlah hayat kitaran bateri berdasarkan peratus kedalaman perlepasan bateri yang berbeza.

ACKNOWLEDGEMENTS

At this moment, I would like to take this opportunity to thank all individuals who are directly or indirectly involved in supporting and assisting me in completing the Final Year Project (FYP), which is a compulsory course for students to complete degree studies at Universiti Technical Malaysia Melaka (UTeM).

First of all, I would like to thank Ir. Ts. Anuar Bin Jaafar, my supervisor, for continually guiding me during the completion of this project. Thank you for the experience and spiritual encouragement that will make this project a success. Also, his action of thought encourages me to always prepare before doing anything.

Next, I am very grateful to my family for their encouragement and financial support. Finally, thanks to my friends who helped to provide ideas and opinions.

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LIST OF SYMBOLS AND ABBREVIATIONS

FPGA	:	Field Programmable Gate Array
DOD	:	Depth of Discharge
LED	:	Light Emitting Diode
LDR	:	Light Dependent Resistor
CO_2	:	Carbon Dioxide
PWM	:	Pulse Width Modulation
MOSFET	:	Metal-Oxide-Semiconductor Field-Effect Transistor
RTL	:	Register Transfer Level
e.m.f	:	Electromotive Force
MPPT	:	Maximum Power Point Tracking

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CHAPTER 1

INTRODUCTION

1.1 Project Background

Global energy demand is increasing, the higher energy demand is also expected in the well-developed and developing countries in the coming decades. Besides that, growing populations and rising living standards would bring much more pressure on energy resources for many people in developing countries [1]. Due to the rise of energy demand, global electricity production has grown yearly since 1974, and most of the electricity production generated from combustion fuels, mostly with fossil fuels [2]. However, electricity produced by burning fossil fuels is harmful to the environment, the carbon dioxide, CO_2 emissions produced by burning fossil fuels can pollute the air. The CO_2 emissions and other greenhouse gases will be released when burning fossil fuel, contributing to global warming and climate change. Also, as non-renewable

resources, fossil fuels will run out or not be replenished for thousands or even millions of years [3].

Due to CO_2 will produce air pollution, it is important to use alternative energy resources for daily uses. Renewable energy is advisable to overcome this issue. Solar energy is a renewable energy source, and solar or photovoltaic (PV) cells are manufactured from silicon or other materials that directly convert sunlight into electricity. This technology offers a practical solution to various power application problems, and most importantly, no air pollution or greenhouse gases are generated by solar energy systems. The solar lighting system is one of the most common applications of solar energy. Since energy-saving lighting is an important factor in sustainable development and energy strategy, the combination of high-efficiency photovoltaics and light-emitting diodes (LEDs) can release solar lighting systems and provide realistic and energy-saving solutions for lighting systems.

A solar-powered lighting system provides power to the load by using sunlight as an energy resource, which means a typically battery-powered lighting system charged using a solar panel. The solar lighting system can come in all shapes and sizes based on different needs, it consisting of a solar panel, lead-acid battery, and LED lights as the output, and the energy stored in the battery is used to light the LED. More than to lights up the rooms, it is also possible to use a solar lighting system in areas that either has no effective 24-hour grid electricity or no grid electricity at all. A rechargeable lead-acid battery stores solar energy through the charging process and supplies power to the LEDs during the discharging process. Rechargeable batteries are commonly used in solar lighting systems because the solar array's electrical energy is not always consistent with the time needed for electrical power [4]. Among the types of batteries,

lead-acid batteries are popular because of their compatible price range, and they are highly affordable compared to other advanced technologies.

The use of LEDs in the lighting system will save energy, minimize CO_2 emissions and numerous advantages over conventional lamps: the better energy efficiency of lighting systems, longer lifecycle, less maintenance, higher flexibility and control of the light level, and lower power consumption and environment-friendly [5]. For the improved version, LEDs can have their light emission control known as dimming. Pulse Width Modulation (PWM) is used to control the luminous flux of the LED, which uses a square wave power supply for these applications, then the light flux is changed by varying the signal's duty cycle [5].

Besides the Field Programmable Gate Array (FPGA), different embedded systems were implemented before FPGA became popular for the solar-powered lighting system. The PIC family microcontroller is frequently used in the solar street light system to controls the solar street light system based on light detections, working with Light Dependent Resistor (LDR) [6][7][8]. In addition, Arduino UNO is also embedded in the solar lighting system to check the battery power and indicate that the discharge at a critical level [9]. However, the FPGA has recently become more widely used in the lighting system, mostly switching the lights by detecting movement[10] and controlling the LED dimming based on different scenarios[5].

1.2 Problem Statement

Most researchers ignore developing the prototype or hardware of a solar-powered lighting system using FPGA[10][11]. However, the results might differ between the simulation and prototype due to the actual factors, such as temperature, weather, and

other factors. Hence, this is hard to determine the efficiency of the solar-powered lighting system using FPGA in real life.

There is a current paucity of evidence-based literature describing the impact of Depth of Discharge on the battery's lifespan [6][9]. Suhil *et al.* had mentioned that the conventional solar lighting system is suffering from the sudden death of light. The conventional solar lighting system always discharged until there is no more energy to light up the LED. When the battery is over-charged and over-discharged continuously, it could damage the battery and shorten its lifespan [7].

1.3 Objectives

The objectives of this project are:

1. To develop a prototype of a solar-powered lighting system using FPGA.
2. To analyze the number of battery lifecycle based on the different Depth of Discharge (DOD) of a solar-powered lighting system.

1.4 Scope of Work

Figure 1.1 shows the block diagrams of the scope of work, including the hardware, software, and the technique applied. For the hardware, the Xilinx Spartan 6 FPGA Development board is the main component used to control the whole system, includes the charging mode and discharging mode. Next, this project will use a monocrystalline solar panel, in which the solar panel's maximum power is 30W, and the maximum power voltage and current of the solar panel are 18V and 1.67A. Additionally, this project will use a rechargeable lead-acid battery, and the model of the battery is GP1272, which a battery voltage is 12V, and the capacity is 7.2Ah. On the other hand, the buck converter is also used to step down the charging voltage. Furthermore, the

Light Dependent Resistor (LDR) will be used as an input sensor to detect light intensity. And the 8-bit analog-to-digital converter is used to convert the analog input into digital form connected to the FPGA, and the model used is AD7822. Also, two NCE6008AS MOSFETs were used as a switch in the charging circuit and discharging circuit. For the software part, Xilinx ISE software is used and based on Hardware Description Language (HDL) called Verilog to design and program the FPGA. In this project, two 4W LEDs will be the output. Furthermore, the Pulse Width Modulation technique (PWM) will be applied in the programming to control the brightness of the LED. For the analysis part, the operating temperature will be assumed at 25℃, and the total hours to complete a whole process will be recorded when the solar lighting system in operation. Also, only analyze the battery life cycle are based on the different DOD at 40%, 50%, and 60%.

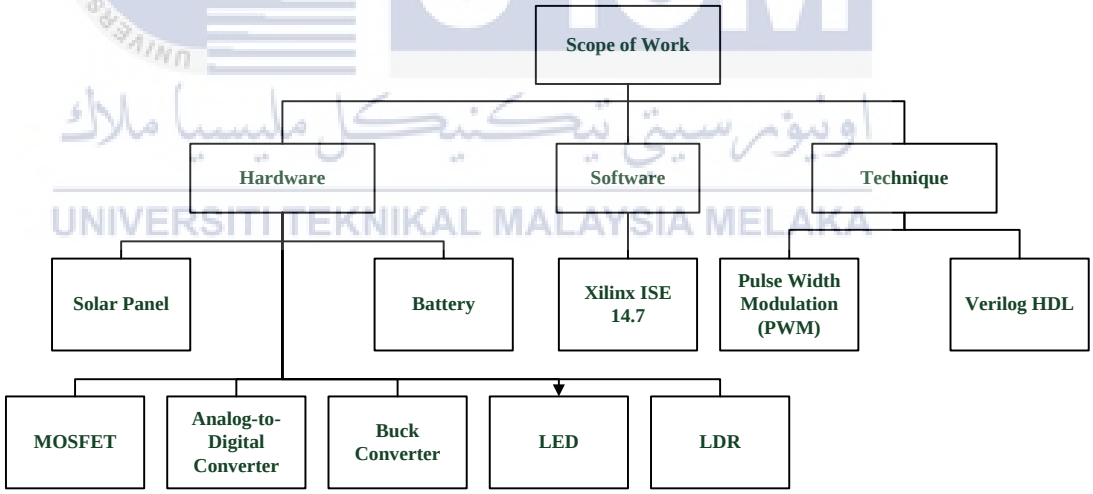

Figure 1.1 Scope of work

1.5 Organisation Structure

This report focuses on designing a solar-powered lighting system using Field Gate Programmable Arrays (FPGA) and the Xilinx ISE software. The report is divided into

five major sections: introduction, background study, methodology, results and discussion, followed by a conclusion and future work.

Chapter 2 discusses the literature research introduction and other related studies to this project by different researchers that contain the basics of solar panel, FPGA, and other fundamental theories. Next, Chapter 3 discusses the methodology used to achieve the project objectives and scope of work. The requirement and flowcharts needed for monitoring the project flow with the study summary will be studied.

Also, all data and results from the study are provided in chapter 4. In this chapter, all the observations and findings are discussed and observed. This chapter will present the results in a suitable diagram for the analysis of battery service life. Finally, the project and the results are concluded in Chapter 5, along with future work explanations.

CHAPTER 2

BACKGROUND STUDY

2.1 Introduction

This chapter discussed all the information about the research summary from books or journals. Also, the overview of the conventional solar-powered lighting system will be addressed in this chapter. This chapter will also briefly discuss the theory of solar panel, rechargeable lead-acid battery, buck converter, dimming method, MOSFET, and the system controller.

2.2 Solar Powered Lighting Systems

The term ‘solar lighting system’ refers to the lighting system using solar radiation energy to charge the battery during the day with the solar panel and supply the LED light equipment with energy at night [6]. Besides that, solar lighting is an energy-efficient technology that uses semiconductor materials to obtain usable energy from

sunlight [12]. The literature on solar-powered lighting has highlighted several components: solar panels, battery, DC-DC converter, system controller, and LEDs [9]. The construction of solar lighting systems can reduce energy imports and reduce dependence on oil and natural gas, thereby reducing the risk of fuel price fluctuations and providing energy for small-scale lighting applications where electricity is the most limited and expensive [12].

2.2.1 The System Operation of Solar Powered Lighting System

Several studies of the operation of the solar lighting system had been reviewed. There is the most well-known operation of the proposed system, firstly the solar panels receive solar radiation during the daytime and convert it into electrical energy through charging and discharging process, which is finally stored in battery [6][13][14]. The presence of sunlight can be sensed by the light-dependent resistor (LDR). The lights are in the OFF position if LDR detects the sunlight, and the light in the ON position when the sunlight is detected [11][15].

2.2.2 Solar Panels as an energy source

The solar or photovoltaic module is a packaged, connected photovoltaic cell known as solar cells [15]. The photovoltaic had been defined as a method of producing electrical energy using semiconductors that exhibit the photovoltaic effect to transform solar radiation into direct current [15]. According to Jordan (2015), the photovoltaic effect can be defined as the process that produces a voltage or electric current in the solar cells when they are exposed to sunlight [16]. Besides that, the photovoltaic had been described as the light enters the photovoltaic cell as pure energy. It provides enough power to release some electrons, which are negatively charged atomic particles. To generate a voltage or photovoltage, the built-in barrier in the battery acts

on these electrons that can be used to drive current through the circuit [17]. However, the photovoltaic cell comprises various semiconductor materials, mainly monocrystalline silicon and polycrystalline silicon, as shown in Figure 2.1.

A polycrystalline solar panel is made from molten silicon by casting a cube-shaped ingot [18], a faster and cheaper process. Polycrystalline solar panel are lower in price, lower efficiency, and have a shorter lifespan than the monocrystalline solar panel [19].

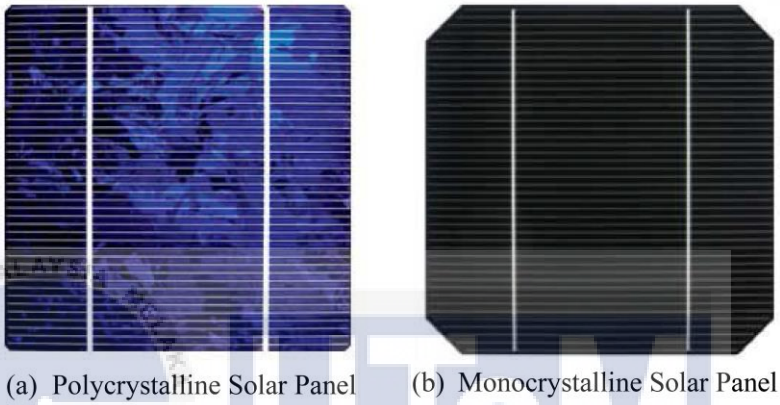

Figure 2.1 Polycrystalline vs Monocrystalline Solar Panels[20]

A monocrystalline solar panel composed of silicon, in which the entire solid crystal lattice is continuous, without breaking its edges, and without any grain boundaries [21]. Their advantages are high efficiency, high output power, less space, and the most extended service life. But also, it makes them more expensive than polycrystalline or thin-film solar panel [18].

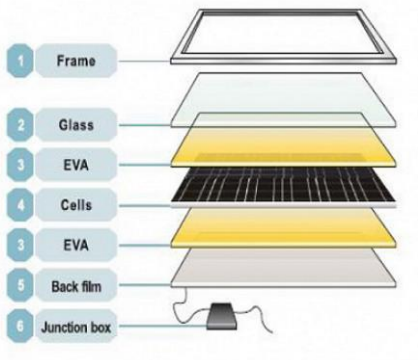

Figure 2.2 The structure of monocrystalline solar panel[22]

A typical monocrystalline solar panel shown in Figure 2.2 consists of six layers [25], including frame, glass, EVA, solar cells, back film, and a junction box. Firstly, the aluminium frame functions to protect the laminate. Secondly, the tempered glass function is to protect the solar cells. The transmittance of the tempered glass typically must be high above 91%, and ultra-white tempering is required[23]. Next, the Ethylene Vinyl Acerate (EVA) film has good radiation transmittance and a low degradation rate. EVA is also a thermoplastic polymer that forms a sealing and insulating film around the solar cells by applying heat to the module. Monocrystalline silicon solar cells have the highest photoelectric conversion efficiency among various solar cells. They have 15-25 years of service life and are encapsulated in tempered glass and waterproof resin.

2.2.3 Rechargeable Lead-Acid Battery as energy storage

Based on the previous journals, the rechargeable lead-acid battery had been selected to store the energy [9][12][24][25]. This is because they are low cost and have a longer service life, although the lead-acid batteries have low energy capacity, medium performance and high maintenance requirements [26]. However, there are two types of lead-acid batteries, which is deep-cycle battery and shallow-cycle battery. The shallow-cycle battery should not be used in PV systems because they are designed to discharge only about 20% of their capacity, or it will damage the battery. On the other hand, the deep-cycle battery is designed to gradually release 80% of its capacity and recharge hundreds or thousands of times depending on the battery capacity [12]. Figure 2.3 shows the construction of the lead-acid battery[27].

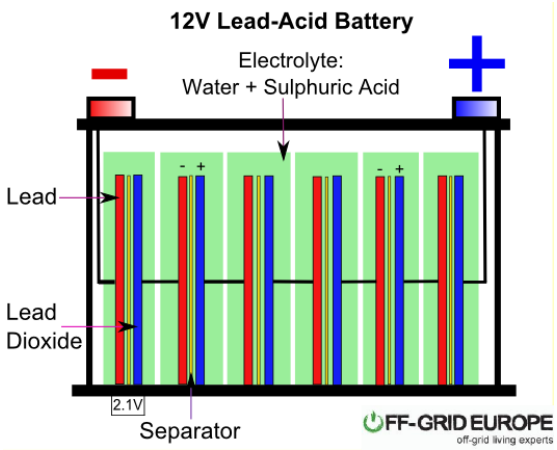

Figure 2.3 Construction of a Lead-acid Battery[27]

A lead-acid battery consists of the anode, cathode, electrolyte, separator, and battery casing[27]. The negative terminal is the cathode, and the positive terminal is the anode. The electrolyte connects them and drives the electrochemical reaction that generates electricity[28]. In the lead-acid battery, the positive plate is made of lead, and the negative plate is made of lead dioxide. Besides that, a separator between the positive and negative plates is made of insulating material, preventing them from contacting or short-circuiting. In addition, the electrolyte in a lead-acid battery is water with sulfuric acid.

There is various method to charge the lead-acid battery, the constant voltage method is the one of the most common charging method used in a lead-acid battery. This is because the charging voltage remains constant throughout the charging cycle, and the current steadily decreases as the battery charge level increases[29], as shown in Figure 2.4.

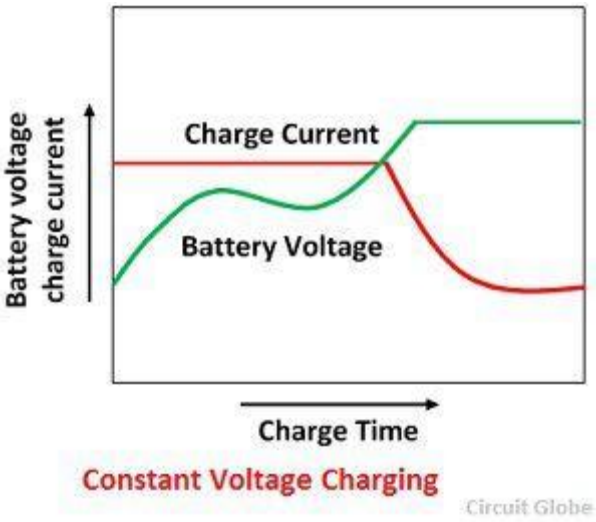

Figure 2.4 Constant voltage charging[30]

The advantage of charging at a constant voltage is that it allows charging batteries with different capacities and discharge levels. The large charging current at the beginning of charging will last for a short time and not damage the battery. Since the battery voltage is almost equal to the voltage of the power circuit, the charging current almost drops to zero at the end of charging[30].

2.2.4 Buck converter circuit for stable power generated

A buck converter is a form of DC-to-DC converter that can take input directly from a DC source. The DC input can be obtained from any DC power source and obtained from AC input through a rectifier and reservoir circuit, as shown in Figure 2.5. The switching transistor between the input and output of the buck converter is continuously turned on and off at high frequencies. In order to maintain a continuous output, the circuit uses the energy stored in the inductor L to continue to provide the load during the “off” period during the “on” period of the switching transistor[31].

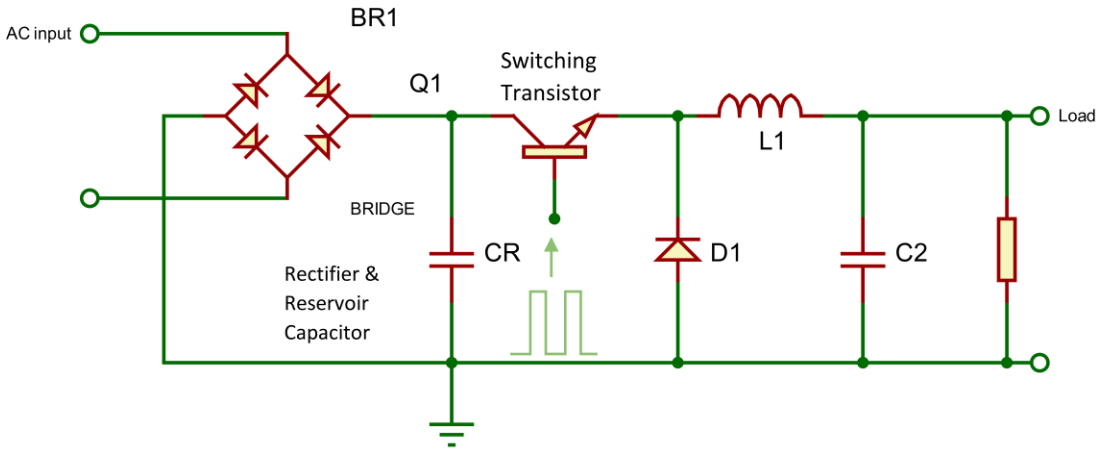

Figure 2.5 Buck Converter Circuit with rectifier and reservoir capacitor

As shown in Figure 2.5, the buck converter circuit consists of the switching transistor, diode D1, inductor L1, and capacitor C2. Current flows through the load through the inductor L1 while the transistor is on. The function of the inductor is to prevent the current changes and used it as energy storage. Since the inductor stores the energy taken from the increased output, the switching transistor's output does not instantly increase to its peak value. The stored energy is then released as back e.m.f into the circuit. Thus, the current flowing through the switching transistor is quickly switched off[31].

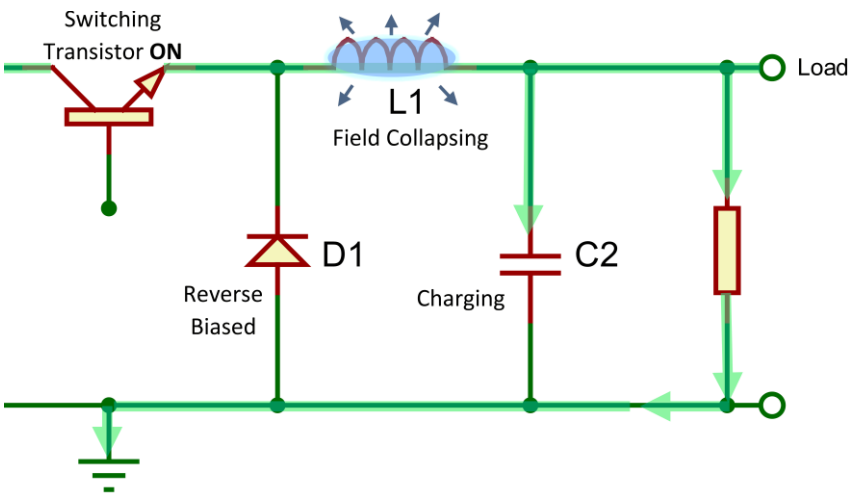

Figure 2.6 Buck Converter when switched on

When the switching transistor is turned on as shown in Figure 2.6, it will provide current to the load. The current flowing to the load is initially reduced since the energy is stored in inductor L1, so the current load and the charge on capacitor C2 gradually increase. During the entire conduction period, there will be a larger positive voltage on the cathode of diode D1 so that the diode will be reverse-biased, and it does not affect this action[31].

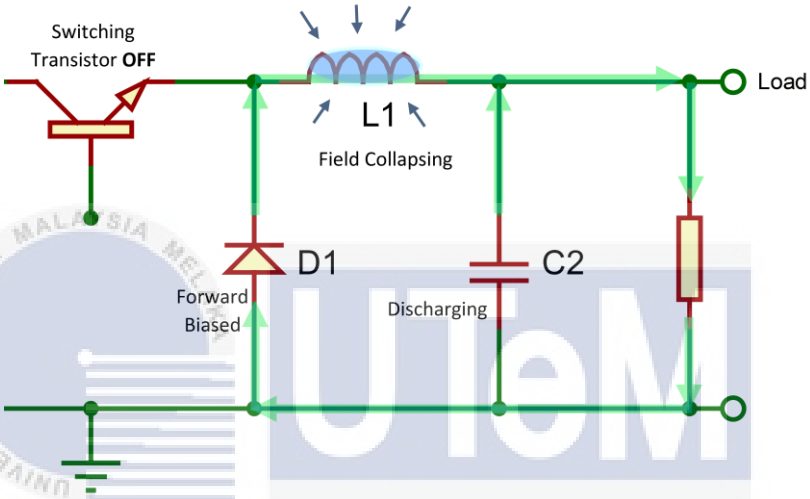

Figure 2.7 Buck converter when switched off

When the transistor switched off as shown in Figure 2.7, the energy stored in the inductor is released back into the circuit. During the "on" period, the back e.m.f across the inductor L1 is opposite in polarity to the voltage across the inductor L1, and there is enough stored energy in the collapsed magnetic field to keep the current flowing. Due to the back e.m.f from inductor L1, the current flows through the circuit through the load and diode D1, which is now forward biased. Furthermore, the charge stored in capacitor C2 will become the primary source of current once the inductor returns most of the stored energy to the circuit and the load voltage begins to drop, then it keeping current flowing through the load until the next "on" period begins[31].

2.2.5 Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET)

MOSFET stands for Metal Oxide Semiconductor Field Effect Transistor and can be called an advanced from FET. In general, the MOSFET shown in Figure 2.8 is a three-terminal device with a Drain (D), Source (S), Gate (G) [32]. They should be biased to alter between cut-off and saturation state if the MOSFET is required to operate as a switch. This is because there are no current flows through the device in the cut-off region. A constant amount of current flows through the device in the saturation region, simulating the behaviour of opening and closing the switch, respectively [33].The MOSFET function as a switch to controls the voltage and current flow between the drain and source. Refer to Figure 2.9, the MOSFET operation depends on the semiconductor surface under the oxide layer between the source and drain. The positive voltage is applied to the drain, and the negative voltage is applied to the source when a drain-source voltage V_{ds} is connected between the drain and source. Therefore, the PN junction is reversed biased at the drain, and there is forward bias at the source, and there will be no current flow between drain and source at this stage. On the other hand, suppose the positive voltage (VGG) is applied to the gate terminal. In that case, the P substrate's electrons will begin to accumulate on the gate contact that forms a conductive bridge between the two n+ regions due to electrostatic attraction.

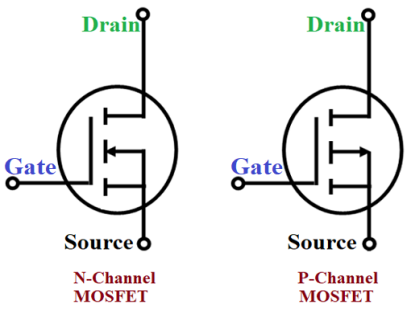

Figure 2.8 Symbol of MOSFET[32]

The number of free electrons accumulated at the gate contact depends on the strength of the positive voltage applied. The greater the applied voltage, the greater the width of the n-channel generated by the accumulation of electrons, the greater the conductivity, and the drain current (Id) will eventually begin to flow between the source and the drain. Apart from a small amount of current due to minority charge carriers, there would be no current flow while no voltage was applied to the gate terminal. The threshold voltage is considered the minimum voltage at which the MOSFET begins conducting[34].

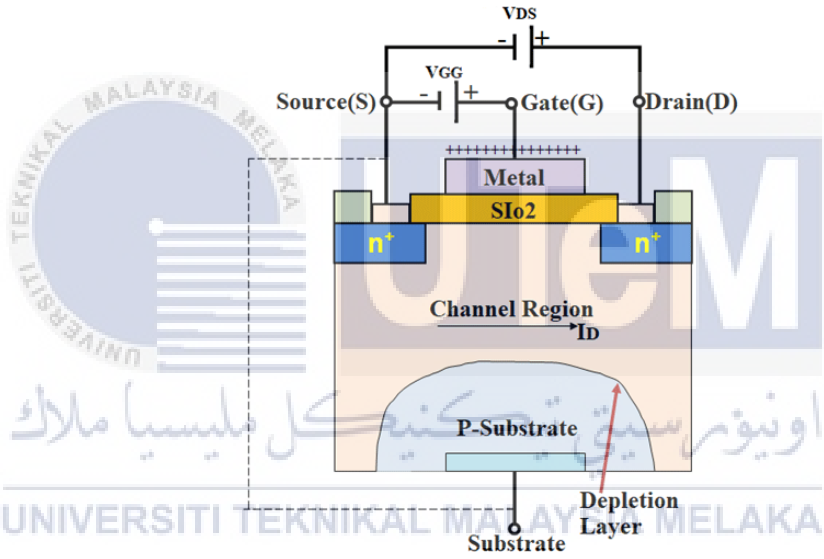

Figure 2.9 The MOSFET block diagram [34]

Two MOSFETs will be required to act as a switch in this project, the first MOSFET is in the charging circuit, and another is in the discharging circuit. The author uses an n-channel MOSFET to drive the LED streetlight using the PWM signals, with 49A drains current and 17.5mΩ in the driving circuit, provided with a heat sink to protect the MOSFET from being overheated [7].

2.2.6 Pulse Width Modulation as LED dimming control

Pulse Width Modulation (PWM) is used to generate the varying frequency signal and duty cycle [7], and their application includes dimming LED and controlling the motor. It can refer to a viable way to control the luminous flux of the LED, and the light emitted wavelength is affected by changing the value of the current flowing through the LED [5]. PWM is a technique for reducing the average transferable power of an applied electrical signal and controlling the average current and voltage transmitted to a load by quickly opening and closing the switch between the load and the power supply[35].

The PWM technique will be applied in this project for LED dimming use. PWM dimming takes advantage of the human eye's slow response time by rapidly turning on and off the LED at a frequency greater than 100Hz without changing the LED current flowing during the turn-on period. Since the human eye does not respond to frequencies higher than 30 Hz, the brightness seems different depending on the duty cycle of the PWM signal[36].

The percentage of time that the PWM signal remains high is called the duty cycle, or it can be described as the percentage of time that the digital signal is turned on in a specific time interval or period. The period is the inverse of the waveform frequency[37]. In addition, the duty cycle refers to the total time the pulse is ‘on’ in the entire cycle, hence at 80% brightness, the duty cycle of the LED is 80%. For example, the LED has to be turned on or off, depending on the 50% duty cycle required during the $400\mu s$. Therefore, a 50% duty cycle is requires the pulse to be on for $200\mu s$ and off for $200\mu s$. As example, the Figure 2.10 and Figure 2.11 shows the PWM signal with 80% and 5% of duty cyle.

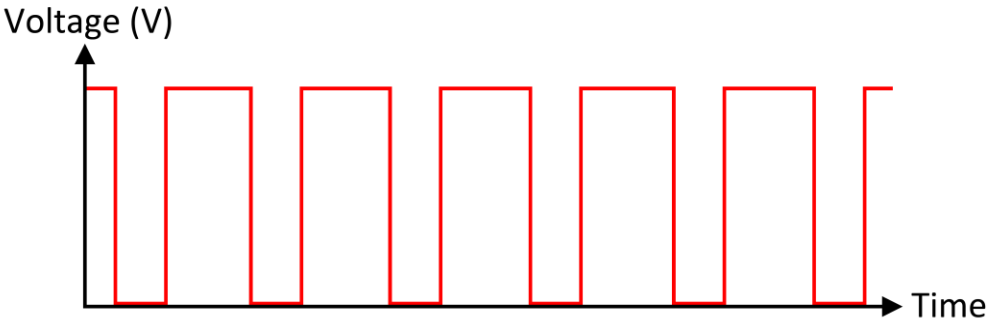

Figure 2.10 PWM signal when LED dimming at 80% brightness

Jasim and Kasim[5] proposed two dimming scenarios to reduce LED brightness levels according to the real-time clock time. The first scenario starts at sunset time with full brightness or 100% duty cycle, the duty cycle changed to 80% at 10 pm, and the duty cycle changed to 60% after 2 hours, and finally turned off as the sunrise time occurred. In another dimming scenario same starts at sunset time with full brightness or 100% duty cycle, the PWM signal changed to 60% at midnight.

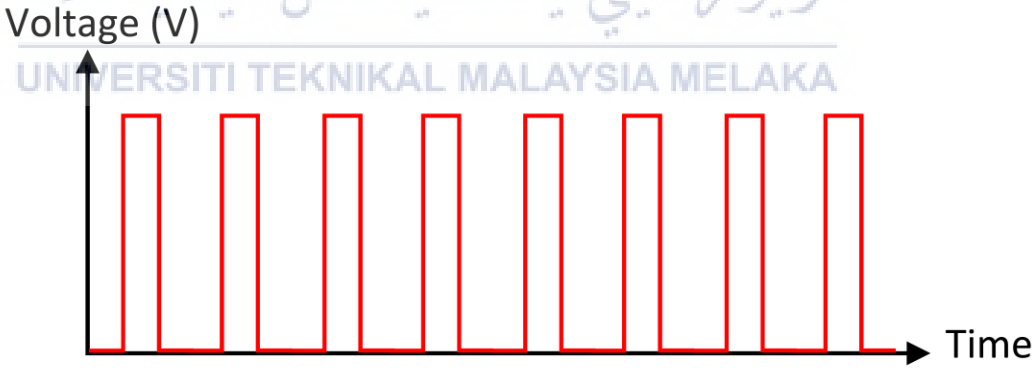

Figure 2.11 PWM signal when LED dimming at 5% brightness

2.3 System Controller for Solar Powered Lighting System

Besides the lighting system, a system controller is also an important part of all the power systems for battery charging [13]. Unchitta *et al*. stated that a discharge controller could prevent excessive discharge, which causes the shortening of the battery lifespan [24]. Several researchers have applied several controller types to control the charging and discharging process, monitor the battery levels, and control the outputs. Oke *et al.* mention that a charge controller is required for the lighting system to prevent damage to the battery and a sensor to help automatic switching [15]. The microcontroller is a computer control system on a single chip, and it has many built-in electronic circuits that can decode written instructions and convert them into electrical signals [6].

2.3.1 Field Programmable Gate Array

Many researchers have focused on the popular programmable hardware in recent years, which is Field Programmable Gate Array (FPGA). A Field Programmable Gate Array (FPGA) is an integrated circuit composed of internal hardware modules and user-programmable interconnects to customize operations for specific applications [38]. FPGA has high programmability and minimum design time; low power consumption, high-speed input and output, and large parallelism are important features [39]. After the FPGA is configured, the internal circuit's connection mode will create the hardware implementation of the software application. The FPGA is not like a processor, it uses dedicated hardware to process logic, and there is no operating system [40]. Figure 2.12 shows the internal structure of the FPGA, which consists of three major blocks: Configurable Logic Block (CLB), I/O Blocks, and Interconnect Wires.

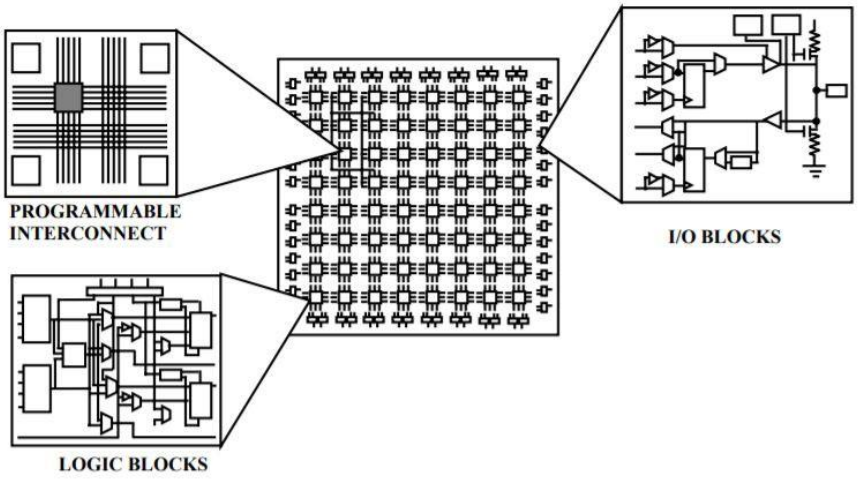

Figure 2.12 The internal structure of an FPGA[40]

The configurable logic block consists of an 8-bit feature generator, two 16-bit feature generators, two flip-flop or latch registers, and a multiplexer. The CLBs are used to execute other design functions, and each of the CLBs has input on each side, allowing them to be flexible for logic mapping and partitioning. Next, the I/O block is used for external peripheral devices to access the FPGA function and using the I/O block. It can also use different peripheral devices to communicate with the FPGA to achieve various applications. Finally, the interconnect wires are used in FPGAs to connect long and short interconnect wires in a flexible combination. It also includes transistors that are used to open or close connections between various lines [41].

P. Anjali *et al.* uses the Xilinx Spartan 3 FPGA board to control the lighting system, automatically turning ON and OFF depending on sunlight and identifying movement or any object [11]. On the other hand, Jasim *et al.* simulate and implements the LED dimming on the Xilinx Spartan 3A FPGA board to control the proposed dimming scenarios [5].

2.3.2 Arduino

Arduino UNO is a microcontroller board developed based on 8-bit Atmega328p [42]. The microcontroller is an essential part of all power systems used for battery charging. The reason for using Arduino UNO Atmega is its low cost, strong compatibility, compact size, and convenient interface with other types of controllers [13]. Sarkar *et al.* uses the Arduino Atmega328p microcontroller to monitor the battery level and check for replacement. The Arduino microcontroller is programmed to compare the full battery level and the present battery level to adjust the LED brightness based on the light intensity and display the brightness percentage of the LED [9]. P. Rodi *et al.* also uses the Arduino Atmega328p to control the whole circuitry lighting system. The sensor would be the microcontroller's input, the arrays of LEDs as the output, also the solar panel and battery connected to it for relay switch action [13].

2.3.3 PIC Microcontroller

Recent studies have been carried out using a microcontroller PIC16F877A to control the street light system [6][7]. PIC16F877A microcontroller is easy to code and low cost, so it becomes one of the most popular microcontrollers in the industry. One of the most significant advantages of using flash technology is that it can be written and erased as much as possible [43]. Priyanka *et al.* explained that a controller also functioned to run the software to manage the system when it receives the collected information transferred from sensors [6].

2.4 The Battery Lifecycle Estimation Method

The battery service life or battery lifecycle is described as a battery estimation time to support the loads before the energy is used up [44]. The battery service life is

specified in the number of cycles. However, the battery service life is most strongly depends on the interrelationship between the following parameters [45]:

1. The method of charging and discharging
2. The Depth of Discharge (DOD)
3. The average battery temperature
4. Low discharge state for a long time

Several methods currently exist for the measurement of the battery lifecycle prediction. Layadi *et al.* proposed two types of battery lifecycle modelling: the battery ageing model depending on DOD and the modelling temperature influence on battery ageing [46]. Wibawa *et al.* introduced a battery lifecycle prediction method to predict the lead-acid battery life cycles with a simple equation (2.1), based on the obtained battery cycle in hours [44].

$$n_{cycle} = \frac{life\ expectancy\ (years)}{cycle(hours)} \times 365 \times 24 \quad (2.1)$$

According to Wibawa [44], a battery cycle comprises the discharged time and recharged time. Therefore, the datasheet provided by the manufacturer should be considered to calculate the number of battery life cycles. With reference to the datasheet of GP1272, the main parameters that need to be considered when measuring are as follows:

Table 2-1 Specification of the GP1272 Battery [47]

Parameter	Value
Nominal Voltage	12V
Nominal Capacity	7.2Ah
Nominal Temperature	25℃ ± 3℃
Max charge current	2.16A
Lifecycle Expectancy	Five years

As seen, the manufacturer's data from Table 2-1 showed that for the GP1272 battery type considered, the battery's service life was expected to be as long as five years.

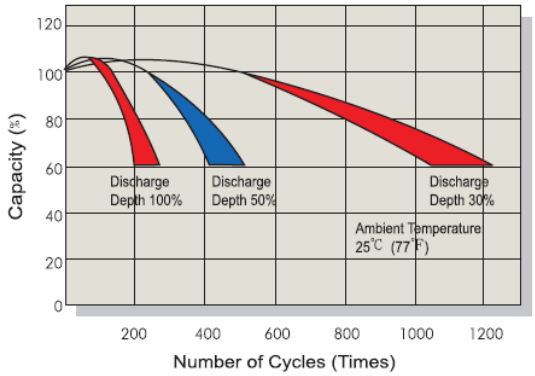

Figure 2.13 Life cycle for GP1272 battery[47]

Figure 2.13 shows the manufacturer's data provide the number of cycles depends on the different Depth of Discharge, which is 100%, 50% and 30% at the ambient temperature 25℃. However, the data from the datasheet is for the ideal situation, and it will vary by other factors in real life. Therefore, this battery lifecycle calculation method will be implemented in this solar lighting system, and the number of cycles will be obtained and analysed in this project through equation (2.1).

2.5 Summary

This section discusses the advantages and disadvantages of the previous project, as listed in Table 2-2. Priyanka *et al.* (2018) used a PIC16F877A microcontroller to control the solar LED street lighting system for power saving[6]. They use the LDR sensor to indicate the light intensity and the photoelectric sensors to detect the movements. In order to develop the system, they design it by using MATLAB and MultiSim software. The system turns on and off the street light based on the two main conditions, whereas light intensity and object movement. Therefore, they save more power when the sodium vapour lamps are replaced by LED, and the LED only lights

up based on different conditions. However, this study is not focusing on the analysis of the battery service life.

Next, Shubham *et al.* (2017) use an Arduino UNO to control the solar street lighting system and design the system by using the Arduino IDE software[9]. The lighting system also uses the LDR sensor to detect the light intensity, and the LED will light up with different levels of brightness based on the changes of the light intensity detected by the LDR sensor. Besides that, they propose the intelligent battery level monitoring unit, which means the microcontroller keeps monitoring the battery level for battery replacement purposes. It also helps to avoid the battery exhausting completely. But they did not focus on the analysis of the battery service life.

Besides that, Amey *et al.* (2016) develop a smart street light system using FPGA, Xilinx ISE 9.2i tools, and ModelSim software. However, the purpose of this project is for energy-saving and reduce power consumption[10]. In the proposed system, the switch on and off of the street light depends on the light intensity detected by LDR. Besides that, they also apply the PWM technique in the dimming control of the LED. In the last project, the simulation result shows there is reducing the power consumption with the design. But the results may vary in real life due to the other component's power consumption since no hardware or prototype is developed.

For this work, a Xilinx Spartan 6 FPGA development board will be used to control the whole solar-powered lighting system and design the system by using the Xilinx ISE 14.7 software. The brightness of LED will vary depending on the LDR sensor's output, and the battery level is always monitored and displayed by the FPGA. The hardware or the prototype will be developed, and the results will be observed.

Table 2-2 Project Summarize Table

Project Title	Type of Controller	Software used	Energy Source	Advantage & Disadvantage	Reference
Control of Solar LED Street Lighting System based on Climate Conditions and Object Movements	PIC16F877A Microcontroller	Matlab/Simulink	Solar	Advantage: Save more power when LED only lights on based on different situations Disadvantage: This study did not focus on analysis on battery lifecycle	Priyanka, Dr.K.Baskaran (2018) [6]
Smart Street Lighting using Green Technology	Arduino UNO	Arduino IDE	Solar	Advantage: Intelligent battery monitoring unit to identify battery replacement Disadvantage: Did not study on battery lifecycle with different Depth of Discharge (DOD)	Shubham, Kshitij, Prajakta (2017) [9]
Smart Street Light System using Reconfigurable FPGA Tool	Xilinx Spartan 3	Xilinx ISE	Not Mentioned	Advantage: Great flexibility and hardware parallelism Disadvantage: Without a prototype	Asha Rani, Anjali (2018) [11]
Solar Powered Lighting System via FPGA	Xilinx Spartan 6	Xilinx ISE 14.7	Solar	Advantage: Fast-processing and great flexibility hardware	This work

CHAPTER 3

METHODOLOGY

3.1 Introduction

This chapter will cover the detail of the methodology used to develop the solar-powered lighting system via FPGA. The charging and discharging algorithm, ADC conversion, seven-segment display on FPGA, LED brightness with PWM technique, prototype implementation, and the battery lifecycle estimation will be explained in this chapter.

3.2 Methodology Flowchart

Figure 3.1 shows the methodology's flow chart, including the components identifying, design stages, simulations on the software, prototype implementation, and analysis.

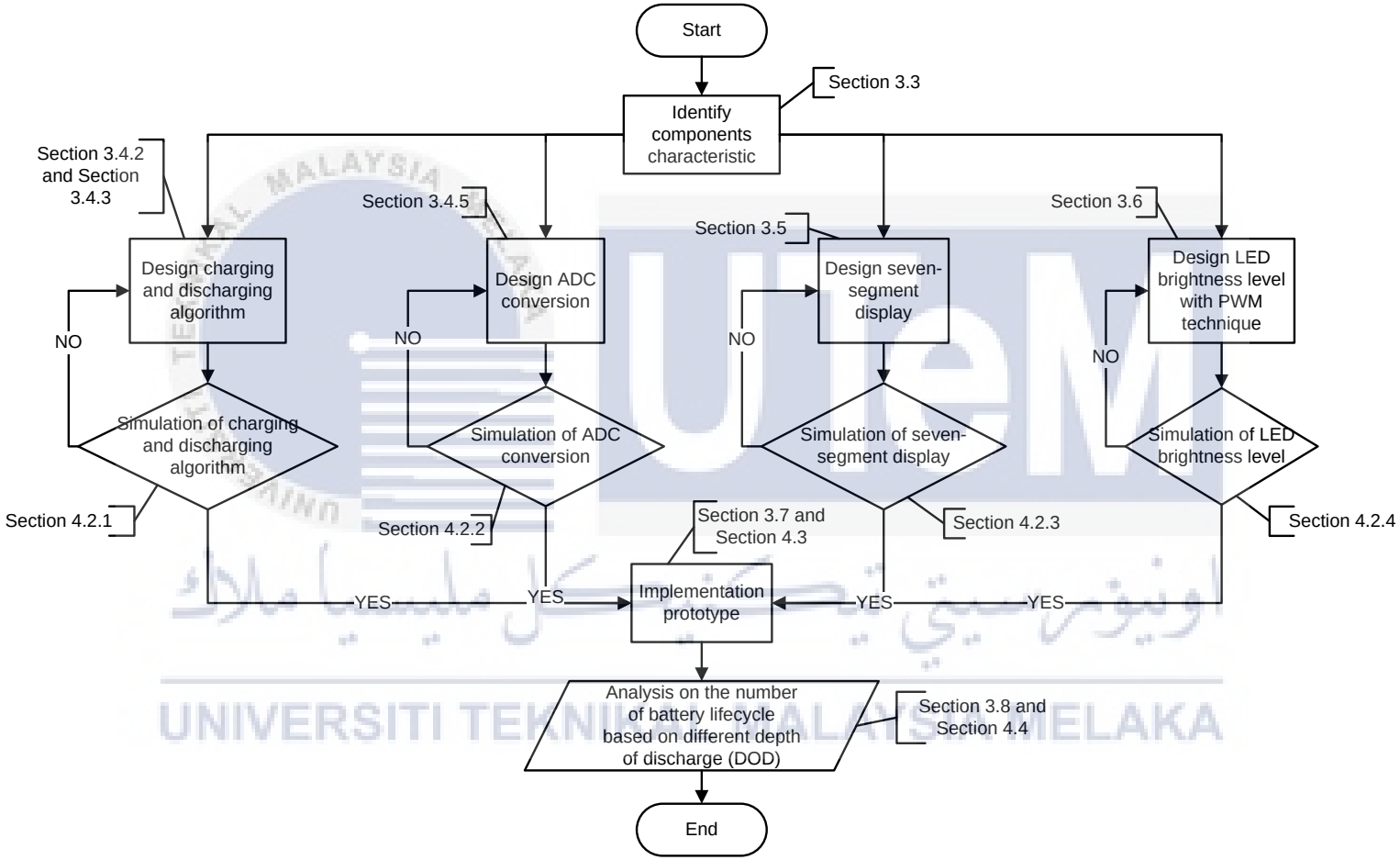

Figure 3.1 Methodology Flowchart

Firstly, the project started with identifying the component's characteristics. Next, the charging and discharging process will be discussed, including the algorithms. Besides that, the simulation of the charging and discharging algorithm will be discussed. Then, the design and the simulation results of ADC conversion will be discussed. After this, the design and simulation results of the seven-segment display will be discussed.

Furthermore, the method and the simulation results of LED brightness levels with the PWM technique will be discussed. Also, the prototype implementation and the results will be explained. Finally, the method and results of battery life cycle analyses based on the different Depth of Discharge (DOD) will also be analyzed.

3.3 Components Characteristic

Xilinx Spartan-6 FPGA Development board, as shown in Figure 3.2, has a 50MHz crystal oscillator frequency. Therefore, by using equation (3.1) below, one clock cycle of the FPGA is 20ns.

$$one\ clock\ cycle = T = \frac{1}{f} = \frac{1}{50MHz} = 20ns \quad (3.1)$$

Figure 3.2 Xilinx Spartan 6 FPGA Development Board

AD7822 [48], as shown in Figure 3.3, is a high-speed parallel 8-bits analog-to-digital converter with a maximum conversion time of 420ns. The input range of the AD7822 is 3V±10%, so a voltage divider was added between the connection of the battery and AD7822. The voltage divider consists of a variable resistor and a 1.1kΩ resistor. The voltage divider circuit becomes adjustable with a variable resistor to control the current flow through the circuit by changing the amount of resistance.

Figure 3.3 AD7822

An NCE6008AS [49] MOSFET, as shown in Figure 3.4, is used as a switch to control the charging mode and the LED brightness, and the advantage of NCE6008AS is fast switching.

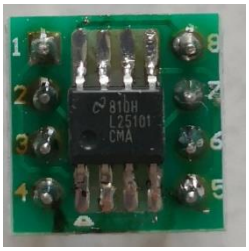

Figure 3.4 NCE6008AS MOSFET

3.4 Charging and Discharging Process of Solar Powered Lighting System

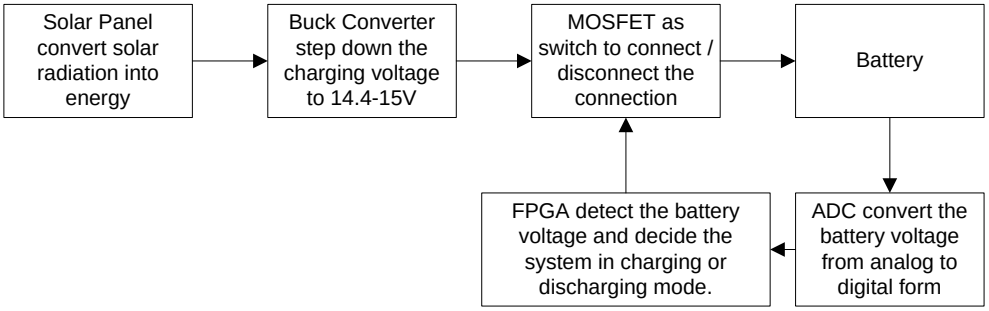

Figure 3.5 Charging Process of Solar Powered Lighting System

Refer to Figure 3.5, the 30W 18V solar panel will charge a 12V 7.2Ah battery through a buck converter. The buck converter will step down the voltage from the solar panel to charge the battery with a stable charging voltage of 14.7Vdc. An NCE6800AS MOSFET controlled by FPGA to connect and disconnect the charging circuit. On the other hand, the AD7822 always converts the battery level into digital form from the battery. The FPGA controls the MOSFET after detect the battery level from AD7822.

Table 3-1 State of Charge (SOC) of the 12V Lead-Acid Battery

Battery Voltage (V)	Volts per cell (V)	State of Charge (SOC)	Status
12.73	2.12	100%	Good
12.62	2.08	90%	
12.50	2.07	80%	
12.37	2.05	70%	
12.24	2.03	60%	
12.10	2.01	50%	
11.96	1.98	40%	
11.81	1.96	30%	Moderate
11.66	1.93	20%	
11.51	1.89	10%	Low
10.5	1.75	0%	

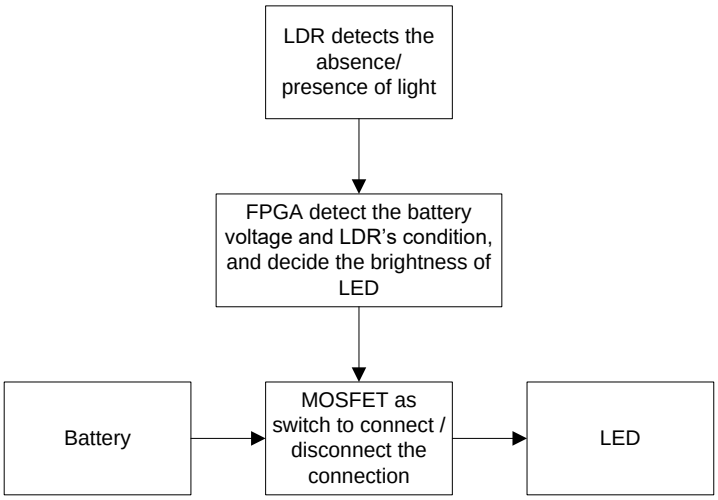

Figure 3.6 Discharging Process of Solar Powered Lighting System

After the battery is fully charged in charging mode, the battery will stop charging, and the system will operate in the discharging mode, as shown in Figure 3.6. In the discharging process, a light-dependent resistor (LDR) module as the input sensor sends the digital signal to detect the light intensity. When the LDR detects no lights, the MOSFET will fast switching according to the duty cycle generated from FPGA. Then, the LED will light on and start to dim based on the condition of battery voltage. Else, the MOSFET will in an OFF state when the LDR detect lights. According to Table 3-1, if the battery voltage is less than 12.24V or 60% of the battery level, the FPGA will stop the discharging mode and start charging.

3.4.1 Clock Divider for Charging and Discharging process

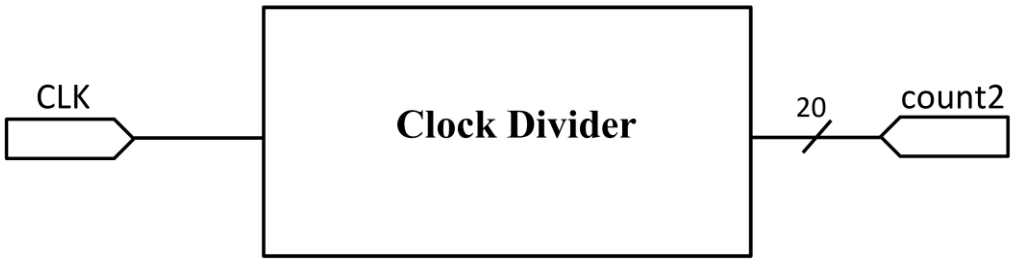

Figure 3.7 RTL of a clock divider

Since different clock frequencies drive several submodules, the clock divider is needed, as shown in Figure 3.7. The clock divider creates lower frequency clock signals from an input clock source. It counts input clock cycles and drives the output clock low and high. The clock divider counts the clock to a specific value of the submodule, and it returns to 0 and becomes a complete cycle. Five clock dividers will be used, first was the clock for hold voltage values, second used for the sequence of decimal place and the display of the seven-segment, third used for the charging, discharging and switching mode, fourth used for the duty cycle of LED brightness, and lastly is for the ADC for control the $\overline{CONVST}$ pin for converting analog signal to digital signal.

3.4.2 Charging Algorithm

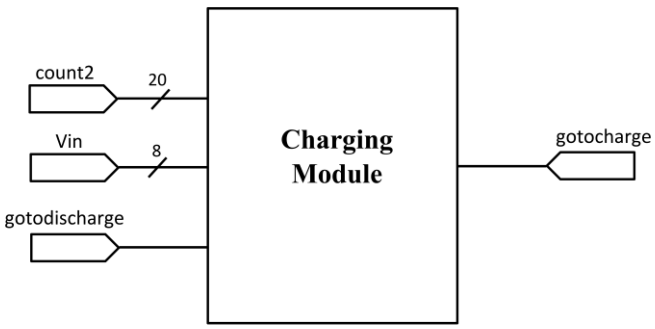

Figure 3.8 RTL of the charging module

In order to avoid overcharging, a charging algorithm was developed, as shown in Figure 3.8 and Figure 3.9. The charging algorithm starts with checking whether the charging mode is equal to 1, the algorithm will go to the next stage. The switch is always toggled and checks the battery voltage when the switch is opened, and the algorithm will repeat this stage if that battery voltage detected is lower than 12.72V. Otherwise, the system will go to the discharging mode when the battery is fully charged. If the charging mode is equal to 0 initially, the system is in the discharging mode and ends the algorithm.

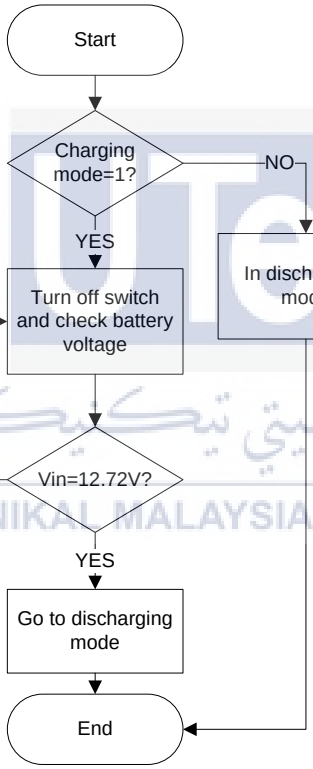

Figure 3.9 Charging Algorithm

3.4.3 Discharging Algorithm

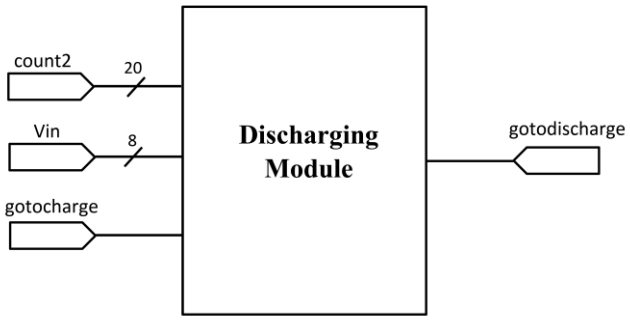

Figure 3.10 RTL of the discharging module

The discharging algorithm was developed to avoid over-discharging the battery, as shown in Figure 3.10 and Figure 3.11. Also, the discharging algorithm is used to determine the status of discharging after read the battery voltage. The discharging algorithm starts with checking whether the discharging mode is equal to 1, the algorithm will go to the next stage. The switch is always toggled and detects the battery voltage when the switch is opened, and the algorithm will repeat this stage if that battery voltage detected is greater than or equal to 12.24V. Otherwise, the system will go to the discharging mode when the battery is fully charged. If the charging mode is equal to 0 initially, this represents the system is in the charging mode and ends the algorithm.

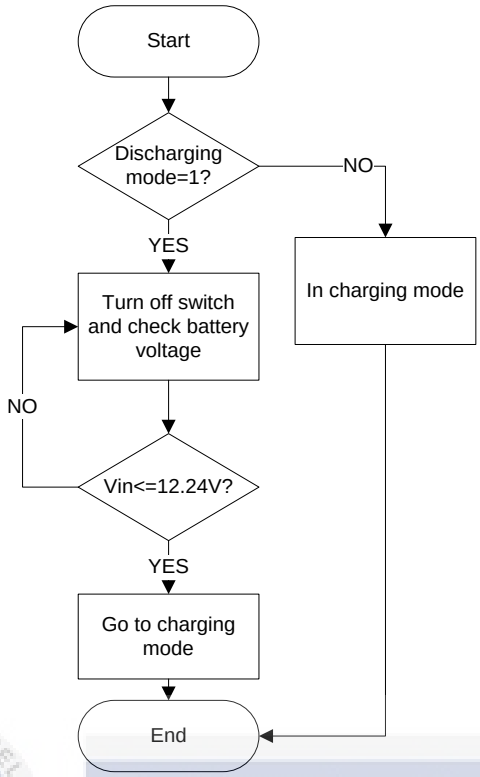

Figure 3.11 Discharging algorithm

3.4.4 Switching Algorithm (MOSFET)

An NCE6008AS MOSFET is used as a charging switch to control the charging mode. The MOSFET gate is connected with the assigned pin 30 of FPGA, and the drain and source of MOSFET are connected between the battery and solar panel. The FPGA will send the signal to make the MOSFET in OFF state to detect the battery voltage, which is there will be no current flow during the voltage reading. This action lets the ADC read the open-circuit voltage, not the input voltage from the solar panel. The FPGA will send the signal to make the MOSFET in ON state after reading voltage, and the system decides to continue charging. Otherwise, the MOSFET will stay OFF state after the system decides to go to discharge mode.

3.4.5 Analog-to-Digital Conversion

Since the FPGA development board has no in-built analog-to-digital converters, AD7822 is used as an external 8-bit ADC to convert the battery voltage from analog to digital. Besides that, AD7822 detects the voltage from the battery by connecting to the voltage divider because the input range of the AD7822 is 2V.

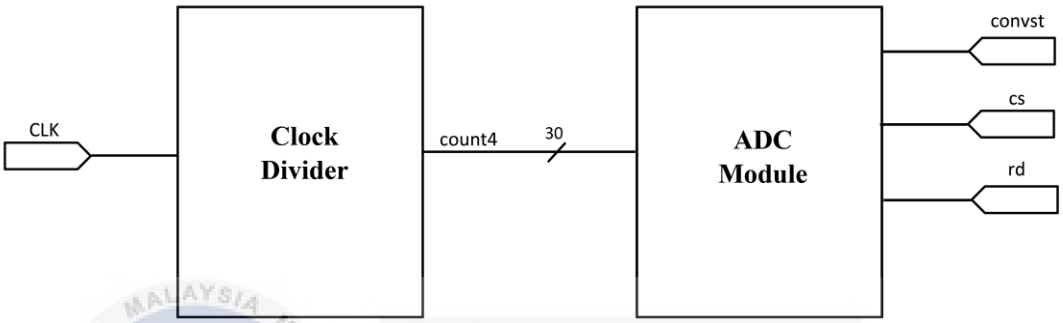

Figure 3.12 RTL of the ADC conversion module

Figure 3.12 shows the RTL circuit of the ADC module, the inputs are a clock divider module called 'clockcount', and the output is the $\overline{\text{CONVST}}$ signal. The $\overline{\text{CONVST}}$ signal is the logic input signal of AD7822, and the conversion start signal initiates an 8-bit analog-to-digital conversion on the falling edge of this signal. When the signal $\overline{\text{CONVST}}$ goes to 0, ADC will start the conversion at the falling edge. After that, the signal goes to 1 before the end of conversion. $\overline{\text{RD}}$ is a signal internally gated with the $\overline{\text{CS}}$, and both signals must be logic low to enable the data bus. Pin 17 of FPGA is connected to the pin $\overline{\text{RD}}$ on ADC, and FPGA's pin 16 is connected to the pin $\overline{\text{CS}}$. The 8-bit converted data will send to pin 56, 57, 58, 59, 61, 62, 66, 67 of FPGA through the DB0-DB7 of ADC.

3.5 Seven-Segment Display on FPGA board

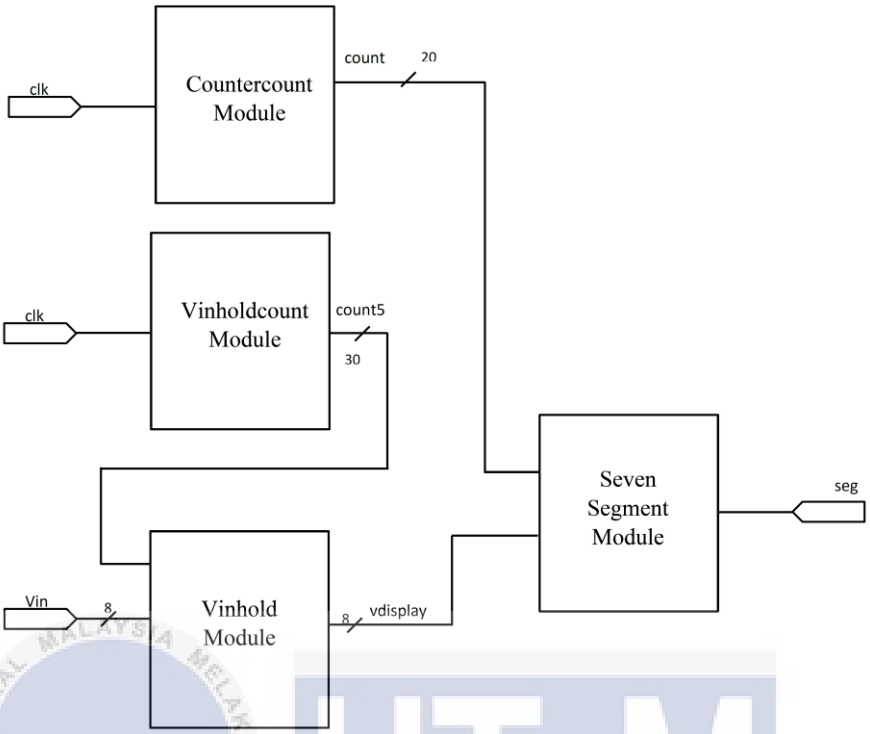

Figure 3.13 RTL of the seven-segment display module

The seven-segment on board will display the battery voltage all the time. According to Figure 3.14, seven-segment on the FPGA board's circuit structure is different from the commonly used ones. It connected these segments, so it can't assign the pin and operate separately on FPGA. Instead, the current will flow to all seven-segment on-board so that those segments will be light up simultaneously. In order to overcome this, a clock divider needed to create another clock in the design, as shown in Figure 3.13. The clock divider allows the seven-segment blinking continuously with much lower frequency but high enough, so the human eye missed out on display had flicking. The ‘vinhold’ module is a module to hold the input voltage value after the end of conversion at ADC and makes the ‘vin’ as the ‘vdisplay’, which will display on the seven-segment.

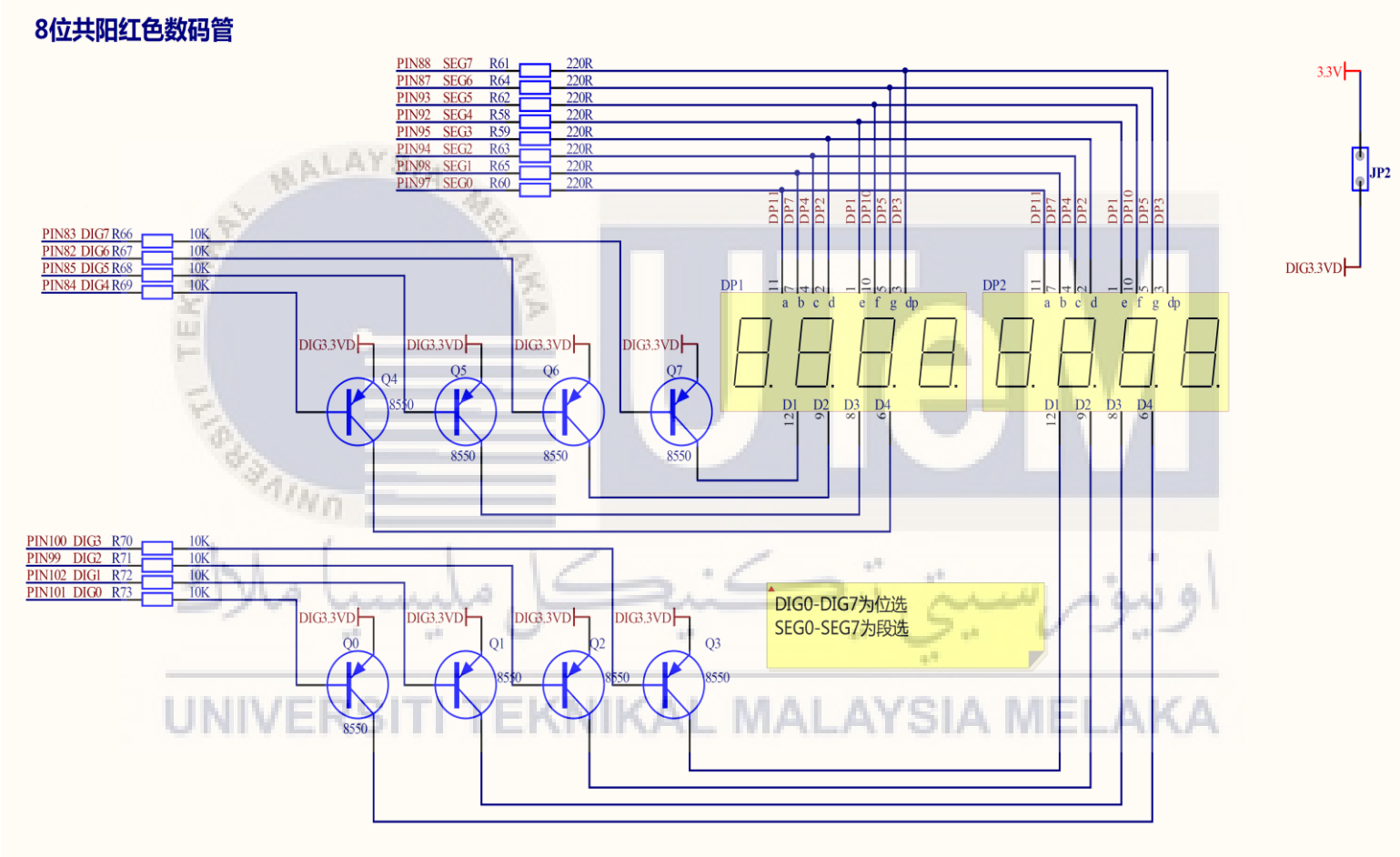

Figure 3.14 The circuit of seven-segment display [50]

3.5.1 Clock Divider for Seven-Segment

The clock divider divides the clocks at 2500, 5000, 7500, 10000, 12500, 15000, 17500, and 20000. Refer to Figure 3.15, the 1st segment will be light up according to the number assigned in the coding when the clock counted to 2500. Next, the 2nd segment will display the number assigned at the clock 5000. The 3rd segment and 4th segment will also display the number assigned at clock 7500 and 10000. However, there will be no number assigned and displayed for the following four seven-segment.

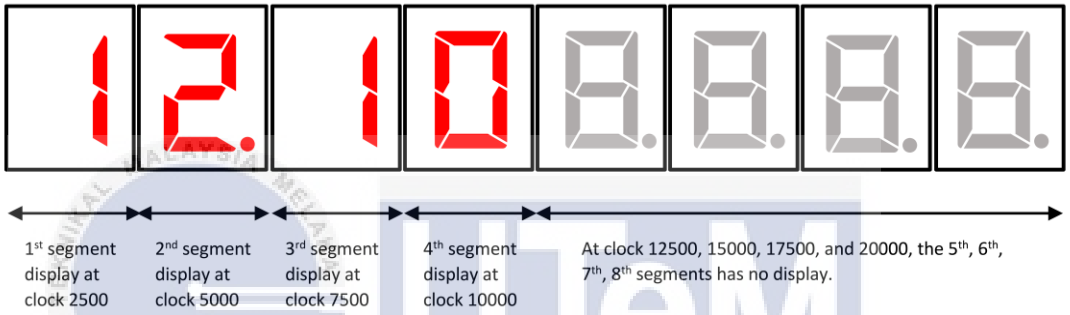

Figure 3.15 Seven-segment display using clock divider

3.5.2 Seven-segment Display

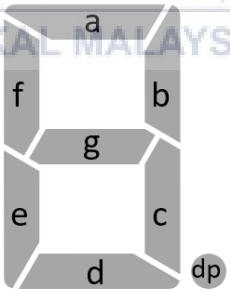

Figure 3.16 The pin diagram of the seven-segment display

Since only four numbers will be displayed on the seven-segment, the values will be assigned only four-digit numbers. Using equation (3.2), the steps of the battery voltage level are 256, which means 256 different values of battery voltage are assigned in the module.

$$steps = 2^n = 2^8 = 256 \quad (3.2)$$

In the seven-segment display module, 15.30V is the highest value after using equations (3.3) and (3.4).

$$voltage\ value\ for\ each\ step\ size = \frac{14.70V}{256} = 0.057 \approx 0.06V \quad (3.3)$$

$$0.06V \times bit = 0.06V \times 255 = 15.30V \quad (3.4)$$

Refer to equations (3.3) and (3.4), the battery voltage level per bit was calculated and converted in binary and hex form for implementation in FPGA. Table 3-2 shows the sequence of the battery voltage levels from 0V to 15.30V.

Table 3-2 The battery voltage in binary and hex form

Battery Voltage (Binary)	Battery Voltage (Hex)	Battery Voltage (V)
0000 0000	0	0V
0000 0001	1	0.06V
0000 0010	2	0.12V
:	:	:
:	:	:
:	:	:
1111 1110	FE	15.24V
1111 1111	FF	15.30V

Refer to Figure 3.16, the pin of the display number is arranged in Table 3-3. Besides that, 256 different voltage values are programmed according to the clock distribution and the truth table of each number. Finally, the simulation result will be discussed in section 4.2.3.

Table 3-3 The truth table of seven-segment with and without decimals

Number	a	b	c	d	e	f	g	Decimal (dp)
1	1	0	0	1	1	1	1	1
2	0	0	1	0	0	1	0	1
3	0	0	0	0	1	1	0	1
4	1	0	0	1	1	0	0	1
5	0	1	0	0	1	0	0	1
6	0	1	0	0	0	0	0	1
7	0	0	0	1	1	1	1	1
8	0	0	0	0	0	0	0	1
9	0	0	0	0	1	0	0	1
0	1	1	1	1	1	1	1	1
1.	1	0	0	1	1	1	1	0
2.	0	0	1	0	0	1	0	0
3.	0	0	0	0	1	1	0	0
4.	1	0	0	1	1	0	0	0
5.	0	1	0	0	1	0	0	0
6.	0	1	0	0	0	0	0	0
7.	0	0	0	1	1	1	1	0
8.	0	0	0	0	0	0	0	0
9.	0	0	0	0	1	0	0	0
0.	1	1	1	1	1	1	1	0

3.6 LED brightness levels with PWM technique

Different brightness levels of the LED were designed with the PWM signal to extend the lighting hours. Figure 3.17 shows the LED brightness module has five inputs: ‘clk’, ‘pwmcount’, ‘gotodischarge’, ‘vin’, and ‘ldr’. The ‘pwmcount’ module is a clock divider module that always counts the clock until 100, and it is the input of the LED brightness module.

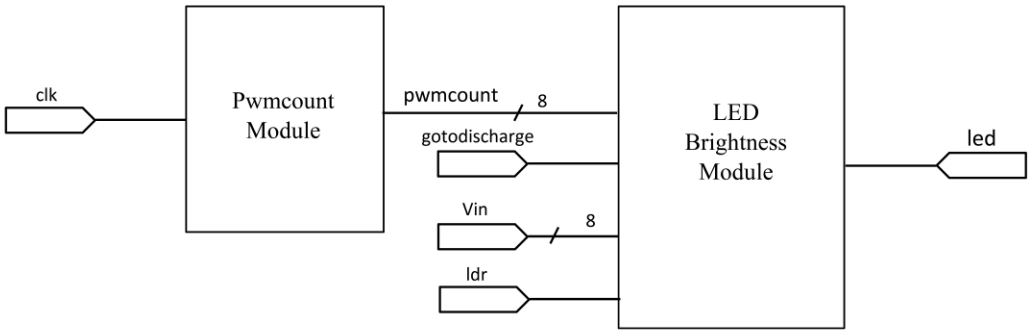

Figure 3.17 RTL of the LED module

In order to design the LED brightness level, Equations (3.5) and (3.6) are used to calculate the total clock required to be in a high state within a count of 100.

$$100 \times 50\% = 50 \quad (3.5)$$

$$100 \times 100\% = 100 \quad (3.6)$$

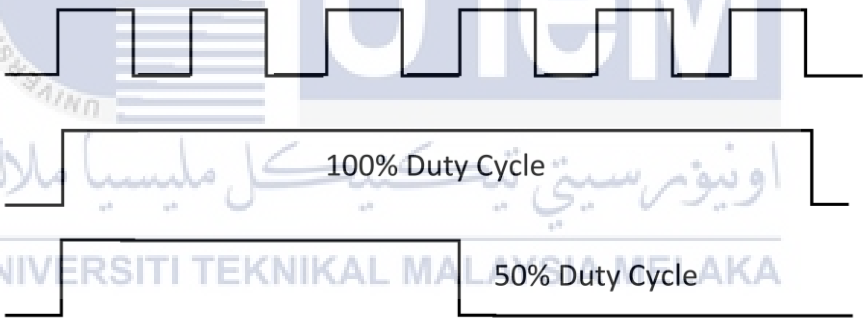

Figure 3.18 Waveform for the 100% and 50% duty cycle of LED

Refer to Table 3-4, the LED will turn on with a full duty cycle, in which the LED brightness is 100% when the LDR sensor detects no light and battery voltage is greater than or equal to 12.48V. However, when the battery voltage is lower than 12.48V, the LED will turn on half of the duty cycle, which the LED brightness is only 50% when the LDR sensor detects no light. For example, the waveform for the different brightness levels is shown in Figure 3.18.

Table 3-4 LED Brightness

Battery Voltage	Brightness (%)
>=12.48V	100%
<12.48V	50%

3.7 Prototype of the Solar Powered Lighting System

The prototype consists of a 30W 18V monocrystalline solar panel, a GP1272 lead-acid battery, a buck converter, two NCE6008AS MOSFETs, a trimmer, two 1kΩ resistors, an 8-bit analog-to-digital converter AD7822, and two 4W LED. A 30W 18V monocrystalline solar panel charges the battery with a stable voltage 14.7Vdc by using a buck converter. In addition, a voltage divider, as shown in Figure 3.19, is placed between the lead-acid battery and AD7822 as the protection circuit since the input range of the AD7822 is 2V.

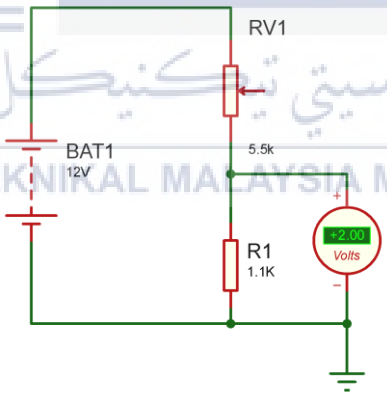

Figure 3.19 Voltage divider for the ADC protection

In the charging circuit, an NCE6008AS MOSFET is connected between the buck converter and the lead-acid battery. In addition, the drain and source pin of MOSFET connected between the solar panel and lead-acid battery, and the gate pin of MOSFET will be connected to pin 30 of the FPGA to control the charging mode shown in Figure 3.20.

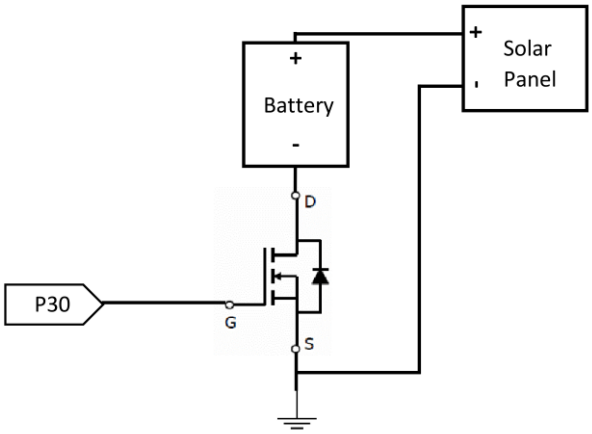

Figure 3.20 MOSFET in charging circuit

Another NCE6008AS MOSFET was used to control the PWM signal from the FPGA in the discharging circuit, as shown in Figure 3.21. The gate pin of the MOSFET will connect to pin 33 of FPGA, the drain and source pin of the MOSFET will connect to the output LED and battery.

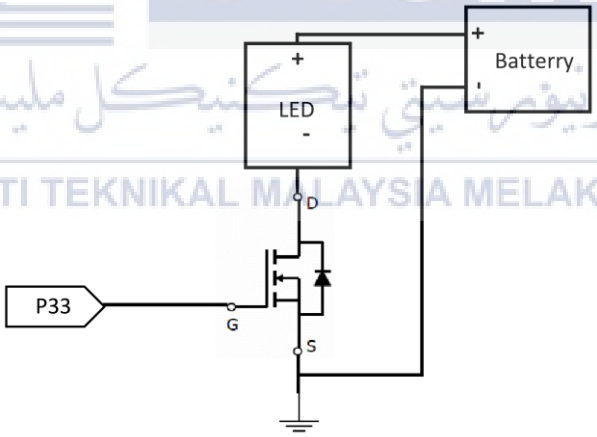

Figure 3.21 MOSFET in discharging circuit

Implementation constraints are instructions given to FPGA implementation tools to direct the mapping, layout, timing when processing the FPGA design. However, the implementation constraints are generally placed at User Constraints File (UCF), which is defined as used to complete timing constraints, pin constraints, and area constraints.

Besides that, UCF files are ASCII code files describing logic design constraints and can be edited with a text editor and Xilinx constraint file editor. Table 3-5 shows the I/O port and its pin allocation in Xilinx Spartan 6 FPGA development board.

Table 3-5 UCF file: I/O Port and the pin allocation

I/O	PIN	I/O	PIN	I/O	PIN	I/O	PIN
DIG[0]	P101	SEG[0]	P97	VIN[0]	P67	CLK	P22
DIG[1]	P102	SEG[1]	P98	VIN[1]	P66	CONVST	P81
DIG[2]	P99	SEG[2]	P94	VIN[2]	P62	CS	P16
DIG[3]	P100	SEG[3]	P95	VIN[3]	P61	RD	P17
DIG[4]	P84	SEG[4]	P92	VIN[4]	P59	EOC	P79
DIG[5]	P85	SEG[5]	P93	VIN[5]	P58	LDR	P35
DIG[6]	P82	SEG[6]	P87	VIN[6]	P57	LED	P33
DIG[7]	P83	SEG[7]	P88	VIN[7]	P56	SWITCH	P30
						ADCLED	P29

3.8 Analysis on the number of battery lifecycle based on the Depth of Discharge (DOD)

This section will discuss the number of battery life cycles based on the Depth of Discharge (DOD). First, the total time in hours to complete one system operation cycle will be obtained, including the charging and discharging process. For analysis, the solar lighting system will operate on three days with similar weather, record the total time in hours from the battery charging to fully charged, and discharge it until the Depth of Discharge is 40%. In order to compare the number of battery life cycle on the different Depth of Discharge (DOD), the system will repeat the whole process a total of three times: first, the battery will be discharged until the Depth of Discharge 40%, second times the battery will discharge until the Depth of Discharge 50%, and the third times the battery will start to discharge until the Depth of Discharge 60%.

3.9 Summary

First of all, the method of charging and discharging process had been discussed in this chapter. The clock divider was developed to produce a slower output frequency by dividing the input clock in the charging process. In order to avoid over-charging and over-discharging of the battery, the charging and discharging algorithm were developed. Also, a switching algorithm was developed to control the charging switch for open-circuit voltage detection and charging circuit connection. Next, $\overline{CONVST}$ signal was generated to let the conversion start signal starts the 8-bit analog-to-digital conversion on the falling edge of the signal.

In addition, the seven-segment display on FPGA also had been discussed. Two clock dividers were developed to hold the display voltage value, and another is used to create a slower frequency for the seven-segment display. Besides that, the different brightness levels of the LED are also discussed. The LED stays in the HIGH state through the PWM signal within a full duty cycle or half of the duty cycle during darkness and meets the specific battery level. Lastly, the hardware circuit of the prototype and the analysis method also had been discussed. The simulation and prototype results will be discussed and analyzed in the next chapter.

CHAPTER 4

RESULTS AND DISCUSSION

4.1 Introduction

This chapter includes all the simulation and hardware implementation results achieved by completing all the methodologies in the previous chapter. Besides that, the result will be described in each part of this chapter. Furthermore, the result of the number of battery life cycles also will be analyzed in this chapter.

4.2 Simulation results of Solar Powered Lighting System

This section is discussing the simulation results of the solar-powered lighting system. In order to verify the methods, simulation of the systems was run by the software Xilinx ISE 14.7.

4.2.1 Simulation results of charging and discharging algorithm

This section is discussing the simulation results of the charging and discharging algorithm. A 2.5kHz clock counter was generated to count 20000 clocks and return to 0, which uses a total $400\mu s$ per cycle. The charging mode module will determine the

status of the charging mode at clock 25 by detects the battery voltage and the state of the charging flag, which is named ‘gotocharge’. It represents a flag to determine the system will be in charging mode or discharging mode. Figure 4.1 shows that the ‘gotocharge’ signal goes to 0 when the battery is fully charged at clock 25, which means the system stops the charging process.

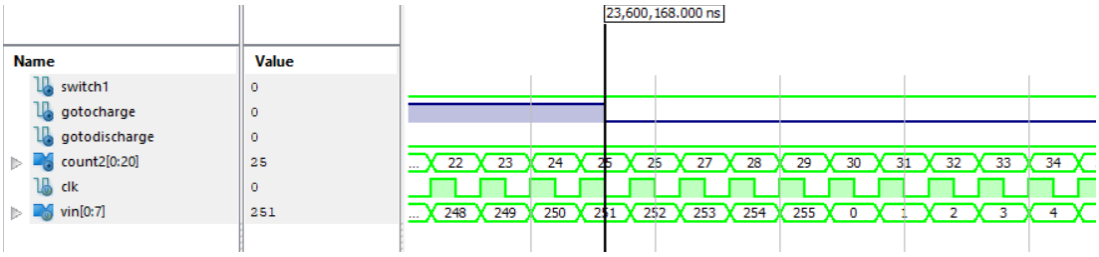

Figure 4.1 Simulation result of charging mode when the FPGA detects the battery is fully charged

Figure 4.2 shows the ‘gotocharge’ signal goes to 1 when the input voltage detected is lower than 12.24V at clock 25, which means the system starts the charging process.

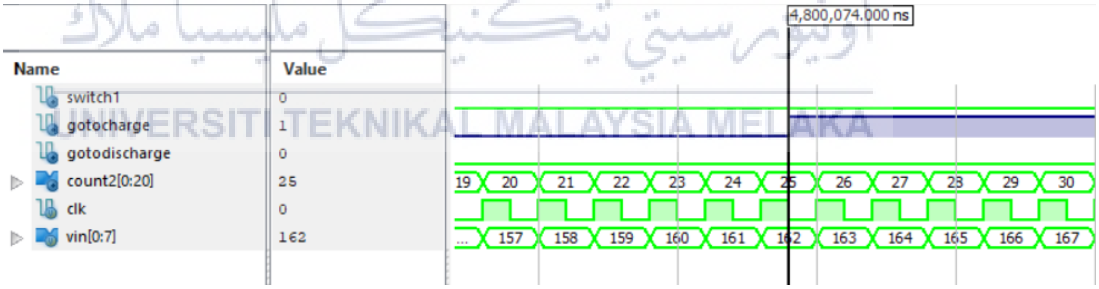

Figure 4.2 Simulation result of charging mode when the system detects the low voltage of the battery

The system will determine the status of the discharging mode at clock 51 by detects the battery voltage and the state of the discharging flag, which is named ‘gotodischarge’. Figure 4.3 shows that the ‘gotodischarge’ signal at clock 51 goes to 0 when the input voltage is lower than 12.24V, which means the system stops the discharging process.

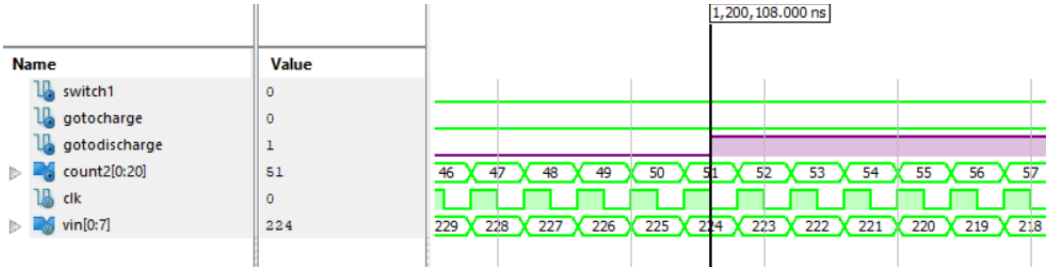

Figure 4.3 Simulation result of discharging mode when the system detects the battery is fully charged

However, Figure 4.4 shows the 'gotodischarge' signal goes to 1 when the battery is fully charged at clock 51, which means the system starts the discharging process.

Figure 4.4 Simulation result of discharging mode when the system detects the low battery voltage

The switching mode module functions to control the charging switch, which is the NCE6008AS MOSFET. Figure 4.5 shows the switch goes 0 which starts from clock one during every cycle, and it is designed to let the system detects the open-circuit input voltage between this gap, and the system will decide the charging switch opened or closed at clock 51, according to the charging signal.

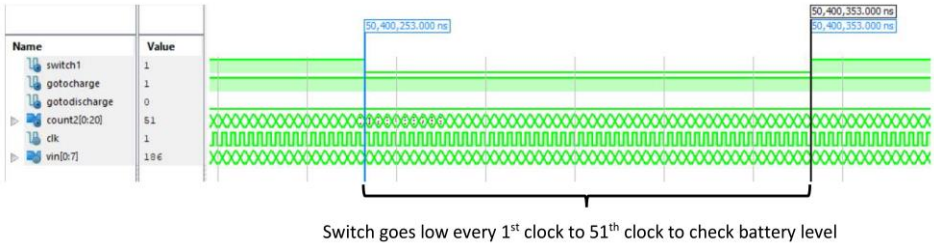

Figure 4.5 Simulation of switching mode

4.2.2 Simulation results of analog-to-digital conversion

The state of ADC conversion is discussed in this section. Figure 4.6 shows the falling edge of the $\overline{\text{CONVST}}$ initiates a conversion at clock 1 to start the conversion and the $\overline{\text{CONVST}}$ signal goes high at clock 3, which before the end of a conversion.

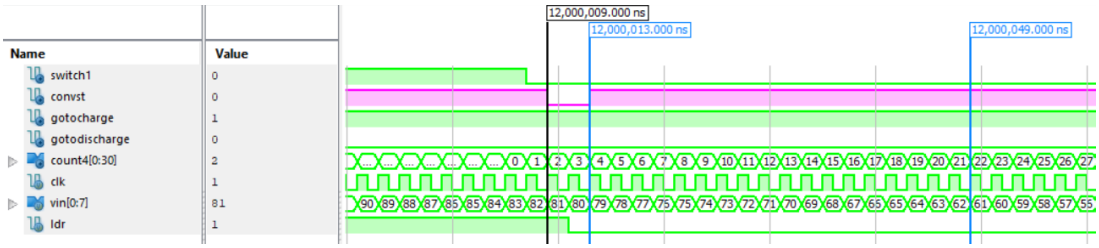

Figure 4.6 Simulation of $\overline{\text{CONVST}}$ signal in conversion process

4.2.3 Simulation results of seven-segment display

This section is discussing the simulation results of the seven-segment display. Figure 4.7 shows that the input voltage value of the clock 20000 is 31, or 1.86V that obtained by using equation (4.1). The voltage value is displayed in four-digit numbers, which is 01.86V.

$$the\ voltage\ value\ of\ 31 = (31 \times 0.06V) = 1.86V \quad (4.1)$$

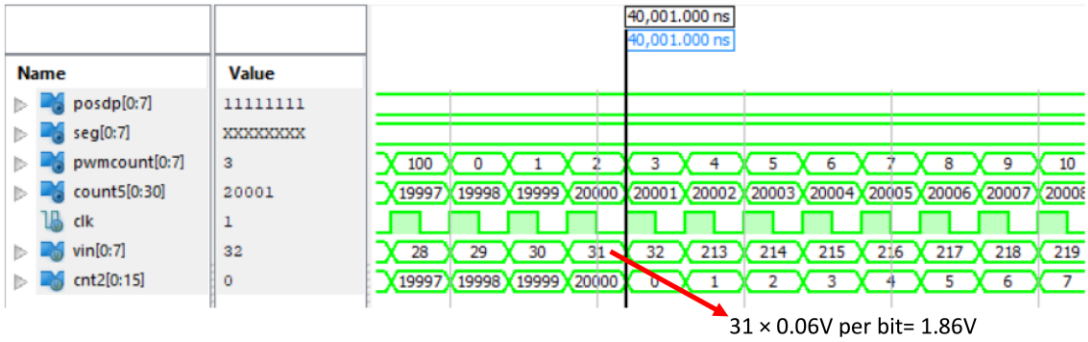

Figure 4.7 The input voltage detected by FPGA

As stated in Table 3-3, Figure 4.8 shows that the number displayed on the first seven-segment is ‘0’. The number displayed on the next seven-segment is ‘1.’ After this, the number displayed is ‘8’ at the third seven-segment, and the number displayed is ‘6’ at the fourth seven-segment.

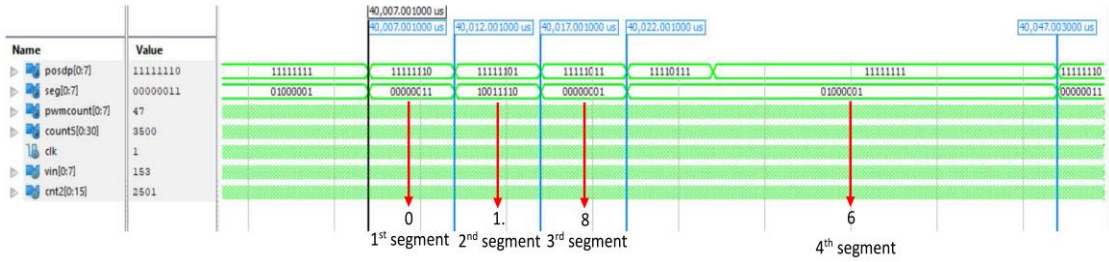

Figure 4.8 The value displayed on the seven-segment

4.2.4 Simulation results of LED brightness levels

In this simulation, the brightness of the LED will be varied by the battery voltage. Figure 4.9 shows the waveform of the LED when it 100% brightness. By using equation (4.1), the input voltage detected is greater than 12.24V. As a result, the LED turns on at 100% duty cycle during LDR in state HIGH with this voltage level.

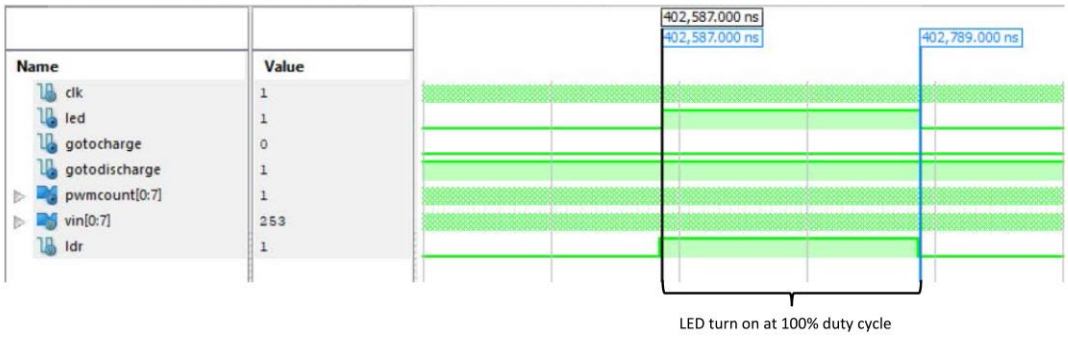

Figure 4.9 Simulation result of 100% brightness of the LED

However, Figure 4.10 shows the waveform of the LED when it 50% brightness, the input voltage detected is lower than 12.24V by using equation (4.1). As a result, the LED turns on at 50% duty cycle during LDR in state HIGH with this voltage level.

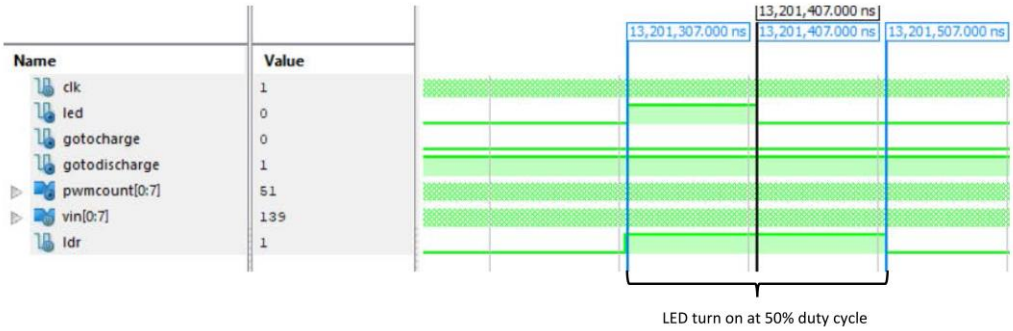

Figure 4.10 Simulation result of 50% brightness of the LED

4.3 Prototype results of Solar Powered Lighting System

After simulation results were obtained, the prototype implementation was done using FPGA. Figure 4.11 shows the hardware circuit of the solar-powered lighting system, which consists of FPGA, MOSFET circuit, ADC, voltage divider circuit, LED, lead-acid battery, and solar panel.

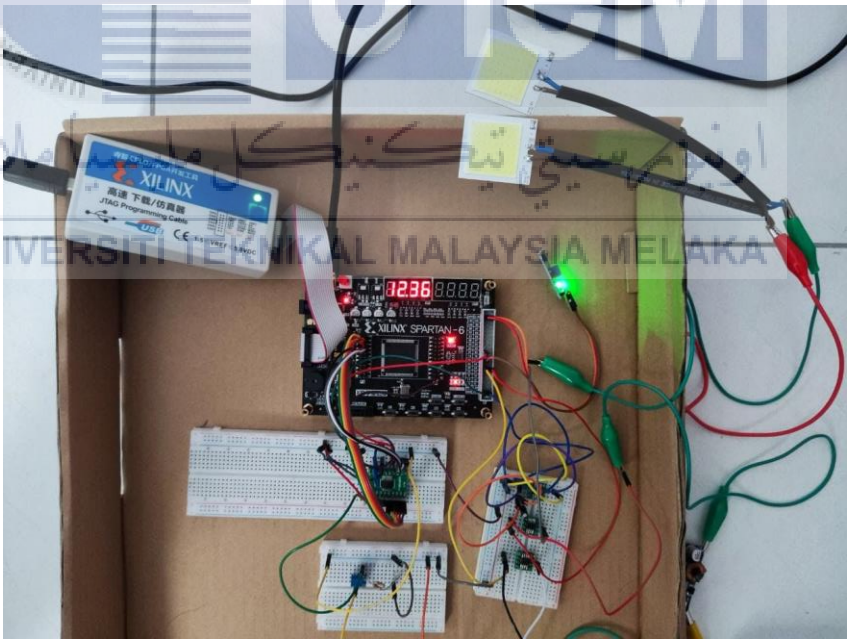

Figure 4.11 Hardware circuit of the Solar Powered Lighting System

In order to protect the AD7822, a voltage divider circuit consists of a trimmer, and two parallel resistors were used to connected between battery and ADC, as shown in

Figure 4.12. In addition, calibration was done before starts the operation to ensure the accuracy of the input voltage reading.

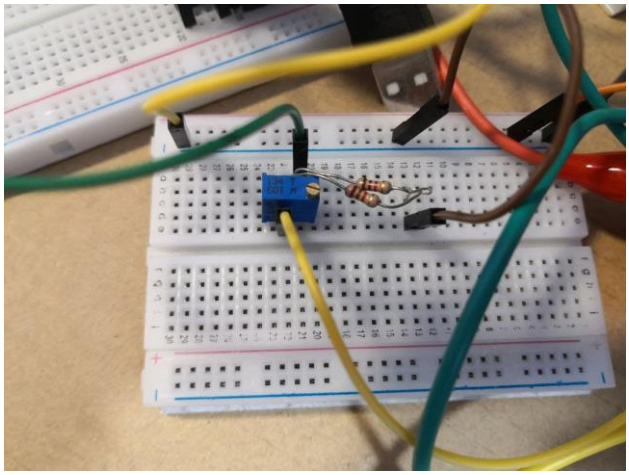

Figure 4.12 Voltage divider circuit

Besides that, the charging and discharging MOSFET were connected with the MOSFET driver shown in Figure 4.13. The MOSFET driver was connected between the PWM output of the FPGA and the gate of MOSFET to operate and ensure the fast switching and reduce related losses.

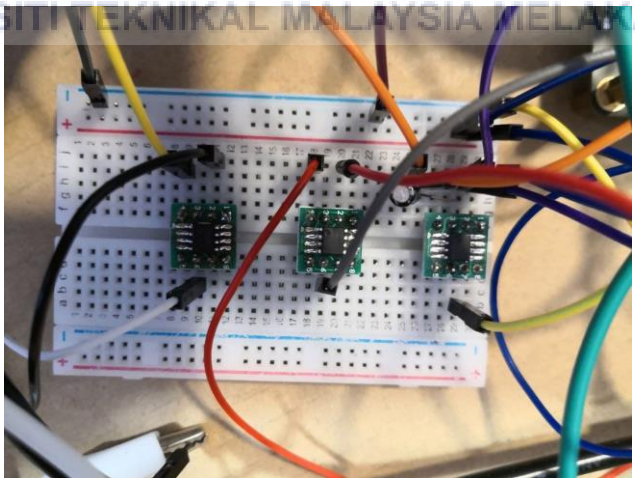

Figure 4.13 MOSFET Driver and N-type MOSFET circuit

The LED was operated in two different brightness levels, which are 50% and 100% brightness. As the results, Figure 4.14 shows that the LED turns on with 50%

brightness during the LDR detects darkness and meets the input voltage lower than 12.48V.

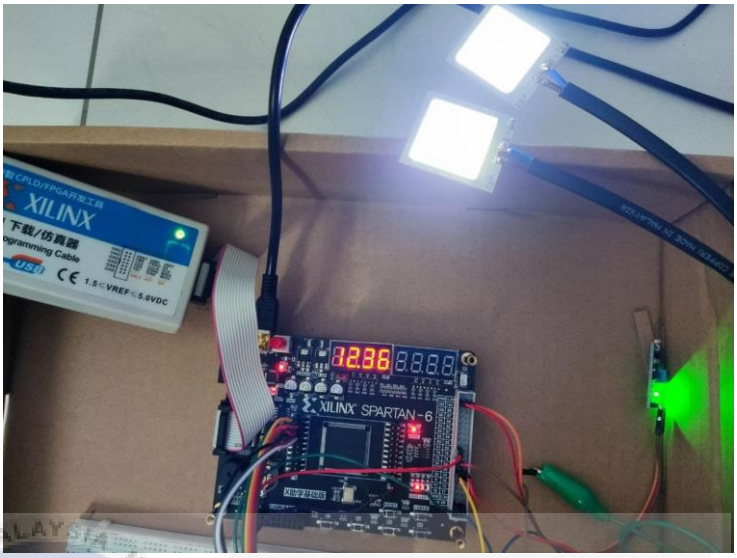

Figure 4.14 LED turn on with 50% brightness

However, Figure 4.15 shows that the LED turns on with 100% brightness during the LDR detects darkness and meets the input voltage greater than 12.48V.

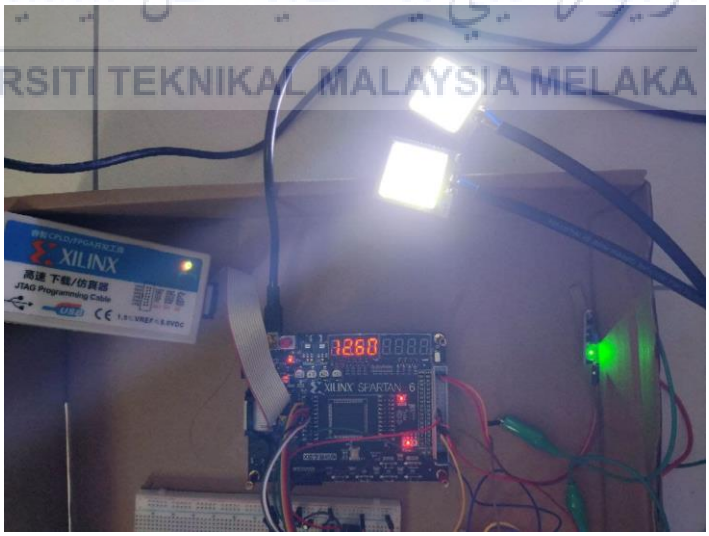

Figure 4.15 LED turn on with 100% brightness

4.4 Analysis on the number of battery lifecycle based on the Depth of Discharge (DOD)

In order to obtain the results, three different experiments based on different Depth of Discharge (DOD) were carried out on three days with similar weather. This section will discuss the results of total charging time, total discharging time, and the number of the battery lifecycle based on three different Depth of Discharge (DOD).

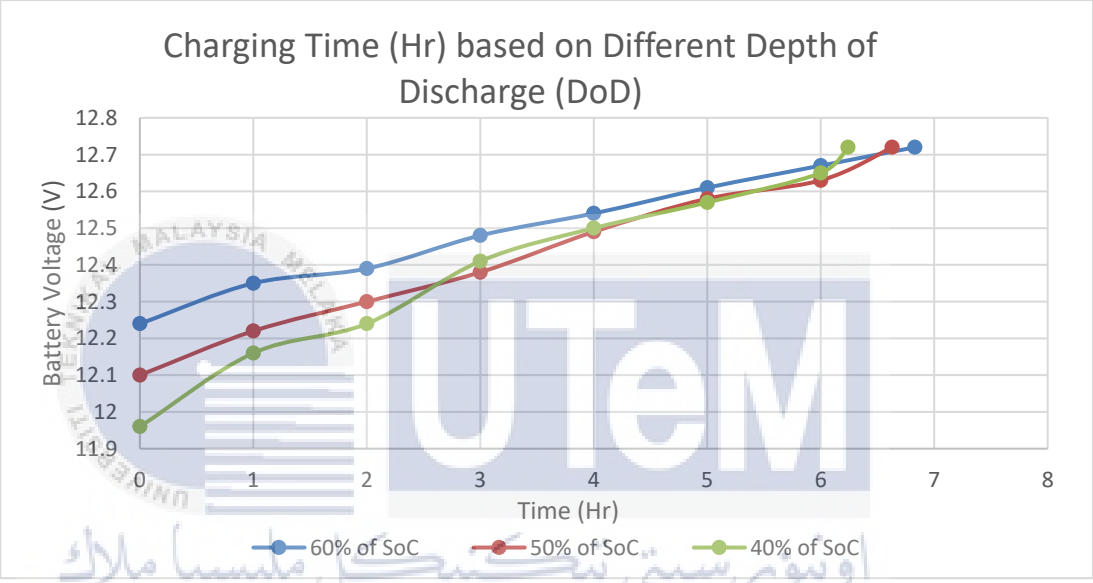

Figure 4.16 Results graph for total charging time based on different Depth of Discharge (DOD)

According to Figure 4.16, the total charging time was obtained based on three different DOD. First, the system starts to charge the battery from 12.24V to fully charged, and the process took 6.83 hours. Next, the system starts to charge the battery from 12.1V to fully charged with 6.63 hours taken. Lastly, the system starts to charge the battery from 11.96V to fully charged, and a total of 6.24 hours is used in this process.

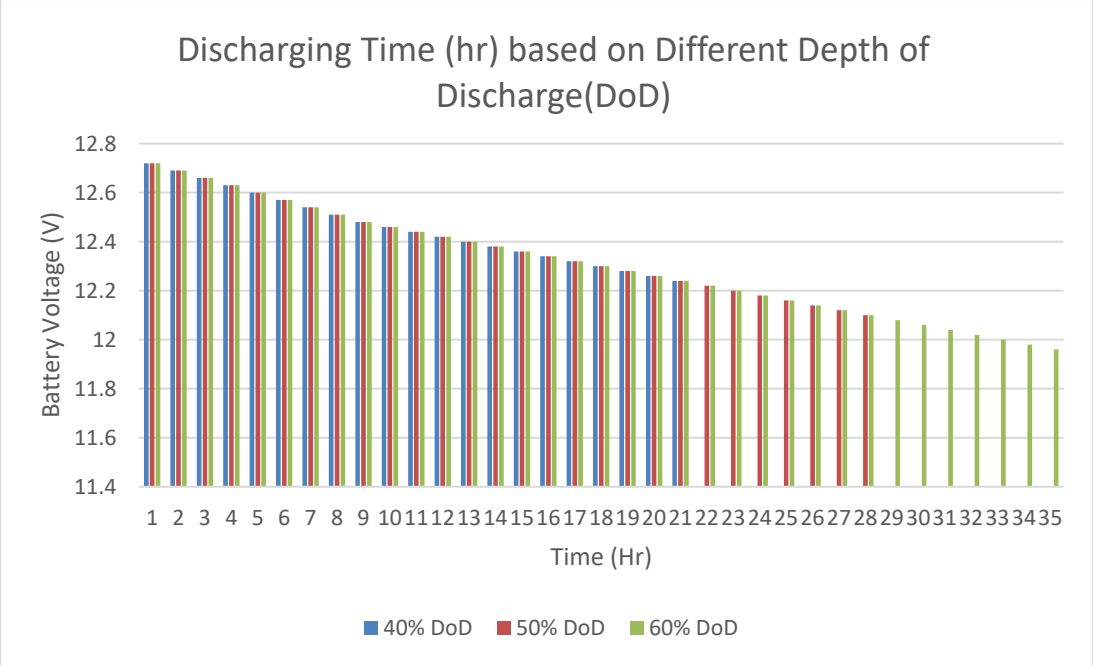

Figure 4.17 Results graph for total discharging time based on different Depth of Discharge (DOD)

According to Figure 4.17, the total discharging time was obtained based on three different DOD. First, in order to discharge the battery with a DOD of 40%, it takes 21 hours to discharge the battery to 12.24V. Next, the discharge process took 28 hours to discharge the battery to 50% of the DOD, which means discharge the battery until it remains 12.1V. Last, it takes 35 hours to discharge the battery to 60% of the DOD, which means the battery discharges to the remaining 11.96V. Total up the charging and discharging time of each operation, the total hours of the operation based on 40% of DOD is 27.83 hours. Based on the 50% of DOD of the system operation, there are 34.63 hours taken to complete the whole process. Lastly, the total hours taken is 41.24 hours for the operation based on 60% of DOD.

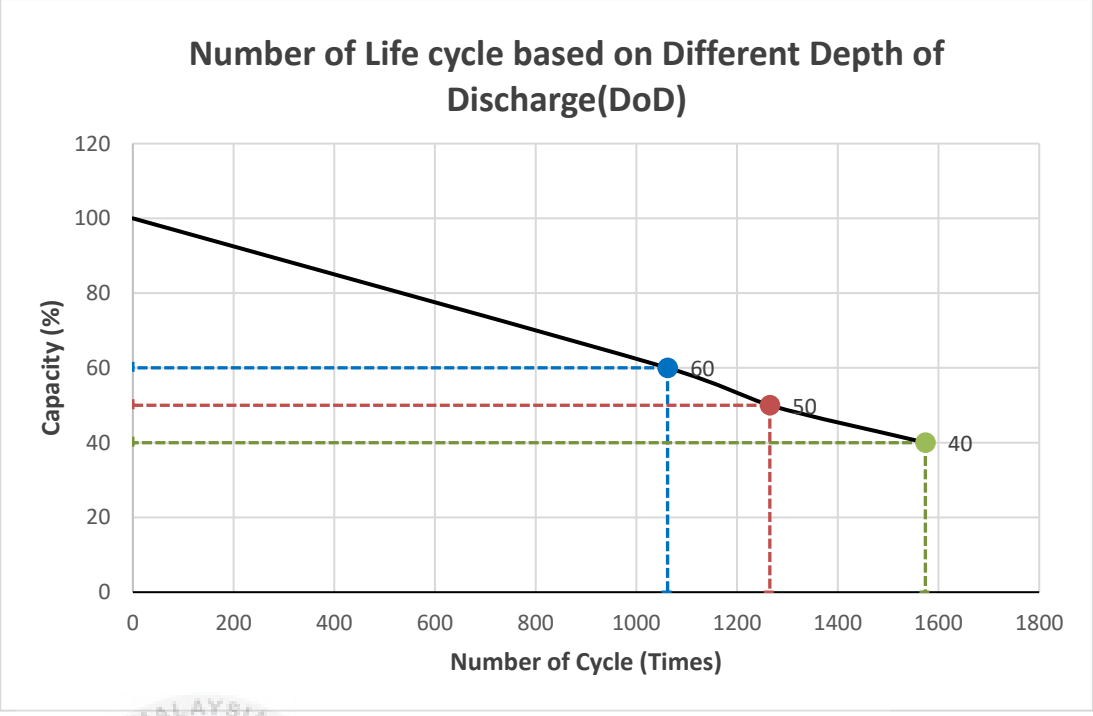

Figure 4.18 Results graph of the number of battery life cycle based on different Depth of Discharge (DOD)

According to Figure 4.18, the number of the battery life cycle based on different Depth of Discharge (DOD) was obtained using equation (2.1). First of all, the number of battery cycles based on 40% DOD is 1574, which means that when the battery is discharged to 40% DOD every cycle, it can be used 1574 times to the end of its life. Secondly, the number of battery cycles calculated at 50% DOD is 1265, which means that when the battery is discharged to 50% DOD per cycle, it can be used 1265 times to the end of its life. Lastly, when the battery is discharged until 60% DOD or 11.96V per cycle, the battery can be used only 1062 times to the end of the battery lifespan.

4.5 Project Features

This solar-powered lighting system is a stand-alone lighting system powered by a solar panel, so there is no reliance on grid energy. In other words, the solar-powered lighting system can be installed anywhere, and it can be installed in a rural area or uses as home lighting and backup lighting.

Next, the solar-powered lighting system is an eco-friendly and sustainable lighting system. As mentioned in the project introduction, the solar-powered lighting system is powered by solar energy. Solar energy is one renewable source that plays an important role in reducing the carbon footprint of energy produced by non-renewable energy sources. Also, sustainability was defined as satisfies the needs of contemporary people without compromising the development of the ability of future generations to meet their needs. Solar energy embodies this widely accepted definition of sustainability because solar energy can be used indefinitely without reducing its future availability.

Also, the solar-powered lighting system is cost-effective, which is no energy bill and no installation fee. In addition, people no longer need to pay the cost of electricity every month because the system is not reliant on grid energy. Instead, all need to pay one-time for the initial cost, and there is a very low maintenance fee.

Furthermore, this solar-powered lighting system extends the lighting hours. This is because the LED of the solar-powered lighting system only uses little power to be lighted up. As a result, the LED of this solar-powered lighting system can be lighted up as long as 21 hours with two different brightness levels. Therefore, installing the solar-powered lighting system in a public area will increase the public's sense of safety, increasing the use of public assets such as recreational areas and parks.

4.6 Summary

This chapter discusses the results obtained when all the described methods are executed correctly. First of all, the simulation of the solar-powered lighting system was carried out using the software Xilinx ISE 14.7, and its results were also discussed. Besides that, the prototype was also implemented by using FPGA. After the prototype

implementation, the total charging and discharging times were also recorded during the system operation. Lastly, the battery life cycle number was carried out and analysed based on different Depth of Discharge (DOD). An overall and more detailed conclusion about these results will be discussed in the next chapter.

CHAPTER 5

CONCLUSION AND FUTURE WORKS

This chapter concludes the entire project, including discussing the achievement of objectives and the general work of the prototype. Future suggestions for improvement of the project are discussed at the end of this chapter.

5.1 Conclusion

To concludes the entire project, it can be said that the project objectives have been successfully achieved. The prototype of the solar-powered lighting system was successfully developed using Xilinx Spartan 6 FPGA Development Board. The system was operated smoothly with the charging and discharging process. The charging and discharging algorithm was successfully developed to avoid overcharging and over-discharging of the battery. Besides that, the FPGA able to read the input voltage through the AD7822 8-bit ADC converter and display the input voltage on the seven-segment. In addition, the lighting hours are successfully extended because the

brightness levels of the LED dimmed accordingly when the battery level is different. Overall, the results show the FPGA allows several tasks to run in parallel at the hardware level. In order to develop the system, the execution of each sub-module was carefully managed to meet the timing requirements of the entire control loop. Therefore, all of these functions can integrate into a single controller by using the truly parallel execution features of the FPGA. To briefly paraphrase, the benefit of this project by using FPGA was also highlighted, which is the FPGA can fully customize with every clock cycle to generate different tasks simultaneously.

Furthermore, the total hours of each operation of the system were obtained successfully. The charging and discharging process was repeated to operate three times with different Depth of Discharge (DOD) to collect the total hours of each operation. The number of battery life cycles based on the different Depth of Discharge (DOD) has been estimated. According to the results, there is a longer lifespan when the lead-acid battery will not be deeply discharged. Depth of Discharge (DOD) is one of the factors that affect the battery life cycle. However, other factors can also be considered, including corrosion, temperature, state of charge, degradation of active materials, and overcharge conditions. In addition, there may be different ways to estimate battery life. Therefore, various methods can be used to make better comparisons to obtain the best battery life cycle estimation in the future.

5.2 Future Work

There are several recommendations listed to improve the solar-powered lighting system using Xilinx Spartan 6 FPGA Development Board. Firstly, the greater the number of bits of precision, the greater the ability to eliminate the slightest difference in the measured value. Therefore, the 8-bit analog-to-digital converter may be changed

to larger bits to obtain more accurate results, such as 10-bit or 16-bit. Next, the charging algorithm can be improved by applying the Maximum Power Point Tracking algorithm (MPPT). Maximum Power Point Tracking (MPPT) is an algorithm to extract all the possible power from the solar panel, increasing the efficiency to charge the lead-acid battery. Lastly, another estimation method for the battery life cycle should be used and compared in the future to get better and more accurate results.

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APPENDICES

ANALOG DEVICES

3 V/5 V, 2 MSPS, 8-Bit, 1-/4-/8-Channel Sampling ADCs

AD7822/AD7825/AD7829

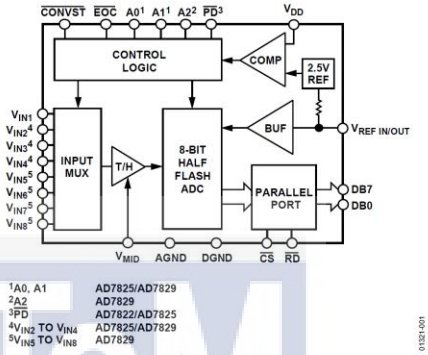
FEATURES

- 8-bit half-flash ADC with 420 ns conversion time
- One, four, and eight single-ended analog input channels
  - Available with input offset adjust
- On-chip track-and-hold
- SNR performance given for input frequencies up to 10 MHz
- On-chip reference (2.5 V)
- Automatic power-down at the end of conversion
- Wide operating supply range
  - 3 V ± 10% and 5 V ± 10%
- Input ranges
  - 0 V to 2 V p-p, V_{DD} = 3 V ± 10%
  - 0 V to 2.5 V p-p, V_{DD} = 5 V ± 10%
- Flexible parallel interface with $\overline{EOC}$ pulse to allow standalone operation

APPLICATIONS

- Data acquisition systems, DSP front ends
- Disk drives
- Mobile communication systems, subsampling applications

FUNCTIONAL BLOCK DIAGRAM



[1]A0, A1 AD7825/AD7829
[2]A2 AD7829
[3]PD AD7822/AD7825
[4]V_{IN2} TO V_{IN4} AD7825/AD7829
[5]V_{IN5} TO V_{IN8} AD7829

01321-001

Figure 1.

GENERAL DESCRIPTION

The AD7822/AD7825/AD7829 are high speed, 1-, 4-, and 8-channel, microprocessor-compatible, 8-bit analog-to-digital converters with a maximum throughput of 2 MSPS. The AD7822/AD7825/AD7829 contain an on-chip reference of 2.5 V (2% tolerance); a track-and-hold amplifier; a 420 ns, 8-bit half-flash ADC; and a high speed parallel interface. The converters can operate from a single 3 V ± 10% and 5 V ± 10% supply.

The AD7822/AD7825/AD7829 combine the convert start and power-down functions at one pin, that is, the $\overline{CONVST}$ pin. This allows a unique automatic power-down at the end of a conversion to be implemented. The logic level on the $\overline{CONVST}$ pin is sampled after the end of a conversion when an $\overline{EOC}$ (end of conversion) signal goes high. If it is logic low at that point, the ADC is powered down. The AD7822 and AD7825 also have a separate power-down pin (see the Operating Modes section).

The parallel interface is designed to allow easy interfacing to microprocessors and DSPs. Using only address decoding logic, the parts are easily mapped into the microprocessor address space. The $\overline{EOC}$ pulse allows the ADCs to be used in a stand-alone manner (see the Parallel Interface section.)

The AD7822 and AD7825 are available in 20-lead and 24-lead, 0.3" wide, plastic dual in-line packages (PDIP); 20-lead and 24-lead standard small outline packages (SOIC); and 20-lead and 24-lead thin shrink small outline packages (TSSOP). The AD7829 is available in a 28-lead, 0.6" wide PDIP; a 28-lead SOIC; and a 28-lead TSSOP.

PRODUCT HIGHLIGHTS

1. Fast Conversion Time. The AD7822/AD7825/AD7829 have a conversion time of 420 ns. Faster conversion times maximize the DSP processing time in a real-time system.
2. Analog Input Span Adjustment. The V_{MID} pin allows the user to offset the input span. This feature can reduce the requirements of single-supply op amps and take into account any system offsets.
3. FPBW (Full Power Bandwidth) of Track-and-Hold. The track-and-hold amplifier has an excellent high frequency performance. The AD7822/AD7825/AD7829 are capable of converting full-scale input signals up to a frequency of 10 MHz. This makes the parts ideally suited to subsampling applications.
4. Channel Selection. Channel selection is made without the necessity of writing to the part.

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 www.analog.com
Fax: 781.461.3113

TIMING CHARACTERISTICS

$V_{REF\ IN/OUT}$ = 2.5 V. All specifications −40°C to +85°C, unless otherwise noted.

Table 2.

Parameter[1, 2]	5 V ± 10%	3 V ± 10%	Unit	Conditions/Comments
t_1	420	420	ns max	Conversion time
t_2	20	20	ns min	Minimum $\overline{CONVST}$ pulse width
t_3	30	30	ns min	Minimum time between the rising edge of $\overline{RD}$ and the next falling edge of convert star
t_4	110	110	ns max	$\overline{EOC}$ pulse width
	70	70	ns min	
t_5	10	10	ns max	$\overline{RD}$ rising edge to $\overline{EOC}$ pulse high
t_6	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ setup time
t_7	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ hold time
t_8	30	30	ns min	Minimum $\overline{RD}$ pulse width
t_9[3]	10	20	ns max	Data access time after $\overline{RD}$ low
t_{10}[4]	5	5	ns min	Bus relinquish time after $\overline{RD}$ high
	20	20	ns max	
t_{11}	10	10	ns min	Address setup time before falling edge of $\overline{RD}$
t_{12}	15	15	ns min	Address hold time after falling edge of $\overline{RD}$
t_{13}	200	200	ns min	Minimum time between new channel selection and convert start
$t_{POWER\ UP}$	25	25	µs typ	Power-up time from rising edge of $\overline{CONVST}$ using on-chip reference
$t_{POWER\ UP}$	1	1	µs max	Power-up time from rising edge of $\overline{CONVST}$ using external 2.5 V reference

[1] Sample tested to ensure compliance.
[2] See Figure 24, Figure 25, and Figure 26.
[3] Measured with the load circuit of Figure 2 and defined as the time required for an output to cross 0.8 V or 2.4 V with V_{DD} = 5 V ± 10%, and time required for an output to cross 0.4 V or 2.0 V with V_{DD} = 3 V ± 10%.
[4] Derived from the measured time taken by the data outputs to change 0.5 V when loaded with the circuit of Figure 2. The measured number is then extrapolated back to remove the effects of charging or discharging the 50 pF capacitor. This means that the time, t_{10}, quoted in the timing characteristics is the true bus relinquish time of the part and, as such, is independent of external bus loading capacitances.

TIMING DIAGRAM

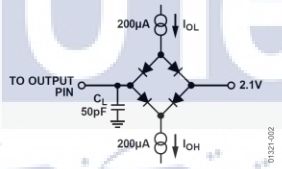


Figure 2. Load Circuit for Access Time and Bus Relinquish Time

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

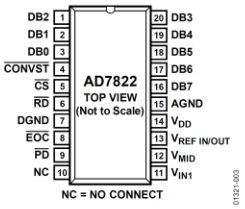


Figure 3. Pin Configuration

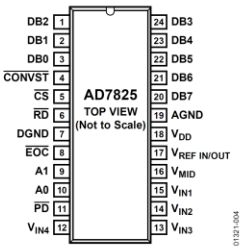


Figure 4. Pin Configuration

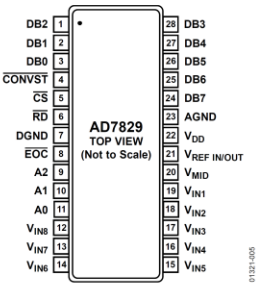


Figure 5. Pin Configuration

Table 4. Pin Function Descriptions

Mnemonic	Description
V_{IN1} to V_{IN8}	Analog Input Channels. The AD7822 has a single input channel; the AD7825 and AD7829 have four and eight analog input channels, respectively. The inputs have an input span of 2.5 V and 2 V depending on the supply voltage (V_{DD}). This span can be centered anywhere in the range AGND to V_{DD} using the V_{MID} pin. The default input range (V_{MID} unconnected) is AGND to 2 V (V_{DD} = 3 V ± 10%) or AGND to 2.5 V (V_{DD} = 5 V ± 10%). See the Analog Input section of the data sheet for more information.
V_{DD}	Positive Supply Voltage, 3 V ± 10% and 5 V ± 10%.
AGND	Analog Ground. Ground reference for track-and-hold, comparators, reference circuit, and multiplexer.
DGND	Digital Ground. Ground reference for digital circuitry.
$\overline{CONVST}$	Logic Input Signal. The convert start signal initiates an 8-bit analog-to-digital conversion on the falling edge of this signal. The falling edge of this signal places the track-and-hold in hold mode. The track-and-hold goes into track mode again 120 ns after the start of a conversion. The state of the $\overline{CONVST}$ signal is checked at the end of a conversion. If it is logic low, the AD7822/AD7825/AD7829 powers down (see the Operating Modes section of the data sheet).
$\overline{EOC}$	Logic Output. The end-of-conversion signal indicates when a conversion has finished. The signal can be used to interrupt a microcontroller when a conversion has finished or latch data into a gate array (see the Parallel Interface section).
$\overline{CS}$	Logic Input Signal. The chip select signal is used to enable the parallel port of the AD7822/AD7825/AD7829. This is necessary if the ADC is sharing a common data bus with another device.
$\overline{PD}$	Logic Input. The power-down pin is present on the AD7822 and AD7825 only. Bringing the $\overline{PD}$ pin low places the AD7822 and AD7825 in power-down mode. The ADCs power up when $\overline{PD}$ is brought logic high again.
$\overline{RD}$	Logic Input Signal. The read signal is used to take the output buffers out of their high impedance state and drive data onto the data bus. The signal is internally gated with the $\overline{CS}$ signal. Both $\overline{RD}$ and $\overline{CS}$ must be logic low to enable the data bus.
A0 to A2	Channel Address Inputs. The address of the next multiplexer channel must be present on these inputs when the $\overline{RD}$ signal goes low.
DB0 to DB7	Data Output Lines. They are normally held in a high impedance state. Data is driven onto the data bus when both $\overline{RD}$ and $\overline{CS}$ go active low.
$V_{REF\ IN/OUT}$	Analog Input and Output. An external reference can be connected to the AD7822/AD7825/AD7829 at this pin. The on-chip reference is also available at this pin. When using the internal reference, this pin can be left unconnected or, in some cases, it can be decoupled to AGND with a 0.1 µF capacitor.
V_{MID}	The V_{MID} pin, if connected, is used to center the analog input span anywhere in the range of AGND to V_{DD} (see the Analog Input section).

CIRCUIT INFORMATION

CIRCUIT DESCRIPTION

The AD7822/AD7825/AD7829 consist of a track-and-hold amplifier followed by a half-flash analog-to-digital converter. These devices use a half-flash conversion technique where one 4-bit flash ADC is used to achieve an 8-bit result. The 4-bit flash ADC contains a sampling capacitor followed by 15 comparators that compare the unknown input to a reference ladder to achieve a 4-bit result. This first flash (that is, coarse conversion) provides the four MSBs. For a full 8-bit reading to be realized, a second flash (that is, fine conversion) must be performed to provide the four LSBs. The 8-bit word is then placed on the data output bus.

Figure 6 and Figure 7 show simplified schematics of the ADC. When the ADC starts a conversion, the track-and-hold goes into hold mode and holds the analog input for 120 ns. This is the acquisition phase, as shown in Figure 6, when Switch 2 is in Position A. At the point when the track-and-hold returns to its track mode, this signal is sampled by the sampling capacitor, as Switch 2 moves into Position B. The first flash occurs at this instant and is then followed by the second flash. Typically, the first flash is complete after 100 ns, that is, at 220 ns; and the end of the second flash and, hence, the 8-bit conversion result is available at 330 ns (minimum). The maximum conversion time is 420 ns. As shown in Figure 8, the track-and-hold returns to track mode after 120 ns and starts the next acquisition before the end of the current conversion. Figure 10 shows the ADC transfer function.

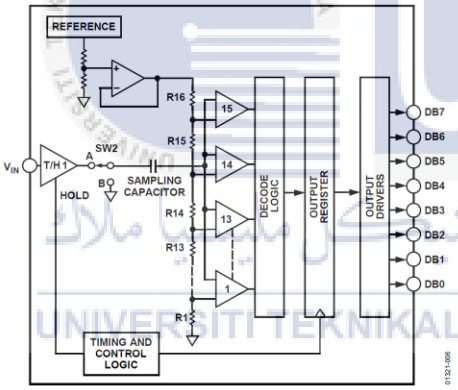


Figure 6. ADC Acquisition Phase

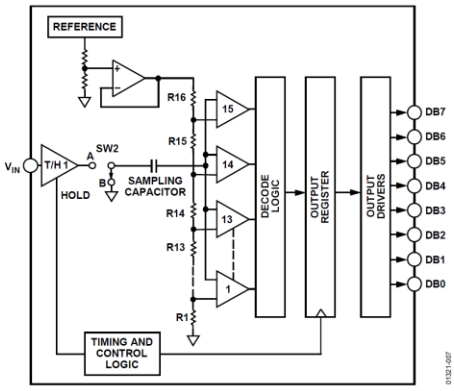


Figure 7. ADC Conversion Phase

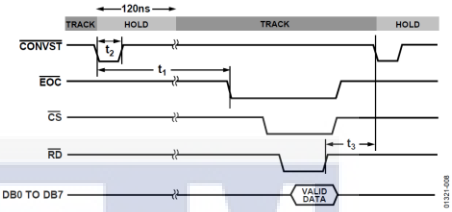


Figure 8. Track-and-Hold Timing

TYPICAL CONNECTION DIAGRAM

Figure 9 shows a typical connection diagram for the AD7822/AD7825/AD7829. The AGND and DGND are connected together at the device for good noise suppression. The parallel interface is implemented using an 8-bit data bus. The end of conversion signal ($\overline{EOC}$) idles high, the falling edge of $\overline{CONVST}$ initiates a conversion, and at the end of conversion the falling edge of $\overline{EOC}$ is used to initiate an interrupt service routine (ISR) on a microprocessor (see the Parallel Interface section for more details.) V_{REF} and V_{MID} are connected to a voltage source such as the AD780, and V_{DD} is connected to a voltage source that can vary from 4.5 V to 5.5 V (see Table 5 in the Analog Input section). When V_{DD} is first connected, the AD7822/AD7825/AD7829 power up in a low current mode, that is, power-down mode, with the default logic level on the $\overline{EOC}$ pin on the AD7822 and AD7825 equal to a low. Ensure the $\overline{CONVST}$ line is not floating when V_{DD} is applied, because this can put the AD7822/AD7825/AD7829 into an unknown state.

NCE N-Channel Enhancement Mode Power MOSFET

Description

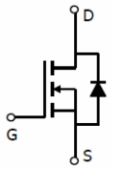
The NCE6008AS uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

General Features

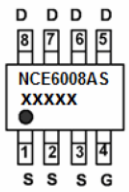
- V_{DS} = 60V,I_D =8A
  $R_{DS(ON)}$ < 20mΩ @ V_{GS}=10V (Typ:15.6mΩ)
  $R_{DS(ON)}$ < 28mΩ @ V_{GS}=4.5V (Typ:20mΩ)
- High density cell design for ultra low Rdson
- Fully characterized avalanche voltage and current
- Low gate to drain charge to reduce switching losses

Application

- Power switching application
- Load switch



Schematic diagram



Marking and pin assignment

SOP-8 top view

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
NCE6008AS	NCE6008AS	SOP-8	-	-	-

Absolute Maximum Ratings (T_C=25℃unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	60	V
Gate-Source Voltage	V_{GS}	±20	V
Drain Current-Continuous	I_D	8	A
Drain Current-Continuous(T_C=100℃)	I_D (100℃)	5.6	A
Pulsed Drain Current	I_{DM}	32	A
Maximum Power Dissipation	P_D	2.1	W
Operating Junction and Storage Temperature Range	T_J,T_{STG}	-55 To 150	℃

Thermal Characteristic

Thermal Resistance,Junction-to-Ambient (Note 2)	$R_{\theta JA}$	60	℃/W

Electrical Characteristics (TC=25℃unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D=250μA	60		-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=60V,V_{GS}=0V	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250μA	1.0	1.6	2.2	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=8A	-	15.6	20	mΩ
		V_{GS}=4.5V, I_D=8A	-	20	28	mΩ
Forward Transconductance	g_{FS}	V_{DS}=5V,I_D=8A	18	-	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C_{lss}	V_{DS}=30V,V_{GS}=0V, F=1.0MHz	-	1600	-	PF
Output Capacitance	C_{oss}		-	112	-	PF
Reverse Transfer Capacitance	C_{rss}		-	98	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=30V, R_L=1Ω V_{GS}=10V,R_{GEN}=3Ω	-	7	-	nS
Turn-on Rise Time	t_r		-	5.5	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	29	-	nS
Turn-Off Fall Time	t_f		-	4.5	-	nS
Total Gate Charge	Q_g	V_{DS}=30V,I_D=8A, V_{GS}=10V	-	38.5	-	nC
Gate-Source Charge	Q_{gs}		-	4.7	-	nC
Gate-Drain Charge	Q_{gd}		-	10.3	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V_{SD}	V_{GS}=0V,I_S=8A	-	-	1.2	V
Diode Forward Current (Note 2)	I_S	-	-	-	8	A
Reverse Recovery Time	t_{rr}	TJ = 25°C, IF =8A di/dt = 100A/μs (Note3)	-	28	-	nS
Reverse Recovery Charge	Qrr		-	40	-	nC

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production

LM25101 3-A, 2-A, and 1-A 80-V Half-Bridge Gate Drivers

1 Features

- Independent High and Low Driver Logic Inputs
- Bootstrap Supply Voltage up to 100-V DC
- Drives Both a High-Side and Low-Side N-Channel MOSFETs
- Fast Propagation Times (25 ns Typical)
- Drives 1000-pF Load With 8-ns Rise and Fall Times
- Excellent Propagation Delay Matching (3 ns Typical)
- Supply Rail Undervoltage Lockout
- Low Power Consumption
- Pin Compatible With HIP2100 and HIP2101

2 Applications

- Motor-Controlled Drivers
- Half and Full Bridge Power Converters
- Synchronous Buck Converters
- Two Switch Forward Power Converters
- Forward With Active Clamp Converters
- 48-V Server Power
- Solar DC-DC and DC-AC Converters

3 Description

The LM25101 high-voltage gate driver is designed to drive both the high-side and the low-side N-Channel MOSFETs in a synchronous buck or a half-bridge configuration. The A version provides a full 3-A of gate drive while the B and C versions provide 2-A and 1-A, respectively. The outputs are independently controlled with TTL input thresholds. An integrated high voltage diode is provided to charge the high-side gate drive bootstrap capacitor. A robust level shifter operates at high speed while consuming low power and providing clean level transitions from the control logic to the high-side gate driver. Undervoltage lockout is provided on both the low-side and the high-side power rails.

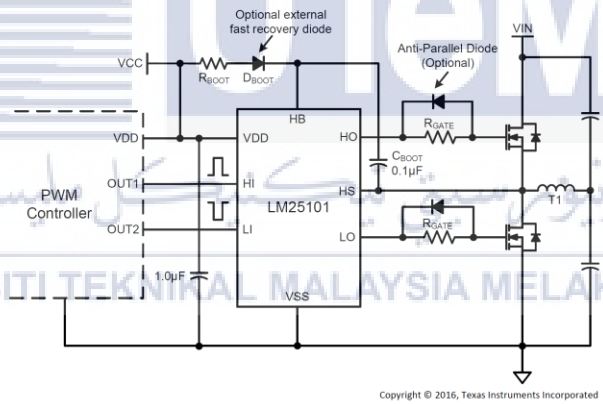
These devices are available in the standard 8-pin SOIC, 8-pin SO-PowerPAD, 8-pin WSON, 10-pin WSON, and 8-pin MSOP PowerPAD packages.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM25101	MSOP PowerPAD (8)	3 mm × 3 mm
	WSON (8)	4 mm × 4 mm
	WSON (10)	4 mm × 4 mm
	SO PowerPAD (8)	3.9 mm × 4.89 mm
	SOIC (8)	3.91 mm × 4.9 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Application Diagram



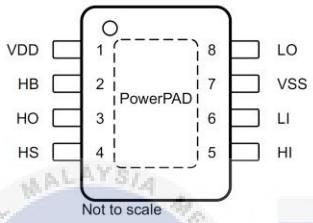
5 Device Options

Table 1. Input/Output Options

Part Number	Input Thresholds	Peak Output Current
LM25101A	TTL	3 A
LM25101B	TTL	2 A
LM25101C	TTL	1 A

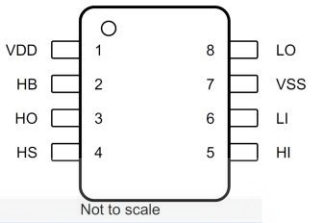
6 Pin Configuration and Functions

DGN and DDA Packages
8-Pin MSOP and SO PowerPAD
Top View



Not to scale

D Package
8-Pin SOIC
Top View



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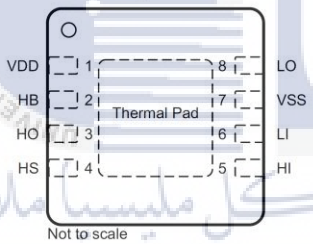
NGT Package
8-Pin WSON
Top View



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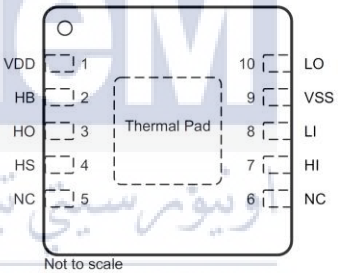
DPR Package
10-Pin WSON
Top View



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Powered by

BATTERY®

GP 1272 ▶ 12V 7.2Ah

GP 1272 is a general purpose battery up to 5 years in standby service or more than 260 cycles at 100% discharge in cycle service. As with all CSB batteries, all are rechargeable, highly efficient, leak proof and maintenance free.

▶ Specification

Cells Per Unit	6
Voltage Per Unit	12
Capacity	7.2Ah @ 20hr-rate to 1.75V per cell @25℃(77℉)
Weight	Approx. 2.4 kg(5.29 lbs)
Maximum Discharge Current	100A/130A(5sec)
Internal Resistance	Approx. 23 mΩ
Operating Temperature Range	Discharge: -15℃~50℃(5℉~122℉) Charge: -15 ℃~40℃(5℉~104℉) Storage: -15℃~40℃(5℉~104℉)
Nominal Operating Temperature Range	25℃±3℃(77℉±5℉)
Float Charging Voltage	13.5 to 13.8 VDC/unit Average at 25℃(77℉)
Recommended Maximum Charging Current Limit	2.16A
Equalization and Cycle Service	14.4 to 15.0 VDC/unit Average at 25℃(77℉)
Self Discharge	CSB Batteries can be stored for more than 6 months at 25℃(77℉). Please charge batteries before using. For higher temperatures the time interval will be shorter.
Terminal	F1/F2-Faston Tab187/250
Container Material	ABS(UL 94-HB/File E50263)*Flammability resistance of (UL 94-V0/File E88637) can be available upon request.

MH14533(N)

TÜV CERT ISO9001 No :041005117

RWTUV ISO 14001 NO.UM 1-12-0045

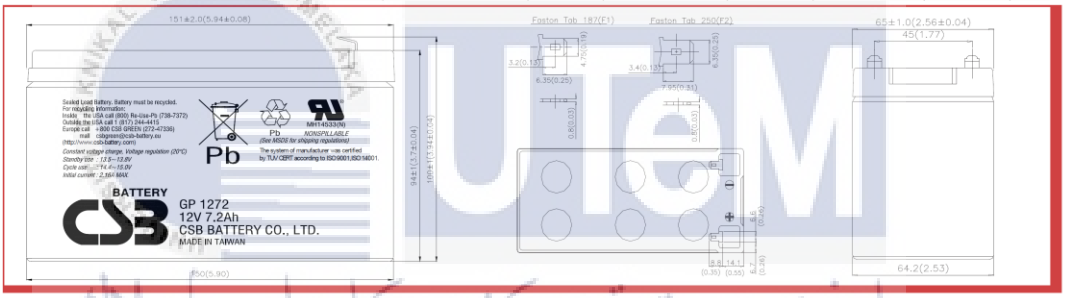
CSB-manufactured VRLA batteries are UL-recognized components under UL924 and UL1989.

CSB is also certified by ISO 9001 and ISO 14001.

▶ Dimensions :

Unit: mm (inch)

Overall Height (H)	Container height (h)	Length (L)	Width (W)
100±1 (3.94±0.04)	94±1 (3.7±0.04)	151±2 (5.94±0.08)	65±1 (2.56±0.04)



Constant Current Discharge Characteristics Unit:A (25℃,77℉)

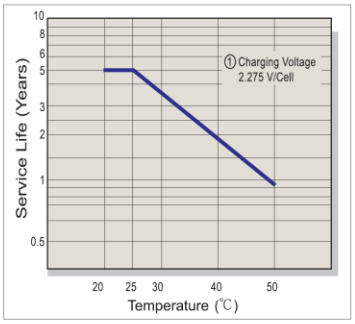
F.V/Time	5MIN	10MIN	15MIN	30MIN	1HR	2HR	3HR	4HR	5HR	8HR	10HR	20HR
1.60V	35.6	22.0	16.5	9.61	5.51	3.08	2.14	1.65	1.35	0.925	0.778	0.456
1.67V	33.1	21.0	15.9	9.36	5.42	3.03	2.09	1.60	1.32	0.906	0.762	0.447
1.70V	31.9	20.5	15.6	9.24	5.37	3.00	2.06	1.58	1.30	0.897	0.756	0.438
1.75V	29.6	19.6	15.1	9.03	5.30	2.96	2.02	1.54	1.28	0.883	0.742	0.428
1.80V	27.2	18.6	14.4	8.77	5.23	2.92	1.99	1.50	1.25	0.871	0.732	0.421
1.85V	24.5	17.4	13.7	8.45	5.14	2.87	1.96	1.48	1.23	0.861	0.720	0.409

Constant Power Discharge Characteristics Unit:W (25℃,77℉)

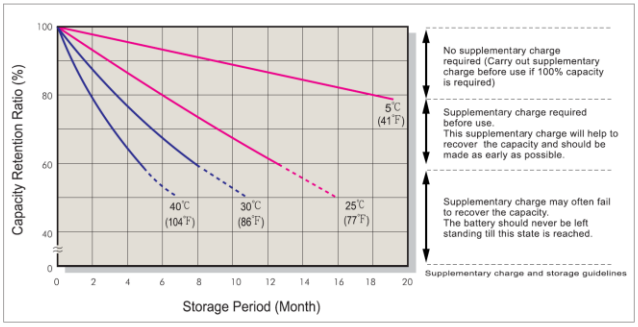
F.V/Time	5MIN	10MIN	15MIN	30MIN	1HR	2HR	3HR	4HR	5HR	8HR	10HR	20HR
1.60V	360	245	183	108	64.4	37.7	26.6	20.8	17.3	11.8	9.80	5.37
1.67V	340	235	177	106	63.6	37.1	26.3	20.5	17.0	11.6	9.69	5.27
1.70V	331	231	174	105	63.1	36.9	26.2	20.4	16.9	11.5	9.54	5.23
1.75V	313	222	170	103	62.4	36.4	25.9	20.2	16.7	11.4	9.48	5.15
1.80V	295	213	165	101	61.7	35.9	25.6	19.9	16.5	11.3	9.40	5.07
1.85V	276	202	158	99.0	60.8	35.4	25.2	19.6	16.3	11.2	9.29	4.99

GP1272 12V 7.2Ah

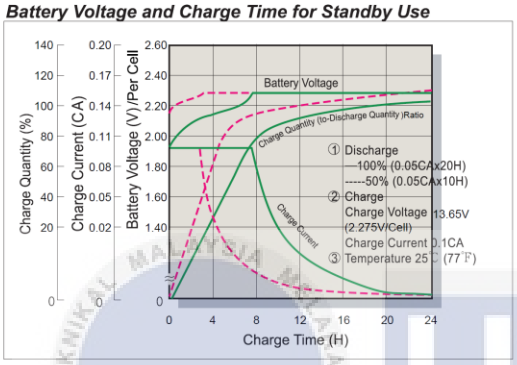
Trickle (or Float) Service Life



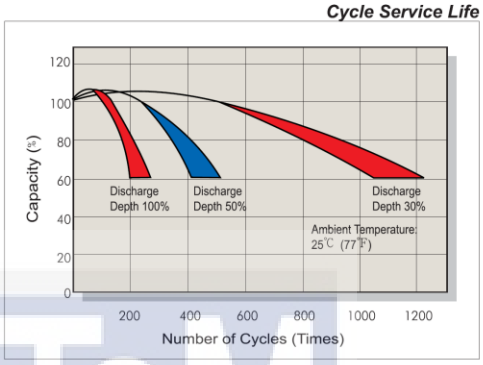
Capacity Retention Characteristic



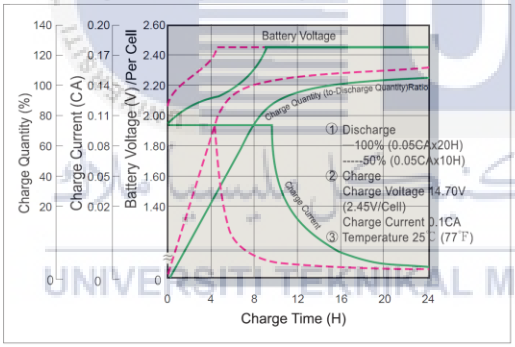
Battery Voltage and Charge Time for Standby Use



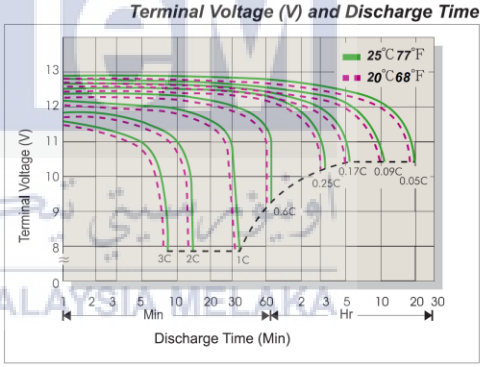
Cycle Service Life



Battery Voltage and Charge Time for Cycle Use



Terminal Voltage (V) and Discharge Time



Charging Procedures

Application	Charge Voltage(V/Cell)			Max.Charge Current
	Temperature	Set Point	Allowable Range	
Cycle Use	25℃(77℉)	2.45	2.40~2.50	0.3C
Standby	25℃(77℉)	2.275	2.25~2.30	

Discharge Current VS. Discharge Voltage

Final Discharge Voltage V/Cell	1.75	1.70	1.60	1.30
Discharge Current(A)	0.2C>(A)	0.2C<(A)<0.5C	0.5C<(A)<1.0C	(A)>1.0C

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