POWER SAVING ANALOG RESERVOIR COMPUTING SYSTEM DESIGN

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This report is submitted in partial fulfilment of the requirements for the degree of Bachelor of Electronic Engineering with Honours

Faculty of Electronic and Computer Engineering
Universiti Teknikal Malaysia Melaka

2021

DECLARATION

I declare that this report entitled “Power Saving Analog reservoir Computing System Design” is the result of my own work except for quotes as cited in the references.

Signature :

Author: CHEW YEE YUEN

Date : 23 June 2021

APPROVAL

I hereby declare that I have read this thesis and in my opinion this thesis is sufficient in terms of scope and quality for the award of Bachelor of Electronic Engineering with Honours.

Signature : .....

Supervisor Name : PM Dr. Wong Yan Chiew

Date : 24 Jun 2021

DEDICATION

A particular thank you to my loving family, friends, lecturers, and supervisor, who have always supported and guided me in successfully completing my final year project.

ABSTRACT

The aim of this project is to design an Analog power saving Spike-Based Delayed Feedback Reservoir Computing System and analyse its performance. The developed system can make the integrated circuit (IC) achieves power saving so that can solve the problem excessive power consumption of supercomputer with good performance. The rate of augmentation is starting to slow down due to the underlying performance limits of the chips, indicating the end of Moore's prediction. Moore's prediction is coming to an end as things are starting to slow down. The urge to get through the barrier has led researchers down a few paths, including innovative computing architectures. Over the last few years, reservoir computing has evolved as a revolutionary notion in the field of machine learning. To process temporal data, reservoir computing combines the memory and Spatio-temporal processing capabilities of recurrent neural networks. In this work, a new class of computationally efficient spike timing-dependent encoders and delay-based reservoirs within reservoir networks has been proposed. Silterra 130nm technology is used to develop the reservoir computing system. The proposed method eliminates the need for power-hungry analog-to-digital converters (ADCs) and operational amplifiers (Op-AMPs), resulting in lower power consumption and a smaller design footprint.

ABSTRAK

Objektif projek ini adalah untuk merancang 'Analog power saving Spike-Based Delayed Feedback Reservoir Computing System' dan menganalisis prestasinya. Sistem yang dibangunkan dapat menjadikan 'IC' mencapai penjimatan tenaga sehingga dapat menyelesaikan masalah penggunaan tenaga superkomputer dengan prestasi yang baik. Kadar peningkatan mulai perlahan kerana had prestasi yang mendasari kerepek, yang menunjukkan berakhirnya 'Moore's prediction'. Dorongan untuk mengatasi halangan telah menyebabkan para penyelidik melalui beberapa jalan, termasuk 'Computer Architectures' yang inovatif. Sejak beberapa tahun kebelakangan ini, 'Reservoir Computing' telah berkembang sebagai gagasan revolusioner dalam bidang 'Machine Learning'. Untuk memproses data temporal, 'Reservoir Computing' menggabungkan memori dan keupayaan pemprosesan Spatio-temporal rangkaian saraf berulang. Teknologi Silterra 130nm digunakan untuk membuat kelas baru pengkod yang bergantung pada masa lonjakan komputasi dan takungan berdasarkan kelewatan dalam rangkaian takungan. Kaedah baru menghilangkan keperluan untuk penukar analog-ke-digital (ADCs) dan penguat operasi (Op-AMP) yang haus kuasa, yang mengakibatkan penggunaan kuasa yang lebih rendah dan reka bentuk yang lebih kecil.

ACKNOWLEDGEMENTS

I would like to appreciate to Silterra track give me a chance to use the transistors in Cadence Virtuoso. In addition, I would want to express my gratitude to Professor Madya Dr. Wong Yan Chiew, my team supervisor, for her invaluable guidance, suggestions, and inspiration in giving me with all the information and knowledge concerning this project. Last but not least, a big thank you to all of my seniors who helped me finish my assignment.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

LIST OF SYMBOLS AND ABBREVIATIONS

For examples:

IC	:	Integrated Circuit
DFR	:	Delay Feedback Reservoir
OpAmp	:	Operation Amplifier
ADCs	:	Analog-to-Digital Converter
SNN	:	Spiking Neural Network
CLK	:	Clock
ECG	:	Electrocardiogram

CHAPTER 1

INTRODUCTION

Due to the inherent performance restrictions of the chips, the rate of augmentation is starting to saturate and slow down, indicating the end of Moore's prediction. Delayed feedback reservoir (DFR) computing is a new reservoir computing model that only uses one nonlinear neuron and a delay loop. It not only makes hardware implementation simple, but it also allows for excellent performance due to the inherent delay and rich intrinsic dynamics. Because power-hungry peripheral components such as Analog-to-Digital converters (ADCs) and operational amplifiers (Op-AMPs) are not included, Analog implementations would be more power efficient and take up less space. Project background, problem statement, objectives, scope of project and overview of the chapter is presented in this chapter.

1.1 Project Background

Moore's rule states that the number of transistors per silicon chip doubles every 18 months, as predicted by American engineer Gordon Moore in 1965 [1]. However, due to the underlying performance restrictions of the chips, the pace of increase is starting to saturate and slow down, indicating the end of Moore's prediction. The desire to tear down boundaries has pushed researchers in a variety of areas, including the development of innovative computing architectures. Reservoir computing is a new notion in the field of machine learning that has emerged in recent years. Reservoir computing is a technique for speeding up machine learning algorithms [2]. A dynamical system is referred to as a reservoir. A mathematical function that represents how a point in space behaves with time is referred to as a dynamical system. Knowing how these systems work can help you forecast where that point in space will be in the future. This reservoir is made up of a collection of randomly connected recurrently connected components.

1.2 Problem Statement

Due to the underlying performance restrictions of the chips, the rate of advancement is currently slowing, indicating that Moore's prediction has come to an end. Aside from that, a high-performance supercomputer necessitates a high level of power consumption. A supercomputer called "Tianhe-1A" consumes 4.04 megawatts (MW), which is enough to power almost 5000 homes for a year. Thus, this work will focus on design an analog power saving Spike-Based Delayed Feedback Reservoir Computing System and analyse the performance of the developed system.

1.3 Objective

Below are the two objectives that need to be achieved:

1. To identify the main circuit components and design parameters in Spike-Based Delayed Feedback Reservoir Computing System.
2. To analyse the power consumption of the developed system.

1.4 Scope of Project

The scope of the project will cover how to design a power saving analog reservoir computing system by using industry standard EDA software Cadence Virtuoso. There are included design schematic of circuit and analyse the performance so that is convenient to improve the performance as well.

1.5 Project Significant

The goal of this initiative is to reduce energy consumption. We can limit the number of hazardous fumes generated by power plants, save the earth's natural resources, and protect ecosystems from damage by consuming less energy. Many folks are unsure about how to save electricity. We live in a society where the issue of power has never been a major concern. We need to think beyond the box and recognize that nothing is certain. Aside from that, the completed project might be used as a starting point for additional research.

1.6 Thesis Outline

Chapter one is the introduction chapter for this project. This chapter will cover the terms, background, and brief explanation of this project. The problem statement based on case studies along with the objectives to achieve would also be highlighted in this chapter along with the scope of work for this project. In Chapter two, background study includes a detailed review of researched area. Past research and theory which included Moore's Law, Neural Network, reservoir computing, delay feedback reservoir (DFR), Spiking Neural Network (SNN), temporal neural encoder, electrocardiogram, analog vs digital neuron and benchmarking table. In Chapter 3, project methodology and flow chart design to implement the process is further discussed. Chapter 4 presented and discussed about the results obtained from the experiments. Lastly, recommendation for future work is summarized in Chapter 5.

CHAPTER 2

BACKGROUND STUDY

This chapter will discuss the theory and background of Moore's Law, Neural Network, reservoir computing, Delay Feedback Reservoir, Spiking Neural Network (SNN), Temporal Encoder, analog vs digital neuron and benchmarking table of some previous projects. To perform analysis of this project, various journal and research paper from previous research based on reservoir computing and Spiking Neural Network is studied and discussed in this chapter.

2.1 Moore's Law

Gordon Moore made a forecast in 1965 that set the tone for our current digital revolution. Moore extrapolated that computing will rapidly rise in power while decreasing relative cost at an exponential rate based on thorough observation of an emerging trend. Of course, Moore's law isn't the same as the laws governing gravity or energy conservation. As technology improves, it is predicted that the number of transistors (electrical switches in computers that represent 0s and 1s) that can fit on a silicon chip will double every 18 months. [1]

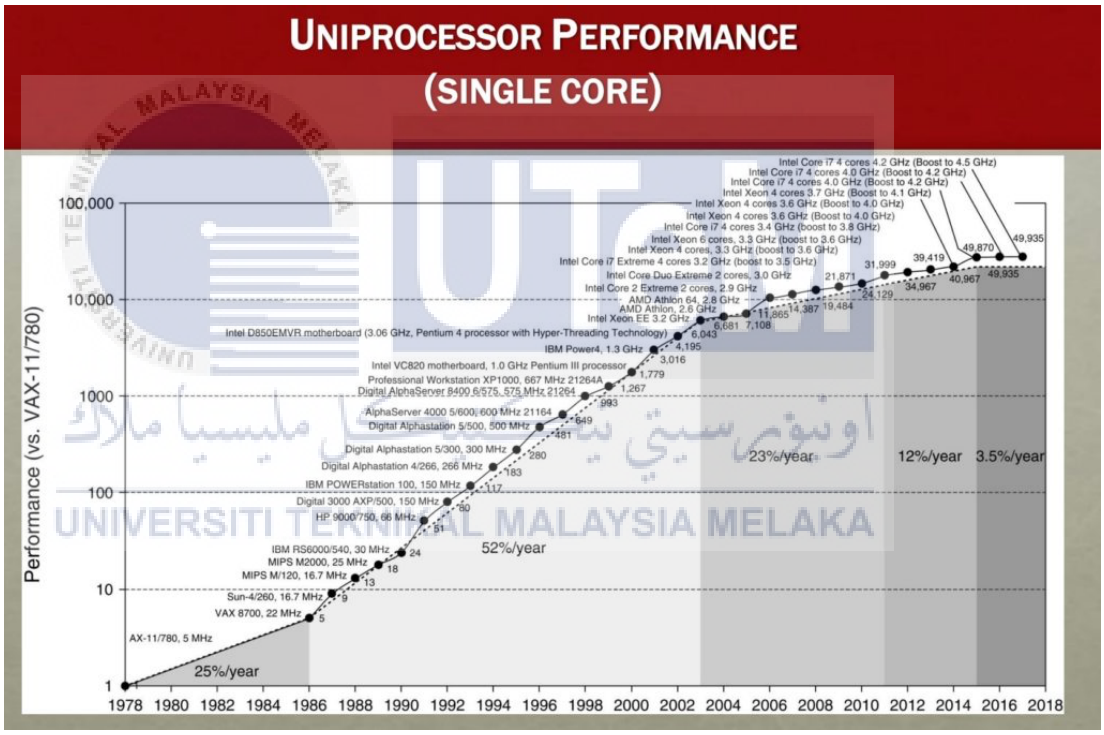

Figure 2.1.1: Uniprocessor Performance [3]

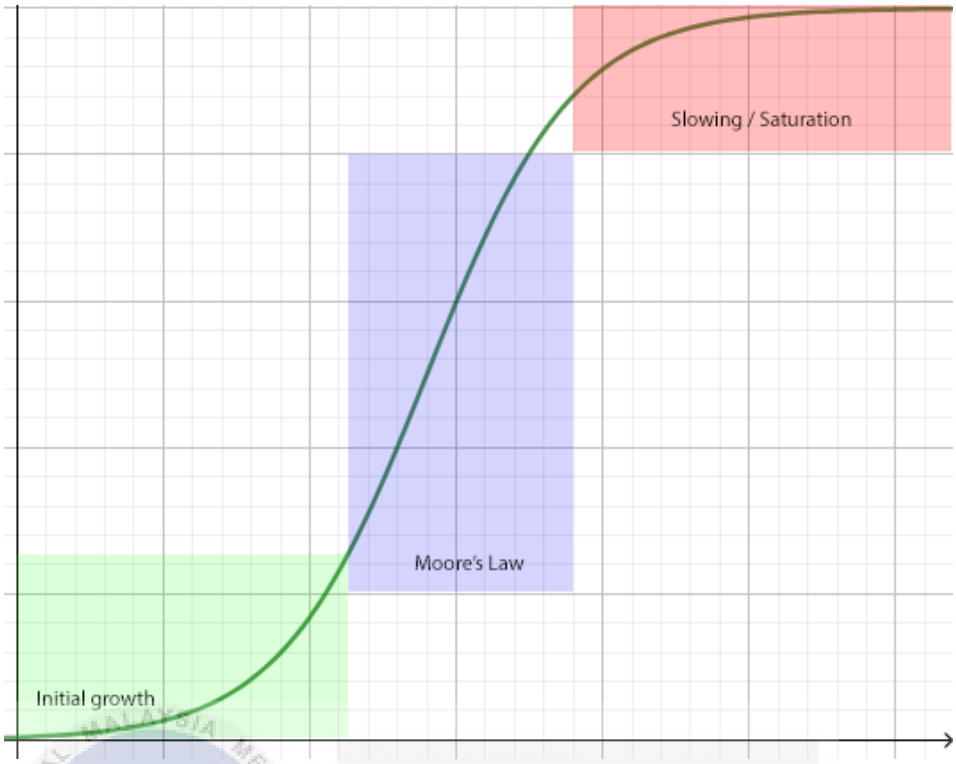

Figure 2.1.2: Moore's Law

As Figure 2.1.1 and Figure 2.1.2, due to the inherent performance limits of the chips, the rate of advancement is starting to saturate and slow down, indicating the end of Moore's prediction. Many technologists have predicted Moore's doubling's end throughout the years, and Moore himself has stated that exponential growth cannot last indefinitely.

2.2 Neural Network

Neural networks are a set of algorithms that imitate the functions of the human brain to recognize patterns in large volumes of data. It's a computer model with self-organization, learning, and decision-making capabilities based on the structure and functioning of biological brain networks. Because neural networks can adapt to changing input, the network delivers the best possible result without requiring the output criteria to be redesigned.

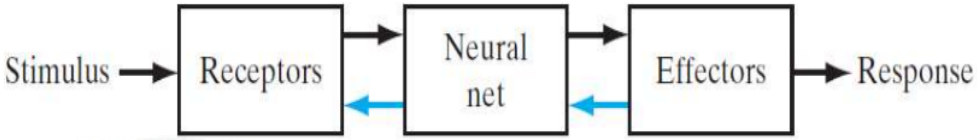

Figure 2.2.1: Biological neural network

As Figure 2.2.1, Biological neural network at the start, the receptors accept inputs from either within or outside the body. Electrical impulses are then sent to the neurons, carrying the information. The neural network then analyses the inputs before making an appropriate output decision. Finally, the effectors convert the brain network's electrical impulses into responses to the external environment. [4]

2.3 Reservoir Computing

Reservoir Computing is a recurrent (with loops, where the data persists or repeats in patters, hence recurrence) neural network that avoids the problems of Back-Propagation through time (BPTT) during training.

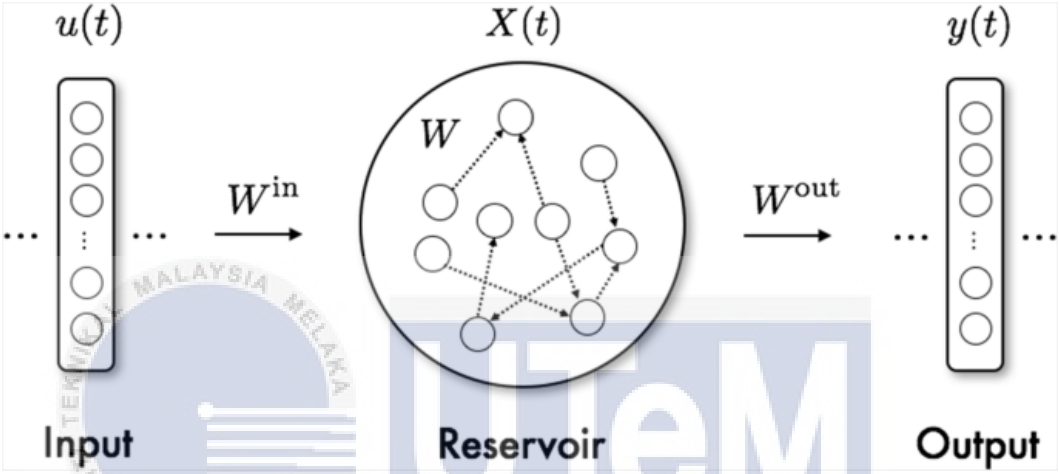

Figure 2.3.1: Reservoir computing architecture.

As Figure 2.3.1, the reservoir computer architecture is made up of three layers: input, reservoir, and output. The input signals are injected into the reservoir using synaptic weights that are created at random. Based on RNN models, the reservoir is made up of randomly connected nodes where nonlinear mapping takes place. Signals from the reservoir are fed into the output layer via output weights in the output layer. [5] Only the output weights are taught in reservoir computing, hence the computational cost of such a computing architecture is significantly lower than that of RNNs. [6]

2.4 Delayed Feedback Reservoir (DFR)

From the diffusion or transit of chemicals to the conduction time of nerves to intrinsic timeframes for synthesis, growth, and reproduction, delay is present in practically every system, especially biological ones. A single nonlinear node and a delay loop make up a delayed feedback reservoir, unlike a regular reservoir. DFR has a resemblance to human brains and is easy to implement on hardware because of the delay incorporated in the system. [7]

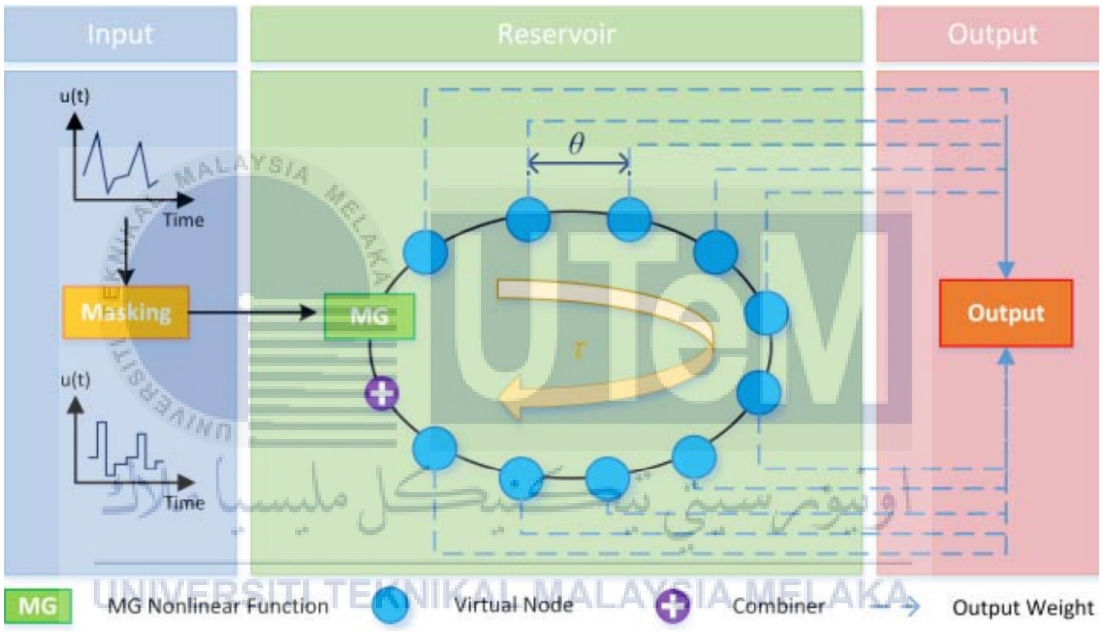

Figure 2.4.1: Scheme of delay-based reservoir computing.

As Figure 2.4.1, the input together with a masking scheme, will be injected straight into the nonlinear node, where the nonlinear mapping will take place. After that, output weights are used to obtain the output. The most frequent method of training is to use linear regression to minimize the mean square error.

2.5 Spiking Neural Network (SNN)

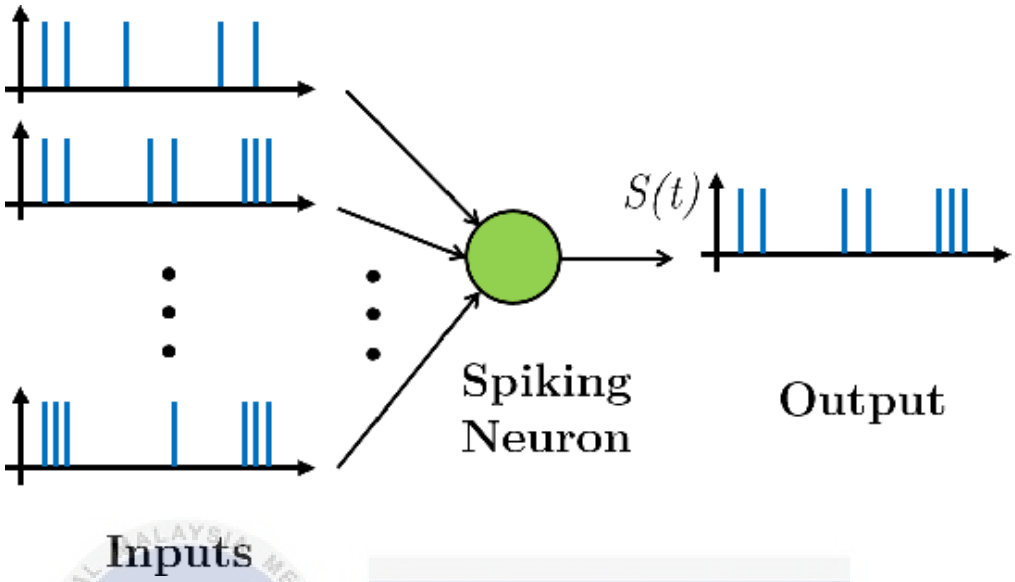

Figure 2.5.1: Spiking Neural Network

Spiking neural networks are the most widely used brain-inspired computer model in hardware neuromorphic computing. As an attempt to replicate the behavior of biological neurons, the spiking neural network (SNN) first arose in computational neuroscience. The leak-integration-launch (LIF) model explains neural activity as the integral of incoming spike voltage and weak dissipation (leakage) to the environment. When the neuron's voltage hits the threshold, it will spontaneously spike train.

Because rate coding is particularly resilient to noise, very weak signals can be used to convey information using the Spiking Neural Network. Second, they introduce novel unsupervised learning techniques. Spike neurons can, in fact, use biologically inspired local learning principles like Herbie learning and spike time-dependent plasticity (STDP) to implement biologically inspired local learning rules. [8]

2.6 Electrocardiogram (ECG) Signal

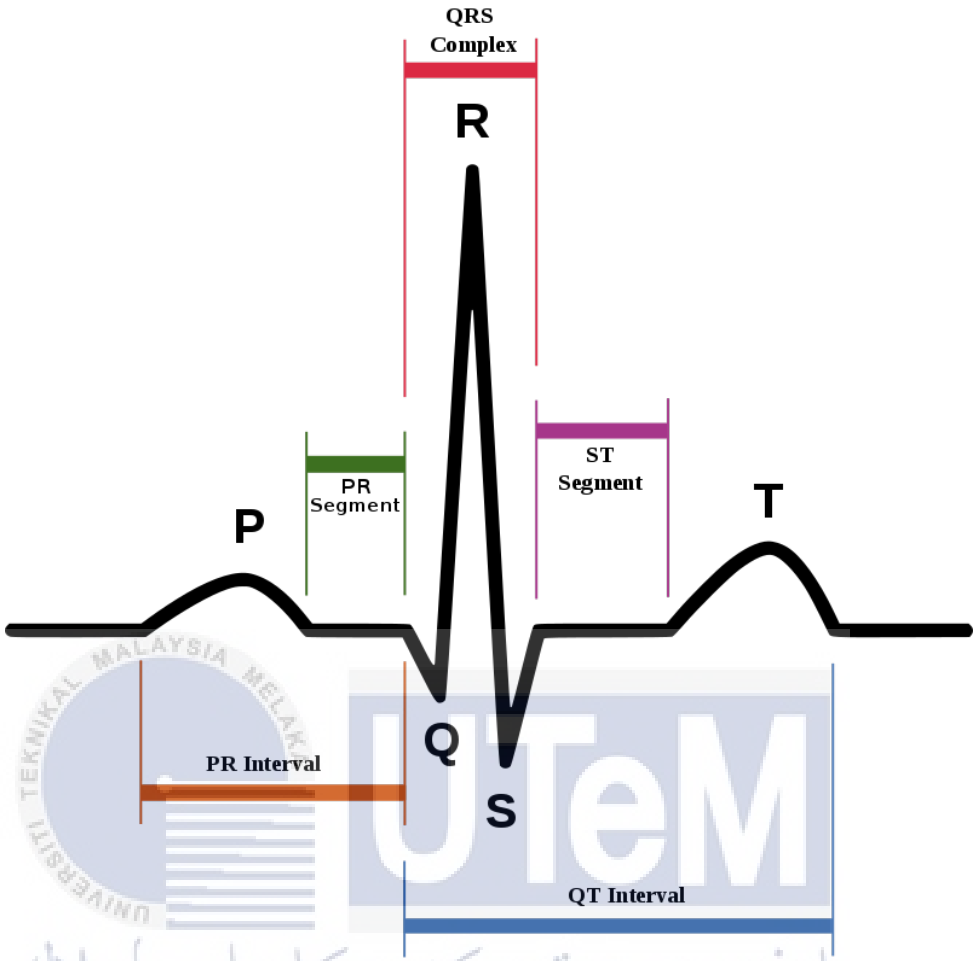

Figure 2.6.1: Electrocardiography

Electrocardiography is the process of producing an electrocardiogram (ECG). It is a graph that shows heart activity by recording electric potential changes between electrodes implanted on a patient's body. Heart rhythm and many cardiac disorders, such as inadequate blood flow to the heart and structural abnormalities, are tracked by an ECG signal. Electrical currents from the heart travel throughout the body thanks to the action potential formed by heart wall contractions. Different potentials are created by the spreading electrical currents at different places in the body, which can be felt by electrodes put on the skin. The electrodes are metal and salt-based biological transducers. In practice, ten electrodes are attached to various bodily parts.

2.7 Temporal Neuron Encoder

Trains of spiking events are fed into spiking neural networks (SNNs). Spike trains are a type of brain activity that can be visualized. Spike trains are obtained in neurophysiological research by detecting action potentials intracellularly or extracellularly but only maintaining the temporal instant at which they occur. Temporal neuron encoder is a combination circuit that can make the analog input convert to spike trains. Different types of input across the encoder will turn to spike train.

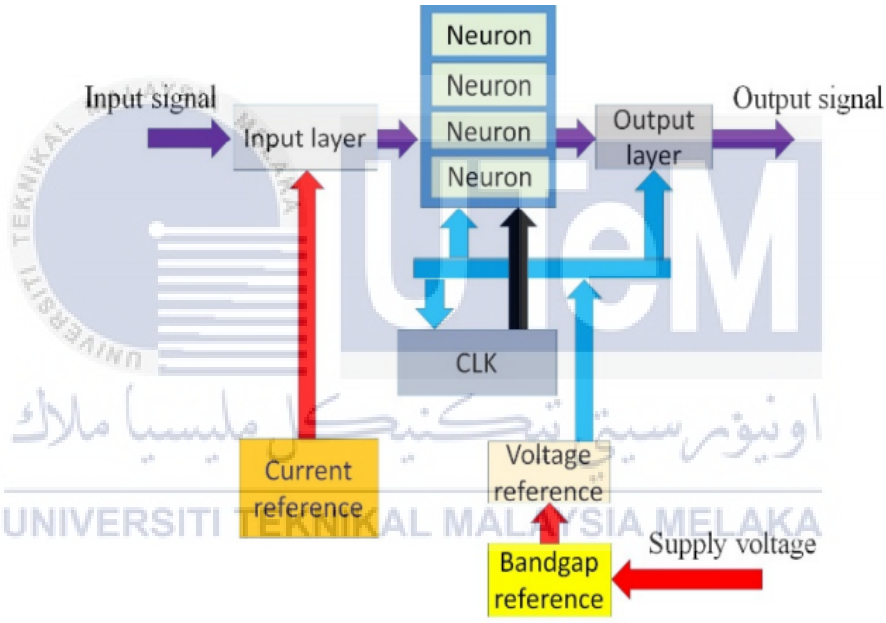

Figure 2.7.1: Structure of the Temporal Encoder

As shown in the Figure 2.7.1, This encoder contained eight units, which were classified into two categories. The input layer, neuron pool, and output layer made up the core temporal encoder. The signal generator, clock (CLK), voltage reference, current reference, and bandgap reference were all part of the function category. The proposed inter-spike intervals temporal encoder is a general encoding system that can be applied to a variety of applications.

The link between the number of neurons and the number of spikes can be represented as follows: $S^N = 2^{N-1}$. where N is the total number of neurons and S_N is the total number of spikes. Usually, the number of neurons and the number of spikes is usually proportionate.

2.8 Analog vs Digital Neuron

In general, there are two implementations available which are digital and analog. Since neurons are the basic components of neuromorphic systems, power consumption and grain size play an important role in neuron system design. The analog and digital implementations of neurons are compared using the LIF model.

	Analog	Digital
Power consumption (μW)	1.15 - 52	14.3 - 100
Die area (μm^2)	74.2	1119.7
Transistor number	19.5	225

Table 2.8.1: Normalized Analog and Digital Implementations [9]

Table 2.8.1 shows that an analog implementation requires lower power consumption, smaller die area, and less transistors when compared to a digital implementation.

The analog implementation provides greater flexibility for controlling the leakage current, thereby improving the accuracy of the model. Physical processes, such as the summing of currents or charges, conduct computationally complex calculations automatically in analog. Furthermore, the analog electronics are more compact and achieve high-speed operation with low energy consumption. However, the analog

implementation is more susceptible to noise and shows higher sensitivity to process variables, which makes the analog implementation more challenging in design.

2.9 Benchmarking Table

Project	**Power Consumption(W)**
ECG Simulator	4.00mW
Solar-Powered Portable ECG Device	3.99mW
A low-power and miniaturized electrocardiograph data collection system	29.74mW
Automatic analysis method for long-term ECG	1.86W

Table 2.9.1: Benchmarking Table

Table 2.9.1 shows the power consumption of previous works. The power consumption of this project can achieve more power saving compared to these pervious projects.

2.10 Summary of Background Study

This chapter can be summarized that I studied theory about Moore's Law is starting to slow down nowadays. Moreover, I also studied about what are Neural Network, Reservoir Computing, Delay Feedback Reservoir, Spiking Neural Network, Electrocardiogram and Temporal Neuron Encoder. Next, I studided about the better implementation between Analog and Digital Neuron, and the Benchmarking table of previous work.

CHAPTER 3

METHODOLOGY

In this section, the procedures and technique which are used in this project is explained discussed. After a lot of research is done, it is stated that Cadence Virtuoso is the most suitable EDA (Electronic Design Automation) software for doing this project. This is due to the fact that Cadence Virtuoso is a comprehensive, system-based solution that enables simulation and LVS-clean layout of ICs and packages from a single design.

3.1 Overall Project Methodology

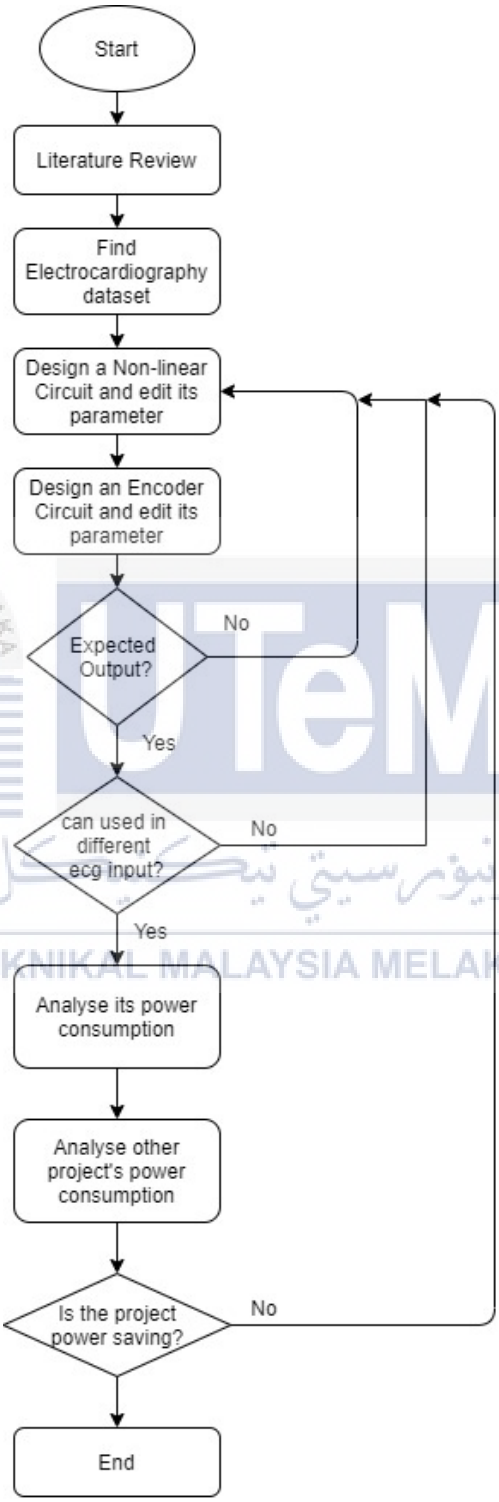

Figure 3.1.1: Flow Chart

Figure 3.1.1 shows that the flow chart of whole project. First at all, I studied a lot of literature reviews about Delay-Feedback Reservoir, Spiking Neural Network, temporal neuron encoder and others. Next, I found the ECG(Electrocardiogram) signal from website PhysioNet [10] as my analog input. Then, the schematic of non-linear circuit and encoder circuits were designed and put into cadence virtuoso. After that, the parameter of components was edited in keep try and error to get the expected output. After the output signal managed to convert to spike train according to the changes of the input, the other ECG signal inputs were tried to get the spike train out"put signal. Then, the power consumption using different ECG input signal were analysed. The other ECG device project's power consumption are recorded and compared to this work. The parameter of components will keep try and error until the power consumption of this project can prove that it is power saving.

3.2 PhysioNet

Figure 3.2.1: PhysioNet

The MIT Laboratory for Computational Physiology manages PhysioNet, a library of openly available medical research data. Since the website PhysioNet is free and trustworthy data, so the ECG dataset is getting from the PhysioNet.

3.3 Cadence Virtuoso

Figure 3.3.1: Cadence Logo

Cadence Design Systems is a US engineering and software company. The company is known for its electronic design automation (EDA) software, in addition to software, hardware and silicon structures for integrated circuits, printed circuit boards and systems on chips. This is due to the fact that Cadence Virtuoso is a comprehensive, system-based solution that enables simulation and LVS-clean layout of ICs and packages from a single design. Since the Cadence Virtuoso software is provided by FKEKK UTeM in MiNE Laboratory, the 'SoftEther VPN Client Manager' software is downloaded to connect the VPN of UTeM and 'Remote Desktop Connection' software is downloaded to control the PC of MiNE Lab. Since the cost of this project is almost free, so the Cadence Virtuoso is the best choice for doing this project.

3.4 Schematic Design

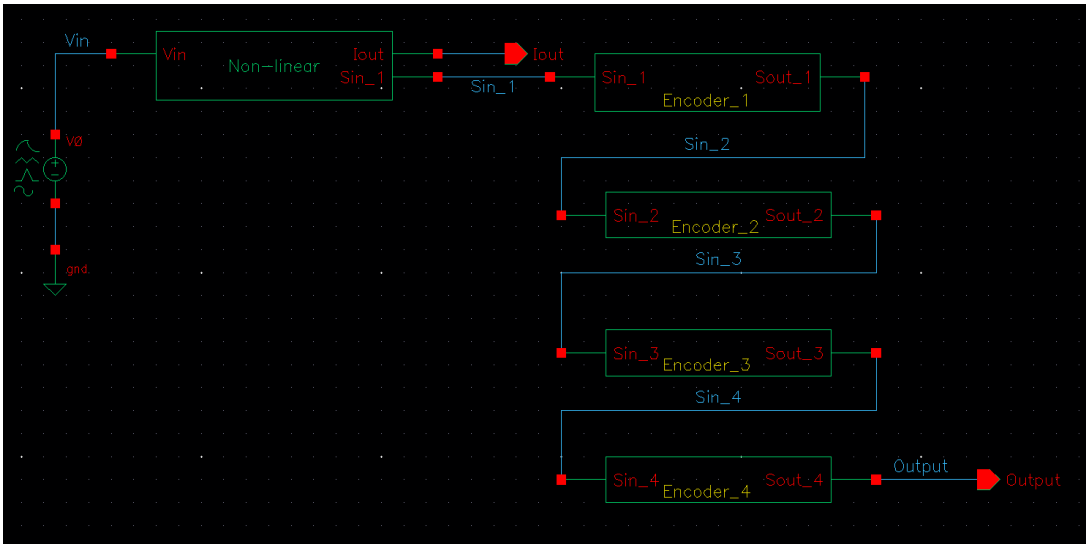

Figure 3.4.1: Schematic Design

Figure 3.4.1 shows the whole schematic in Cadence Virtuoso, the ECG dataset is put into the V0 as the input signal of the project. After that, the signal will across a non-linear transformation circuit and process an output voltage, VNT (Voltage Non-linear Transformation). Then the VNT across a buffer and process a signal input (Sin) of first encoder circuit (Encoder_1).

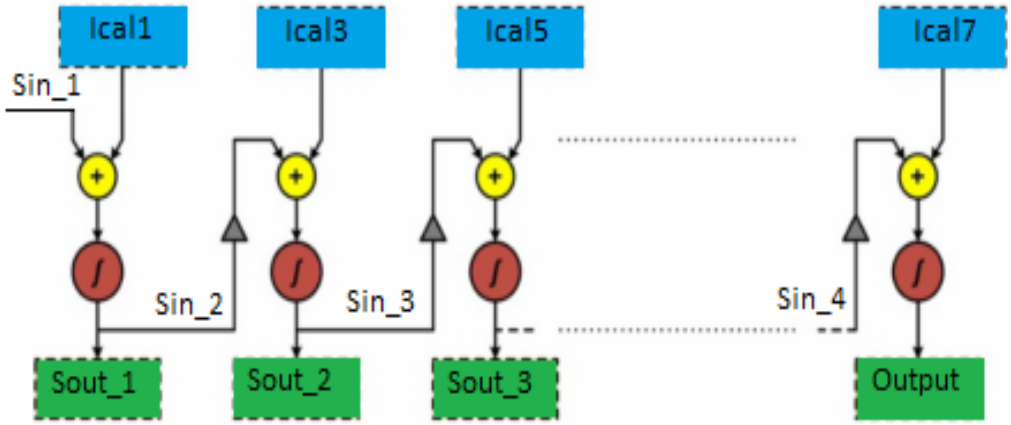

Figure 3.4.2: Encoders

As Figure 3.4.2, the signal will across the encoder circuit and process an output spike train signal. The output signal of Encoder_1 (Sout_1) will become the input signal of the second encoder circuit (Sin_2). Then, The Sin_2 will across the second, third and fourth encoder circuits (Encoder_2, 3 & 4) and process a spike train.

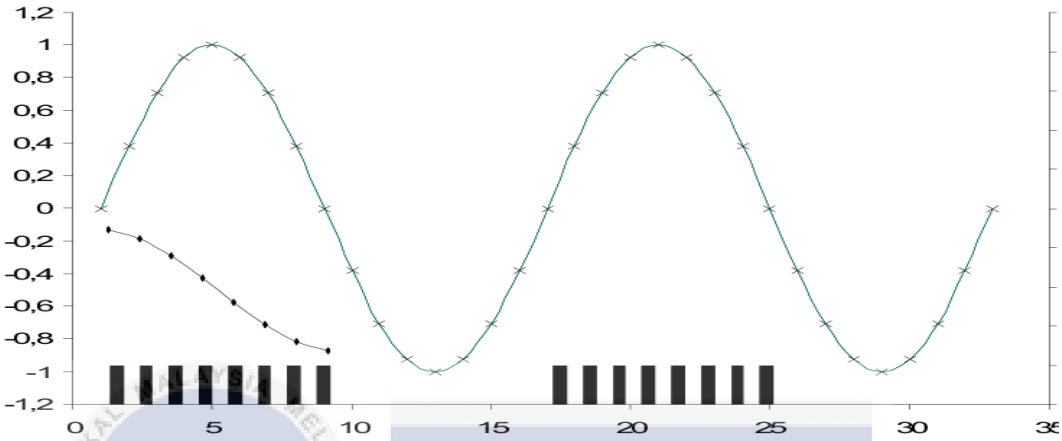

Figure 3.4.3: Spike Train

As Figure 3.4.3, the signal will become spike train after across the encoder circuit. Four encoders are used because it can form a short-term memory for the system, this will make the system could predict the signal.

3.5 Non-Linear Circuit

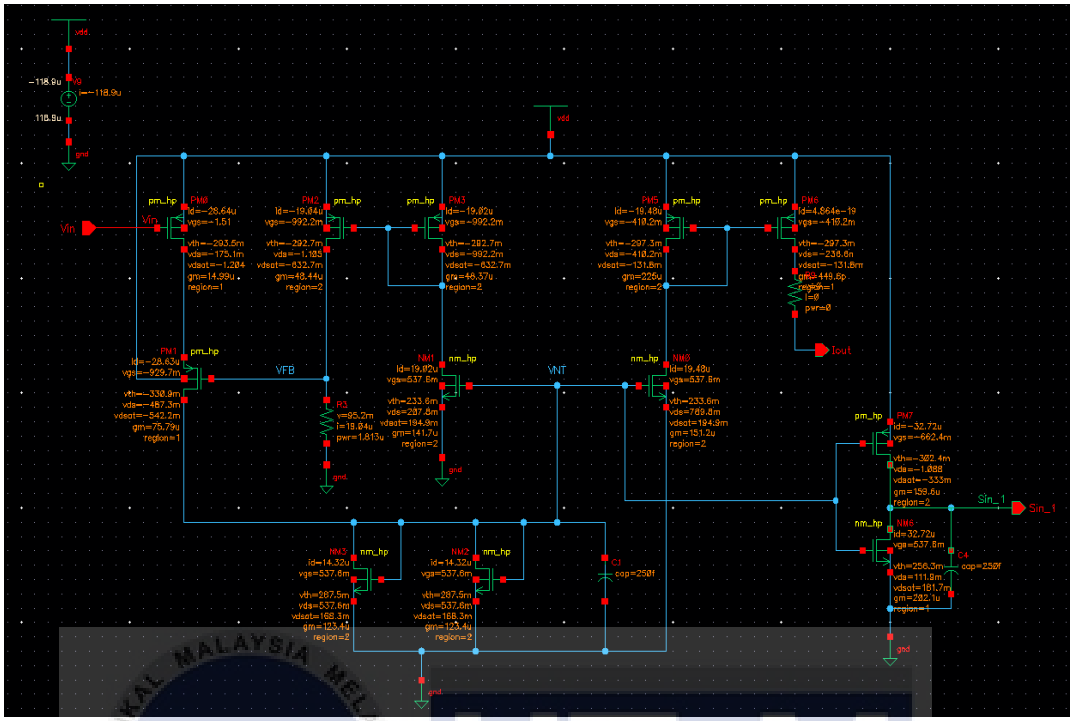

Figure 3.5.1: Non-linear Circuit

Figure 3.5.1 shows the simplified design scheme of non-linear. This circuit included two input triggers (PM0 and PM1), non-linear transformer (NM2, NM3 and C1), a feedback current mirror (PM2, PM3 and NM1), an output current mirror (PM5, PM6 and NM0), and a buffer (PM7, NM6 and C4).

During reset period, the input charged to VDD, such that (VDD −Vin) < Vth,p , where Vth,p is the input trigger's threshold potential (PM0 and PM1). The input trigger will be deactivated, and the nonlinear transformer will be discharged, resetting the output to zero.

During the decision-making process, the nonlinear transformer's two parallel nmos (NM2 and NM3) continually read the input signal and charge up its intrinsic capacitor (C1) to regulate the biassing voltage, VNT. Then, the VDS of NM0 increase rapidly

until its saturation level is reached. When the voltage VNT is smaller than the threshold of NM0, the VDS of NM0 would be 0, such that the output current mirror of the pmos PM5 diode-connected structure fully enables the output current mirror to achieve the maximum output current. In contrast, when the voltage VDS of NM0 reaches its saturation level, the transistor PM5 would drops into its sub-threshold region and decrease the output current (Iout). Meanwhile, the feedback current mirrors (PM2, PM3, and NM1) form a positive feedback loop to generate a high voltage at VFB, disabling the input trigger and keeping the nonlinear node in a state of rest until the next input data arrives. At the same time, the VNT also across a buffer (PM7, NM6 and C4) and process the signal (Sin_1) at the output.

Parameter	**Name**	**Value**	
VDD	V9	1.2V	
Resistor	R3	5kΩ	
Capacitor	C1, C4	250fF	
		Length	**Width**
Input Triggers	PM0	2.4u M	4.8u M
	PM1	2.4u M	4.8u M
Non-linear Transformer	NM2	300n M	700u M
	NM3	300n M	700u M
Feedback current mirror	PM2	2u M	2u M
	PM3	2u M	2u M
	NM1	4u M	8u M
Output current mirror	PM5	2u M	40u M
	PM6	2u M	40u M
	NM0	4u M	8u M
Buffer	PM7	1u M	5u M
	NM6	1u M	5u M

Table 3.5.1: Parameter of Non-linear Circuit

Table 3.5.1 shows that the parameter of VDD, resistor, capacitor and the value of length and width of the transistor which included input triggers, non-linear transformation, feedback current mirror, output current mirror and buffer.

3.6 Encoder

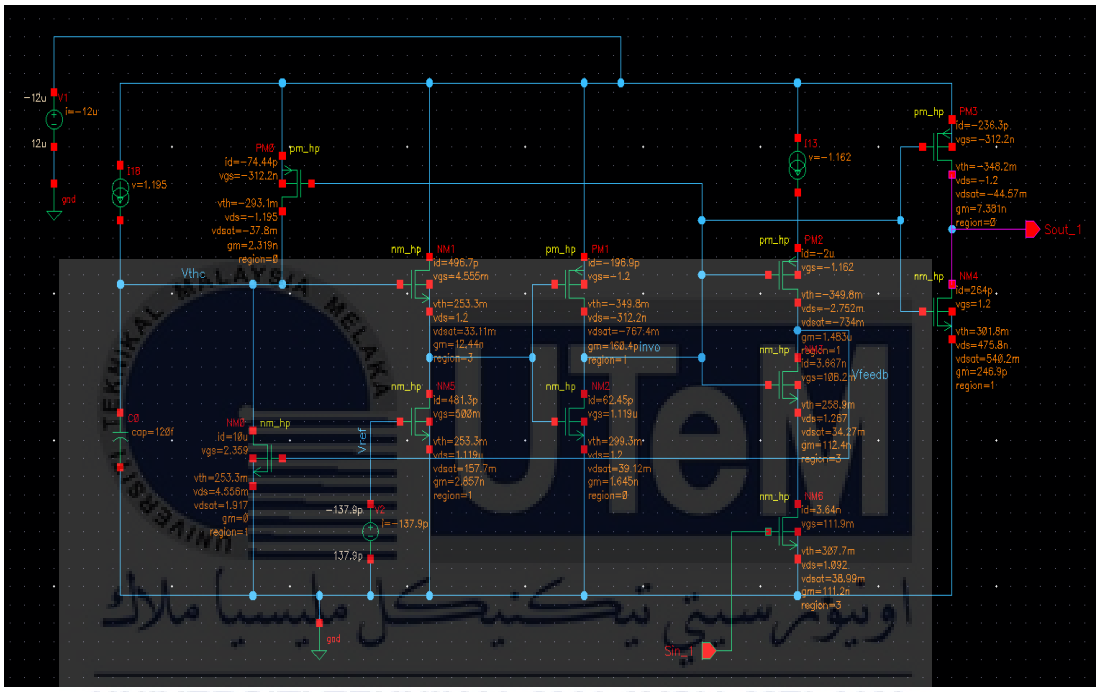

Figure 3.6.1: Encoder Circuit

Figure 3.6.1 shows design scheme of encoder circuit. The dynamic behavior of our analog DFR computing system changes as the delay changes with the delay embedded.

During operation, the sensing capacitance Cs (C0) continually tracks and charges up the calibration current Ical (I18) generated by the delay calibration module. When the voltage potential across the membrane capacitance Vthc, exceeds the threshold level of both of input transistor nmos (NM1 and NM5), the two cascading inverters (PM1, NM2 and PM3, NM4) fire an output spike. At the same time, the positive feedback

loop (PM2, NM3) provides a high voltage at Vreset, triggering the reset transistor (NM0), allowing the sensing capacitor Cs(C0) to discharge completely.

The delay time is regulated by the integrating time of sensing capacitor Cs(C0). The delay time constant can be written like this (1)

$$: \tau_{delay} = C_s \cdot \frac{V_{thc}}{I_{cal}} \quad (1)$$

The output spike train of Encoder_1 will become the input signal (Sin_2) of Encoder_2 and continue to across the third encoder and fourth encoder. For making the system could predict the signal, 4encoders are used because it can form a short-term memory for the system.

Parameter	**Name**	**Value**	
VDD	V1	1.2V	
Ical	I18	Ical	
Cs	C0	120fF	
Ical2	I13	2uA	
Vref	V2	500mV	
		Length	**Width**
Input transistor	NM1	1.2u M	8u M
	NM5	1.2u M	8uM
Cascading Inverter 1	PM1	240n M	2.4u M
	NM2	240n M	800n M
Cascading Inverter 2	PM3	240n M	2.4uM
	NM4	240n M	800n M
Feedback Loop	PM2	240n M	2.4u M
	NM3	800nM	2.4u M
Reset Transistor	NM0	1.2u M	8u M

Table 3.6.1: Parameter of Encoder Circuit

Table 3.6.1 shows that parameter of all components in encoder circuit. There are included value of VDD, Ical, Cs, Ical2, Vref and the value of length and width of input transistor cascading inverter 1, 2, feedback loop and reset transistor. Different encoders have different value of Ical, because those Ical needs to cover different pattern of input signal. Therefore, Ical for Encoder 1,2,3 and 4 are set at value 10uA, 20uA, 30uA and 40uA.

3.7 Power Consumption and Comparison

In [11], I learned that the power used when the transistor is not in the act of switching is known as static power, and it is calculated using (2)

$$: P_{static} = VDD \cdot I_{static} \quad (2)$$

where VDD is the supply voltage and I_{static} is the total current flowing through all the branch devices. CMOS technology has traditionally been recognised for its low static power. However, as devices scale up, gate oxide thicknesses decline and the likelihood of tunnelling increases, resulting in increasingly significant leakage currents. The Boltzmann distribution [12], which governs this subthreshold leakage current, is determined by thermodynamics.

The total power consumption of this project is recorded and compare to other ECG device projects. If the power consumption is higher than other projects, the parameter of schematic design need to troubleshoot and make sure the spike train output signal is maintained.

3.8 Summary of Methodology

In this chapter, I can summarize that flow chart is explained how I complete the project step by step. At first, a lot of literature review is done to understand how the project work and what I needed to do. After that, the Electrocardiogram Signals are found in PhysioNet because of the datasets from this website are free. The Cadence Virtuoso software is free through the PC of MiNE Laboratory. The software 'SoftEther VPN Client Manager' is downloaded and used, the VPN of UTeM is applied by using own card matric. The 'Remote Desktop Connection' is also downloaded to control the PC of MiNE Laboratory.

After that, the non-linear circuit and encoder circuit are designed to fire output spike train. The parameter is kept try and error to get the expected output. The different ECG signal inputs are tried to confirm the system is working, the parameter is edited until those ECG signals can process output spike train. After that, the power consumption is calculated by using formula (2) and the power consumption is averaged of 5 results by using 5 different ECG signal inputs. The result is recorded and compared to the results of previous work.

CHAPTER 4

RESULTS AND DISCUSSION

This chapter will discuss about the results of output spike train with using different input ECG signals. The results explained that how the calibration current affect the time delay. This chapter also shows the power consumption value of the system, and the results are compared with other projects.

4.1 Output Spike Train

The results of this project are simulated by using Cadence Virtuoso. As in Figure 4.1.1, the result of normal ECG signal (ECG signal_1) is plotted and the result shows that the spike train is depend on the fluctuation of input signal.

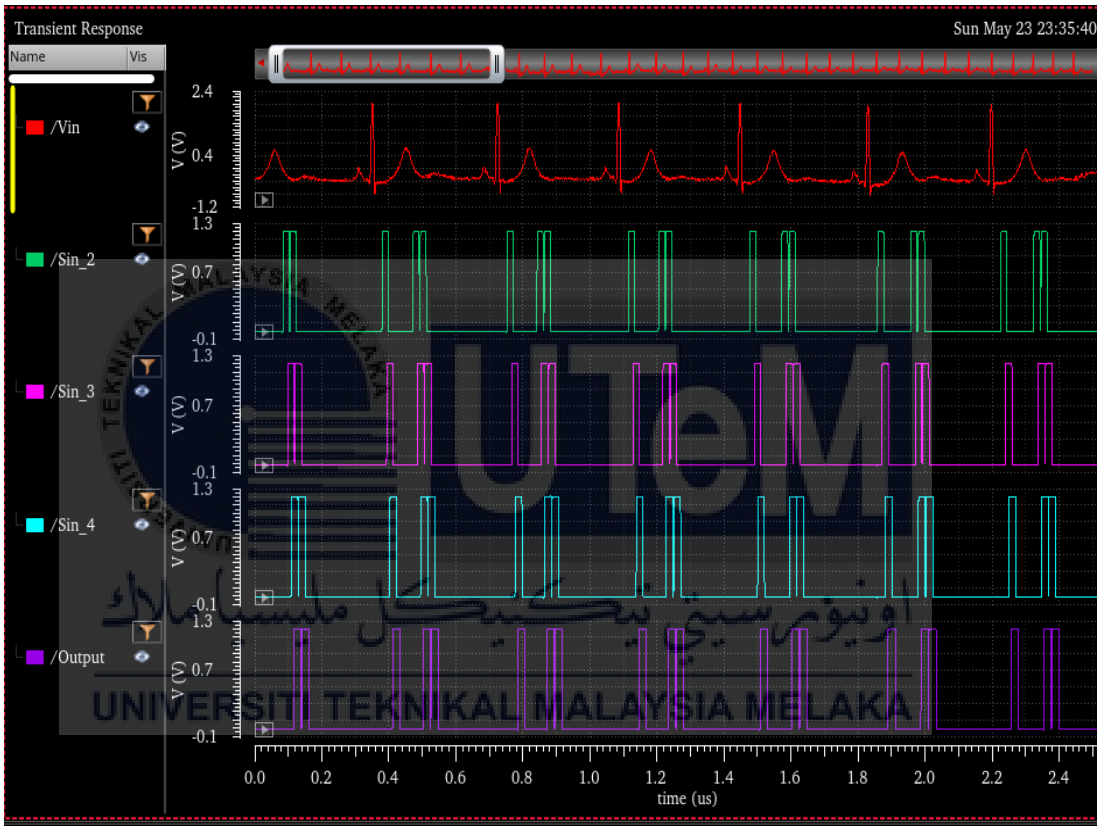

Figure 4.1.1: Result of ECG signal_1

In Figure 4.1.2, another situation by using another ECG signal input (ECG Signal_2). I observed that the R point (the highest point of an ECG signal as shown in Figure 2.6.1) of first part of signal is 2.35V, R point of second part is 1.86V and the R point of third part is 1.42V. This prove the higher the voltage, the increase the number of spike. Four different values of Ical are used to cover different pattern of input signal.

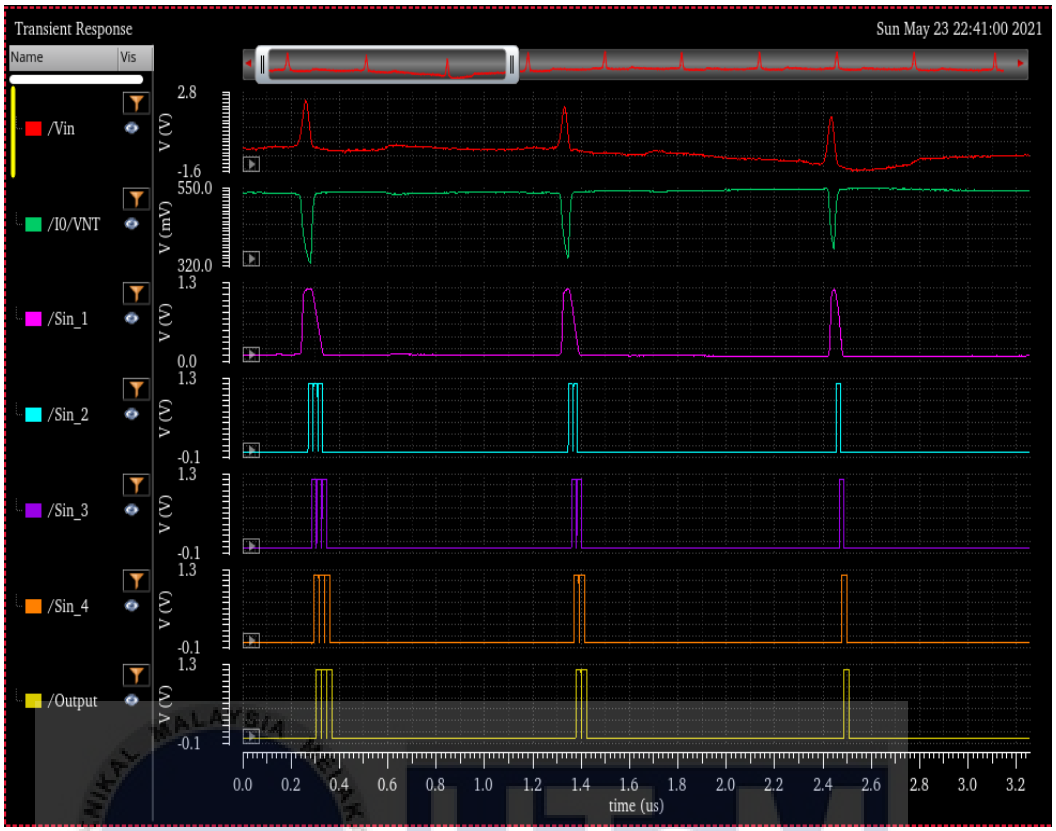

Figure 4.1.2: Result of ECG signal_2

4.2 Time Delay

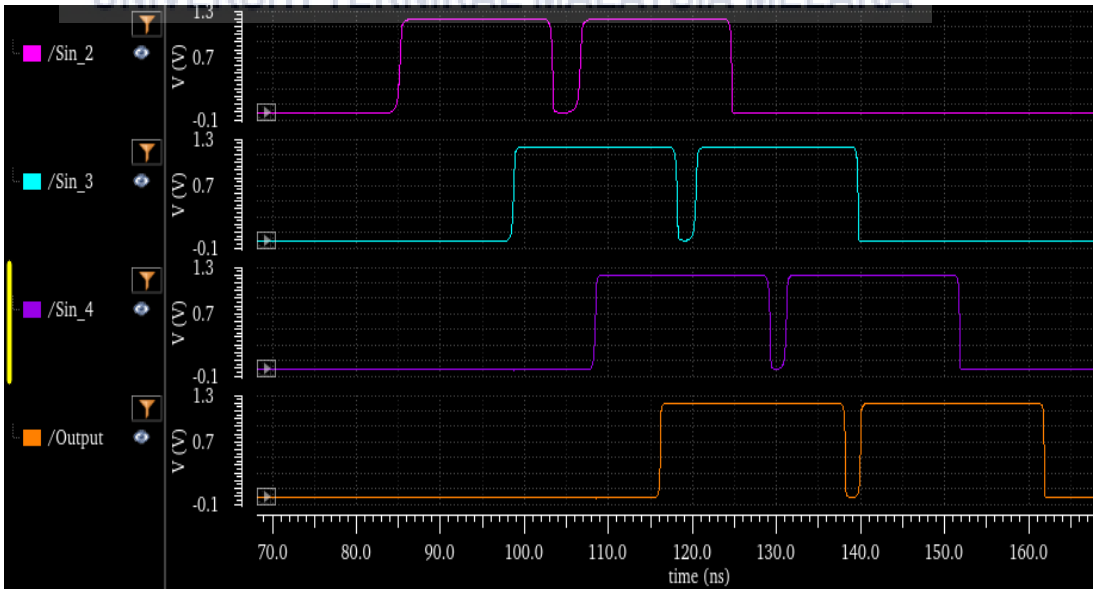

Figure 4.2.1: Distance between spikes

In Figure 4.2.1, since the Ical 1,3,5,7 are set in 10uA,20uA,30uA and 40uA, so we can observe that the distance between Sin_2, 3, 4 and output, align with the formula define in (1).

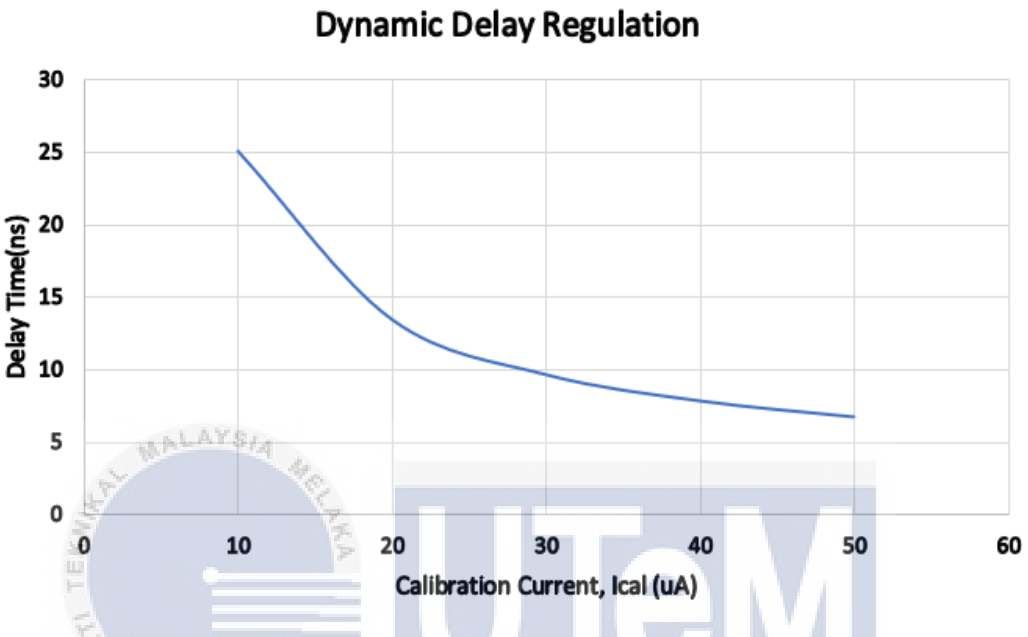

Figure 4.2.2: Dynamic Delay Regulation

As plotted in Figure 4.2.2, the calibration current, Ical, characterises the dynamic range of the delay time, τdelay. It can be seen from the delay characteristic testing findings that the observed that the increase the calibration current (Ical), the lower the delay time (τdelay).

4.3 Power Consumption

The total power consumption is calculated by using power static in (2). The Static Power is equal to Static Current multiply with VDD, and static current is equal to sum of the current in operation point from each branch device. The average power consumption is calculated by using average of five different ECG input signals which included 106_6, CU_VENTRICULAR, SLEEP_HEART, CHARIS_DATABASE, ECG_ID_DATABASE.

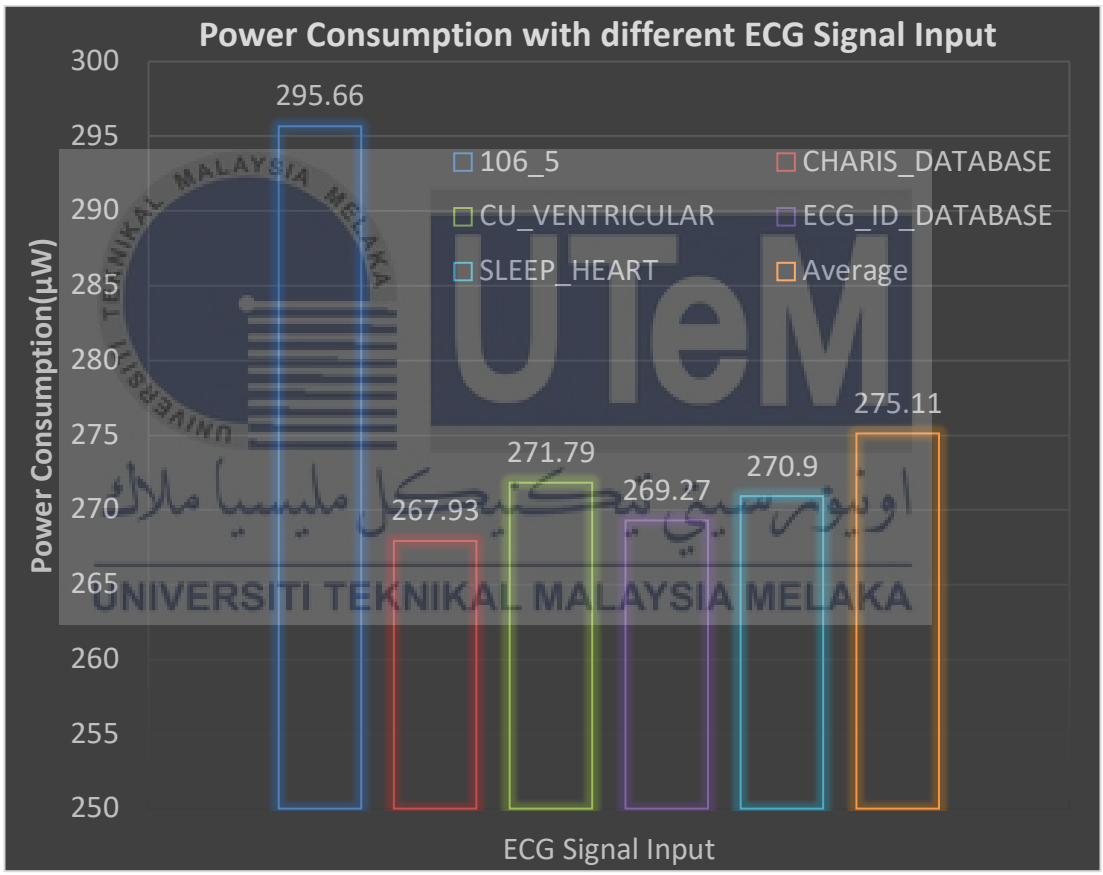

Table 4.3.1: Power Consumption with different inputs

Table 4.3.1 shows that I found the power consumption of 5 different signal inputs and get the average power consumption is equal to 275.11uW.

4.4 Benchmarking Table

Project	Power consumption (W)	Cite
ECG SIMULATOR	4.00mW	[13]
Solar-Powered Portable ECG Device	3.99mW	[14]
A low-power and miniaturized electrocardiograph data collection system	29.74mW	[15]
Automatic analysis method for long-term ECG	1.86W	[16]
This Work	275.11µW	

Table 4.4.1: Benchmarking table of power consumption

Table 4.4.1 shows that the benchmarking table of power consumption. After a lot of research are done, the power consumption of previous project is found and put into benchmarking table for comparison. After comparison, the results proved this project is using the lowest power consumption, which just using 275.11µW, demonstrating the power saving of the system.

4.5 Environment and Sustainability

Many people believe that going green means saving green – as in money – by lowering their energy bills. However, going green through home energy efficiency also entails environmental protection. Simply explained, energy efficiency is the practise of utilizing less energy to accomplish the same task while avoiding excessive energy bills and unneeded emissions. Many households and businesses use significantly more energy than is necessary. There is an obvious link between human energy consumption and the environment, even if it is not immediately evident. We can help restrict the number of toxic emissions generated by power plants, save natural resources, and safeguard ecosystems by consuming less energy.

With the progress of the times, technology is constantly updated, and electricity is one of the indispensable energies for people. When the demand for electricity continues to increase, it has indirectly affected the environment and has become a big problem that people must face. Therefore, we should pay more attention and continue to find ways to solve excessive energy consumption. Therefore, for sustainable development, energy saving is the constant pursuit of people。

4.6 Summary of Results and Discussion

This chapter can be summarized that the spike train is emerged, and it depended on the fluctuation of input ECG signal. The result also proved the higher the voltage, the increase the number of spikes. To cover the different pattern of input ECG signal, four different values of calibration current (ICal) are used.

The result also shows that when the increase the calibration current (ICal), the lower the delay time (τdelay). After that, the average power consumption proved that the power consumption of this project will not too far from the average power consumption. Then, the power consumption of this project is compared with another previous projects which already discuss in Chapter 2. As the benchmarking table, the project is achieved power saving successfully because this project having the lowest power consumption compared to the other previous projects. In this chapter, the environment and sustainability are also discussed.

CHAPTER 5

CONCLUSION AND FUTURE WORKS

This chapter will discuss about the conclusion, sustainable, and future recommendation. The conclusion part will discuss about how the objective achieved. Next, the sustainable part will discuss how the project affect sustainability, social and environment. After that, the future recommendation part will discuss about how to improve the project and what can do for the project in future.

5.1 Conclusion

Since the output fire spike train and it is following the fluctuation of input ECG signal, the first objective to identify the main circuit components and design parameters in Spike-Based Delayed Feedback Reservoir Computing System is achieved correctly. For the second objective is to analyse the power consumption of this project is also achieved because the power consumption is recorded and compared to those previous projects. Therefore, I concluded that two objectives are achieved.

5.2 Sustainable

Moreover, this project also achieved the three sustainable. For Sustainability, energy saving is the constant pursuit of people. For Social, the advancement of technology, all electronic products need better performance. For Environment Impact, when people consume less power, it can reduce the amount of toxic smoke released by power plants, protect the earth's natural resources, and protect the ecosystem from damage.

5.3 Future Recommendation

For the future work, the Back End part of this project can be do which included Design Rule Check (DRC), Layout vs Schematic (LVS) Check and post layout simulation. The foundry will set rules to make sure the design can be fabricated through DRC. By checking the LVS, the layout can make sure that is matching with the design schematic. After the LVS matches, the layout parasitic needed to extract and back annotate them to the schematic for simulation.

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