DESIGN AND ANALYSIS OF 18nm GRAPHENE/HfO_2/WSi_x NMOS DEVICE USING TAGUCHI METHOD.

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This report is submitted in partial fulfilment of the requirements for the degree of Bachelor of Electronic Engineering with Honours

Faculty of Electronic and Computer Engineering
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JULY 2021

DECLARATION

I declare that this report entitled "**DESIGN AND ANALYSIS OF 18nm GRAPHENE/HfO2/WSix NMOS DEVICE USING TAGUCHI METHOD**" is the result of my own work except for quotes as cited in the references.

Signature : ……

Author : HARIVINTHAAN A/L MAGENTHIRAN

Date : 25/06/2021

APPROVAL

I hereby declare that I have read this thesis and in my opinion this thesis is sufficient in terms of scope and quality for the award of Bachelor of Electronic Engineering with Honours.

Signature : ……

Supervisor Name : DR. AFIFAH MAHERAN BT. ABDUL HAMID

Date : ……25/6/2021……

DEDICATION

A special dedication to my family, supervisor and all my fellow friends for helping me to accomplish this final year project.

ABSTRACT

A bilayer-graphene in a planar structure was enhanced and analysed on an 18 nm NMOS device to obtain an optimum value for the performance parameters. The device is made of a high-k material called Hafnium Dioxide (HfO_2) and a metal gate called as Tungsten Silicide (WSi_x). The Silvaco software which consist of ATHENA and ATLAS modules were used to simulate the fabrication process of virtual devices and analyses their electrical properties. The Taguchi L9 orthogonal array method was then used to improve the system process parameters threshold voltage (V_{TH}) and minimum leakage current (I_{LEAK}), which are 0.540 V ± 12.7% for VTH and 20 nA/m for I_{LEAK} according to the International Technology Roadmap Semiconductor (ITRS 2013) specification. The most important factor for the V_{TH} optimization were signal to noise ratio (SNR) of nominal the better (NTB) an I_{LEAK} will be evaluated by the percentage influencing the process parameter. Hence, the optimized result of V_{TH}, 0.549704 V which is 1.8% nearer to the ITRS 2013 target while holding I_{LEAK} value of 5.31801nA/ μm which is lower than the predicted value and it shows that the system has an excellent device efficiency when the parameters are set appropriately.

ABSTRAK

Sebuah graphene dwi-lapisan dalam struktur planar ditingkatkan dan dianalisis pada perangkat NMOS 18 nm untuk mendapatkan nilai optimum untuk parameter prestasi. Peranti ini dibuat daripada bahan high-k iaitu Hafnium Dioxide (HfO_2) dan get logam yang disebut sebagai Tungsten Silicide (WSi_x). Modul perisian Silvaco yang terdiri daripada modul ATHENA dan ATLAS digunakan untuk merangsangkan proses fabrikasi peranti maya dan menganalisis sifat elektriknya. Kaedah tatasusunan ortogonal Taguchi L9 kemudian digunakan untuk meningkatkan parameter proses voltan ambang (V_{TH}) dan kebocoran arus minimum (I_{LEAK}), iaitu 0.540 V ± 12.7% untuk V_{TH} dan 20 nA/m untuk I_{LEAK} menurut spesifikasi roadmap semikonduktor teknologi antarabangsa (ITRS 2013). Faktor yang paling penting untuk pengoptimuman V_{TH} adalah isyarat kepada nisbah bunyi (SNR) nominal yang lebih baik (NTB) dan I_{LEAK} akan dinilai oleh peratusan yang mempengaruhi parameter proses. Oleh itu, hasil V_{TH} yang dioptimumkan, 0.549704 V yang 1.8% lebih dekat dengan sasaran ITRS 2013 sambil memegang nilai I_{LEAK} 5.31801nA/μm yang lebih rendah daripada nilai yang diramalkan dan menunjukkan bahawa sistem mempunyai kecekapan peranti yang sangat baik apabila parameter ditetapkan dengan betul.

ACKNOWLEDGEMENTS

Praise to god for providing me with the strength to complete this final year project. The project presented in this paper could not have been completed without the help of many people. Dr. Afifah Maheran Binti Abdul Hamid, my supervisor, had been extremely helpful in putting this final year project together. Next, I'd like to take this opportunity to express our heartfelt gratitude to my family for their patience and support during this critical period of research and completion of my final project.

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LIST OF SYMBOLS AND ABBREVIATIONS

SiO_2	:	Silicon Dioxide
WSi_x	:	Tungsten Silicide
FET	:	Field Effect Transistor
Si	;	Silicon
MOSFET	:	Metal-Oxide-Semiconductor-Field-Effect-Transistor
V_{TH}	:	Threshold Voltage
I_{LEAK}	:	Leakage Current
ITRS	:	International Technology Roadmap for Semiconductor
V_{GS}	:	Gate voltage
NF	:	Noise Factor
High-K	:	High dielectric
CMOS	:	Complementary metal-oxide-semiconductor
Poly-Si	:	Polycrystalline Silicon
S	:	Source
G	:	Gate
B	:	Body
D	:	Drain
I_{DS}	:	Drain-Source current

V_{DS}	:	Drain-Source voltage
V_P	:	Pinch-off Voltage
I_{DSS}	:	Saturated current
ZrO_2	:	Zirconium Dioxide
TiO_2	:	Titanium Dioxide
Bf_2	:	Boron Difluoride
BPSG	:	Borophosilicate Glass
SNR	:	Signal-to-Noise-Ratio
NTB	:	Nominal-The-Best
ANOVA	:	Analysis of Variance
PSG	:	Phosphor Silicate Glass
LPCVD	:	Low Pressure Chemical Vapor Deposition Process
RIE	:	Reactive ion Etching

LIST OF APPENDICES

CHAPTER 1

INTRODUCTION

1.1 Introduction

This chapter covers a brief introduction about a bilayer-graphene NMOS device with a planar device structure and a detailed background of this project are being discussed. In addition, the problem statement was discussed in this chapter in order to achieve the project's purpose, as well as the project objectives, scope, and outline structure.

1.2 Background

Advancement in electronics generation has resulted in a significant amount of innovation and development in the Metal Oxide Semiconductor Field Effect Transistor (MOSFET) when it comes to dimensioning, as well as improvements in the physical properties and efficiency of the devices. Moore's Law states that every 18 months, the quantity of transistors integrated on a 1x1cm chip increases at an exponential rate [1]. This invention was predicted to be a promising design with scaling in the next 15 years by International Technology Roadmap for Semiconductors (ITRS). As a result, MOSFET transistor scaling is concerned with reducing the overall size of the device as much as technology allows while maintaining the geometric ratios found in larger devices.

The inspection of a CMOS device that requires less power usage for an ever-increasing number of mobile applications and can provide low standby power, improved performance, and active power without incurring increased costs. This is why Moore's Law must be followed in order to achieve high integration densities with faster switching times, as well as lower power at lower costs, as previously mentioned. As traditional MOSFET efficiency increases, additional downscaling results in higher integration density, as well as higher transistor driving current and density for quicker switching speed [2]. Short channel effect (SCE), hot carrier effect, which causes a major leakage current catastrophe, and high current consumption are all issues. To summarize, a transistor with a shorter gate length of 5nm can perform worse than a transistor with a longer gate length of 20nm.

To improve performance, High-Dielectric (High-K)/metal gate were used to meet the above requirements. Silicon dioxide (SiO2) had been popularly used as a gate

oxide material over years, and as MOSFETs downscale, the thickness of silicon dioxide gate dielectric will be reduced as well, resulting in increased gate capacitance (per unit area) and improved device efficiency. As the device's thickness decreases to 2nm, the leakage current induced by tunneling increases drastically, resulting in high power consumption and a decrease in performance [2]. To prevent both of these problems, high-k materials were replaced with silicon dioxide, which allows gate capacitance without the leakage problems that come with it. Although high-k/metal gate technology reduces carrier mobility due to distant coulomb dispersion and variations in material parameters, it also reduces gate leakage and provides better electrostatic integrity than silicon dioxide [3].

Graphene is a two-dimensional single-layer thick crystalline allotrope of carbon. It's a great material for potential smaller and faster electronics, but it'll take a lot of study to get there [4]. In this study, graphene is used as channel material in field effect transistors (FETs). This study analyzed the impact of process parameters on the performance parameter of a planar 18 nm HfO_2/WSi_x NMOS MOSFET, and the results are presented in this paper. The robust Taguchi method analysis will then be used to determine the device's performance.

1.3 Problem statement

In order to meet effective and sustainable requirements, new technologies and industries have made replacement and improvements for the design and manufacturing of electronic devices over the last few decades. In every research and analysis, the scaling down technology of MOSFETs was achieved according to Moore's Law and the International Technology Roadmap Semiconductor (ITRS) predictions. Silicon dioxide (SiO_2) has been used as a gate dielectric material for

decades because it requires a thin film thickness that scales down to less than 2nm [5]. What concerns is the lack of reliability and an unclear integration path. Tunnelling current became the dominant leakage path as a result of this problem, as did the short channel effect and oxide breakdown, leading to poor device performance and high gate leakage current. To overcome the problem, high-k dielectric materials was introduced as a replacement of gate dielectric and this makes a smaller gate length that will be fabricated. The improvements in the downscaling of the NMOS structure are measured by enhancing the process parameter via Taguchi method in order to achieve a device with the ideal threshold voltage (VTH).

1.4 Objectives

There are two objectives in this study which are:

I. To design and simulate a bi-layer graphene on Hafnium Oxide (HfO_2)/Tungsten Silicide (WSi_x) on 18nm NMOS device using Silvaco software.

II. To analyse and optimize the electrical characteristics of NMOS device with Taguchi Orthogonal Array technique.

1.5 Scope of work

This project will be completed using Silvaco software. The device will be designed using Silvaco's ATHENA software, and the electrical properties will be evaluated using ATLAS. In this study, the Taguchi method will be used to perform arithmetic analysis in order to find the optimal combination that will result in a higher-performing device. Next, the structure of the device are with high-k is HfO_2 and WSi_x as metal gate. In this study, there is no need of equipment needed as it will be simulated through software as virtual fabrication will be done for designing the NMOS transistor. In this project, V_{TH} and I_{LEAK} will be optimized because this are the two parameters that will make a good, efficient MOSFET. Finally, the size of the gate length of NMOS device is 18nm. Figure 1.1 shows the flowchart of the project scope.

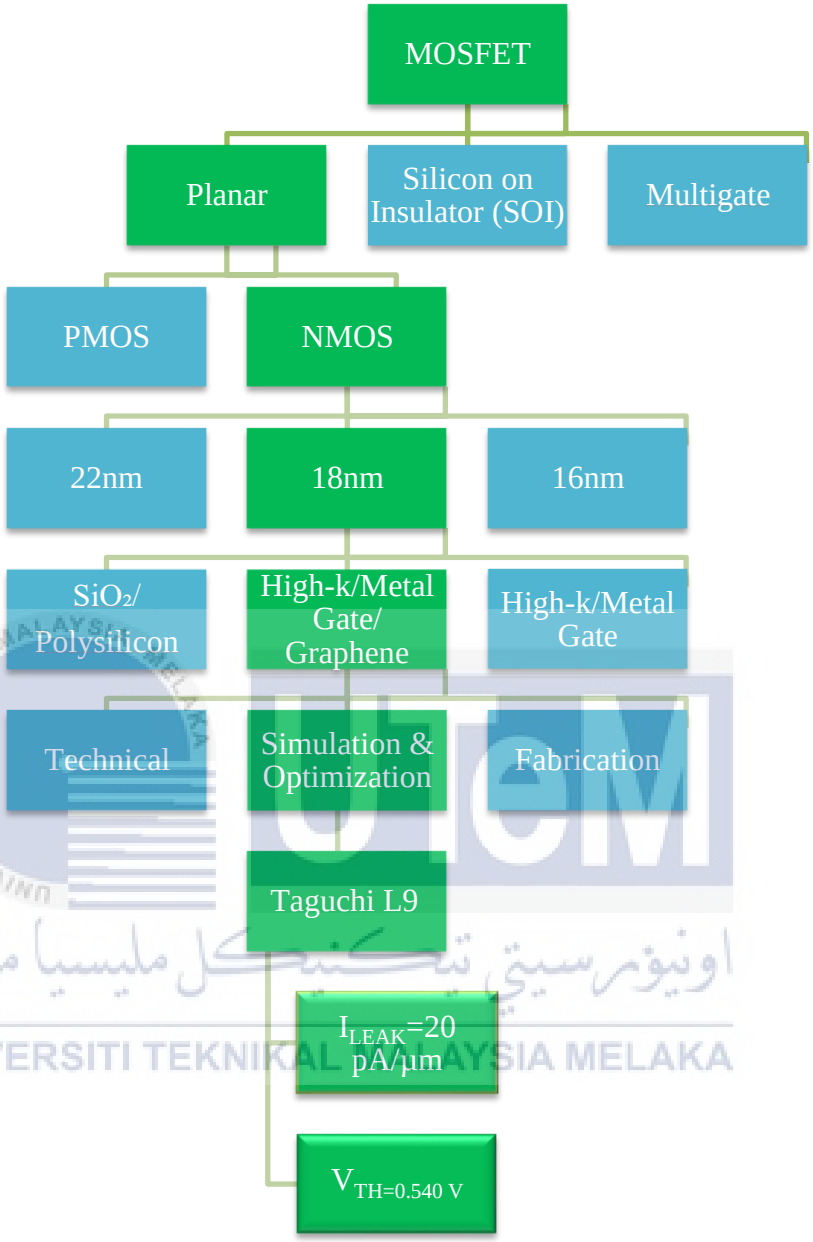


Figure 1.1 Scope of Work Flowchart

1.6 Organization of report

Using the Silvaco software, this report focuses on designing and virtual simulating a bilayer-grpahene on HfO_2/WSi_x on an 18nm NMOS device. Introduction, background study, methodology, results and discussion are the five main parts of the paper, which are followed by conclusion and future work A brief overview of the project's context, problem statement, objectives, scope of the project, and report structure was addressed in Chapter 1. In Chapter 2, discusses the literature study introduction and other related studies to this project by different researches, which include the MOSFET fundamentals, Moore's Law, high-k, graphene properties, and other fundamental theories. Following that, Chapter 3 discusses the methodology employed in order to achieve the project's goals and scope of work. The requirement and flowcharts that are required to track down the project flow in order to achieve the goal, as well as the study summary, will be studied here. In Chapter 4, is very much about project's results and discussion, the Taguchi L9 method will be used to discuss the virtual transistor that is being fabricated in the software, as well as the device's electrical properties and process parameters. Finally, Chapter 5 wraps up the project as well as the results, as well as future work explanations.

CHAPTER 2

BACKGROUND STUDY

2.1 Introduction

In this chapter, a brief discussion on understanding the MOSFET device and the Moore's Law which are the law that is been introduced over the years for transistor scaling process. Moreover, in this chapter also reviews the materials that will be used in order to proceed with the NMOS device design in the planar as well discussion about the advantages of the material properties will also discussed. This chapter also reviews the previous research studies that have been conducted in relation to this project.

2.2 Fundamental of MOSFET

Field Effect Transistor (FETs) have a few drawbacks, including a high drain resistance, a moderate input impedance, and a slower operation. The MOSFET, which is an advanced invention FET model, was invented to solve these problems. Insulated Gate Field Effect Transistor (IGFET) is also another name for this device. This MOSFET is capable of operating in both depletion and enhancement modes. The device has four terminals: source (S), gate (G), drain (D), and body (B). The MOSFET's source terminal is connected to the device's body, creating a three-terminal device similar to a field-effect transistor. MOSFETs are used in both analogue and digital circuits and are commonly referred to as transistors. [6].

As a result, the device's functionality is determined by the electrical variations in the channel width, as well as the flow of carriers, which are either holes or electrons. Charge carriers which invades through the source and exit via drain. There are two types of MOSFET transistors which are so called as the NMOS and PMOS transistor which differ for the current transistor in the polarity of the carrier responsible [6]. A PMOS MOSFET's current flow is in the direction of positive charge holes, whereas an NMOS MOSFET's current flow is in the direction of negatively charged electrons. Figure 2.1 shows the basic structure of a MOSFET [7].

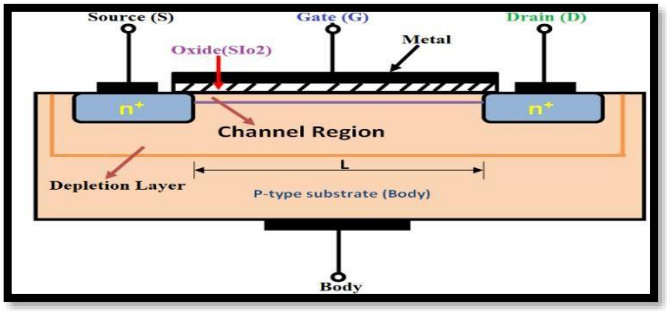


Figure 2.1 MOSFET structure

2.2.1 MOSFET operation

The MOSFET operates on the principle of a switch, controlling the voltage and current flows between the source and drain. The working theory of the MOSFET is solely depends on the MOS capacitor, which is the semiconductor surface beneath the oxide layers between the source and drain terminals and is the MOSFET's primary component. It can be inverted from p-type to n-type by applying positive or negative gate voltages. The holes under the oxide layer will be forced down with the substrate when a repulsive force is applied at the positive gate voltage [8].

The region of depletion where acceptor atoms' bound negative charges which are correlated. A channel is formed when electrons are reached. The positive voltage also attracts electrons into the channel from the n + source and drain regions. Current flows freely between the source and the drain when a voltage is supplied between the drain and the source, and the gate voltage regulates the electrons in the channel. A hole channel forms under the oxide layer when a negative voltage is applied instead of a positive voltage [8]. The working principle of a MOSFET is shows in the figure below. Figure 2.2 shows the operation of the MOSFET [9].

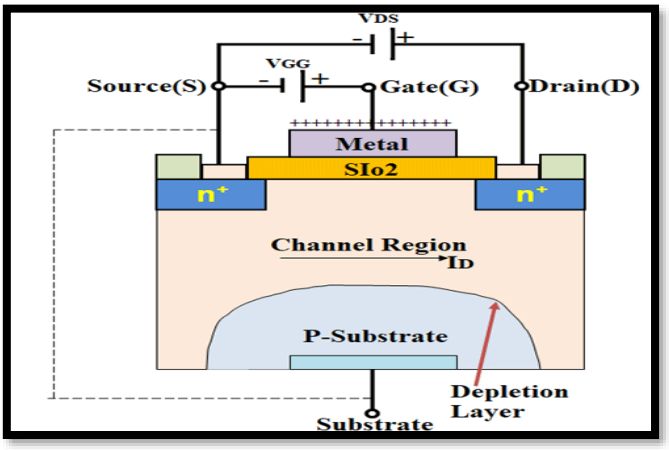


Figure 2.2 Operation in MOSFET

2.2.2 N-channel MOSFET

An N-channel region exists between the source and drain terminals of an N-Channel MOSFET. The four terminals in this type of transistor which are gate, drain, source, and body, with the drain and source being strongly doped n + regions while the substrate or body being P-type. Negatively charged electrons drive current flow in this type of MOSFET. The holes underneath the oxide layer are pushed downwards into the substrate whenever a positive voltage is supplied to the gate terminal with repulsive force [10]. The depletion area is populated by the bound negative charges related with the acceptor atoms. Upon the reach of electrons, the channel is created. The positive voltage also draws electrons into the channel from the n + source and drain regions. Figure below shows the illustration of enhancement and depletion mode of N-channel. Figure 2.3 shows enhancement and depletion mode of N-channel [11].

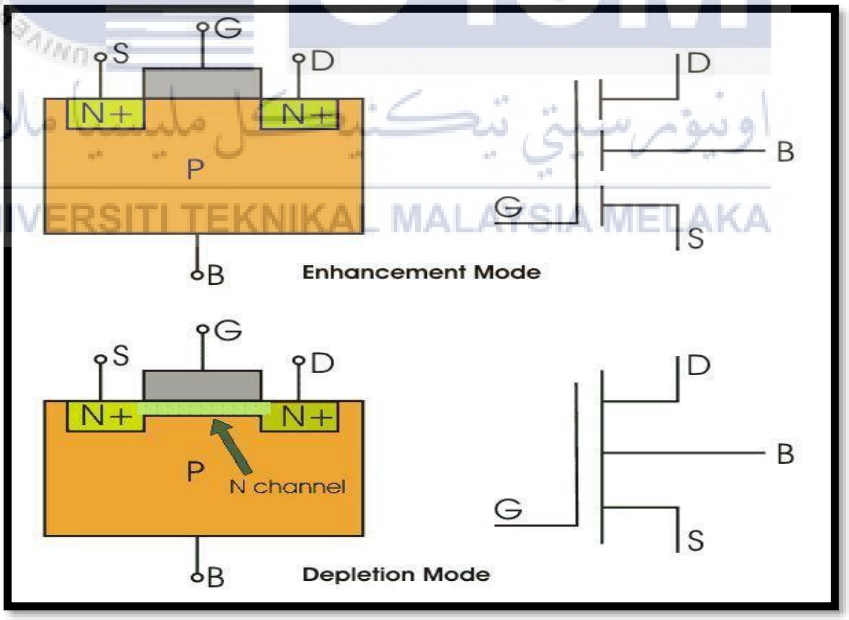


Figure 2.3 Enhancement and Depletion mode of N-channel

2.2.3 Transistor Electrical Characteristics

In general, cut-off, linear or ohmic region, and saturation region are the three operating regions of any MOSFET. The drain-to-source current versus gate-to-source voltage transfer characteristics for n-channel enhancement type are shown in the Figure 2.4 [11]. Once the V_{GS} reaches the V_{TH} threshold voltage, the device current through it will undoubtedly zero. This is because the device in this state lacks a channel that would attach the drain and source terminals. As the corresponding performance characteristics show (I_{DS} versus V_{DS}), even a rise in V_{DS} will lead to no current flow under this condition. As a result, this situation is a cut-off zone for MOSFET operations.

With an increase in I_{DS}, the current through the device rises initially (Ohmic region) then saturates at a value defined by the V_{GS} (operation saturation region) once V_{GS} passes V_{TH} [11]. In addition, as shown in the figure below, the pinch-off voltage locus, from which V_P rises with an increase in V_{GS}.

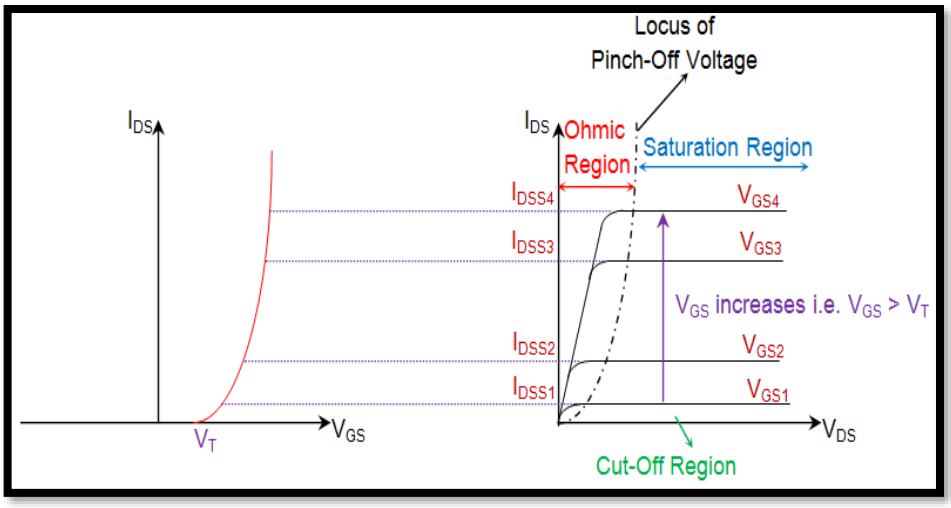


Figure 2.4 Enhancement mode curve

The transfer characteristics of an n-channel MOSFET during depletion are shown in Figure 2.5 [11]. Even though V_{GS} is 0V, this shows clearly that the device is has a current flow. As can be seen by V_{GS} curve, these devices perform even when the gate terminal is left unbiased. In this state, as the value of V_{DS} (Ohmic region) results in an increase, the current through the MOSFET increases until V_{DS} equals pinch-off voltage V_P. After that, I_{DS} will be saturated to a specific I_{DSS} (saturation region of operation) level [11], where it will increase as V_{GSS} increases.

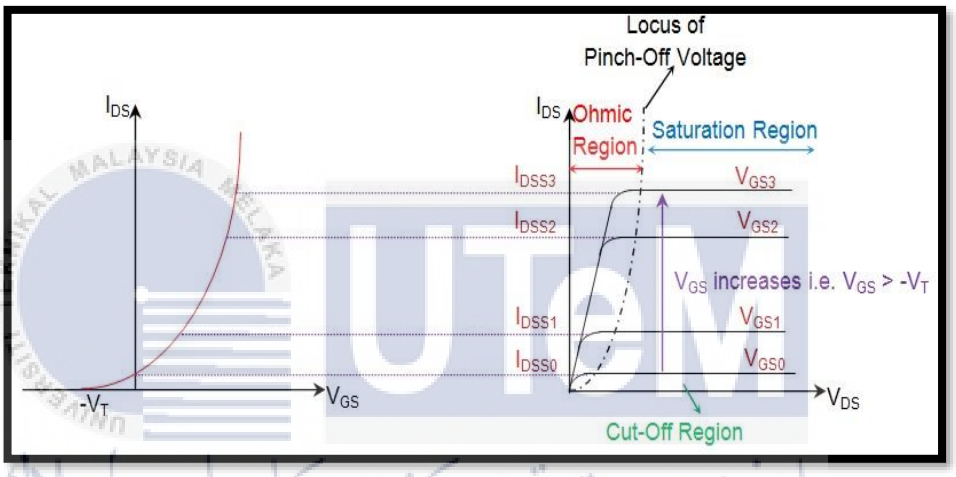


Figure 2.5 Depletion mode curve

2.2.4 Moore's Law

Moore's law states that the number of transistors per silicon chip doubles every year, as predicted by American engineer Gordon Moore in 1965. According to Moore's Rule, the pace and capacity of computers will increase every couple of years, while the cost will decrease [12]. Moore's Law is often believed to be exponential, and the prediction has been used in the semiconductor industry to direct long-term planning and set research and development goals, acting as a self-fulfilling prediction in several ways. As seen in the Figure 2.6, a single microprocessor now has nearly half a billion integrated transistors. This remarkable development demonstrates Gordon

Moore's foresight in this field, as well as the importance of it for today's technologies [13]. Figure 2.6 shows Moore's Law visualization [14].

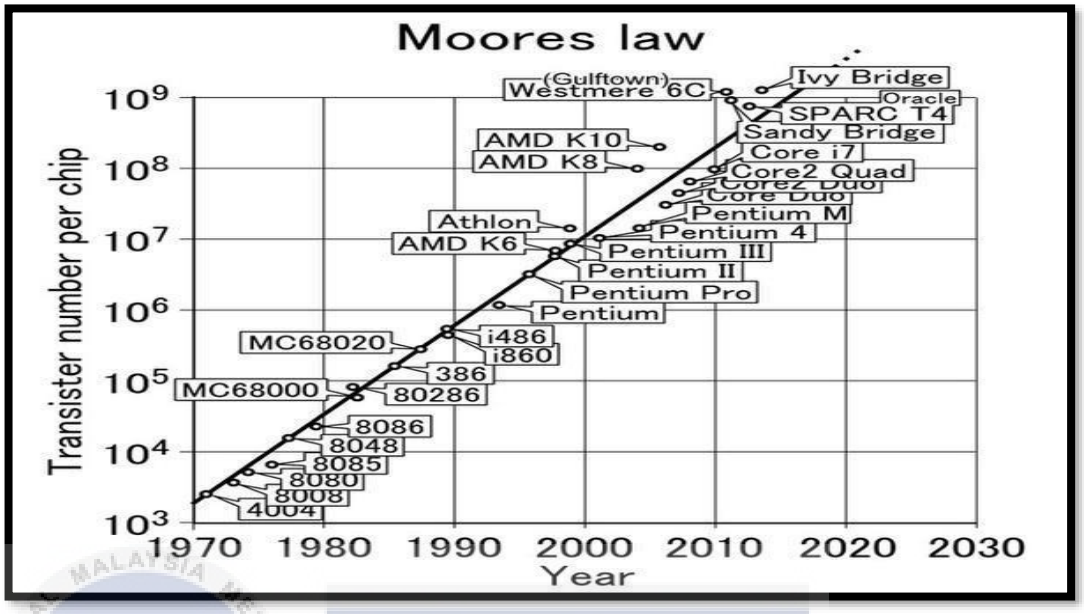


Figure 2.6 Moore's Law visualization

2.2.5 High Permittivity (high-k) Dielectric

As previously addressed with Moore's law, progress is made by scaling MOSFETs to smaller and smaller physical dimensions. For traditional thermally grown SiO2 gate dielectrics, the miniaturization has resulted in remarkable tunneling current leakage levels. In order to develop the best high-k dielectrics that could replace the traditional SiO_2 and SiON gate insulators in MOS transistors, numerous studies and researches were conducted.

Without the associated leakage effects, elevated gate capacitance can be done by changing the silicon dioxide gate dielectric with a high-k material [15]. High-k materials such as ZrO_2, TiO_2, and HfO_2 have been used and researched for many years. Many studies have chosen HfO_2 as their high-k dielectric permittivity in CMOS applications. Furthermore, Hafnium has excellent electrical properties as well as

thermal stability. It would be beneficial to maintain a low current of leakage. The high-k dielectrics are coupled with the metal gate in order to prevent Poly-Si depletion.

2.3 Graphene

2.3.1 Graphene Bandgap

Graphene is now being studied by electron-device researchers, rather than condensed matter physicists. Graphene-based transistors, in particular, have made rapid progress and are now considered a viable post-silicon electronic alternative. Single-layer graphene is purely two-dimensional material with a lattice of regular hexagons on each corner with a carbon atom. Since the bandgap is zero, switching off devices with large-area graphene channels is difficult, making it unsuitable for logic applications. The band structure of graphene, on the other hand, can be adjusted and a bandgap can be opened in three different ways which are by restricting large-area graphene to shape graphene nanoribbons in one-dimension, biasing bilayer graphene, and applying graphene strain [16]. The greater the bandgap that opens the nanoribbons, the further the valence and transmission bands become parabolic rather than cone-shaped, as seen in the Figure 2.7. This decreases the curvature of the charge carriers around the K point and raises the effective mass, lowering mobility [17]. Figure 2.7 shows the bandgap of graphene [18].

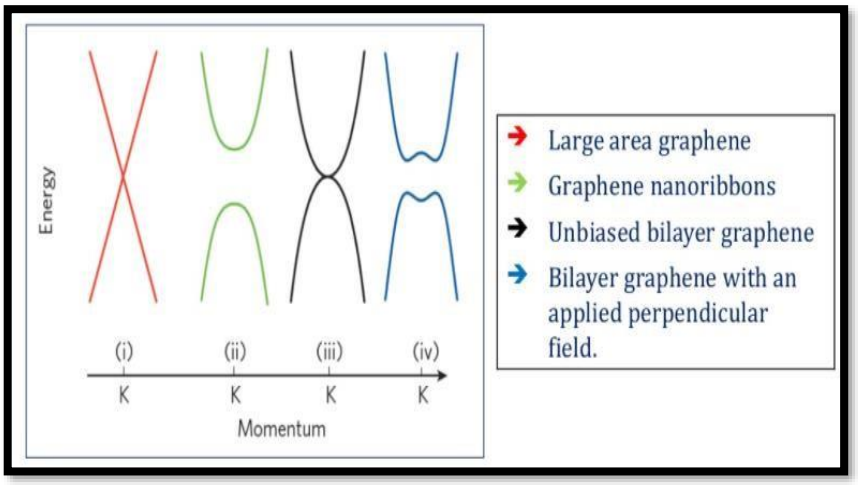


Figure 2.7 Bandgap of Graphene

2.3.2 Graphene Mobility

The most commonly discussed benefit of graphene is its high carrier mobility at room temperature. The use of a top-gate dielectric in early graphene MOS structures affected mobility. Recent observations of mobility in top-gated graphene MOS channels, as well as similar mobility before and after top-gate formation, show that high-mobility graphene MOS channels can be made with the appropriate dielectric gate and deposition process optimization [18]. The electron mobility of typical semiconductors tends to decrease as the bandgap increases. Mobility refers to carrier transport in low electric fields; in modern FETs, short gate lengths result in high fields in a significant proportion of the channel, reducing mobility's importance to the system's performance [2]. Monolayer and bilayer graphene mobility is entirely dependent on the thickness of a top dielectric high-k metal oxide layer.

2.4 Fundamentals of Planar

The primary method for creating integrated circuits is silicon planar technology. This technology is used to construct circuits on wafer substrates layer by layer. A symmetric source and drain region separated by the channel area has been around for more than four decades and maintains much the same basic structure design. For years, the shrinking size of MOSFET's physical properties has dominated its efficient growth. Figure 2.8 shows the structure of planar MOSFET [19].

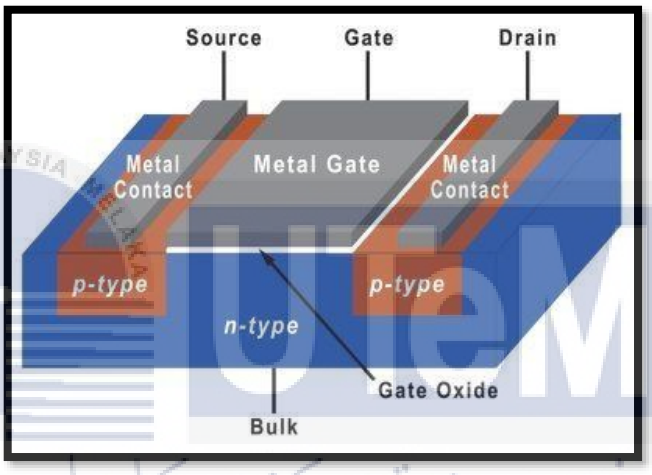


Figure 2.8 Planar MOSFET

2.5 Summary of Previous researches

Table 2.2 shows a summary of previous studies.

Table 2.1 Summary of previous research

No.	Reference	Author/Journal/Year	Summary
1	[2]	A H Afifah Maheran, E N Firhat, F Salehuddin, A S Mohd Zain, I Ahmad, Z A Noor Faizah, P S Menon, H A Elgomati,Ameer F Roslan, "Minimum leakage current optimization on 22 nm SOI NMOS device with HfO_2/WSi_x/Graphene gate structure using Taguchi method",2019.	• A 22nm SOI NMOS device. • Tungsten Silicide (WSi_x) as metal gate and Hafnium Dioxide (HfO_2) as high-k. • I_{LEAK}=9.29746nA/µm. • Taguchi L9 method.
2	[20]	Mah, S. K., Ahmad, I., Ker, P. J., Tan, K. P., & Faizah, Z. A. N. (2018). "Modeling, Simulation and Optimization of 14nm High-K/Metal Gate NMOS with Taguchi Method",2018.	• A 14nm NMOS deivce. • High-k as Lathanum oxide (La_2O_3) and metal gate as Tungsten Disilicide (WSi_2). • Optimization using L9 Taguchi. • V_{TH}= 0.233321 V • I_{OFF}=4.732375x10^{-11} A/µm.
3	[21]	K.E. Kaharudin,F. Salehuddin,A.S.M. Zain, M.N.I.A. Aziz, "Taguchi Modeling With The Interaction Test For Higher Drive Current In Wsi_x/TiO_2 Channel Vertical Double Gate NMOS Device" 2016.	• Vertical Double Gate NMOS device. • Titanium Dioxide and Tungsten Silicide (WSi_x) as metal gate. • Taguchi L12 method.

			• I_{ON}= 2859.7 µA/µm.
4	[22]	S. K. Mah, I. Ahmad, P. J. Ker, Noor Faizah Z. A, "Modelling of 14NM Gate Length La_2O_3-based n-Type Mosfet",2016.	• 14nm NMOS device. • Lathanum oxide (La_2O_3) as gate dielectric and Titanium Silicide ($TiSi_2$) as metal gate. • V_{TH}= 0.208397 V • I_{LEAK}= 1.00402 x 10^{-7} A/µm.
5	[23]	Noor Faizah, Z. A., Ahmad, I., Ker, P. J., Siti Munirah, Y., Mohd Firdaus, R., Md. Fazle, E., & Menon, P. S. "Process Parameters Optimization of 14nm MOSFET Using 2-D Analytical Modelling", 2016.	• A 14nm CMOS transistor. • Tungsten Silicide (WSi_x) as metal gate and Hafnium Dioxide (HfO_2) as high-k
6	[24]	Faizah, Z. A. N., Ahmad, I., Ker, P. J., Roslan, P. S. A., & Maheran, A. H. A., "Modeling of 14 nm gate length n-Type MOSFET", 2015.	• A 14nm N-type MOSFET. • High-k as Hafnium Dioxide (HfO_2) and Tungsten Disilicide (WSi_2). • V_{TH}= 0.232291 V • I_{LEAK}=77.11x10^{-9} A/µm.
7	[25]	Norani Atan , Burhanuddin Bin Yeop Majlis , Ibrahim Bin Ahmad , K. H. Chong, "Influence of optimization of control factors on threshold voltage of 18 nm HfO_2/$TiSi_2$ NMOS", 2019.	• A planar 18nm NMOS transistor. • High-k as Hafnium Dioxide (HfO_2) and Titanium Silicide ($TiSi_2$). • V_{TH}= 0.3055 V • ITRS 2012.

8	[26]	Noor Faizah Z.A., I. Ahmad, P.J. Ker, P.S. Menon, Afifah Maheran A.H, S.K. Mah, "Optimization of Process Parameters for Threshold Voltage and Leakage Current based on Taguchi Method", 2018.	• A 14nm p-type planar transistor. • High-k as Hafnium Dioxide (HfO_2) and Tungsten Disilicide (WSi_2). • V_{TH}= 0.241102 V • I_{LEAK}= 21.285A/µm • Taguchi L9 method.
9	[27]	K.E.Kaharudin, F.Salehuddin, A.S.M.Zain,M.N.I.A.Aziz, "Application of Taguchi-based Grey Fuzzy Logic for Simultaneous Optimization in TiO2/WSix-based Vertical Double-gate MOSFET", 2016.	• 10nm vertical double gate n-channel transistor. • High-K material of Titanium Dioxide (TiO_2) and for the metal, Tungsten Silicide (WSi_x) had been used. • I_{OFF}= $8.483x10^{-10}$ A/µm. • L9 Taguchi method.
10	[28]	K. E. Kaharudin, F.Salehuddin, A. S. M. Zain and M. N. I. A. Aziz, "Comparison Of Taguchi Method And Central Composite Design For Optimizing Process Parameters In Vertical Double Gate MOSFET', 2017.	• Optimizing process parameters. • Taguchi L27 method had been used and followed with CCD for utilizing inorder tooptimize the six process parameter. • $V_{TH\_using\_Taguchi}$= 0.445 V • $I_{OFF\_using\_Taguchi}$=$4.227x10^{-16}$A/µm.

CHAPTER 3

METHODOLOGY

3.1 Introduction

This chapter will go through the methodology that was utilized to create a virtual fabrication of an 18nm NMOS device, as well as a complete review. Many methodologies or results from this area are primarily published in journals for others to benefit from and develop as future research. During the development of the device, a methodical approach was necessary to ensure that the project ran smoothly. To complete this project, there are several phases that must be completed, including the development of an NMOS device using SILVACO software and a thorough explanation of the Taguchi L9 process.

3.2 Flowchart of Project

The project began with literature review and required background studies, as seen in the flowchart below. After that, the Silvaco ATHLAS and ATHENNA modules were used to design and model a graphene on Hafnium Dioxide (HfO_2)/Tungsten Silicide (WSi_x) on an 18nm NMOS device. The electrical characteristics of the device will then be investigated using the ITRS 2013 specifications. If the design's electrical characteristics match the prediction, the design is considered a successful design that can be implemented. The Taguchi Orthogonal Array approach will be used to ensure that the device operates properly. In order to attain the desired result, the Taguchi method seeks to find a feasible combination of design factor. It has the potential to be a powerful tool for increasing research and development efficiency. The Taguchi method would improve the quality of the finished product or process while consuming the least amount of time and money. Finally, the threshold voltage and leakage current results will be compared to see whether they can be reduced or optimized.

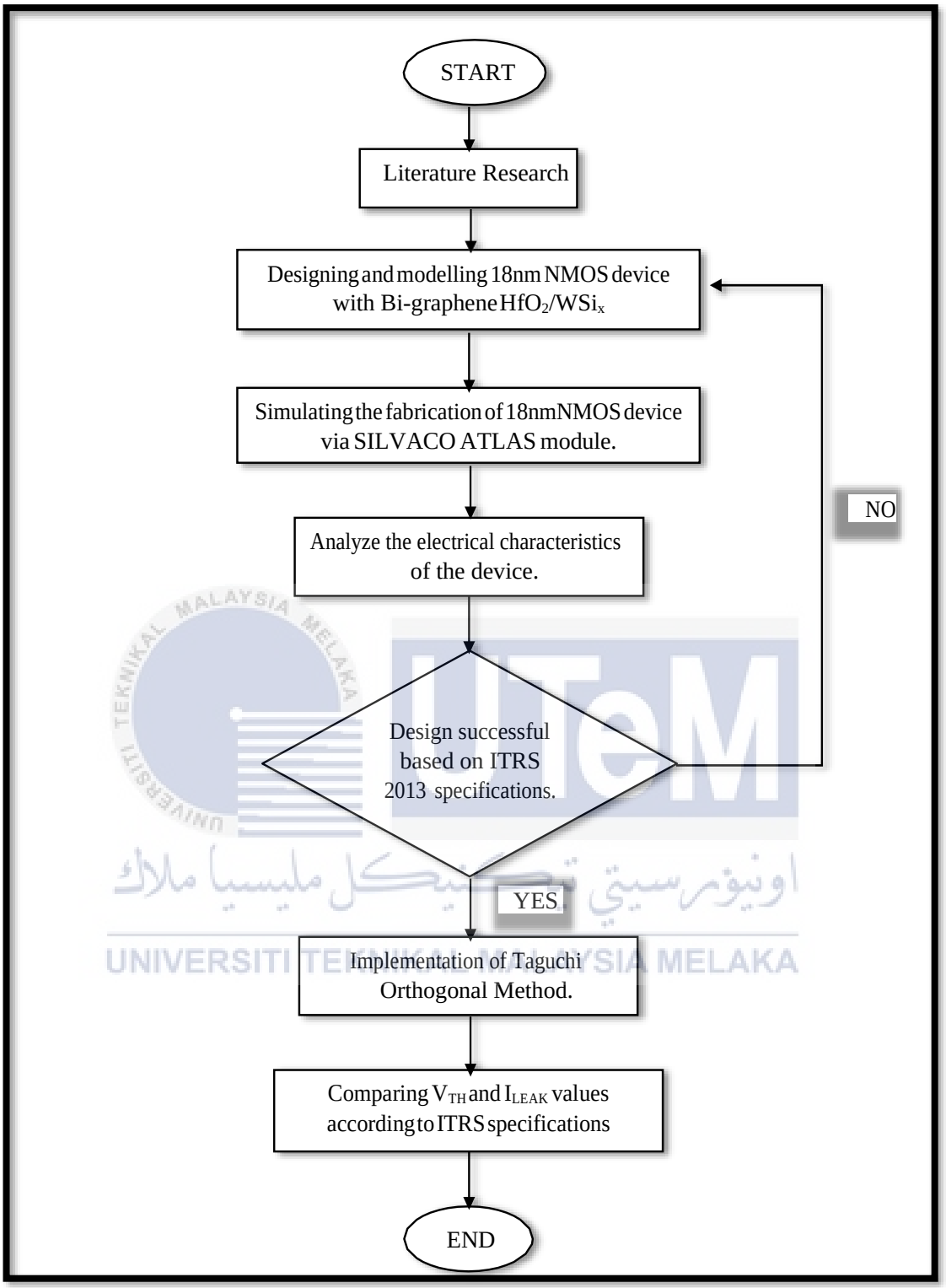


Figure 1.1 Flowchart of project

3.3 Experimental Setup

The ATHENA module was used to virtually fabricate an 18nm bilayer-graphene high-k/metal gate of an NMOS device, and the ATLAS module was used to perform electrical characteristics measurements. This fabrication process contains the same well-matched top-down transistor process flow with a few process parameters such as doping density and annealing temperature to achieve the typical ITRS expectation. Furthermore, the NMOS MOSFET process and device simulations used in the ATHENA and ATLAS modules of the SILVACO TCAD instruments, respectively.

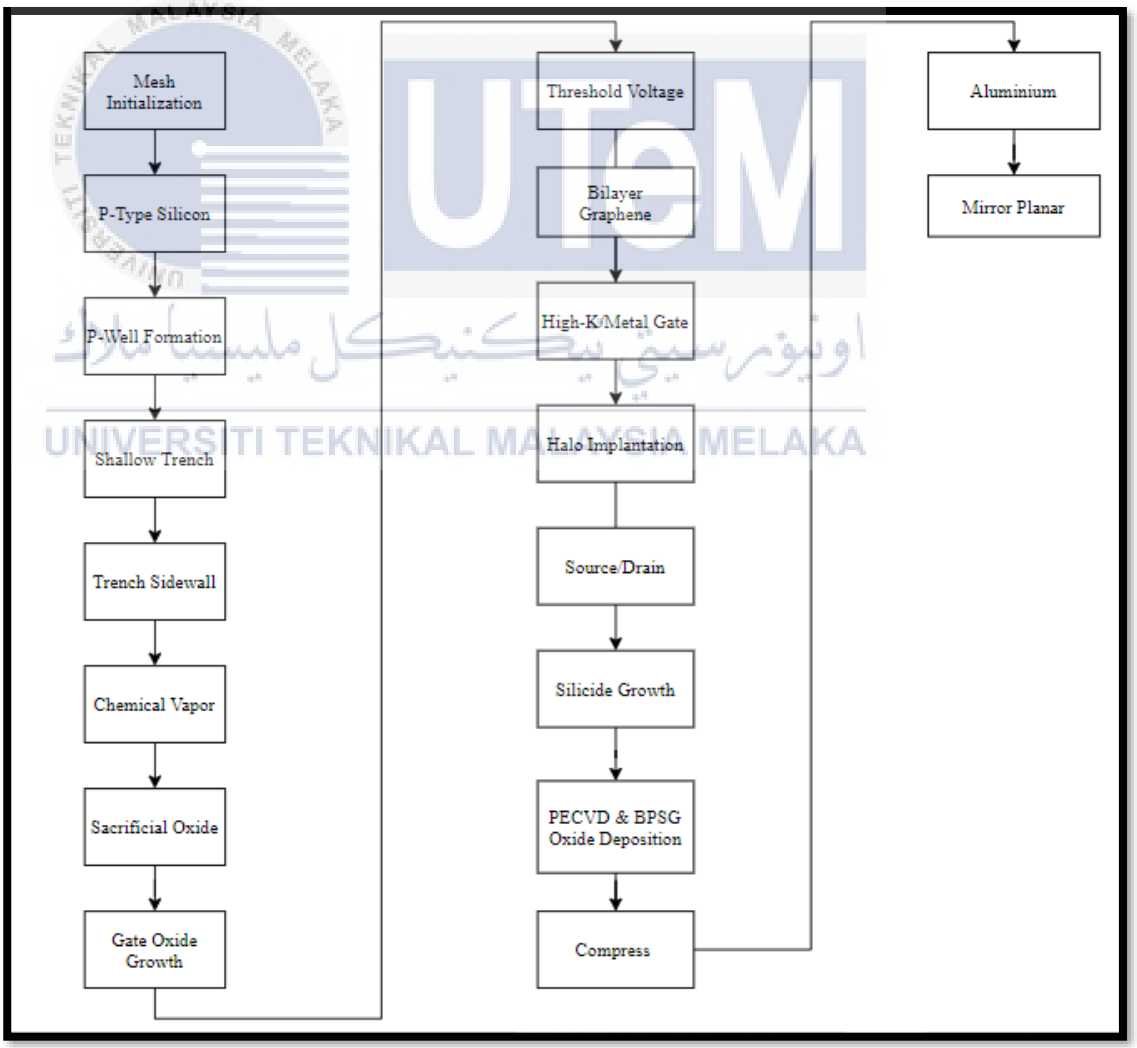


Figure 3.2 Fabrication Step of NMOS

3.3.1 18nm Bi-Graphene NMOS Virtual Fabrication Process flow

The following are the virtual modelling in the Athena module for 18nm NMOS. The original substrate is made up from a p-type Silicon boron where it had been doped with a dose of 7 x 10^{14} ions/cm2 and an orientation of <100> that was prepared as the first step in the fabrication process. The next step is to develop an 200Å oxide screen on the wafers to create a P-well region with 3.75 x 10^{12} ions/cm^2 dose of boron. Next, the silicon wafer will undergo to an annealing process which is at 999℃ in Nitrogen and also in dry oxygen to make sure that the boron is spread evenly in the wafer. Next, a 1500Å thickness of the Shallow Trench Isolator (STI) by etching process to remove the mask and creating it with dry oxygen for about 20 minutes followed by the Low-Pressure Chemical Vapor Deposition Process (LPCVD) and also Reactive ion Etching (RIE) process. After that, a sacrificial oxide layer (PSG) was formed on the top of the substrate layer after the wafer was annealed at 950°C to complete the trench structure. Next, at the temperature of 900℃ for the growth of dry oxygen is completed followed by the threshold adjustment implantation and development of 9.15 x 10^{11} ions/cm^2 dose of Boron Difluoride Bf_2.

In order to have an optimal value for the NMOS transistor, the halo structure had been implanted with and indium dose of 2.857 x 10^{13} ions/cm^2. Next a highly doped bilayer graphene which had been placed on the SiO_2 with a dielectric permittivity of 2.4 and with a thickness of 0.0005µm. This layer will create a smooth path which is due to dopant concentrations for electrons or the holes which will be injected into the channel. The next process is a 18nm gate length of the HfO_2 of a high-k dielectric material which had been deposited on top of the graphene with a permittivity of 25 and WSi_x as a metal gate length also at 18nm which had been deposited on top of 0.05µm in thick layer of HfO_2. The sidewall spacer which had

been developed which had been used as source and drain mask. Here the Arsenic which is source-drain implantation 4.8 x 10^{13} ions/cm^2 with accompanied with 1.75 x 10^{11} ions/cm^2 using the phosphorous. Next step is developing the Borophosilicate (BPSG) with a thickness of 0.015µm layer. After depositing the BPSG deposition, the wafer is been annealed at the temperature of 920℃. On top of the structure, an aluminum layer is deposited to form a metal contact for the device.

Finally, it moves on to the electrical process, which employs the ATLAS to determine the device's leakage current based on the ITRS 2013 prediction.

3.3.2 Taguchi Method to Parameter Design

The Taguchi approach involves minimizing variance in a process by robust design of experiments. The ultimate goal of the strategy is to give a high-quality device to the manufacturer at a reasonable cost. Taguchi developed a method for designing experiments to see how different parameters affect the mean and variance of a process efficiency, which determines how effectively a process works. Because noise factors can't be measured while the product is being used, several studies have been carried out to manipulate the noise factor for variations. The results indicate the best control factor settings for making the process resilient to noise variations. The highest value of the signal to noise ratio (SNR) is determined by the control factor settings that reduce the effect of the noise factor.

There are two types of Taguchi optimization methods. The first uses the SNR to determine control variables that can reduce variability. The control factor that pushes the mean to the target has been identified as having no effect on the SNR. The SNR can be used to measure a variety of noise levels. In this project, nominal-the-

best (NTB) is used to optimize V_{TH} value while minimizing I_{LEAK} by using smaller the-best (STB).

To obtain the minimum of significant data, the Taguchi L9 method is used with the fewest number of tests possible. In order to optimize the experimental design, it uses orthogonal arrays to generate a grid of experiments without overlooking any limitations. The goal is for inventors to be able to successfully understand and analyses the impact of numerous controllable variables on standard quality characteristics and distinctions. Four control parameters and two noise factors were chosen for this investigation based on previous research. As the most persuasive parameters, the V_{TH} and I_{LEAK} variables have been omitted. The control factor and noise factor values for each stage are shown in Chapter 4. Table 3.1 is the control factors table for the L9 Taguchi orthogonal array.

Table 3.1 Standard L9 Orthogonal array

Experiment No.	A	B	C	D
1	1	1	1	1
2	1	2	2	2
3	1	3	3	3
4	2	1	2	3
5	2	2	3	1
6	2	3	1	2
7	3	1	3	2
8	3	2	1	3
9	3	3	2	1

CHAPTER 4

RESULTS AND DISCUSSION

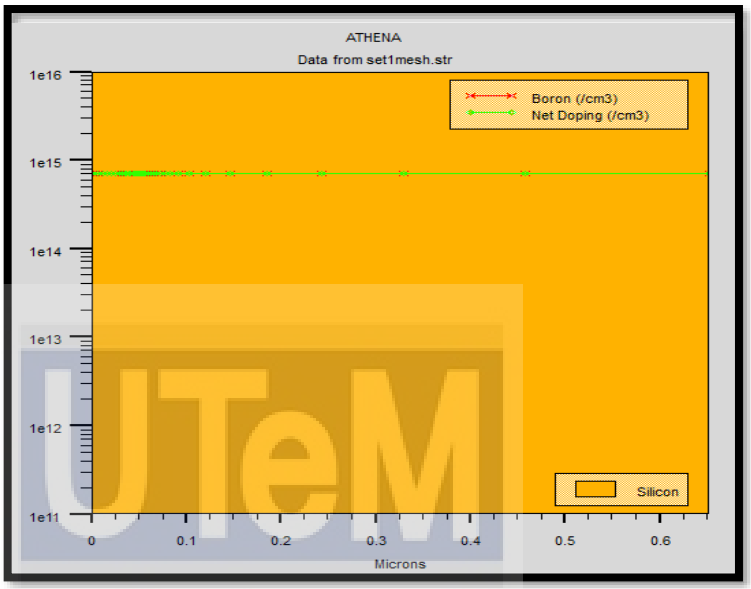
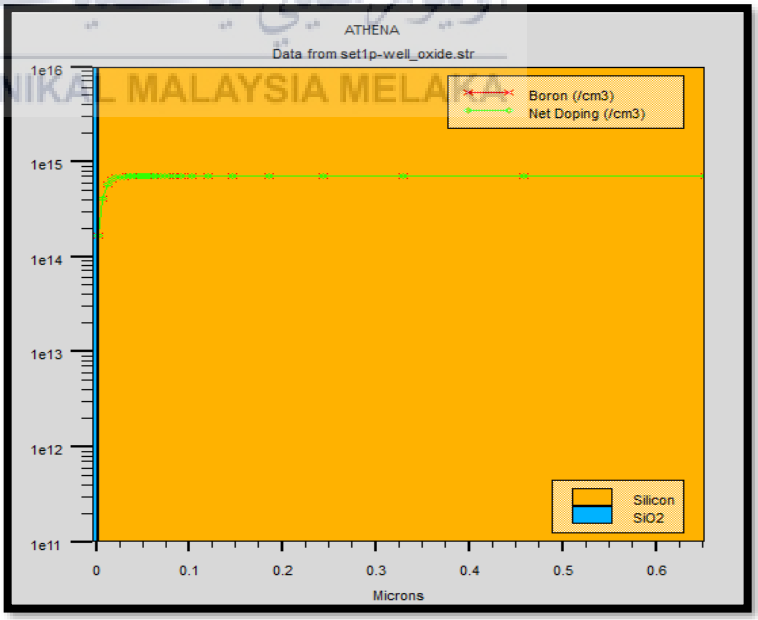
4.1 Fabrication Using Silvaco TCAD Software

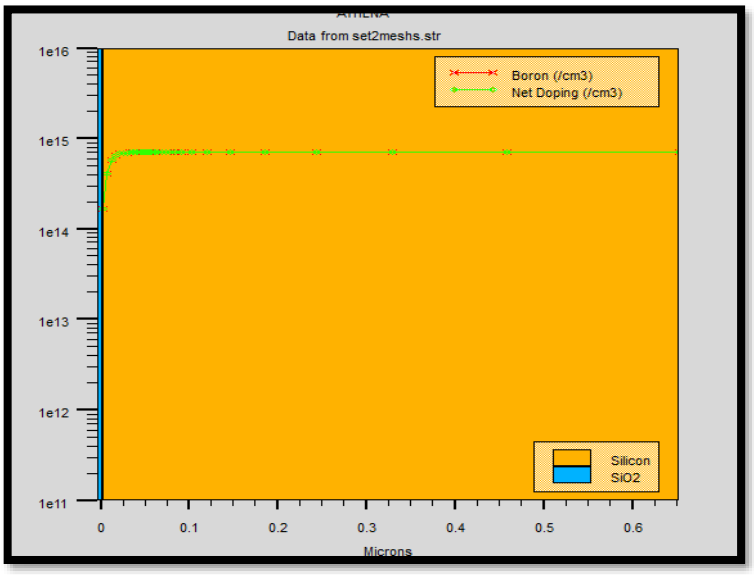
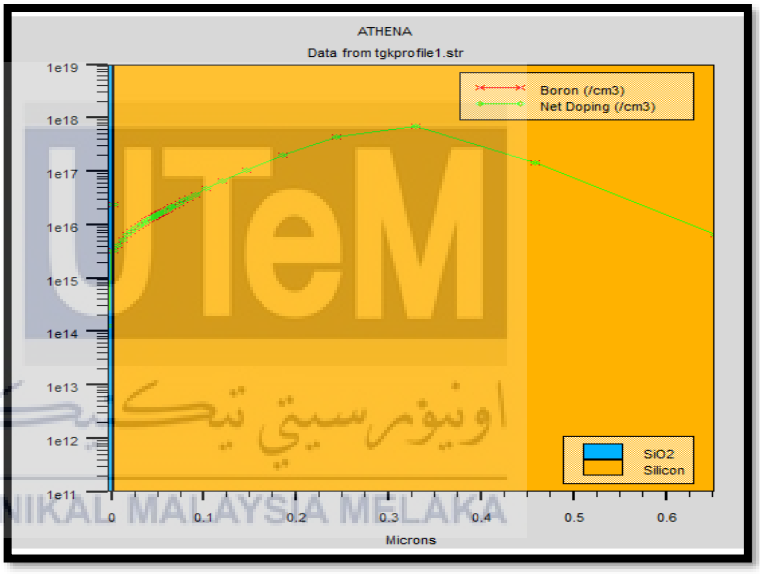
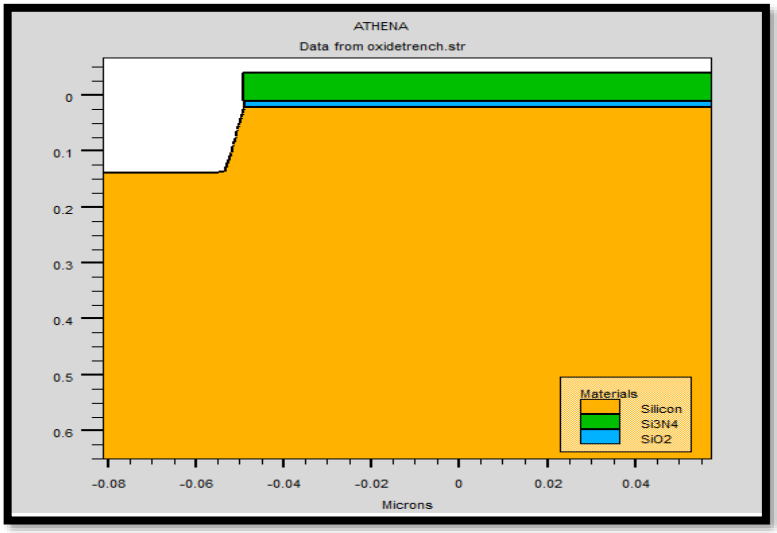
The program that had been used in this project is Silvaco software which consists of two parts which are ATHENA and ATLAS. The ATHENA is a simulator where it provides the general capabilities whereby processing the semiconductor numerical, physically based, two-dimensional simulation. This tool conducts structure initialization and modification, and provides basic deposition and etch features. The electrical characteristics associated with given bias conditions are predicted using ATLAS module [30]. ATLAS is a general ability for physically-based two-dimensional (2D) and three-dimensional (3D) semiconductor device simulation [30].

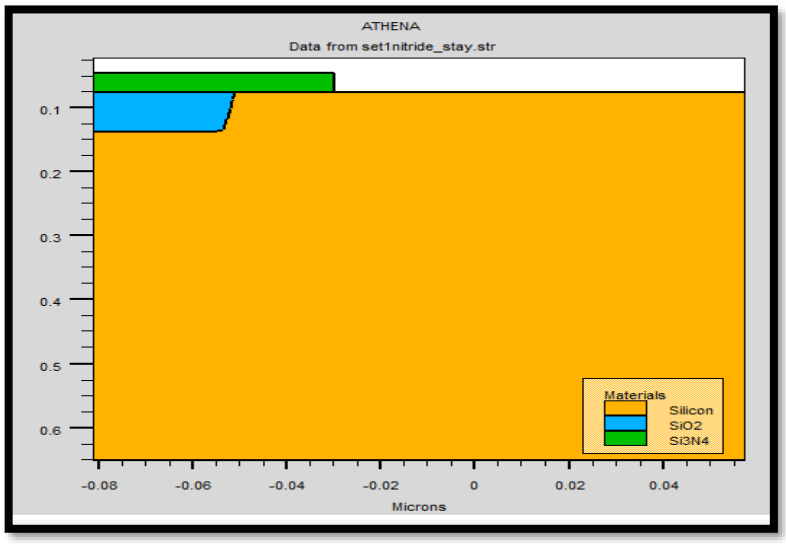
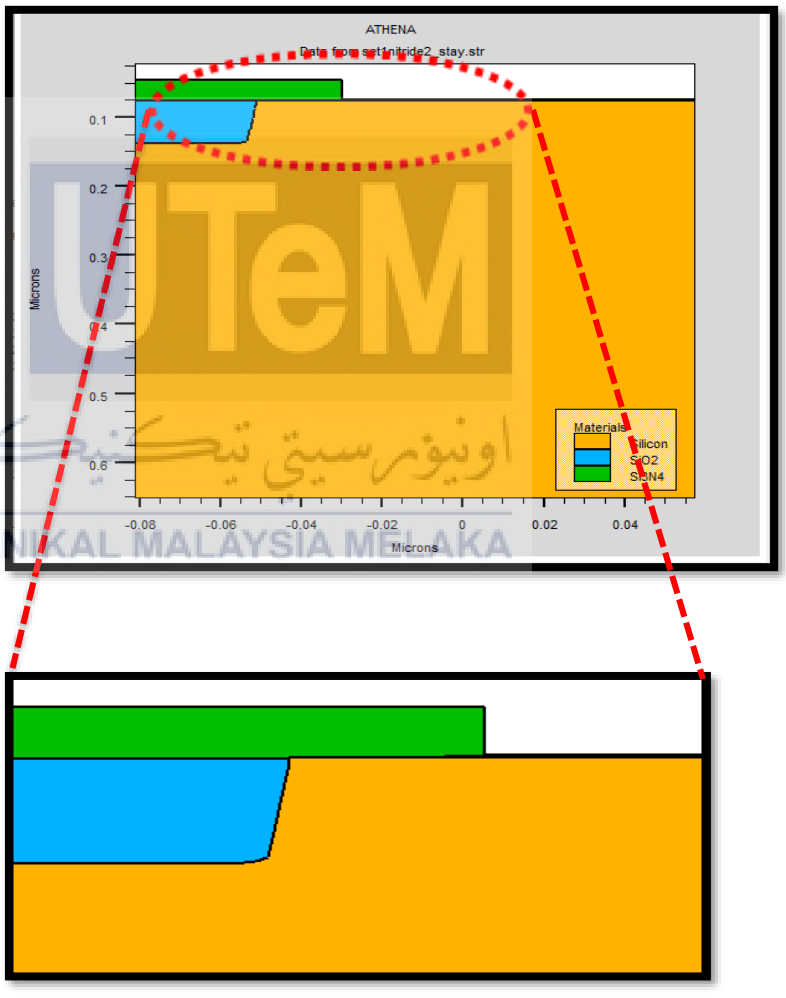
4.2 Virtual MOSFET Fabrication using Silvaco ATHENA

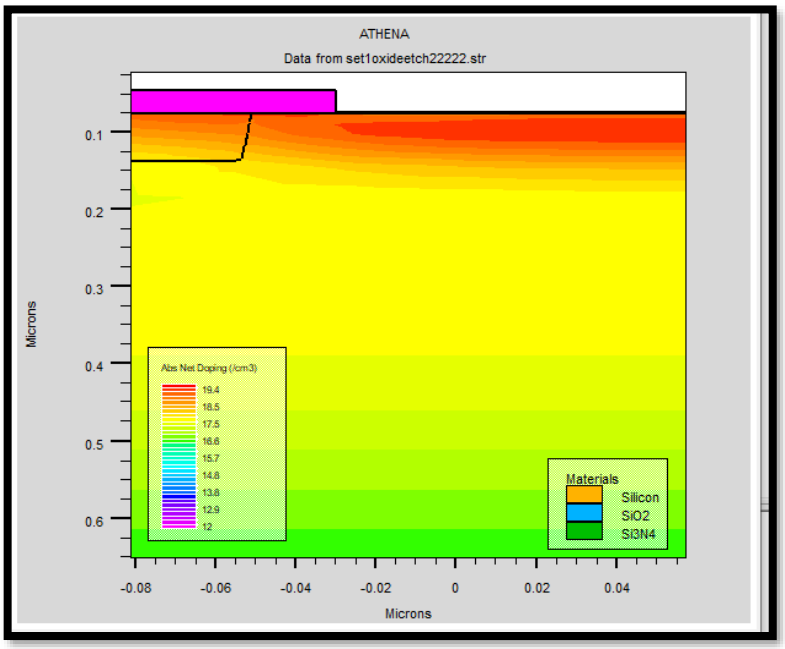
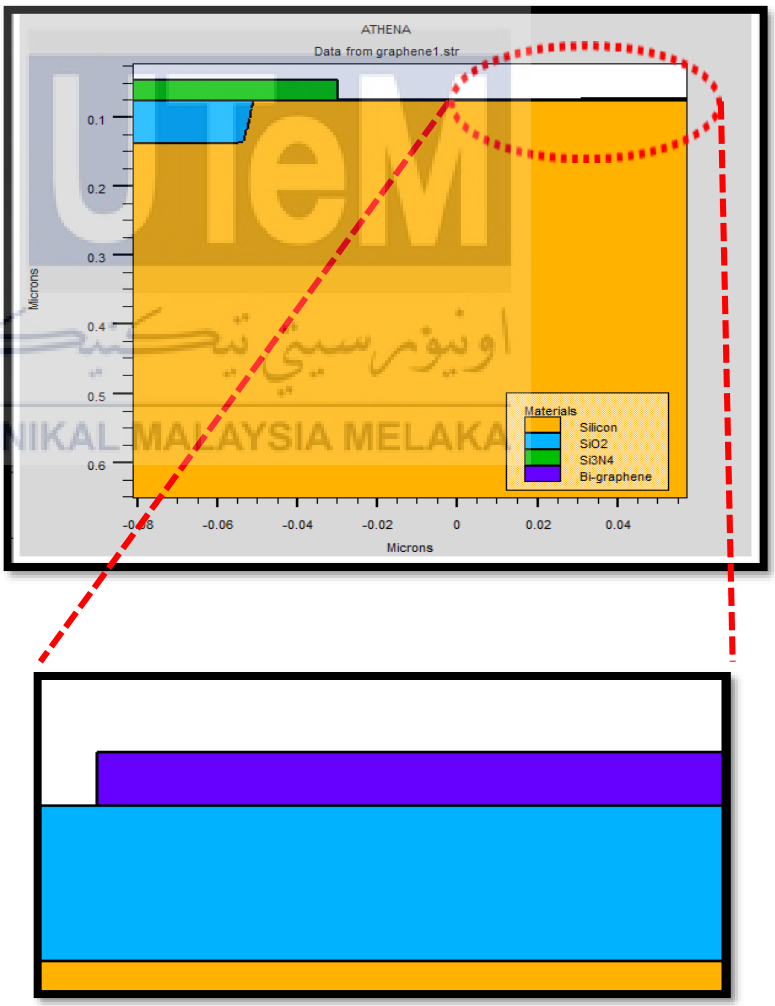
The results of the NMOS transistor fabrication using Silvaco ATHENA are shows below in table 4.1.

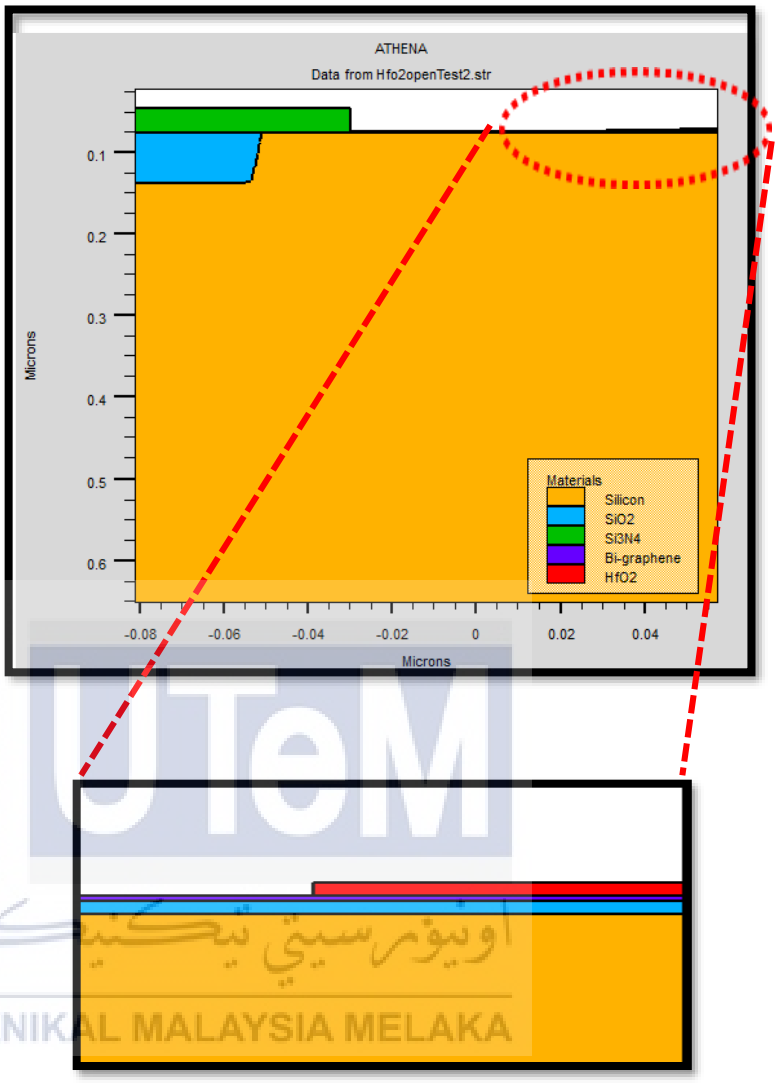
Table 4.1 Fabrication Outcomes

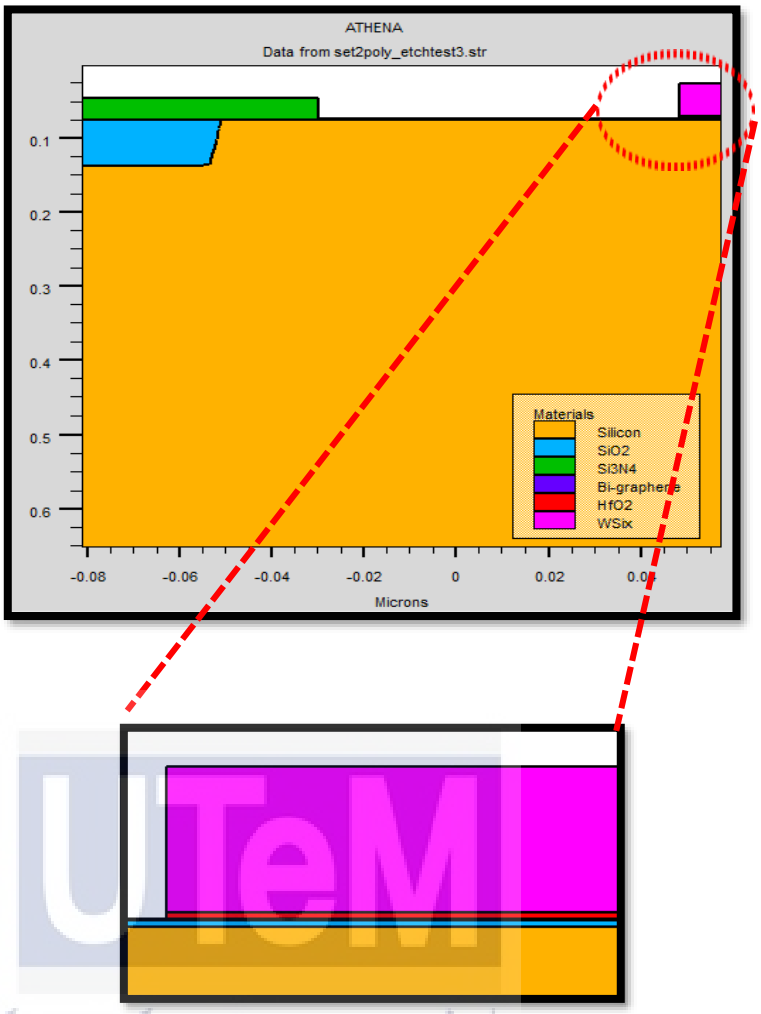
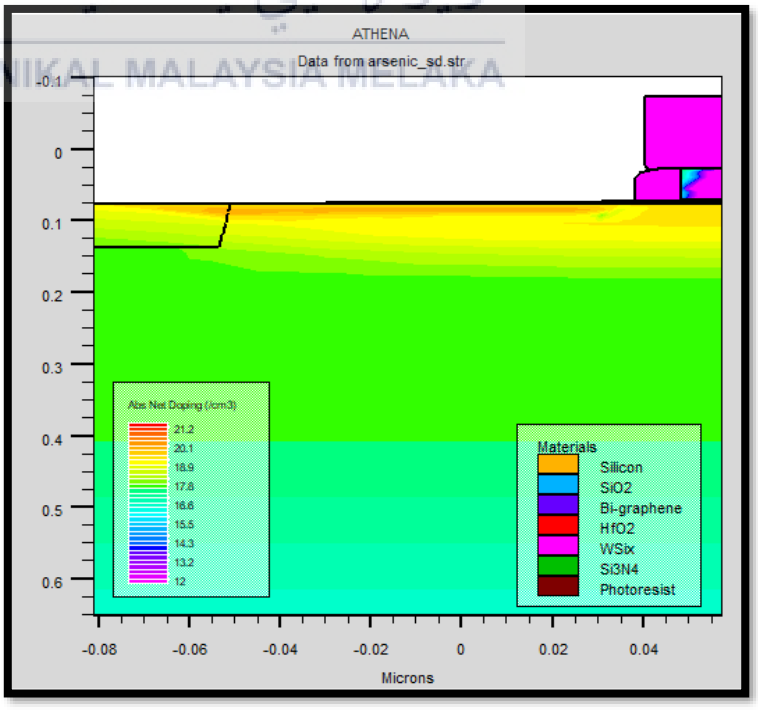
No	Fabrication Steps	Fabricated Figures
1.	Silicon Bulk	
2.	P-Well Implantation	

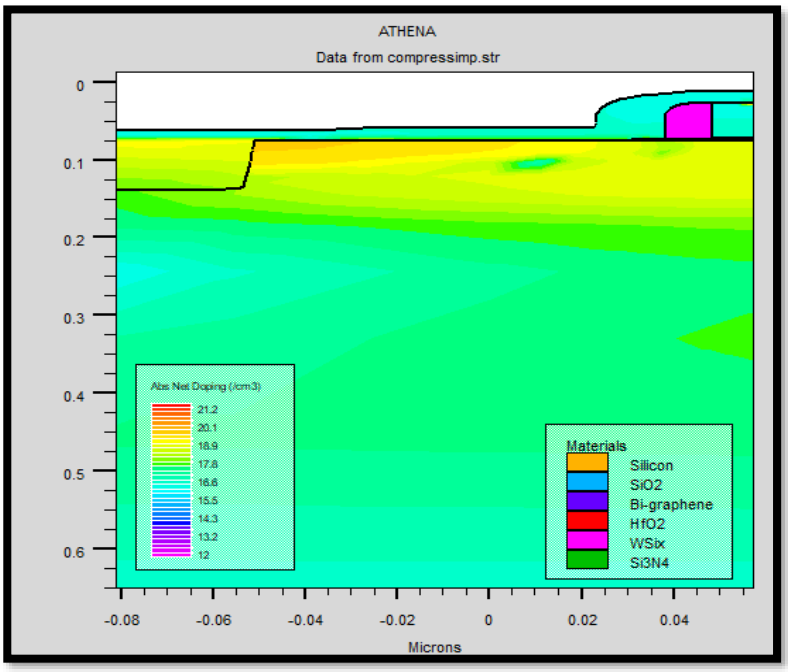
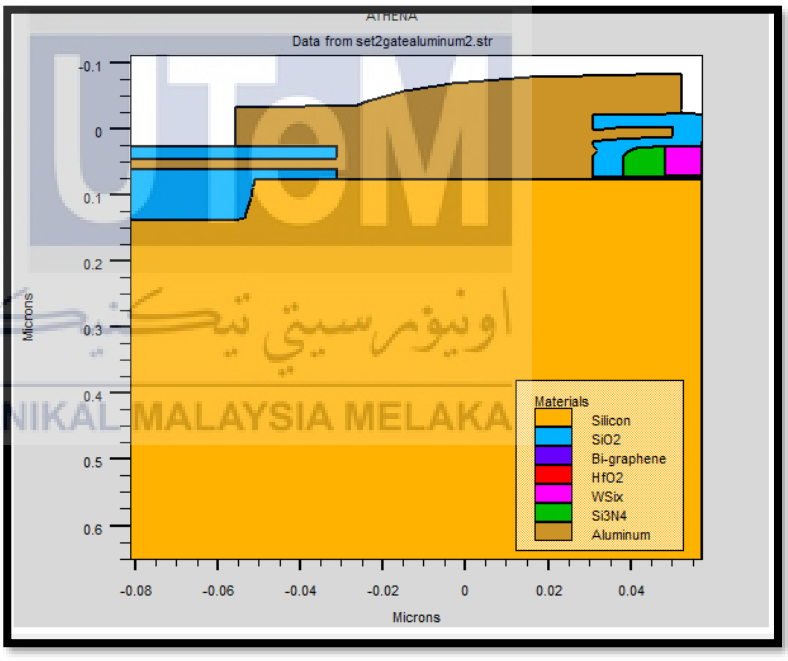
3.	Deposit Silicon	
4.	P-Wells Anneal	
5.	Shallow Trench Isolator (STI)	

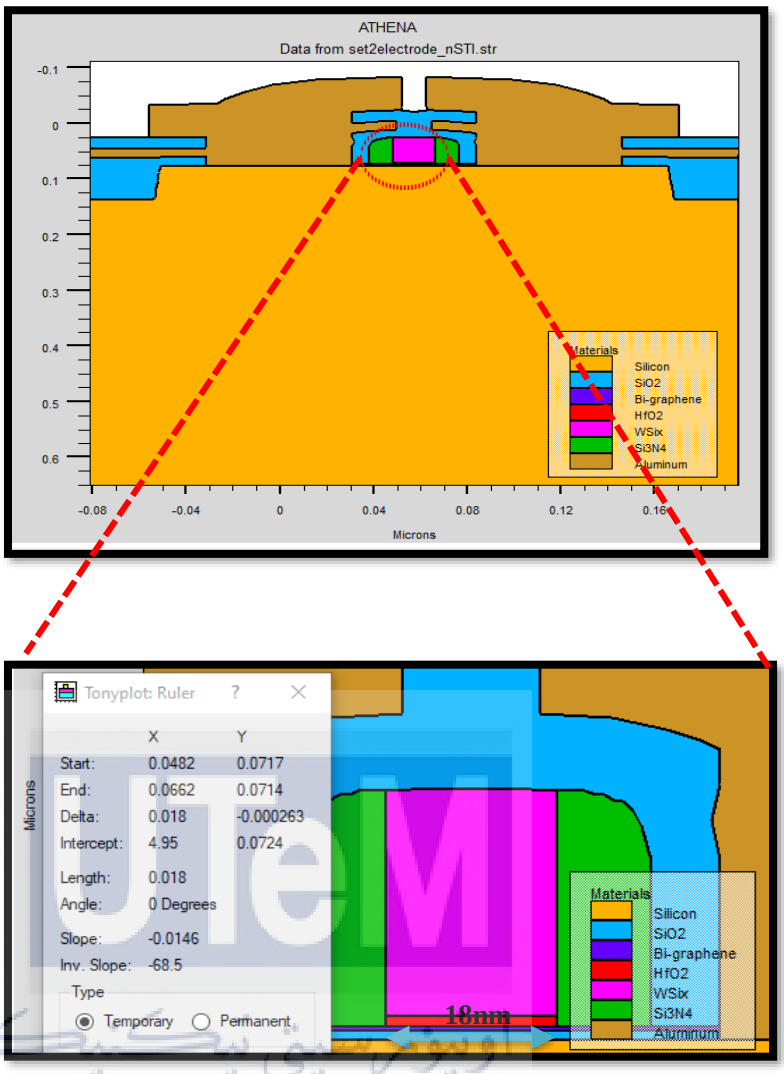
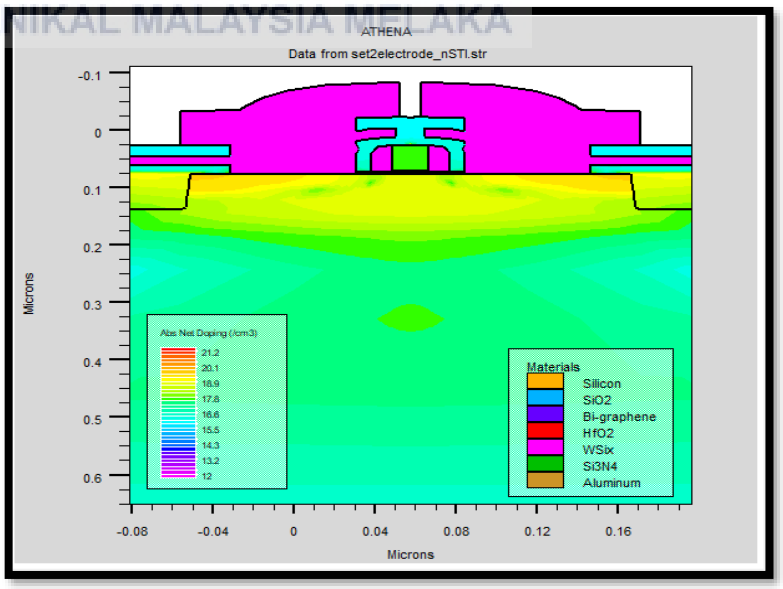
6.	PSG	
7.	Gate Oxide Growth	

8.	Halo Implantation	
9.	Bi-Graphene Deposition	

10.	High-K Deposition	

11.	Metal Gate Deposition	
12.	Source/Drain (S/D) Implantation	

13.	Compensation Implantation	
14.	Aluminum metallization	

15.	Complete 18nm NMOS virtual transistor	
16.	Doping Profile of NMOS transistor	

4.3 NMOS Electrical Characteristics using ATLAS module

From the Silvaco ATLAS, the electrical characteristics and properties of a bilayer graphene NMOS with a planar MOSFET had been achieved. Figure 4.1 shows the I_{DS}-V_{DS} characters curve of the NMOS device. The MOSFET observed at V_{GS} lower than the voltage of the threshold (V_{TH}) which is called as the sub threshold current of drain leakage (I_D) occurs. I_{LEAK} is the I_D measured at the V_{GS}=0 and V_{DS}=V_{DD} (voltage supply) where it is turned off and the and there is no current in the channel. A great MOSFET design comes when the I_{OFF} is 0A. It's crucial to keep I_{OFF} low in order to reduce the amount of static power consumed by a circuit even when it's in standby mode. Leakage currents become one of the key drawbacks that must be considered as the device's sizes are reduced.

The critical parameters of the device's threshold voltage influence the device's performance. The applied gate voltage required to attain the threshold inversion point is known as the threshold voltage.

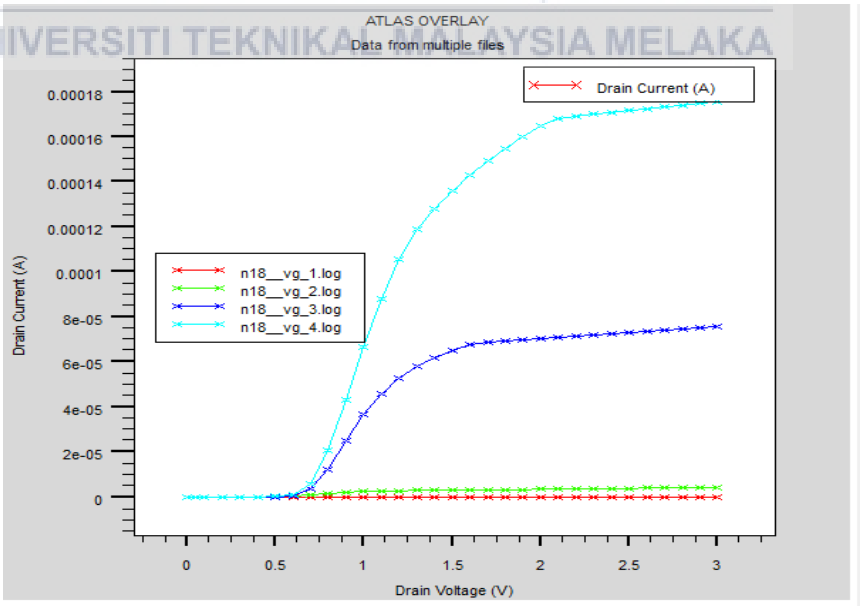


Figure 4.1 I_{DS}-V_{DS} characteristics of NMOS

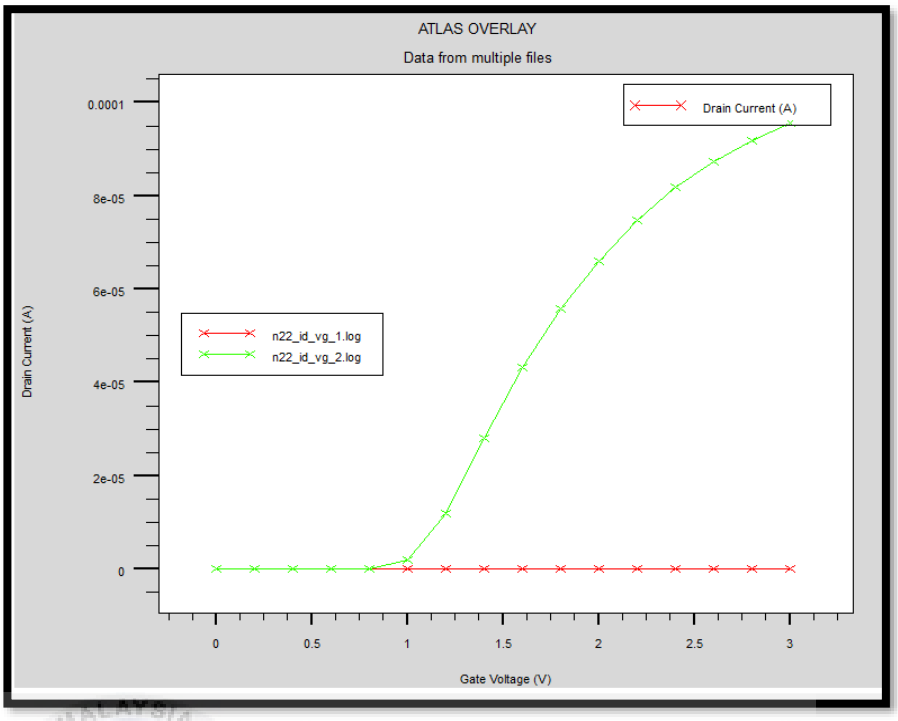


Figure 4.2 I_{DS}-V_{GS} characteristics of NMOS

4.4 Taguchi Orthogonal L9 Array Method

Taguchi orthogonal L9 array technique had been used to construct the four process parameters and each value had been listed in Table 4.2 and Table 4.3 where is consists of two noise factors at various levels.

Table 4.2 Process Parameter

Factor	Process Parameters	Unit	Level 1	Level 2	Level 3
A	HALO Implantation Dose ($\times 10^{13}$)	Atom/cm³	2.797	2.857	2.917
B	Halo Tilting Angle	Degree	33	35	37
C	S/D Implantation Dose ($\times 10^{13}$)	Atom/cm³	4.740	4.800	4.860
D	Compensation Implantation Dose ($\times 10^{12}$)	Atom/cm³	2.333	2.393	2.453

Table 4.2 Noise Factors

Symbol	Noise Factor	Unit	Level 1	Level 2
X	Sacrificial Oxide Layer (PSG) Annealing	°C	950	953
Y	BPSG Oxide Temperature Annealing	°C	920	923

4.4.1 Analysis of 18nm NMOS Device

The L9 array for 36 simulations results of V_{TH} and I_{LEAK} were shown in detail in Table 4.4 and Table 4.5. As the per the results attained, important control factors such as the mean, variance, and signal-to-noise (SNR) process parameters needs to be defined. The control factor is a factor that enhances the NMOS efficiency. The SNR ensures that the design is completely comprehensive to the variances. To achieve the threshold value according ITRS 2013 (0.540V), Nominal-the-best (NTB) SNR used in this experiment for the V_{TH} analysis and performed to calculate the process parameters for each level. Despite its performance features categories, the performance results in a consistent increase and decrease in the SNR value.

In terms of the principle, the maximum SNR is an ideal level of process parameter. The SNR and NTB, η can be expressed as 4.1:

$$\eta = 10 \log_{10} \left[\frac{\mu^2}{\sigma^2}\right] \tag{4.1}$$

Table 4.4 V_{TH} Value Result

Experiment No	*V_{TH} (V)*			
	X_0Y_0	***X_0Y_1***	***X_1Y_0***	***X_1Y_1***
1	0.583714	0.524164	0.583703	0.524158
2	0.494763	0.436044	0.494757	0.436036
3	0.416696	0.391263	0.416693	0.39126
4	0.61359	0.540209	0.613579	0.540203
5	0.512975	0.457181	0.512969	0.457173
6	0.510227	0.454572	0.510221	0.454564
7	0.641542	0.559832	0.641532	0.559818
8	0.643922	0.564004	0.643912	0.563991
9	0.52614	0.473143	0.526134	0.473135

Table 4.5 I_{LEAK} Value Results

Experiment No	*I_{LEAK} (nA/μm)*			
	X_0Y_0	***X_0Y_1***	***X_1Y_0***	***X_1Y_1***
1	6.02514	6.46003	6.0252	6.46009
2	6.75283	7.17902	6.75289	7.17907
3	7.41037	7.7217	7.41041	7.72173
4	5.87695	6.30319	5.87701	6.30325
5	6.59932	7.03998	6.59937	7.04004
6	6.60951	7.049	6.60957	7.04906
7	5.73452	6.14834	5.73457	6.1484
8	5.71652	6.12686	5.71657	6.12692
9	6.46645	6.91536	6.46651	6.91541

The dominant factor and adjustment factor are determined using these 36 analyses. For the SNR of NTB analysis, the dominant factor and adjustment factor are two values that must be studied. The dominant factor, which contributes to a large variation in output response, is said to be the factor with the largest percentage of SNR of NTB. Next, the adjustment factor with the least percentage of factor influence on NTB SNR but the highest percentage of factor effect SNR (Mean). It is a factor that had been used to adjust the output until the output reaches to the nearest targeted value.

4.4.2 Analysis of Variance (ANOVA)

It's a statistical method for separating observed variance elements into multiple components so that additional tests can be performed. Table 4.6, Table 4.7, and Table 4.8 shows the S/N response and ANOVA results for V_{TH} and I_{LEAK} of the device. The dominant factor as well as the adjustment factor were identified through the analyzation, allowing the best optimal value of process parameters that will be determined. According to the observation, A_{sweep}, B_3, C_3 and D_3 are considered the best optimal value of process parameters.

In order to study the optimal process parameter in Analysis of Variance (ANOVA), another analysis is required to conclude the best combination of process parameters. The percentage of the SNR effect factor reflects the process parameter's preference for scaling down the variance. The table is used to identify the dominating factor and adjustment factor in order to discover the best combination of process parameters.

Table 4.6 SNR Response for V_{TH}

Factor	SNR (Nominal)			Total mean SNR
	Level 1	Level 2	Level 3	
A	25.23	23.26	22.90	25.40
B	22.97	22.88	25.53	
C	23.34	23.23	24.81	
D	23.99	22.79	24.60	

Table 4.7 Result of ANOVA for V_{TH}

Factor	Factor Effect on SNR (NTB)(%)	Factor Effect on SNR (Mean)(%)
A	28.85	35.28
B	41.26	52.86
C	14.36	11.54
D	15.52	0.31

Table 4.8 SNR Response and ANOVA Result for I_{LEAK}

Factor	SNR Ratio (Mean)			Total mean SNR Ratio	Factor Effect (%)
	Level 1	Level 2	Level 3		
A	163.21	163.64	164.18	163.33	33.68
B	164.30	163.67	163.07		54.25
C	163.98	163.64	163.42		11.44
D	163.63	163.65	163.76		0.64

From the results, the factor effect on SNR and NTB shows that Factor B (Halo Tilting Angle) with a highest percentage of 41.26% as the most dominant factor as in the V_{TH} as a result from the MOSFET. From here the adjustment factor can be identified as Factor A (Halo Implantation Dose) with 28.85% for NTB and 35.28% of mean. From the observation, it can be distinguished that the highest percentage factor on average and lowest percentage on NTB. Due to the adjustment factor is the halo implantation dose, the range of process parameter values had been varied in accordance for obtaining the threshold voltage that is closer to the nominal value. The optimal dose for the halo implantation dose by sweeping with the value of 2.992 x 10^{13} atom/cm^2.

4.4.3 Optimum Factor Combination

From the analysis, the finalized combination parameters for an optimal threshold voltage for the NMOS are A_{sweep}, B_3, C_3 and D_3 in accordance to the analysis for best combination. Next, the best combination for the I_{LEAK} were A_3, B_1, C_1 and D_3. From the table 4.9 and 4.10, it displays the best predicted setting of process parameter for the combination of V_{TH} and I_{LEAK} through L9 Taguchi method. The final parameters were used to simulate together with noise factor for acquiring the optimal results for V_{TH} and I_{LEAK}, as shown in Tables 4.11 and 4.12.

Next, the final development through the noise factor parameter process, the obtain threshold voltage, V_{TH} were within the ITRS 2013 prediction with the values of 0.540V± 12.7%. By the process combination attained of A_{sweep}, B_3, C_3 and D_3 with X_1 and Y_0 and the obtained value of 0.549704 V which is 1.8% closer to the nominal value that had been obtained. According to the results of the analysis, the Halo Tilting Angle and Halo Implantation dose have the greatest impact on the device's

performance due to local doping concentration near the channel surface, which reduces the V_{TH}. Now the lowest leakage current, I_{LEAK} at X_0 and Y_0 is 5.31801 nA/μm. Table 4.13 shows that V_{TH} and I_{LEAK} After optimization, the values were almost accordant to ITRS 2013 predictions, and the view was improved.

Table 4.9 Best Combination of the process parameters (V_{TH})

Factor	Process Parameter	Unit	Level	Best Value
A	HALO Implantation Dose ($\times 10^{13}$)	Atom/cm³	Sweep	2.992
B	Halo Tilting Angle	Degree	3	37
C	S/D Implantation Dose ($\times 10^{13}$)	Atom/cm³	3	4.860
D	Compensation Implantation ($\times 10^{12}$)	Atom/cm³	3	2.453

Table 4.10 Best Combination of the process parameters (I_{LEAK})

Factor	Process Parameter	Unit	Level	Best Value
A	HALO Implantation Dose ($\times 10^{13}$)	Atom/cm³	3	2.917
B	Halo Tilting Angle	Degree	1	33
C	S/D Implantation Dose ($\times 10^{13}$)	Atom/cm³	1	4.740
D	Compensation Implantation ($\times 10^{12}$)	Atom/cm³	3	2.453

Table 4.11 Final Result of V_{TH} with added Noise

$V_{TH}1$ (X_0, Y_1)	$V_{TH}2$ (X_0, Y_1)	$V_{TH}3$ (X_1, Y_1)	$V_{TH}4$(X_1, Y_1)
0.549709 V	0.501379 V	0.549704 V	0.501372 V

Table 4.12 Final Result of I_{LEAK} with added Noise

$I_{LEAK}1$ (X_0, Y_0)	$I_{LEAK}2$(X_0, Y_1)	$I_{LEAK}3$(X_1, Y_0)	$I_{LEAK}4$ (X_1, Y_1)
5.31801×10^{-9}	5.65861×10^{-9}	5.31805×10^{-9}	5.65867×10^{-9}

Table 4.13 Simulation Results versus ITRS 2013 Predictions

Performance Parameter	ITRS Predictions	Non-Optimized Result	Optimized Result
V_{TH}	0.540 ± 12.7 V	0.5381 V	0.549704 V
I_{LEAK}	20 pA/μm	6.34746 nA/μm	5.31801 nA/μm

CHAPTER 5

CONCLUSION AND FUTURE WORKS

5.1 Conclusion

In this chapter, the project's conclusion had been explained, as well as some recommendations for improvement. A brief explanation of 18nm bilayer graphene with virtual design on HfO_2/WSi_1 and planar NMOS devices and its semi-analytical model is done. The NMOS design that is appropriate for performance analysis and design parameter research. In the L9 Taguchi orthogonal method, halo implantation, halo tilt angle, S/D implantation, and compensation implant were used as the four control factors. The Taguchi orthogonal technique is employed because it’s used to improve the research on the parameter that has the greatest impact on device performance and aids in the optimization of design reliability. In this study, halo implantation dose and halo tilt angle are adjustment and dominant factor respectively. From here it can be seen that a minor change on the dopant value will affect completely

the performance of the device. Finally, V_{TH} and I_{LEAK} results are reliable with the high-performance device requirement according to the requirement of ITRS 2013 prediction.

5.2 Sustainability and Environmental Friendly

In the aspect of sustainability and environmental, this project is always relevant because planar is still being used for sensor applications. This innovation where it does not involve any waste of physical materials, reduce manufacturing costs and also optimize the manufacturing process as by producing a virtual fabrication via the Silvaco software. This also allows to the manufacturers to correct any errors in the device before producing a physical device. Therefore, this becomes a benchmark for electronic designers in designing the transistor. Next, it also helps to have early analysis in the testing and analysis accordance to the device parameters.

5.3 Future Works

When discussing about the future work of research, it is crucial that the MOSFETs with high performance can be made by using metal gate electrodes on a high-k dielectric. With reference to ITRS 2013, this NMOS device is primarily designed to support Low Performance Devices. Furthermore, rather than V_{TH} and I_{LEAK}, it is possible to examine the I_{ON} and sub threshold voltage to increase and optimize the parameters.

By lowering the thickness of the graphene layer to a much thinner layer, the oxide layer beneath it will be removed. By adjusting the high-k/metal gate, the performance of others combined with bilayer graphene will be observed.

Besides, the L18 Taguchi method will be used for the Taguchi method in order to have more precise measurements for the process parameter. Meanwhile, a different process parameter and appropriate noise factors, such as the silicon anneal temperature, might be considered for the noise factor's process parameter and gate oxide growth annealing.

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APPENDICES

APPENDIX A: INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTOR (ITRS 2013)

MG	375	375	375	375	375	375	375	300	300	300	300
I_{off} (pA/μm)[9]											
Bulk	10	10	20	20	50						
SOI											
MG	10	10	10	10	10	10	10	20	20	20	20
$I_{d,sat}$: NMOS Drive Current (μA/μm)[10]											
Bulk	490	459	456	485	422						
SOI											
MG	643	610	618	589	574	556	550	533	537	461	458
$V_{t,lin}$ (V)[11]											
Bulk	0.619	0.639	0.636	0.676	0.647						
SOI											
MG	0.483	0.492	0.492	0.496	0.507	0.507	0.510	0.501	0.507	0.521	0.511
$V_{t,sat}$ (V)[12]											
Bulk	0.528	0.543	0.533	0.540	0.530						
SOI											
MG	0.446	0.453	0.453	0.454	0.461	0.459	0.461	0.447	0.446	0.454	0.453
R_{sd} : Total Parasitic Series Source/Drain Resistance (Ω -μm)[13]											
Bulk	188	179	171	162	156						
SOI											
MG	128	146	130	126	124	117	120	116	112	111	113
Gate Fringing Capacitance (fF/μm)[14]											
Ratio of fringing capacitance to intrinsic	1.1	1.2	1.3	1.4	1.5	1.6	1.7	1.8	1.9	2.0	2.0
Fringing capacitance Bulk/SOI/MG	0.64	0.65	0.66	0.70	0.68	0.69	0.69	0.68	0.68	0.66	0.63
$C_{g,total}$: Total Gate Capacitance (fF/μm)[15]											
Bulk/SOI/MG	1.21	1.19	1.17	1.19	1.14	1.12	1.09	1.06	1.03	1.00	0.95
CV^2 : NMOSFET Dynamic Power Indicator (fJ/μm)[16]											
Bulk/SOI/MG	0.90	0.86	0.81	0.78	0.73	0.68	0.65	0.60	0.57	0.52	0.48
τ =CV/I: NMOSFET Intrinsic Delay (ps)[17]											

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