# MULTI RESPONSE OPTIMIZATION IN STRAINED SI/SIGE NMOS DEVICE USING TAGUCHI BASED GRA

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**This report is submitted in partial fulfilment of the requirements for the degree of**
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# DECLARATION

I declare that this report entitled "Multi Response Optimization in strained Si/SiGe NMOS device using Taguchi Based GRA" is the result of my own work except for quotes as cited in the references.



Signature : .....

Author : Parwathy a/p Yoganathan .....

Date : 11/1/2022 .....

# APPROVAL

I hereby declare that I have read this thesis and in my opinion this thesis is sufficient in terms of scope and quality for the award of Bachelor of Electronic Engineering with Honours. .



Signature : .....

Supervisor Name : PM.DR.Fauziyah binti Salehuddin

Date : 11/1/2022

# DEDICATION

A big thank you and huge love towards my parents, to my supervisor who being my support system through out this project and last but not least to my lovely friends.

# ABSTRACT

This research will present the optimization of strained single gate Si/SiGe NMOS device with statistical Taguchi method together with Grey Relational Analysis (GRA) technique. The solution to overcome Short Channel Effect (SCE)in MOSFET scaling down technology will be explored. The virtual fabrication of the N-Channel Metal Oxide Semiconductor (NMOS) device is simulated by using ATHENA module of SILVACO Techonology Computer Aided Design (TCAD) whereas the electrical characteristics of the device will be performed using ATLAS module of TCAD. The electrical characteristics that will be explored are threshold voltage (VTH), leakage current (IOFF), drive current (ION), current state ratio (ION/IOFF), and sub threshold slope (SS). The process parameter that will be used are halo implant dose, halo implant energy, S/D implant energy and S/D implant dose. Meanwhile, Orthogonal Array (OA) Taguchi method will be used to analyze the signal to noise ratio (SNR) and Analysis of Variance (ANOVA) on the effect of process parameters.All normalised experimental results will be transformed to grey relational grade (GRG), and the process parameter with the highest GRG will be chosen as the best level.According to International Technology Road Map for Semiconductor (ITRS) 2017,the derived optimal level value must match the requirements of low power (LP) technology for the year 2017.

# ABSTRAK

*Penyelidikan ini akan membentangkan pengoptimuman peranti Si/SiGe NMOS menggunakan Analisis Hubungan berasaskan Taguchi (GRA). Penyelesaian untuk mengatasi kesan saluran pendek (SCE) dalam teknologi penskalaan MOSFET akan diterokai. Fabrikasi maya peranti NMOS disimulasikan dengan menggunakan modul ATHENA TCAD SILVACO manakala ciri-ciri elektrik peranti akan dilakukan menggunakan modul ATLAS TCAD. Ciri-ciri elektrik yang akan diterokai adalah voltan ambang (Vth), arus kebocoran (Ioff), arus pemacu (Ion), nisbah keadaan semasa (Ion/Ioff), dan cerun sub ambang (SS). Parameter proses yang akan digunakan adalah dos implan halo, tenaga implan halo, tenaga implan S/D dan dos implan S/D. Sementara, kaedah Orthogonal Array (OA) Taguchi akan digunakan untuk menganalisis isyarat nisbah bunyi (SNR) dan Analisis Varians (ANOVA) mengenai kesan parameter proses. Semua nilai eksperimen yang dinormalkan akan ditukar kepada gred hubungan kelabu (GRG) dan GRG tertinggi parameter proses akan dipilih sebagai tahap yang paling optimum. Nilai tahap optimum yang akan diperolehi mesti memenuhi keperluan teknologi tenaga rendah (LP) bagi tahun 2017 seperti yang diramalkan oleh International Roadmap Semiconductor (ITRS) 2017.*

# ACKNOWLEDGEMENTS

I'd like to offer my heartfelt gratitude to my supervisor PM DR FAUZIAH BINTI SALEHUDDIN for providing their guidance, comments and suggestions throughout this project. Her support and guidance enable me to finish this thesis on time. Next, I would like to thank my parents for giving me space, time and encouragement to complete this thesis without any obstacles. Last but not least, thanks to GOD for giving me a beautiful opportunity to learn on this project.

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# LIST OF ABBREVIATIONS

**ANN** Analysis Neural Network.

**ANOVA** Analysis of Variance.

**DF** Degree of Freedon.

**DIBL** Drain Induced Barrier Leakage.

**GRC** Grey Relational Coefficient.

**GRG** Grey Relational Grade.

**IOFF** Leakage Current.

**ION** Drive Current.

**ION/IOFF** Current State Ratio.

**ITRS** International Technology Road Map for Semiconductor.

**MOSFET** Metal Oxide Field Effect Transistor.

**MSSQ** Mean Sum of Square.

**NMOS** N-Channel Metal Oxide Semiconductor.

**OA** Orthogonal Array.



**S/N** Signal to Noise Ratio.

**SCE** Short Channel Effect.

**SIO2** Silicon Dioxide.

**SNR** Signal to Noise Ratio.

**SS** Sub Threshold Slope.

**SSQ** Sum of Square.

**TCAD** Techonology Computer Aided Design.

**TIO2** Titanium Oxide.

**VTH** Threshold Voltage.

**WSI2** Tungsten Silicide.

# CHAPTER 1

# INTRODUCTION

## 1.1 Background Of Project

MOSFET basically stands for Metal Oxide Semiconductor Field Effect Transistor. It is a type field effect of transistor with an insulated gate that is made through controlled oxidation of a semiconductor which known as silicon.Metal Oxide Field Effect Transistor (MOSFET) has four terminals known (S) source, (D) drain and (B) body or bulk. The source terminal is connected to the body of the MOSFET, forming a three-terminal device which is similar to a field-effect transistor.The body terminal of the device will always be connected to the source terminal that makes the MOSFET to operate as a three-terminal device.Because of its compact size, a MOSFET is commonly referred to as a core or integrated circuit that is developed and produced on a single chip.The MOSFET is classified into two type of operations that known as Enhancement mode and Depletion mode. The formation of MOSFET consists of very lightly doped substrate where it gets diffused with heavily doped region. The substrate that is being used is called as p-type and n-type substrate. The n-channel MOSFET, or NMOS, is a MOSFET with electrons as the majority carrier in the channel.The term p-channel MOSFET or PMOS refers to a MOSFET that fills with holes as the majority carrier in the channel.

In MOSFET technology, scaling of transistor is introduced based on Moore's Law to increase it efficiency by reducing its dimension.According to Moore's Law observation the number of transistors in a closely packed integrated circuit doubles every two year. The scaling of MOSFET causes decrease in IC size without downgrading it and to increase the functionality with the same size. The further scaling of MOSFET improves the power efficiency, improves the transistor performances and reduces the fabrication costs per chip. The gate length reduction in MOSFET provides great enhancement in its operation.

When MOSFET continues its scaling down process, it undergoes some technical challenges and it gets even worse when it comes to nanometer dimensions as it causes Short Channel Effect (SCE) and Drain Induced Barrier Lowering (DIBL) [1]. To address this problem, some improvement and changes in device structure and material are needed to provide higher drive current, faster speed, and lower power consumption. Therefore, the purpose of this project is to optimize the single gate n channel MOSFET by strained the silicon using Taguchi based GRA.Power consumption can be reduced with straining process as it provides higher mobility by allowing the use of lower drain voltage (VDS) and higher threshold voltage while maintaining desirable device speed [2].



Silicon can be easily oxidized as SiO2 with excellent quality as an insulator layer for MOSFET. The electrical properties of transistor is obtained by implementing several input process parameters. The process parameters were optimized using statistical method of Taguchi to obtain the optimal value of electrical characteristics to meet the ITRS prediction [1].The Taguchi technique is a statistical strategy that is changed and standardised based on the experimental design(DOE).The tool used in Taguchi method is the orthogonal array (OA) [1].

Orthogonal Array is the matrix number arranged in column and row.To assess the current variance,the Taguchi uses a generic signal to noise ratio (S/N).The S/N are used as measures of the effect of noise factors on performance characteristics [1].However, the Taguchi method is only limited to the solution of single response and it could be difficult to optimize as it involves more than one process parameters. Therefore,

the Grey Relational Analysis (GRA) method is introduced to optimize multi process parameter variations [3]. The normalized experimental values of L9 Taguchi method will be utilized to compute grey relational coefficients (GRG) and grades to obtain optimized results.

## 1.2 Problem Statement

For over years, the MOSFET industry has keep on consistently scaling the design rules, increasing the chip and wafer, and slowly improving the design of devices and circuits. The scaling down enable the industries has enjoyed the exponential increases in chip speed performance, and decreases in power dissipations and cost of manufacturing. In the process of further scaling down MOSFET into nano scales, the semiconductor industries face some challenges due to its physical limitations that causes degradation of device performances. This causes affect in gate leakage current, drain induced barrier lowering, threshold voltage, subthreshold slope and short channel effect. To overcome this problems, the analyzation on process parameters and electrical characteristics of the device need to explore and carried on [2].

## 1.3 Objective

The objectives of this project are as follow:

1. To design 16nm single gate strained Si/SiGe NMOS device using SILVACO TCAD tools.
2. To analyze the electrical characteristics of strained Si/SiGe NMOS device using SILVACO TCAD tools.
3. To optimize the process parameter of 16nm strained NMOS device using Taguchi based grey relational analysis (GRA).

## 1.4 Scope Of Project

This project focusses on the optimization of strained single gate Si/SiGe NMOS device. The NMOS device is designed with scales down to 16nm using SILVACO TCAD software. During the process, the design will undergo virtual fabrication using the ATHENA module of SILVACO TCAD tool. Then, the ATLAS module will be used to simulate the electrical characteristics of 16nm NMOS. For further optimization process Taguchi method is applied together with Grey Relational Analysis (GRA) to meet the ITRS prediction for high performance achievement.

## 1.5 Thesis Outline

This thesis is divided into five chapters: introduction, literature review, methodology, results and discussion, and conclusion and recommendations for future project improvements.

Chapter 1 of this project gives an overview of background of this project, problem statement related to this research, objectives and scope of project. The main idea of the project will be discussed here.

Chapter 2 of this project presents the literature reivew related to this research. This gives a comprehensive summary of previous researches related to this project. Chapter 3 of this project is about methodology of this research. In this section, the designing of NMOS structure, steps involved, development of the transistor in SILVACO were implemented.

Chapter 4 of this project comprises of results and discussion that need to obtain at the end of the project.This describes the optimization process and the expected results that meet the objective of this thesis. Chapter 5 of this project is the last part of the thesis which is conclusion and future work recommendation that conclude the overall of this project and further future improvement that can be implemented.

# CHAPTER 2

# LITERATURE REVIEW

This chapter explains on MOSFET scaling theories and its related researchers that have done by researchers about this project. This researches help us to get detailed understandings on this project.

## 2.1 Scaling

For more than thirty-five years, the IC industry has undergone an explosive growth and keep steadily its technology on scaling the MOSFET design.This results an increment in the chip and wafer sizes, and cleverly improving the design of MOSFET devices and circuits [4]. As a result, the industry has successfully grows at a rapid rate in chip speed and functionality with exponential decreases in both power dissipation and cost per function over time,as projected by Moore's Law [5]. Scaling is the reduction of MOSFET size in its dimension using VLSI technology [4]. Using Moore's Law in the scaling technology, the performances of MOSFET device such as processing speed, memory capacity and efficiency have been improved greatly. Scaling of MOSFET transistor creates a series of challenges in the process of design the device [4].When the device dimensions of a MOS transistor are reduced, the electrical characteristics of the device change.

Continuous reduction in the size of MOS transistors is limited due to difficulties in device fabrication process. Over the 25 to 30 year lifetime the fabrication process of MOSFET has become very mature. This technology is now well-developed and are widely applied in semiconductor industries as it gives them successful performances. Scaling causes reduction in the dimensions of a MOS device, and makes improvement in the device density and functional capacity of the chip. This enables more number of smaller MOS transistors to be packed into a smaller chip area. The cost of a VLSI chip depends upon the number of chips that can be produced per wafer which makes reduction in overall fabrication cost of the chip. The smaller the MOS transister chip area, the lower the fabrication costs [4]. When transistor undergoes reduction in its dimension, then there will be some changes in its electrical characteristics too.

In the scaling process, the threshold voltage is the most important factor in defining the device's functionality.It should be kept as low as feasible, along with the leakage currents, in order to maximise the device's speed by reducing the time it takes for charge to collect in the channel for a transistor to switch on.As the further down-scaling of the transistor device reaches the submicron regime, the short channel effect problem will arise [6].The charge distribution will be influenced by the short channel effect, which will induce variations in the electric field at the drain and source areas.The short-channel effects are attributed to two physical phenomena which are the limitation imposed on electron drift characteristics in the channel and the modification of the threshold voltage due to the shortening channel length [6]Essential electrical aspects of transistor devices, such as threshold voltage value and transistors' on off-current, will be disrupted due to the non-linearity of the physical and electrical characteristics of the materials used in a device.This adds to the difficulty and complication of obtaining a good Vth value.The leakage current between the source and drain, as well as between the gate and the channel, causes the transistor to be 'ON' even when no voltage is applied to the gate.

## 2.2 Short Channel Effect (SCE)

The MOSFET device seemed to have short channel effect,when the length of the channel gets in the same order of magnitude of the depletion-layer widths of the device's source and drain junctions.When the channel length L is reduced to enhance both the operation speed and the number of components per chip, short channel effect difficulties develop.This short channel effects are assigned to two physical phenomena which is the limitation imposed on electron drift characteristics in the channel and the modification of the threshold voltage due to the shortening of channel length.Polysilicon gate depletion effect, threshold voltage roll-off, drain-induced barrier lowering (DIBL), velocity saturation, reverse leakage current rise, mobility loss, and hot carrier effects are some of the challenges that result from this.

Other than the reformation of VTH, the influence of SCE generated restrictions in characteristics of electron drift within the channel.The gate length is proportional to the concerns on reducing silicon depletion depth and gate oxide thickness.Variations in process parameters effect the acquisition of optimal VTH, driving current (ION), and leakage current (IOFF), as well as SS.However,the difficulties continued in establishing the electrical characterization based on process parameter fluctuations.

Short channel effect causes MOSFET device characteristics be dependent like threshold voltage upon the channel length.The subthreshold slope deteriorates and the drain off current rises as the controllability of gate voltage to drain current deteriorates.Thus,adding high k-material, thinning of gate oxide and using of shallow source/drain junction can be effective ways in preventing short channel effect.Since,the gate has less control over channel depletion due to increasing charge sharing from the source and drain, the absolute value of threshold voltage decreases as the channel length decreases.The drain induced barrier lowering (DIBL) effect, which produces a fall in threshold voltage as the channel length decreases, can be used to explain the short channel effect.When it comes to silicon on insulator (SOI), thin film thickness, thin film doping density, substrate biassing, buried oxide thickness, and processing technique all play a role in the short channel effect (SCE).

## 2.3 Drain Induced Barrier Lowering (DIBL)

Drain Induced Barrier Leakage (DIBL) is a short channel effect in MOSFETs that refers to a fall in the transistor's threshold voltage with increasing drain voltages.The bottleneck in channel formation occurs far enough away from the drain contact in a classic planar field effect transistor with a long channel that it is electrostatically shielded from the drain by the substrate and gate, so the threshold voltage was traditionally independent of the drain voltage.When the drain is close enough to gate the channel in short-channel devices, this is no longer true, and a high drain voltage might open the bottleneck and switch on the transistor prematurely.

Barrier lowering increases as channel length is reduced, even when there is no reverse bias applied to increase the depletion widths.This is because the source and drain form PN junctions with the body that contains associated built-in depletion layers.The effects of DIBL in the subthreshold region (weak inversion) appear as a simple translation of the subthreshold current vs. gate bias curve with change in drain voltage, which may be described as a simple change in threshold voltage with drain bias when channel length is reduced.

However,the gate bias requires larger changes to give impact on drain current as the slope's current vs gate bias is reduced due to shorter lengths.At extremely short lengths, the gate entirely fails to turn the device off. These effects cannot be modeled as a threshold adjustment.In the active state, DIBL changes the current vs. drain bias curve, causing the current to rise with drain bias and lowering the MOSFET output resistance.This increase is not often treated as a threshold adjustment because it occurs in addition to the normal channel length modulation effect on output resistance.

## 2.4 Strain

Strained-silicon devices have been receiving a great feedback from designers in semiconductor industry because of their ability to improve channel mobility and drive current, as well as their compatibility with silicon based processing.MOSFET drive current can be improved with straining process by fundamentally altering the band structure of the channel and can therefore enhance performance even at aggressively scaled channel lengths [7]. Here, the variation in device characteristics of the n-channel strained MOSFET or known as NMOS is provided, while changing the parameter like channel length and Ge content of the device.

After straining effect the results of the simulation verifies the enhanced drain current by decreasing channel length. The straining process happens when the silicon-germanium layer is placed just below the channel region of MOSFET. The figure below shows the cross-section of the nanoscale bulk strained Si/SiGe MOSFET.

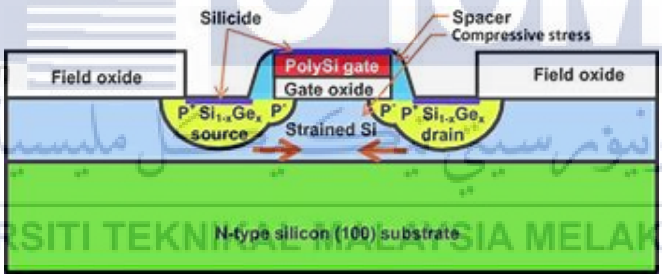


Figure 2.1: Figure 2.1

The low field mobility of carriers (eff) is enhanced due to strain in Si thin films that has been developed pseudomorphically over a relaxed SiGe substrate [8]. The enhanced current drive and transconductance undergone observations in strained-Si device. When a MOSFET dimensions shrink to the nanoscale regime, velocity overshoot became the prominent that related with improvement in current drive in short channel MOSFETs [8]. When the electric field exceeds the saturation velocity for a period shorter than the energy relaxation time it results in electron velocity and causes the electron to approach ballistic transport conditions.

Strain in the silicon thin film also leads to an increase in the energy relaxation time (w) of carriers, this causes an increase in the velocity of overshoot. Hence, the velocity overshoot effect has to be considered for current enhancement in short channel strained Si devices [8]. Straining in the silicon is known as emerging powerful technique in increasing MOSFET performances.

## 2.5 Taguchi Method

The Taguchi method is introduced in optimizing single quality characteristics of process paramaters. The optimization of NMOS device formed using this statistical method by varying the process parameters [9]. This method has been introduced by Dr. Genichi Taguchi and he has proven that it is a valuable tool in various field of engineering. This technique of taguchi is one of the statistical robust tool that allows independent evaluation of the responses with minimum number of experiments. This method utilizes a special orthogonal array (OA) for design of experiment (DoE) and signal to noise ratio (SNR) analysis to predict the most optimal level settings of multiple process parameters. Using this Taguchi method, the experimental results can be analyzed easily through the SNR and analysis of variance (ANOVA) method and determining the significance of the process parameter simultaneously in term of their contribution to the device characteristics. This Taguchi method has been modified for experimental approach and standardized based on design of experiment (DoE). This design of experiment (DoE) has been widely used in industries to improve the product quality for high quality of the device.



Taguchi method uses a special design of orthogonal arrays table in this method.The orthogonal array (OA) has been used in Taguchi method to make the design of experiments (DoE) becomes easier and consistence and requires only a small number of experiments to study the entire process parameter space. Thus, this makes the optimization process of time and cost saved efficiently [3].The design of experiment (DoE) results are transformed into signal to noise ratio (SNR). The higher value of process parameters indicates the better quality characteristics. The signal to noise ratio and analysis of variance method are used in Taguchi method as a performance characteristic to measure the process of robustness and to evaluate deviation from desired values. In this project, orthogonal array were chosen.

Each OA experimental row consists of a single trial with a specific set of control factor levels, followed by all possible combinations of noise factors.The two noise factors will create four set of experimental data that consists of 36 runs.The minimum number of results required for this project analysis is four sets of L9 orthogonal array runs.There will be 36 experiments taken to run and the resulting threshold voltage were recorded accodingly and analyzed.The optimized results from Taguchi's method were then simulated, in order to verify the predicted optimal design.

## 2.6 Taguchi Based Grey Relational Analysis (GRA)

Taguchi method with orthogonal array (OA) offers less experiment runs and simpler design of experiments (DoE), but it is only limited to single response in optimization process. Hence grey relational analysis (GRA) is introduced in Taguchi method as it can solve multi response electrical characteristics.GRA is most commonly used to answer practical problems with a limited number of data.It's most commonly used to estimate the behaviour changes of uncertain systems that don't have a black-and-white answer.Grey relational analysis (GRA) mostly applied in optimizing problems involved multiple factors and response. GRA utilizes normalization of values to compute grey relational coefficients (GRC) and grey relational grade (GRG) [3]. It computes the optimal process level and ANOVA is connected to forecast the optimal level of grey relational grades. The main function of grey relational analysis (GRA) is to determine the relational degree between two measurement sequence by utilizing a discrete measurement approach to compute the distances and to enhance the optimization process of MOSFET.

# CHAPTER 3

# METHODOLOGY

## 3.1 Introduction

This chapter three is all about the overall process development of strained Si/SiGe N-channel MOSFET with 16nm of single gate length. The aim of this project is to design 16nm Si/SiGe N-channel with optimization using Taguchi based GRA. The fabrication on designing the NMOS device is made virtually using SILVACO TCAD software. This SILVACO is the semiconductor technical aided design computer software program that used for creation, fabrication and simulation of semiconductor devices for various applications. SILVACO TCAD contains two module known ATHENA and ATLAS to conduct the semiconductor simulations. Performing a real fabrication process is quite expensive in real time and require a long time. As a result,the ATHENA module is used to design and optimise the structure of N-channel MOSFETs, while the ATLAS module of SILVACO TCAD is utilised to simulate the MOSFET device's electrical characteristics [10]. The structure designing of NMOS is made by writing a coding in deck build of ATHENA module.

The structure analyzation of NMOS will be adjusted or changed according to the requirement in deck build. The ATLAS module plays role in extracting and plotting the electrical characteristics of NMOS structure that undergone the fabrication process. The electrical characteristics includes threshold voltage (leakage current (), drive current (, sub threshold slope (SS) and current state ratio (/). The electrical characteristics parameter can be obtained from the graph from ATLAS simulations. All the parameter that obtained from the simulation must meet the standard prediction of International Roadmap for Semiconductors (ITRS) that can be acceptable by Low Power Technology (LPT) [10].

A comparison needed to make on the extracted electrical parameters versus ITRS prediction to fulfil the requirement. If the extracted parameters are valid from ITRS prediction than the NMOS structure need to undergo optimization process using Taguchi method that comes together with Grey Relational Analysis (GRA). If the extracted parameters are away from the standard ITRS prediction, than the simulation of the structure needed to repeat again till receive the correct values. The Figure 3.1 shows the overall flow process of this project. Since all this process is happening in SILVACO. Hence, the SILVACO working process is shown in Figure 3.2.

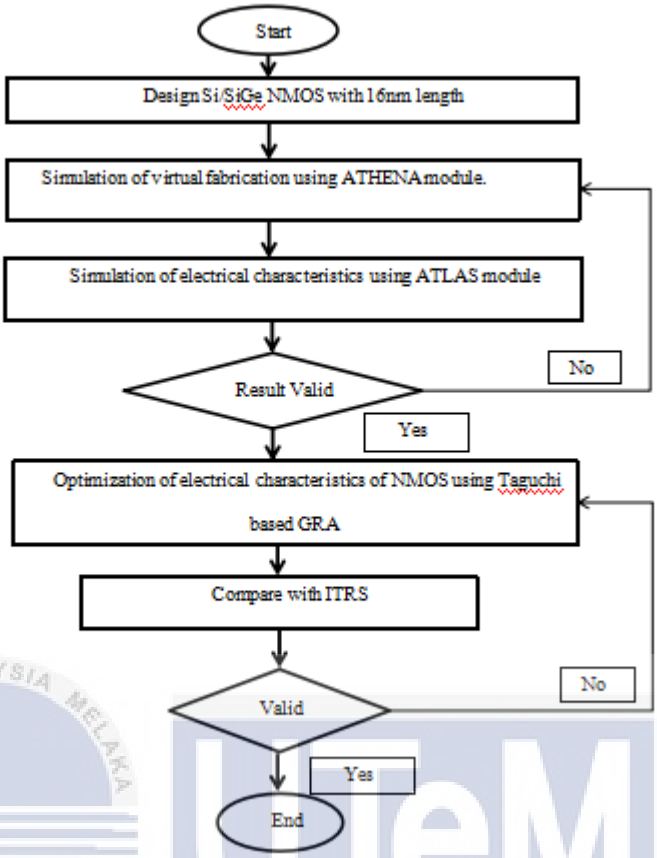


Figure 3.1: Flowchart of the overall project

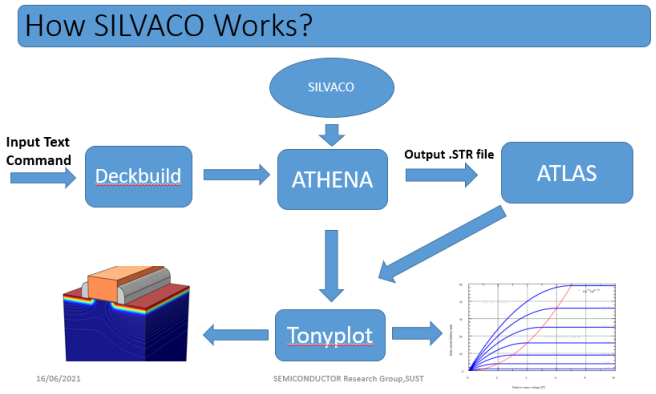


Figure 3.2: SILVACO TCAD flow process

Deck-Build is an initial stage window where coding will implemented to start the designing of MOSFET.It is the graphical user interface (GUI) for the SILVACO TCAD programme,and it allows the user to proceed directly from ATHENA simulation to ATLAS device simulation.Debugging features in Deck-Build include powerful extract statements, GUI-based process file input, line-by-line runtime execution, and understandable input file syntactical error alerts, among others.ATHENA is a framework that combines multiple smaller application designs to create a more comprehensive process simulation tool. It's a modular programme that combines simulations into a more comprehensive package that can simulate a wide range of semiconductor production processes.



ATLAS is a device structure simulation tool that works in two and three dimensions (3D).This module is used to simulate the electrical behaviour of various semiconductor structures and provides insight into the device's internal physical mechanics.The physical structures and doping profiles obtained by ATHENA are frequently utilised in combination with ATLAS.

TONYPLOT is the structure visualization tool in SILVACO TCAD. It has a wide range of features for viewing and evaluating simulator output.The data can be plotted as desired by the user either in one or two-dimensional graphs. When comparing multiple simulation runs,the overlays function comes in handy.TONYPLOT offers animation elements that allow for 12 different viewing sequences when displaying structure solutions as a function of a parameter.

## 3.2 Development of Virtual Fabrication

Semiconductor device fabrication is the process of making chips and integrated circuits, which are found in most electrical and electronic equipment.Silicon is the most often used semiconductor material in this fabrication technique because it has outstanding physical and thermal properties and is considered mature chemistry for fabrication.The manufacture of 16nm strained Si/SiGe N-channels can begin with wafer preparation, well creation, isolation formation, transistor production, and connectivity in the ATHENA simulator.In initial stage, the silicon wafer need to get prepared by getting required material to make the substrate and this includes substeps like epitaxial growth, doping, oxidation, photolithography, diffusion, ion implantation, etching, isolation and metallization [10]. In this fabrication process certain parameters such as energy, tilt, angle, rotation and diffusion temperatures need to be considered as it will cause changes to VTH value and for short channel effect. The Figure 3.3 shows the flow chart of virtual fabrication process.

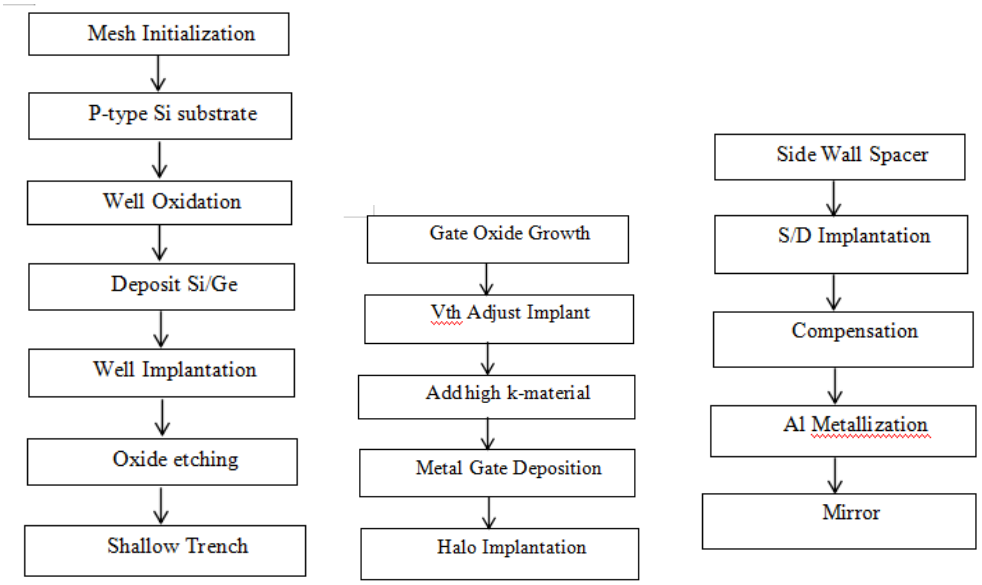


Figure 3.3: Flow chart of Virtual Fabrication Process

During the design and manufacturing process of 16nm N-channel MOSFET mesh grid needed to be specified in ATHENA.The mesh initialization process is crucial in this process since it determines the simulation's accuracy and time.Numerical iterations will be formed on each fine mesh grid and this will create a solution to the differential equations. So, calculations occur at the intersection of mesh points. Hence, finest grid is needed as it will create active surface region for NMOS transistor. Then, the following step in fabrication process is initializing the substrate region by specifying silicon as the material. In this substrate Boron is chosen as background doping for p-type with the concentration about 7.0 x atom/. The orientation that chosen for this substrate is equal to 100 [10]. The Figure 3.4 shows the silicon substrate with boron as background doping.

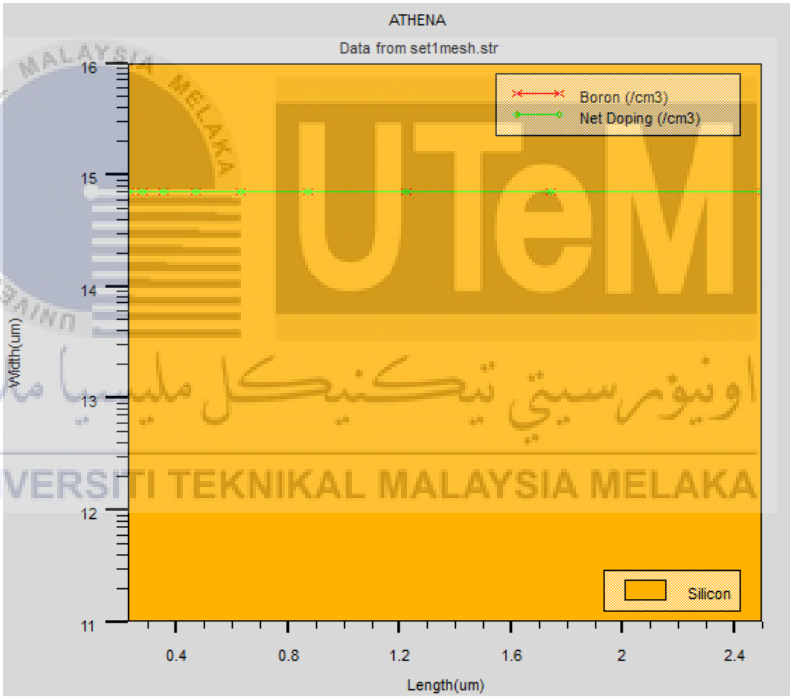


Figure 3.4: P-type silicon substrate

Then well oxidation is done on top of silicon wafer by developing 200A oxide screen using dry oxidation process at temperature of 987°C for 14 minutes. Then silicon germanium is deposited on silicon wafer with the thickness of about 0.025 to form straining effect. The next fabrication process in designing 16nm n- channel is to create a p-well. This process was done using deposition of Boron as dopant with a dose of 3.51 x atom/ with energy implantation of 100keV. Later annealing process take place on silicon wafer substrate at 900°C for 30 minutes under Nitrogen environment. This process used dry oxygen at atmospheric pressure of 1 to ensure the boron atom is spread evenly in the silicon wafer. Then the oxide layer is etched. The Figure 3.5 shows the well implantation process whereas the Figure 3.6 shows deposition of silicon germanium thickness on wafer.

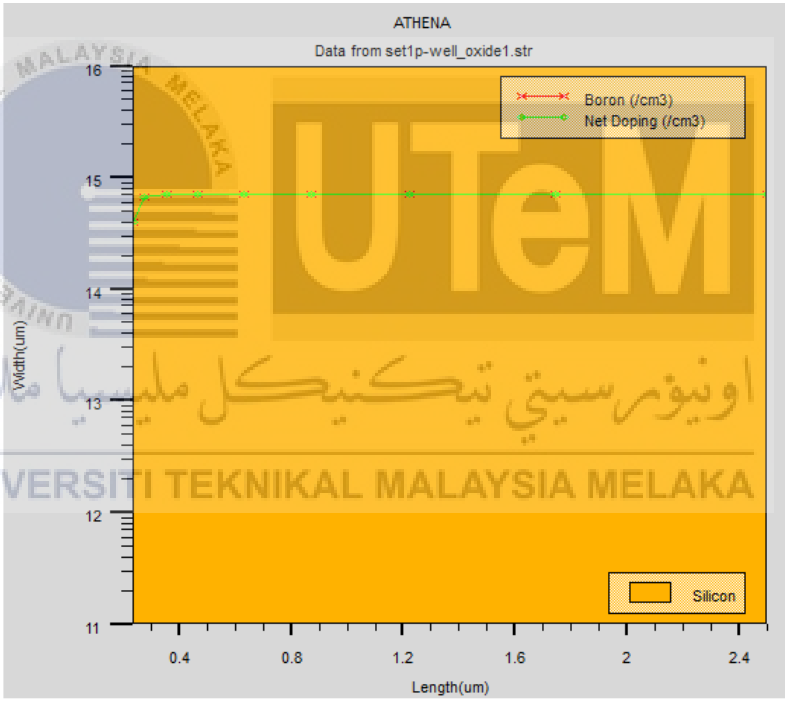


Figure 3.5: Well Oxidation

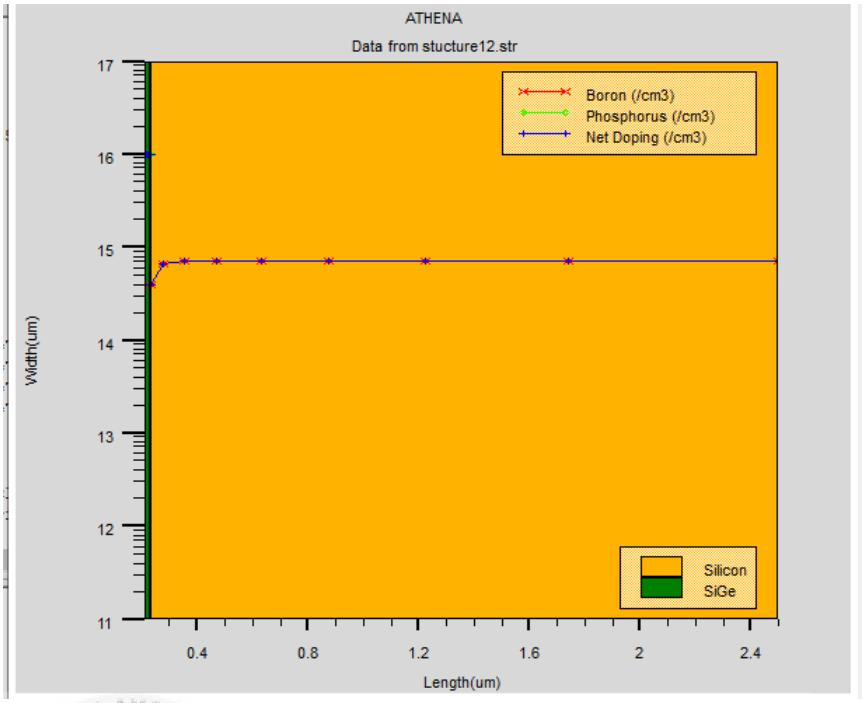


Figure 3.6: Deposition of SiGe

The next process is a shallow trench isolation process.The technique of shallow trench isolation, also known as box isolation, is used to avoid electric current leakage between nearby semiconductor device components.This technique is applied in fabrication process before the formation of transistor. So, the shallow trench isolator (STI) is produced with 1350A thickness of nitride layer on top of the oxide layer. The substrate was oxidized using dry oxygen around 25 minutes with the temperature of 900°C [10]. Mostly dry oxygen is used because of its high quality even though it gives slow process. After that, the gate oxide growth was implemented using dry oxidation with temperature of 812°C for 0.1 min. The Si layer that formed by oxidation prevents diffusion of almost all impurities. The Figure 3.8 shows the 16nm NMOS structure after gate oxide growth.

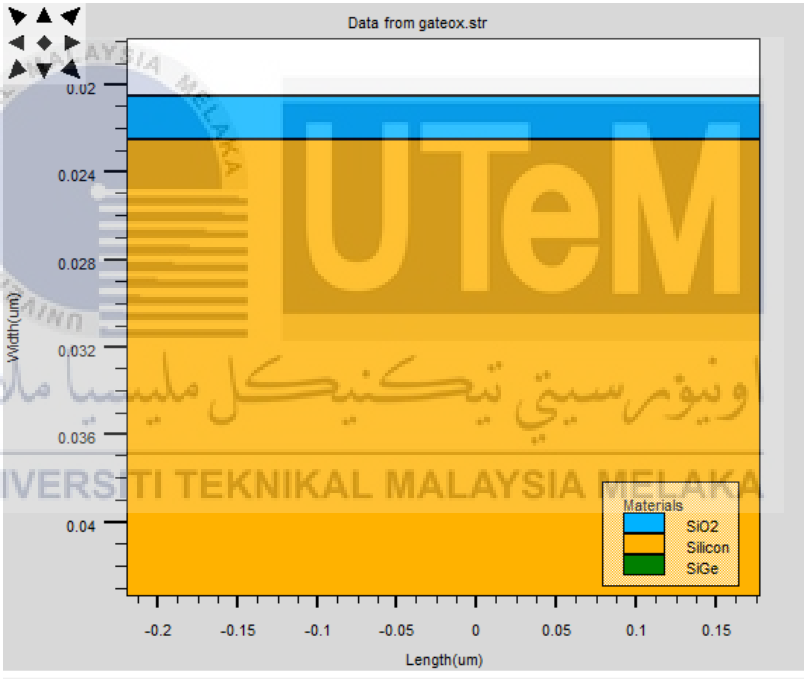


Figure 3.7: Structure after gate oxide growth

The 16nm designing process further continues with threshold voltage adjustment implantation. Threshold voltage control is the most important application in ion implantation process in MOS technology as it is used for an optimization process of an output response. The implantation is done using boron difluoride (B) with dosage of 1.76 x . The energy implant applied for this process is 5keV with tilt of 7° and rotated at an angle of 30° ,120° ,210° and 300°. This underwent an annealing process under nitrogen environment with the temperature of 800° C around 20 minutes.

Next the process continues by adding High k material.Mostly, Silicon Dioxide (SIO2) has been used as a gate oxide material. The thickness of the silicon dioxide gate dielectric has steadily dropped as the size of metal-oxide-semiconductor field-effect transistors (MOSFETs) has decreased, increasing gate capacitance (per unit area) and hence driving current (per device width), improving device performance. Tunneling leakage currents grow dramatically when the thickness scales below 2 nm,resulting in excessive utilization of power and lower device dependability. By replacing the silicon dioxide gate dielectric with a high-capacity material, the gate capacitance can be enhanced without the leakage effects. In this project, the high k material that used is Titanium Oxide (TIO2). Then, the process continues with metal gate deposition of Tungsten Silicide (WSI2) on top of high k material. The Figure 3.8 shows the high k material process and Figure 3.9 shows structure after metal gate deposition.

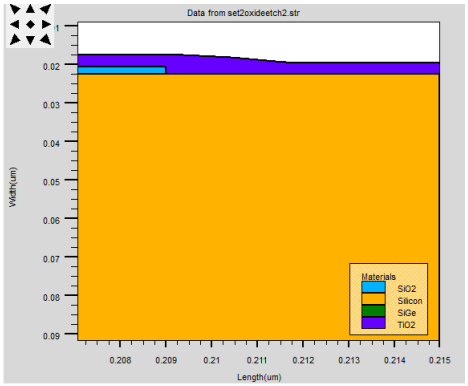


Figure 3.8: Structure after High k material

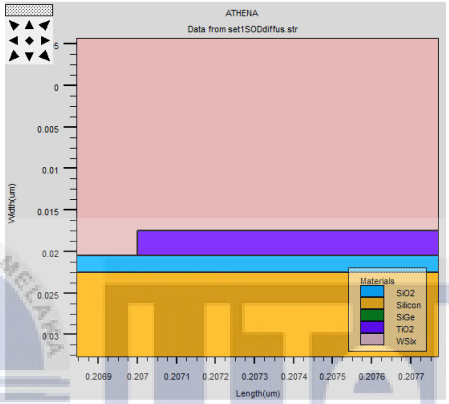


Figure 3.9: Structure after metal gate deposition

Next, Halo Implantation process continued in designing n-channel for an optimum device performances.In the fabrication process, halo implantation is employed to reduce the punch through effect [11].This implantation is done using indium with dosage of 2.7 x . The implantation is done with energy of 170, tilting of 24 and rotation angle of 25°, 115°, 205° and 295°.The top surface of the silicon layer will next be exposed after a nitride layer is placed on top of the metal gate and etched.After that, source and drain regions were constructed at the sides of each metal gate.For source and drain implantation, side wall spacers were used as a mask.The Figure 3.10 shows structure after halo implantation process.

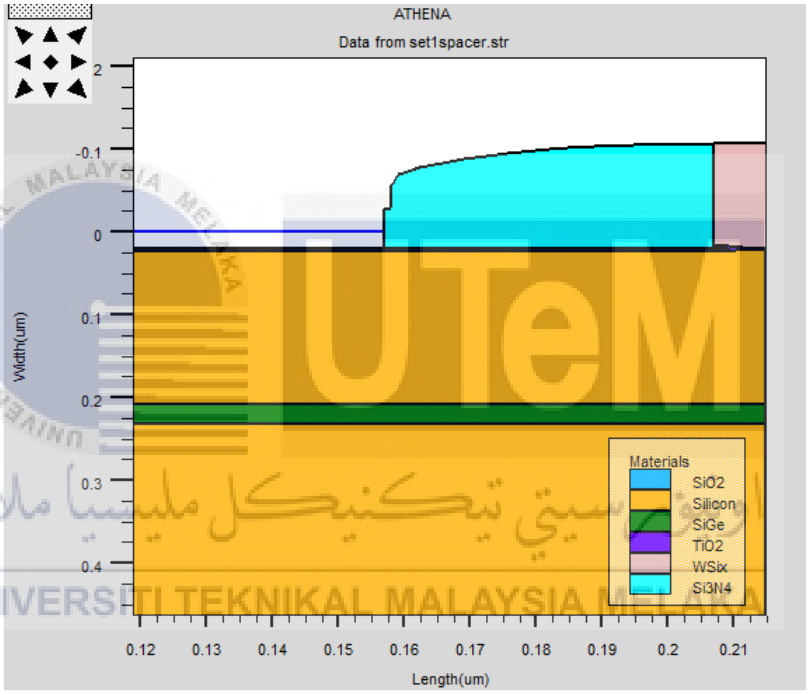


Figure 3.10: Structure after Halo Implantation

Then the NMOS structure continued begin with source and drain implantation process with an arsenic dose of 9.85 x . Following that,phosphorous at a dose of 1.0 x is added to ensure a smooth current flow in the device.After that, diffusion take place around 10 minutes for 900°C under nitrogen environment. Figure 3.11 shows structure after source and drain implantation.

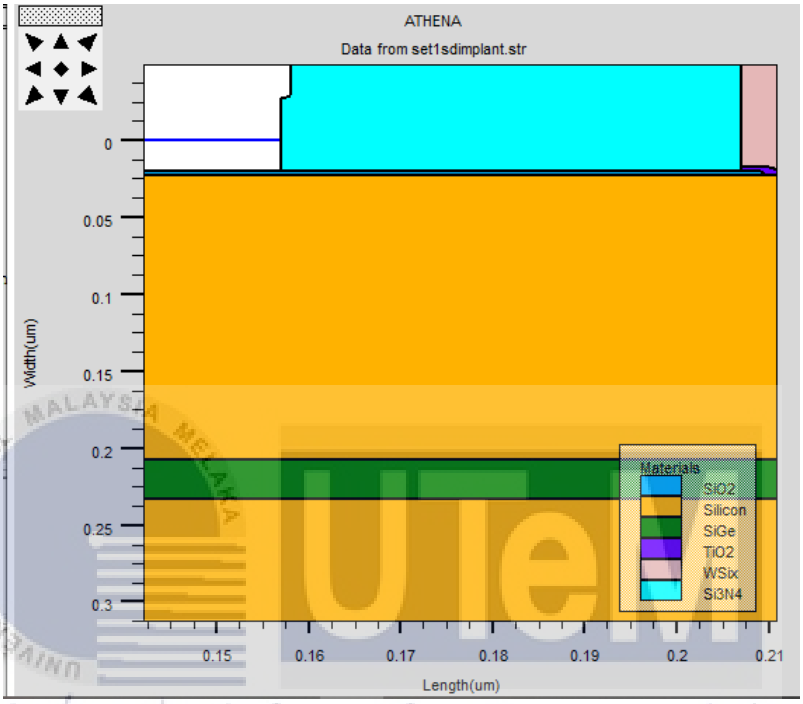


Figure 3.11: Structure after Source Drain Implanatation

The following step involves compensating implantation with phosphorous at a dose of 4.03 times, an energy level of 63 keV, and a tilt of 7 degrees.This procedure is used to reduce the parasitic impact, which could cause the current to drop [12]. Then, on top of the structure, an aluminium layer was deposited and etched to make the metal contact for the source and drain.At this process,the NMOS is complete and to get two dimensional view mirroring process should take place. Figure 3.12 shows the structure after compensation process. The Figure 3.13 shows the structure after aluminium metallization whereas the Figure 3.14 shows the complete structure after mirror.

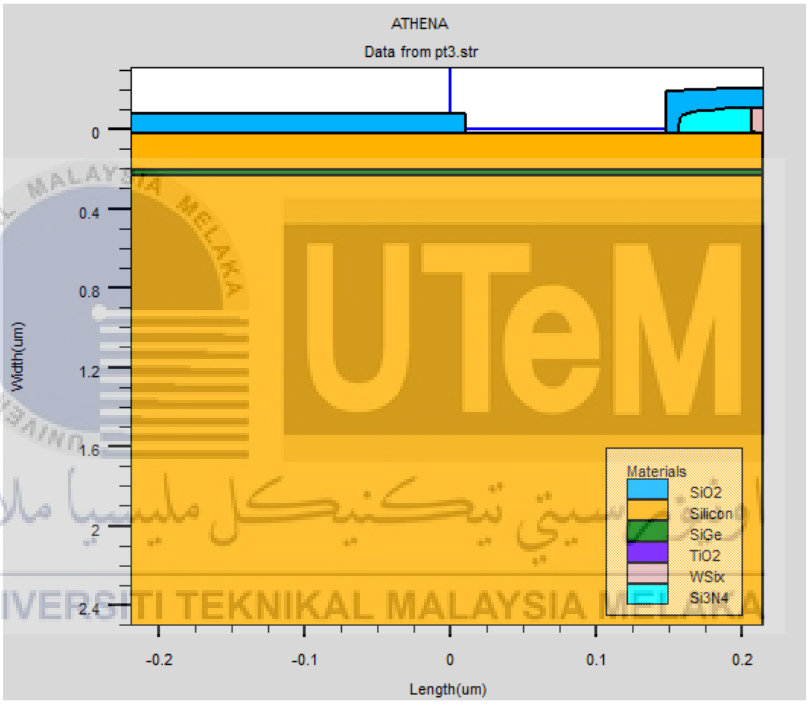


Figure 3.12: Structure after compensation process

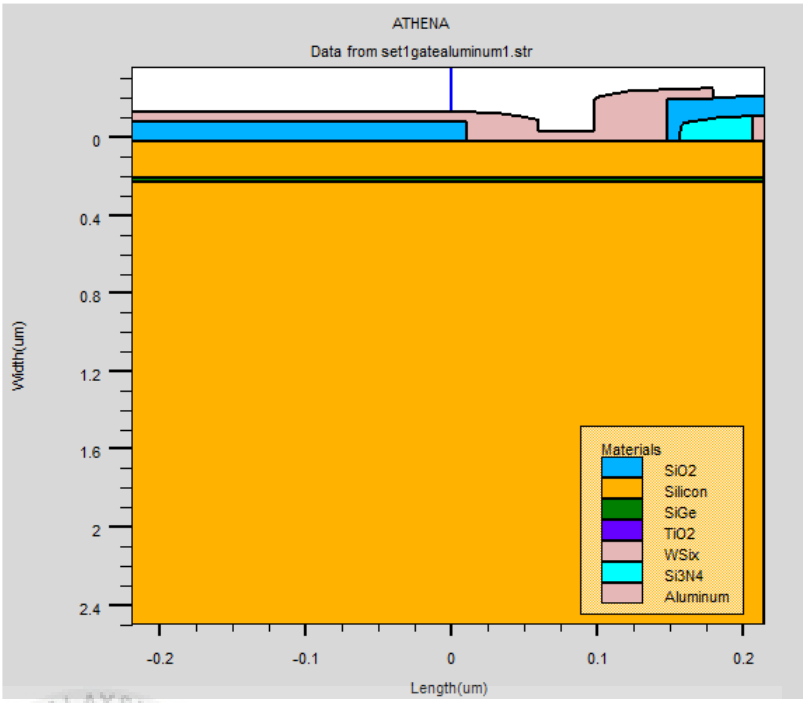


Figure 3.13: Structure after Aluminium Metallization process

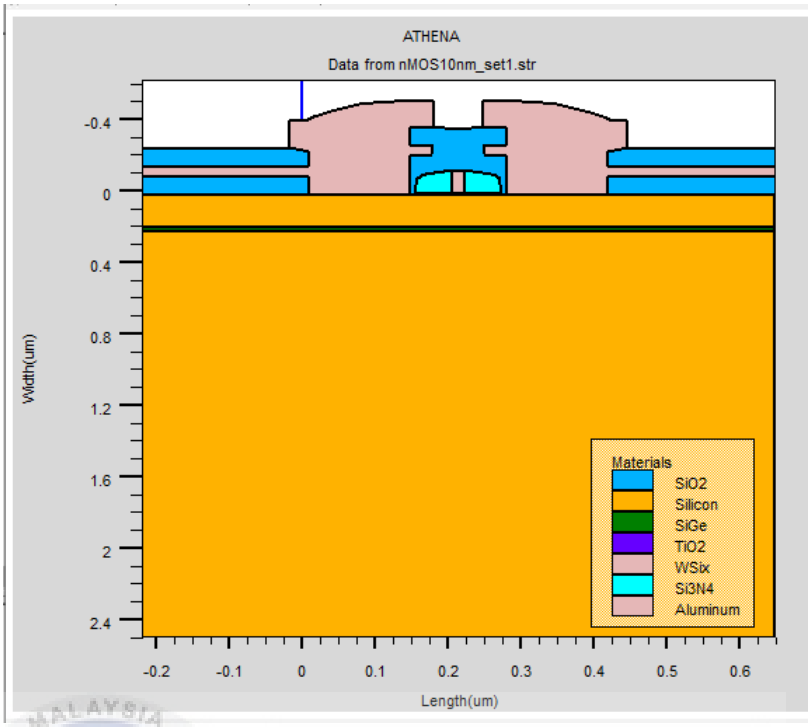


Figure 3.14: Complete 16nm NMOS structure after mirror

## 3.3 Electrical Characteristics Simulation using ATLAS Module

The designed NMOS strcuture will be used in ATLAS module to simulate the electrical characteristics. From here, the Id versus Vgs and Id versus Vds curves will be generated. The extraction of electrical characteristics like threshold voltage(Vth), drive current(Ion), leakage current(Ioff), current state ration(Ion/Ioff) and subthreshold slope(SS) for 16nm NMOS structure will take place in ATLAS simulator.

## 3.4 Taguchi Optimization Method

Variation in fabrication process parameters (factor) is now one of the most important aspects of future technological scalability. Because this is a follow-up to our earlier experiment,four processes were investigated in earlier studies.The variables were chosen to investigate the influence of variability. In this case,three levels of each element were studied, as well as two noise factors [10].To fulfill the L9 orthogonal array,two new levels were added.The structure of orthogonal array analysis.There were 36 experiments in total.To complete the variability, a combination simulation is done [10].Taguchi Method's recommended approach, and lastly to find the best amount of process parameter combination in 16nm NMOS device was designed.Halo implantation dose,Halo implantation energy,S/D implantation dose and S/D implantation energy were the process parameters investigated in this experiment.The noise factors were the annealing and nitride temperature.To obtain a more realistic design, the noise factors were added.Designing the experiment with an orthogonal array could help the designers quickly and cost-effectively study the influence of multiple controllable factors on the average of quality characteristics and variations, while analysing the experimental data with a signal-to-noise (S/N) ratio could help the product or manufacturer's designers quickly find the best parametric combinations [10].There are three types of performance qualities to consider when looking at the S/N ratio: the lower-the-better, the higher-the-better,and the nominal-the-better.

The S/N ratio for each level of process parameters is obtained using the S/N analysis.The figure shows the flow diagram of taguchi method of optimization.The higher the S/N ratio, regardless of the performance characteristic category, the better [13] [14]. As a result, the largest S/N ratio is the ideal level of process parameters.The second criterion is to use the analysis of variance (ANOVA) result to establish the design's dominating factor. The largest percentage of factor effect on variance in an ANOVA study implies that the factor is a dominating factor, resulting in the most sensitive effect and biggest influence on process variation [14]. As a result, the dominating factor's variability must be treated seriously.Finally, once the process parameters have been set, the selected level from the analysis will be simulated again with respect to the noise factor in order to create the best design possible. The figure shows the flow diagram of taguchi method.

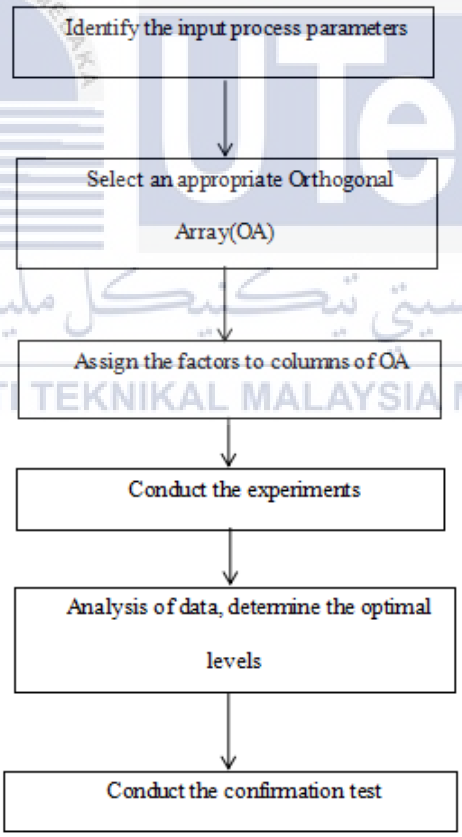




Figure 3.15: Taguchi flow diagram

Since, taguchi method is only limited to single response characteristics, grey relational array(GRA) technique is applied in taguchi method for multi response optimization process.GRA was used to explore a number of the device's electrical features. The GRA approach converts the device's many electrical characteristics, such as ION, IOFF, and SS, into grey relational coefficients (GRC).All electrical characteristics acquired from the Taguchi method's L9 OA are first normalised in the range of 0 to 1.The Grey relational analysis (GRA) method consists of three main steps that includes the data pre-processing, locating the grey relational coefficient and data normalization [3].These electrical properties are classified into different performance characteristics, with ION being classified as a higher-than-average performance characteristic and IOFF and SS being defined as lower-than-average performance characteristics.The goal is to have a maximum ION value and a minimum IOFF and SS value, since this will result in a better ION/IOFF ratio and more efficient power use.The following equations are used to normalize the electrical characteristics [15].

$$x^*(k) = \frac{x_i^0(k) - \min x_i^0(k)}{\max x_i^0(k) - \min x_i^0(k)}$$

, higher the better

$$x^*(k) = \frac{\max x_i^0(k) - x_i^0(k)}{\max x_i^0(k) - \min x_i^0(k)}$$

, smaller the better



The original data (x) firstly is represented as reference (x0) and comparative series (x1) followed by data normalization.The number of experimental data items is represented by m, and the parameter numbers are represented by n. The largest and smallest value for the x(k) are represented by the respective max x(k) and min x(k).After data normalisation, the grey relational coefficient was calculated using a pre-processed sequence. [16].The GRC sequence is as follows:

$$\xi_i(k) = \frac{\Delta_{\min} + \xi\Delta_{\max}}{\Delta_{oi}(k) + \xi\Delta_{\max}}$$

where $\xi_{(k)}$ denotes the number of identifying coefficients.The GRG can be obtained in conjunction with the identification coefficient by computing the GRC average after GRC derivation.The GRA implementation is aided by estimating the GRG using the ideal level based on the optimal level with a number of process parameters.A factor effect graph based on the GRG completed by each level can be used to understand the best values for each level of process parameters.The GRG value with the highest value indicates that the multiple responses are closer to the expected values.Once the preferred level from the analysis has been determined, TCAD will be used to simulate it again in order to create the best design.

# CHAPTER 4

# RESULTS AND DISCUSSION

## 4.1 Introduction

This chapter is all about result on optimization of electrical characteristics using taguchi and taguchi based gra after the complete structure of 16nm NMOS design in ATHENA module.The electrical characteristics that focusess on optimization process are threshold voltage(Vth),drive current(Ion),off current(Ioff),current state ratio(Ion/Ioff), and sub-threshold slope(SS).This device simulation is done using ATLAS module of SILVACO TCAD tool.All the simulated values of electrical characteristics are recorded and analysed and they should be within the International Technology Roadmap Semiconductor(ITRS) 2013 prediction for the year 2017.



## 4.2 Analysis of 16nm Si/SiGe NMOS device

The figure 4.1 shows the Id-Vg curve of Si/SiGe of n-channel MOSFET.The electrical characteristics that has been extracted and analysed from this curve are threshold voltage(Vth),drive current(Ion),off current(Ioff),current state ratio(Ion/Ioff) and sub-threshold slope(SS).To boost the transistor's switching speed, a good transistor specification requires a high driving current and an ideal threshold voltage.The most important factor in determining the device's operation is the threshold voltage. It should

be kept as low as possible, along with the leakage currents, in order to maximise the device's speed by reducing the time it takes for charge to collect in the channel for a transistor to switch on.In designing the MOSFET,process parameters plays an important role in determining its behaviour as it will affect the threshold voltage variationThe variation will have an impact on the device's performance.The minimum gate voltage that required to produce a channel between source and drain is known as threshold voltage(VTH).It's used to see if the device is working properly or not.The intended design is finalised using the Taguchi method by picking the optimum performance under specific conditions.The Taguchi Method was used to assess and process the threshold voltage (VTH) values in order to obtain the best design.The optimized results from Taguchi Method were simulated in order to verify the predicted optimal design.In order to get the optimal value of threshold voltageI(Vth),the drive current(Ion) must be higher,leakage current(Ioff) should be lower,current state ratio(Ion/Ioff) must be higher and sub-threshold slope(SS) should be lower to prevent transistor scaling down problems like short channel effect(SCE).

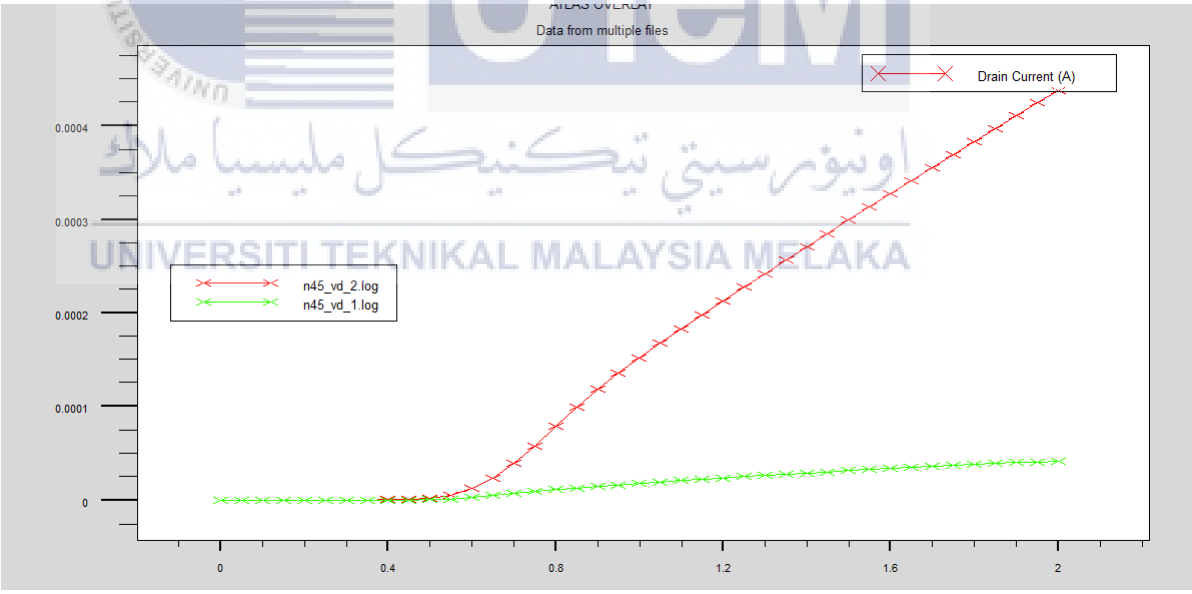


Figure 4.1: Id-Vd graph for 16nm Si/SiGe NMOS

## 4.3 L9 Orthogonal Array(OA) of Taguchi Approach

When several process factors are involved in the process, the Taguchi technique is an effective problem-solving tool for the design of experiments. This technique decreases the amount of time and money spent on experiments while also improving the process, system, design, and product's performance.L9 orthogonal array were chosen for this method.In L9 orthogonal array only nine times of experiment were carried on.There are four control factors were assigned to four columns of L9.Each row represents an experiment having a combination of control factor levels.Columns are considered to be orthogonal if all combinations of factor levels occur an equal number of times for any pair of columns [10].

This study chose four process parameters: halo implant dose, halo implant energy, S/D implant dose, and S/D implant energy. The noise factors that were chosen are as listed.

Table 4.1: Original Value of Process Parameter

| Symbol | Process Parameter | Units | Original Value $^{\circ}C$ |
|---|---|---|---|
| A | Halo Implant Dose | atom/cm$^{-}$3 | 2.7E+13 |
| B | Halo Implant Energy | KeV | 170 |
| C | S/D Implant Dose | atom/cm$^{-}$3 | 9.8E+13 |
| D | S/D Implant Energy | KeV | 12 |

There are three levels of value that has been chosen to run the simulations.The process parameters and levels are shown in table 4.2, while the assigned noise factors and levels are shown in table 4.3.Multiple levels of L9 process parameters are shown in table 4.4.

Table 4.2: Process Parameter and their Levels

| Symbol | Process Parameter | Units | Level 1 | Level 2 | Level 3 $^{\circ}C$ |
|---|---|---|---|---|---|
| A | Halo Implant Dose | atom/cm$^{-}$3 | 2.65E+13 | 2.7E+13 | 2.75E+13 |
| B | Halo Implant Energy | KeV | 172 | 170 | 168 |
| C | S/D Implant Dose | atom/cm$^{-}$3 | 9.75E+13 | 9.8E+13 | 9.85E+13 |
| D | S/D Implant Energy | KeV | 11.5 | 12 | 12.5 |

Table 4.3: Noise Factor and their Levels

| Symbol | Noise Factor | Units | Level 1 | Level 2 $^{\circ}C$ |
|---|---|---|---|---|
| U | Annealing Temperature | Degree | 852 | 855 |
| V | Nitride Temperature | Degree | 800 | 805 |

Table 4.4: Multiple Levels of L9 Process Parameter

| EXP | Process Parameter | | | |
|---|---|---|---|---|
| | A | B | C | D |
| 1 | 1 | 1 | 1 | 1 |
| 2 | 1 | 2 | 2 | 2 |
| 3 | 1 | 3 | 3 | 3 |
| 4 | 2 | 1 | 2 | 3 |
| 5 | 2 | 2 | 3 | 1 |
| 6 | 2 | 3 | 1 | 2 |
| 7 | 3 | 1 | 3 | 2 |
| 8 | 3 | 2 | 1 | 3 |
| 9 | 3 | 3 | 2 | 1 |

## 4.4 Analysation of Process Parameter

The figure 4.3 shows the interaction of noise components and process parameters.It is widely acknowledge that there were four outputs of electrical characteristics which is Vth,Ion,Ioff,Ion/Ioff and SS in each level of the experiments due to the four combinations of noise factors.The data of combined levels of the noise factors represented as U1V1,U1V2,U2V1,U2V2.The value of those electrical characteristics in each set of experiment to the combination level of noise factors were observed and recorded as shown in each figures.

Table 4.5: Combination of Noise level factor and Process Parameter

| EXP | Process Parameter | | | | Electrical Characteristics | | | |
|---|---|---|---|---|---|---|---|---|
| | A | B | C | D | U 1 V 1 | U 1 V 2 | U 2 V 1 | U 2 V 2 |
| 1 | 1 | 1 | 1 | 1 | | | | |
| 2 | 1 | 2 | 2 | 2 | | | | |
| 3 | 1 | 3 | 3 | 3 | | | | |
| 4 | 2 | 1 | 2 | 3 | | | | |
| 5 | 2 | 2 | 3 | 1 | | | | |
| 6 | 2 | 3 | 1 | 2 | | | | |
| 7 | 3 | 1 | 3 | 2 | | | | |
| 8 | 3 | 2 | 1 | 3 | | | | |
| 9 | 3 | 3 | 2 | 1 | | | | |

Table 4.6: Values of Threshold Voltage

| EXP | Process Parameter | | | | Threshold Voltage (Vth), V | | | |
|---|---|---|---|---|---|---|---|---|
| | A | B | C | D | U 1 V 1 | U 1 V 2 | U 2 V 1 | U 2 V 2 |
| 1 | 1 | 1 | 1 | 1 | 0.543 | 0.544 | 0.542 | 0.543 |
| 2 | 1 | 2 | 2 | 2 | 0.521 | 0.522 | 0.520 | 0.520 |
| 3 | 1 | 3 | 3 | 3 | 0.518 | 0.519 | 0.517 | 0.518 |
| 4 | 2 | 1 | 2 | 3 | 0.523 | 0.524 | 0.522 | 0.523 |
| 5 | 2 | 2 | 3 | 1 | 0.560 | 0.561 | 0.558 | 0.559 |
| 6 | 2 | 3 | 1 | 2 | 0.540 | 0.541 | 0.538 | 0.539 |
| 7 | 3 | 1 | 3 | 2 | 0.540 | 0541 | 0.539 | 0.540 |
| 8 | 3 | 2 | 1 | 3 | 0.541 | 0.542 | 0.540 | 0.541 |
| 9 | 3 | 3 | 2 | 1 | 0.591 | 0.593 | 0.590 | 0.590 |

Table 4.7: Values of Drive Current

| EXP | Process Parameter | | | | Drive Current (Ion), $\mu A/\mu m$ | | | |
|---|---|---|---|---|---|---|---|---|
| | A | B | C | D | U 1 V 1 | U 1 V 2 | U 2 V 1 | U 2 V 2 |
| 1 | 1 | 1 | 1 | 1 | 462.29 | 460.56 | 464.56 | 462.29 |
| 2 | 1 | 2 | 2 | 2 | 508.33 | 506.53 | 511.27 | 509.49 |
| 3 | 1 | 3 | 3 | 3 | 518.25 | 516.43 | 521.42 | 519.61 |
| 4 | 2 | 1 | 2 | 3 | 507.26 | 505.49 | 510.23 | 508.47 |
| 5 | 2 | 2 | 3 | 1 | 438.54 | 436.77 | 440.73 | 438.97 |
| 6 | 2 | 3 | 1 | 2 | 473.68 | 471.85 | 476.34 | 474.50 |
| 7 | 3 | 1 | 3 | 2 | 473.49 | 471.83 | 476.11 | 474.45 |
| 8 | 3 | 2 | 1 | 3 | 473.73 | 471.87 | 476.44 | 474.59 |
| 9 | 3 | 3 | 2 | 1 | 407.47 | 405.68 | 407.76 | 407.76 |

Table 4.8: Values of Ioff Current

| EXP | Process Parameter | | | | Leakage Current (Ioff), $\mu pA/\mu m$ | | | |
|---|---|---|---|---|---|---|---|---|
| | A | B | C | D | U 1 V 1 | U 1 V 2 | U 2 V 1 | U 2 V 2 |
| 1 | 1 | 1 | 1 | 1 | 1.03E-011 | 9.65E-012 | 1.20E-011 | 1.03E-011 |
| 2 | 1 | 2 | 2 | 2 | 1.00E-010 | 9.36E-011 | 1.20E-010 | 1.12E-010 |
| 3 | 1 | 3 | 3 | 3 | 1.41E-010 | 1.32E-010 | 1.71E-010 | 1.60E-010 |
| 4 | 2 | 1 | 2 | 3 | 6.94E-011 | 6.49E-011 | 8.35E-011 | 7.81E-011 |
| 5 | 2 | 2 | 3 | 1 | 2.38E-012 | 2.22E-012 | 2.75E-012 | 2.57E-012 |
| 6 | 2 | 3 | 1 | 2 | 1.34E-011 | 1.24E-011 | 1.59E-011 | 1.47E-011 |
| 7 | 3 | 1 | 3 | 2 | 1.12E-011 | 1.05E-011 | 1.33E-11 | 1.25E-011 |
| 8 | 3 | 2 | 1 | 3 | 9.67E-012 | 8.98E-012 | 1.15E-011 | 1.07E-011 |
| 9 | 3 | 3 | 2 | 1 | 4.19E-013 | 3.93E-013 | 4.43E-013 | 4.43E-013 |

Table 4.9: Values of Ion/Ioff Current

| EXP | Process Parameter | | | | Current State Ratio (Ion/Ioff), | | | |
|---|---|---|---|---|---|---|---|---|
| | A | B | C | D | U 1 V 1 | U 1 V 2 | U 2 V 1 | U 2 V 2 |
| 1 | 1 | 1 | 1 | 1 | 4.47E+007 | 4.77E+007 | 3.86E+007 | 4.47E+007 |
| 2 | 1 | 2 | 2 | 2 | 5.07E+006 | 5.41E+006 | 4.26E+006 | 4.54E+006 |
| 3 | 1 | 3 | 3 | 3 | 3.67E+006 | 3.91E+006 | 3.05E+006 | 3.25E+006 |
| 4 | 2 | 1 | 2 | 3 | 7.31E+006 | 7.80E+006 | 6.11E+006 | 6.51E+006 |
| 5 | 2 | 2 | 3 | 1 | 1.84E+008 | 1.97E+008 | 1.60E+008 | 1.70E+008 |
| 6 | 2 | 3 | 1 | 2 | 3.55E+007 | 3.80E+007 | 3.00E+007 | 3.22E+007 |
| 7 | 3 | 1 | 3 | 2 | 4.21E+007 | 4.47E+007 | 3.57E+007 | 3.78E+007 |
| 8 | 3 | 2 | 1 | 3 | 4.90E+007 | 5.25E+007 | 4.13E+007 | 4.43E+007 |
| 9 | 3 | 3 | 2 | 1 | 9.71E+008 | 1.03E+009 | 9.20E+008 | 9.20E+008 |

Table 4.10: Values of Sub Threshold Slope

| EXP | Process Parameter | | | | Sub-Threshold Slope (SS), mV/dec | | | |
|---|---|---|---|---|---|---|---|---|
| | A | B | C | D | U1V1 | U1V2 | U2V1 | U2V2 |
| 1 | 1 | 1 | 1 | 1 | 0.0772 | 0.0770 | 0.0776 | 0.0772 |
| 2 | 1 | 2 | 2 | 2 | 0.0904 | 0.0899 | 0.0919 | 0.0914 |
| 3 | 1 | 3 | 3 | 3 | 0.0930 | 0.0925 | 0.0947 | 0.0942 |
| 4 | 2 | 1 | 2 | 3 | 0.0868 | 0.0863 | 0.0885 | 0.0879 |
| 5 | 2 | 2 | 3 | 1 | 0.0745 | 0.0744 | 0.0747 | 0.0746 |
| 6 | 2 | 3 | 1 | 2 | 0.0777 | 0.0775 | 0.0784 | 0.0781 |
| 7 | 3 | 1 | 3 | 2 | 0.0771 | 0.0769 | 0.0776 | 0.0774 |
| 8 | 3 | 2 | 1 | 3 | 0.0766 | 0.0764 | 0.0771 | 0.0769 |
| 9 | 3 | 3 | 2 | 1 | 0.0735 | 0.0736 | 0.0736 | 0.0736 |

## 4.5 Analysation of Signal to Noise Ratio

After the completion of nine L9 array trials, the following phase is to find the control factor settings that can have a greater impact on device characteristics.Under various noise situations, the signal-to-noise ratio evaluates how the response fluctuates in relation to the nominal or target value.The optimal process parameters and experimental data were determined using the Signal to Noise Ratio (S/N) ratio.The Signal to Noise Ratio (SNR) for each input process parameter is determined using the S/N response analysis.In the examination of SNR, there are three types of performance characteristics which is nominal-the-best, lower-the-best, and higher-the-bestRegardless of the performance characteristic category, a higher SNR leads to better performance characteristics [17].As a result, the ideal process parameter setting is the one with the maximum SNR.

The Threshold Voltage (VTH) is specified as nominal-the-best to allow the optimised values for the VTH to be close to or equivalent by 12.7% or equivalent to the desired ones, which are at 0.530V.The The smaller-the-best characteristics are applied towards both Leakage Current (IOFF) and Sub Threshold Slope (SS) to be considered as minimum as possible whereby the IOFF is aimed to be lesser than 50 pA/m by the ITRS 2017.The use of larger-the-best characteristics is justified by the ITRS 2017 prediction that the Drive Current (ION) will be larger than 422 A/m, hence larger-the-best characteristics are used to get the ION as large as feasible without compromising other features [17].The equations for nominal the best were expressed as shown.

$$\eta = 10\log_{10}\left[\frac{\mu^2}{\sigma^2}\right] \tag{4.1}$$

[18] Where:

$$\mu = \frac{Y_i + \ldots\ldots + Y_n}{n}$$
$$\sigma^2 = \frac{\sum_{i=1}^{n}(Y_i - \mu)^2}{n-1} \tag{4.2}$$

[18]

The number of test is $n$,and the experimental value of threshold voltage is $Y_i$.The mean is $\mu$ and the variance is $\sigma$.In nominal-the-best S/N ratio, there are two types of factors; the dominant and the adjustment.The table 4.11 shows the computed values of SNR for Vth.The SNR for lower the best of Ioff and SS is expressed as shown.

$$\eta = -10\log_{10}\left[\frac{1}{n}\sum_{i=1}^{n} y_i^2\right] \tag{4.3}$$

[18]

where $n$ is the number of experiments and $Y_i$ is IOFF and SS experimental values.Each experiment's S/N ratio (lower-the-better) was calculated and recorded in Tables 4.12 and 4.13.The equation for larger the best were expressed as shown.

$$\eta = 10\log_{10}\left[\frac{1}{\mathrm{n}}\sum\left(\left(\frac{1}{\mathrm{Y}_1^2}\right)+\left(\frac{1}{\mathrm{Y}_2^2}\right)+\cdots+\left(\frac{1}{\mathrm{Y}_\mathrm{n}^2}\right)\right)\right] \tag{4.4}$$

[18]

Table 4.11: Value of Vth for Mean,Variance and S/N Ratio

| Exp | Mean | Variance | S/N (Mean) | S/N Ratio (Nominal The Best) |
|---|---|---|---|---|
| 1 | 5.43E-01 | 1.05E-06 | -5.31E+00 | 5.45E+01 |
| 2 | 5.21E-01 | 9.23E-07 | -5.67+00 | 5.47E+01 |
| 3 | 5.18E-01 | 8.67E-07 | -5.72E+00 | 5.49E+01 |
| 4 | 5.23E-01 | 9.23E-07 | -5.63E+00 | 5.47E+01 |
| 5 | 5.60E-01 | 2.09E-06 | -5.04E+00 | 5.18E+01 |
| 6 | 5.39E-01 | 1.08E-06 | -5.36E+00 | 5.43E+01 |
| 7 | 5.40E-01 | 1.02E-06 | -5.36E+00 | 5.46E+01 |
| 8 | 5.41E-01 | 1.08E-06 | -5.34E+00 | 5.43E+01 |
| 9 | 5.91E-01 | 1.21E-06 | -4.57E+00 | 5.46E+01 |

Table 4.12: Value of Ioff for Mean Sum of Square and S/N Ratio

| Exp | Mean Sum of Square | S/N Ratio (Smaller The Better) |
|---|---|---|
| 1 | 1.13E-22 | 219.47 |
| 2 | 1.14E-20 | 199.41 |
| 3 | 2.30E-20 | 196.37 |
| 4 | 5.52E-21 | 202.58 |
| 5 | 6.19E-24 | 232.08 |
| 6 | 2.00E-22 | 216.98 |
| 7 | 1.43E-22 | 218.45 |
| 8 | 1.06E-22 | 219.76 |
| 9 | 1.81E-25 | 247.42 |

Table 4.13: Value of SS for Mean Sum of Square and S/N Ratio

| Exp | Mean Sum of Square | S/N Ratio (Smaller The Better) |
|---|---|---|
| 1 | 5.97E-03 | 22.24 |
| 2 | 8.26E-03 | 20.83 |
| 3 | 8.76E-03 | 20.57 |
| 4 | 7.64E-03 | 21.17 |
| 5 | 5.56E-03 | 22.55 |
| 6 | 6.07E-03 | 22.17 |
| 7 | 5.97E-03 | 22.24 |
| 8 | 5.89E-03 | 22.30 |
| 9 | 5.41E-03 | 22.67 |

Table 4.14: Value of ION for Mean Sum of Square and S/N Ratio

| Exp | Mean Sum of Square | S/N Ratio (Larger The Better) |
|---|---|---|
| 1 | 4.68E-06 | 53.30 |
| 2 | 3.86E-06 | 54.13 |
| 3 | 3.71E-06 | 54.30 |
| 4 | 3.88E-06 | 54.11 |
| 5 | 5.19E-06 | 52.84 |
| 6 | 4.45E-06 | 53.52 |
| 7 | 4.45E-06 | 53.51 |
| 8 | 4.45E-06 | 53.52 |
| 9 | 6.03E-06 | 52.20 |

Table 4.15: Value of ION/IOFF for Mean Sum of Square and S/N Ratio

| Exp | Mean Sum of Square | S/N Ratio (Larger The Better) |
|---|---|---|
| 1 | 5.28E-16 | 152.77 |
| 2 | 4.41E-14 | 133.55 |
| 3 | 8.55E-14 | 130.68 |
| 4 | 2.14E-14 | 136.70 |
| 5 | 3.22E-17 | 164.92 |
| 6 | 8.90E-16 | 150.50 |
| 7 | 6.36E-16 | 151.97 |
| 8 | 4.69E-16 | 153.29 |
| 9 | 1.09E-18 | 179.62 |

To improve the quality of Vth, the S/N ratio must be increased.As a result, if the quality characteristic value was closer to the target, the device quality would be better [18]The influence of each process parameter on the S/N ratio at different levels may be isolated because the experimental design is orthogonal.The signal to noise ratio on each process parameter were computed in table 4.16.The mean graph and S/N ratio graph shown in figure 4.2 [19].Thus,the optimum value for 16nm Nmos device was obtained at level A3,B3,C3 and D3.

Table 4.16: Value of S/N responses on Vth

| Sym | Process Parameter | SNR (Nominal the Best) | | | Selected Level | Total Mean SNR |
|---|---|---|---|---|---|---|
| | | Level 1 | Level 2 | Level 3 | | |
| A | Halo Implant Dose | 54.69 | 53.59 | 54.49 | 3 | |
| B | Halo Implant Energy | 54.59 | 53.58 | 54.60 | 3 | 54.26 |
| C | S/D Implant Dose | 54.36 | 54.67 | 53.74 | 3 | |
| D | S/D Implant Energy | 53.62 | 54.51 | 54.65 | 3 | |

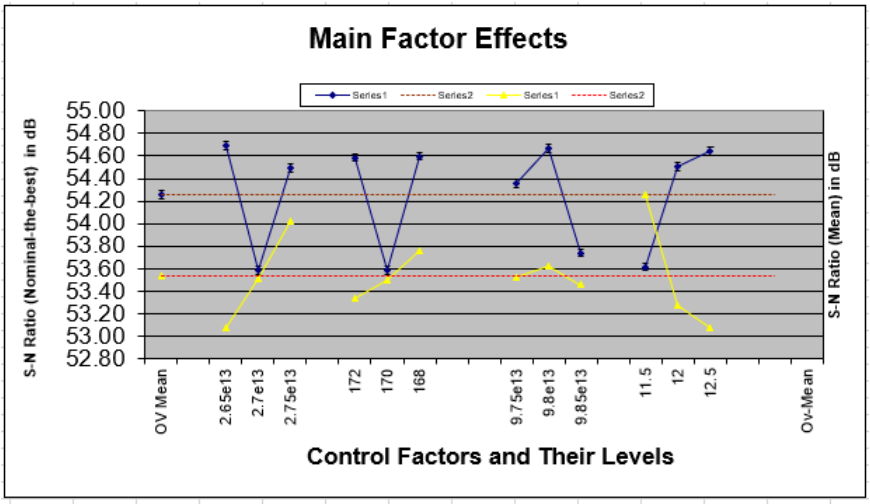


Figure 4.2: S/N Graph of Vth

The S/N ratio of Ion and Ion/Ioff characteristics were in larger the best level.The table 4.17 and 4.18 shows the S/N ratio responses on Ion and Ion/Ioff.The figure 4.3 and 4.4 represents the S/N graph of Ion and Ion/Ioff.Therefore, the optimum level of Ion was A1,B1,C3 and D3 whereas the optimum level of Ion/Ioff was A3,B3,C1 and D1.Basically,the device is considered to have better quality when the quality characteristics is higher or closer to the target [18].

Table 4.17: Value of S/N responses on Ion

| Sym | Process Parameter | SNR (Larger the Better) | | | Selected Level | Total Mean SNR |
|---|---|---|---|---|---|---|
| | | Level 1 | Level 2 | Level 3 | | |
| A | Halo Implant Dose | 53.91 | 53.49 | 53.08 | 1 | |
| B | Halo Implant Energy | 53.64 | 53.50 | 53.34 | 1 | 53.49 |
| C | S/D Implant Dose | 53.45 | 53.48 | 53.55 | 3 | |
| D | S/D Implant Energy | 52.78 | 53.72 | 53.98 | 3 | |

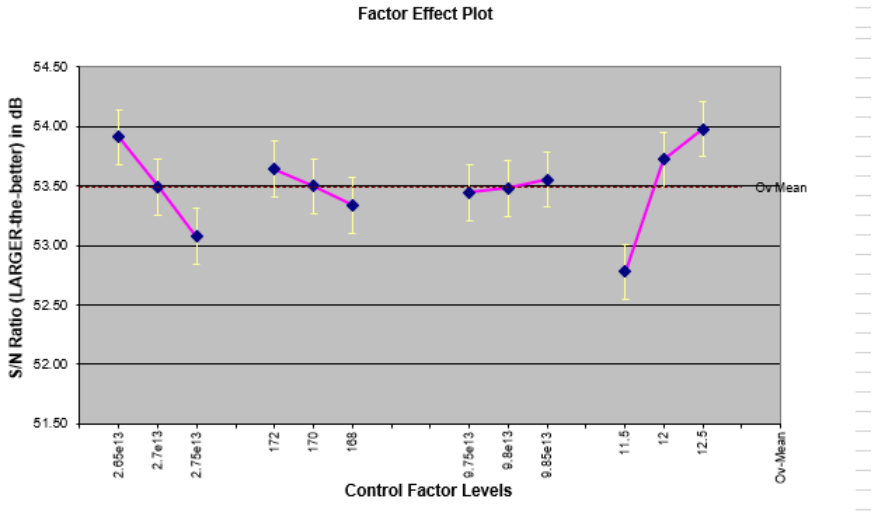


Figure 4.3: S/N Graph of Ion

Table 4.18: Value of S/N responses on Ion/Ioff

| Sym | Process Parameter | SNR (Larger the Better) | | | Selected Level | Total Mean SNR |
|---|---|---|---|---|---|---|
| | | Level 1 | Level 2 | Level 3 | | |
| A | Halo Implant Dose | 139 | 150.71 | 161.63 | 3 | |
| B | Halo Implant Energy | 147.15 | 150.59 | 153.60 | 3 | 150.45 |
| C | S/D Implant Dose | 152.19 | 149.96 | 149.19 | 1 | |
| D | S/D Implant Energy | 165.77 | 145.34 | 140.22 | 1 | |

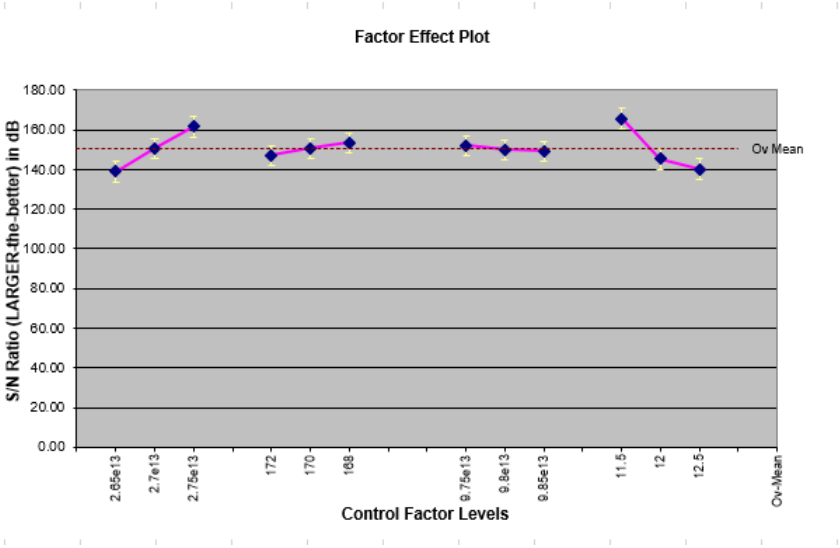


Figure 4.4: S/N Graph on Ion/Ioff

## 4.6 Analysis of Variance (ANOVA)

To determine which device characteristics have a substantial impact on performance metrics, an analysis of variance (ANOVA) is utilised [20].It determinates electrical characteristic parameters such as Sum of Square (SSQ),Mean Sum of Square (MSSQ), Degree of Freedon (DF),variance, F-value and percentage of each factor [21].The results of anova are shown in table 4.19,4.20,4.21,4.22.



Table 4.19: Result of Anova on Vth

| Output Response | Process Parameter | Df | SSQ | MSSQ | F-after Pooling | Factor Effect on SNR (%) |
|---|---|---|---|---|---|---|
| Vth | Halo Implant Dose | 2 | 2 | 1 | 1032 | 28 |
| | Halo Implant Energy | 2 | 2 | 1 | 1018 | 28 |
| | S/D Implant Dose | 2 | 1 | 1 | 667 | 18 |
| | S/D Implant Energy | 2 | 2 | 1 | 935 | 26 |

Table 4.20: Result of Anova on Ion

| Output Response | Process Parameter | Df | SSQ | MSSQ | F-after Pooling | Factor Effect on SNR (%) |
|---|---|---|---|---|---|---|
| Ion | Halo Implant Dose | 2 | 1 | 1 | 13 | 29 |
| | Halo Implant Energy | 2 | 0 | 0 | - | 4 |
| | S/D Implant Dose | 2 | 0 | 0 | - | 1 |
| | S/D Implant Energy | 2 | 2 | 1 | 29 | 66 |

Table 4.21: Result of Anova on Ion/Ioff

| Output Response | Process Parameter | Df | SSQ | MSSQ | F-after Pooling | Factor Effect on SNR (%) |
|---|---|---|---|---|---|---|
| Ion/Ioff | Halo Implant Dose | 2 | 768 | 384 | 20 | 40 |
| | Halo Implant Energy | 2 | 63 | 31 | - | 3 |
| | S/D Implant Dose | 2 | 15 | 7 | - | 1 |
| | S/D Implant Energy | 2 | 1096 | 548 | 28 | 56 |

Table 4.22: Result of Anova on Ioff

| Output Response | Process Parameter | Df | SSQ | MSSQ | F-after Pooling | Factor Effect on SNR (%) |
|---|---|---|---|---|---|---|
| Ioff | Halo Implant Dose | 2 | 826 | 413 | 20 | 39 |
| | Halo Implant Energy | 2 | 69 | 34 | - | 3 |
| | S/D Implant Dose | 2 | 15 | 8 | - | 1 |
| | S/D Implant Energy | 2 | 1202 | 601 | 29 | 57 |



According to the table 4.19, the dominant levels of electrical characteristics can be determined from the factor effect which is the halo implant dose and energy is 28%, S/D implant dose is 18% and S/D implant energy is 26%.Whereas the halo dose of Ion is 29%,halo energy is 4%,S/D dose is 1% and S/D energy is 66%.Then, the halo dose of Ion/Ioff is 40%,halo energy is 3%,S/D dose become 1%, and S/D energy is 56%.At last, for table 4.22 the halo dose is 39%,halo energy is 3%, and 1% for S/D dose and 57% for S/D energy [18] [19].

## 4.7 Confirmation Test for Taguchi Method

The confirmation run's primary goal is to verify the data obtained during the analysis phase.The best optimal level from each process parameter required to obtain first.The factor effect from each process parameter will be compared to get the most optimal level.The table 4.23 shows the comparison of factor effect and selected optimal levels.The final overall best setting by using Taguchi Method are A3,B3,C3 and D3.The overall best setting values are as shown in table 4.24.Then, the final step in Taguchi method is to run the device with new overall best settings that have been obtained.Thus,table 4.25 shows new result of electrical characteristics with new optimal levels.

Table 4.23: Factor Effect and Selected Optimal Levels Comparison

| Process Parameter | Vth | | Ion | | Ion/Ioff | | Ioff | | Best Setting |
|---|---|---|---|---|---|---|---|---|---|
| | Level | Effect on SNR | Level | Effect on SNR | Level | Effect on SNR | Level | Effect on SNR | |
| A | 3 | 28 | 1 | 29 | 3 | 40 | 3 | 39 | A3 |
| B | 3 | 28 | 1 | 4 | 3 | 3 | 3 | 3 | B3 |
| C | 3 | 18 | 3 | 1 | 1 | 1 | 1 | 1 | C3 |
| D | 3 | 26 | 3 | 66 | 1 | 56 | 1 | 57 | D3 |



Table 4.24: Noise Factor and their Levels

| Symbol | Process Parameter | Units | Original Value |
|---|---|---|---|
| A | Halo Implant Dose | atom/cm$^{-}$3 | 2.75E+13 |
| B | Halo Implant Energy | KeV | 168 |
| C | S/D Implant Dose | atom/cm$^{-}$3 | 9.85E+13 |
| D | S/D Implant Energy | KeV | 12.5 |

Table 4.25: Result with New Optimal Levels

| Electrical Characteristics | Noise Factor Combinations | | | | Average |
|---|---|---|---|---|---|
| | U1V1 | U1V2 | U2V1 | U2V2 | |
| Vth (V) | 0.5424 | 0.5434 | 0.5408 | 0.5419 | 0.5421 |
| Ion ($\mu A/\mu m$) | 472.109 | 470.264 | 474.861 | 473.021 | 472.56 |
| Ioff (pA/$\mu m$) | 8.64294E-012 | 8.03247E-012 | 1.03357E-011 | 9.60755E-012 | 9.15E-12 |
| Ion/Ioff | 5.46236E+007 | 5.8545E+007 | 4.5944E+007 | 4.92343E+007 | 5.21E+07 |
| SS (mV/dec) | 0.0763 | 0.0761 | 0.0768 | 0.0766 | 76.45 |

## 4.8 Grey Relational Method (GRA)

For resolving interrelationships among many responses, the grey relational approach is applied. First,the responses are needed to transform into the S/N ratio of $Y_{nj}$ using the appropriate equations depending on the quality characteristics.Then, the S/N ratio will be applied to normalize and to equally divide the data and scale it into a range that may be used for further analysis by the equations as follows [22].The Signal to Noise ratio was computed to analyze the effect of process parameters more accurately.



$$Z_{\mathrm{nj}} = \left(Y_{\mathrm{nj}} - \min Y_{\mathrm{nj}}\right) / \left(\max Y_{\mathrm{nj}} - \min Y_{\mathrm{nj}}\right) [forlargerthebettercase] \quad (4.5)$$

[22]

$$Z_{\mathrm{nj}} = \left(\max Y_{\mathrm{nj}} - Y_{\mathrm{nj}}\right) / \left(\max Y_{\mathrm{nj}} - \min Y_{\mathrm{nj}}\right) [forsmallerthebettercase] \quad (4.6)$$

[22]

The normalised value of the nth trial for the jth dependent response is Znj.The Grey Relational Coefficient (GRC) will then be computed using the normalised S/N ratio data using the equation below.

$$GC_{nj} = (\Psi_{min} + \delta\Psi_{max}) / (\Psi_{nj} + \delta\Psi_{max}) \quad (4.7)$$

[22]

where GC represents the grey co-efficient for the nth trial of the jth dependent response, d represents the quality loss, and W represents the distinguishing coefficient, which ranges from 0 to 1.At last,Grey Relational Grade (GRG) be calculated to get the optimized values.From here,the single response optimization received from multiple response optimization process.The only objective function is the overall grey relational grade.After that, the best parametric combination is determined by maximising the grey relational grade overall.The table 4.26 shows the normalized electrical characteristics based on L9 Orthogonal Array (OA) of Taguchi Method.

Table 4.26: Normalized Electrical Characteristics based on Taguchi Method

| EXP | Process Parameter | | | | Electrical Characteristics | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | A | B | C | D | Vth | Ion | Ioff | Ion/Ioff | SS |
| 1 | 1 | 1 | 1 | 1 | 0.543 | 462.42 | 1.05E-11 | 43.92E06 | 77.25E-03 |
| 2 | 1 | 2 | 2 | 2 | 0.521 | 508.91 | 1.06E-10 | 14.82E06 | 90.9E-03 |
| 3 | 1 | 3 | 3 | 3 | 0.518 | 518.93 | 1.51E-10 | 3.47E06 | 93.6E-03 |
| 4 | 2 | 1 | 2 | 3 | 0.523 | 507.86 | 7.40E-11 | 6.93E06 | 87.38E-03 |
| 5 | 2 | 2 | 3 | 1 | 0.560 | 438.75 | 2.48E-12 | 177.85E06 | 74.55E-03 |
| 6 | 2 | 3 | 1 | 2 | 0.539 | 474.09 | 1.41E-11 | 33.92E06 | 77.93E-03 |
| 7 | 3 | 1 | 3 | 2 | 0.540 | 473.97 | 1.19E-11 | 40.12E06 | 77.25E-03 |
| 8 | 3 | 2 | 1 | 3 | 0.541 | 474.16 | 1.02E-11 | 46.77E06 | 76.75E-03 |
| 9 | 3 | 3 | 2 | 1 | 0.591 | 407.17 | 4.25E-13 | 960.52E06 | 73.58E-03 |

Table 4.27: Electrical Characteristics deviation sequences

| Exp. no. | Deviation Sequences | | | |
|---|---|---|---|---|
| | Ion | Ioff | Ion/Ioff | SS |
| 1 | 0.505637 | 0.066910178 | 0.75305 | 0.183317 |
| 2 | 0.089656 | 0.701145609 | 0.916671 | 0.865135 |
| 3 | 0 | 1 | 0.980489 | 1 |
| 4 | 0.099052 | 0.48862693 | 0.961035 | 0.689311 |
| 5 | 0.71743 | 0.013647684 | 0 | 0.048452 |
| 6 | 0.401217 | 0.090818529 | 0.809277 | 0.217283 |
| 7 | 0.402291 | 0.07620787 | 0.774417 | 0.183317 |
| 8 | 0.400591 | 0.064917815 | 0.737026 | 0.158342 |
| 9 | 1 | 0 | 1 | 0 |

The best optimum value can be obtained from computational value of grey relational coefficient and grade.The optimum value said to be achieved when the corresponding parameter obtained higher grey relational grade [16].Therefore from table 4.28,the optimal process parameter based on highest GRG obtained was A2,B2,C3 and D1.

Table 4.28: Calculated value of GRC and GRG

| Exp. no. | Grey Relational Coefficient | | | | GRG |
|---|---|---|---|---|---|
| | Ion | Ioff | Ion/Ioff | SS | |
| 1 | 0.49719726 | 0.881974 | 0.399026 | 0.731725 | 0.592732 |
| 2 | 0.84795144 | 0.416269 | 0.35294 | 0.366264 | 0.539054 |
| 3 | 1 | 0.333333 | 0.337726 | 0.333333 | 0.55702 |
| 4 | 0.83465273 | 0.505752 | 0.342223 | 0.420412 | 0.560876 |
| 5 | 0.41070116 | 0.97343 | 1 | 0.911658 | 0.79471 |
| 6 | 0.5548054 | 0.846284 | 0.38189 | 0.697075 | 0.594326 |
| 7 | 0.55414518 | 0.867742 | 0.392336 | 0.731725 | 0.604741 |
| 8 | 0.55519126 | 0.885084 | 0.404195 | 0.759484 | 0.614824 |
| 9 | 0.33333333 | 1 | 0.333333 | 1 | 0.555556 |

Table 4.29: Computed GRG Process Parameter at Different Levels

| Symbol | Process Parameter | GRG | | | Selected Level | OV Mean GRG |
|---|---|---|---|---|---|---|
| | | Level 1 | Level 2 | Level 3 | | |
| A | Halo Implant Dose | 0.5629 | 0.6400 | 0.5917 | 2 | 0.6015 |
| B | Halo Implant Energy | 0.5861 | 0.6495 | 0.5690 | 2 | |
| C | S/D Implant Dose | 0.6006 | 0.5518 | 0.6522 | 3 | |
| D | S/D Implant Energy | 0.6477 | 0.5794 | 0.5776 | 1 | |

## 4.9 Analysis of Variance for GRG

Generally,a confirmation test will be carried on when the best condition has been found.The Analysis of Variance (ANOVA) test is applied to determine the relative importance of different components as well as their interactions.This can be done by separating the total variability of GRG measured by the sum of squared deviations from the overall mean of GRG.A total can be estimated using the equation as shown.

$$SS_T = \sum_{j=1}^{N} (yj - ym)^2 \tag{4.8}$$

[23]

where $N$ denotes the total number of trials in the OA, $yj$ denotes the mean GRG for the $jth$ trial, and $ym$ denotes the overall GRG average.Divide the SS by the matching degree of freedom to get the mean square (MS).

$$MS = \frac{SS}{DF} \tag{4.9}$$

[23]



Table 4.30: Computed ANOVA for GRG

| Control Factor | DF | SSQ | MS | F | P | P (%) |
|---|---|---|---|---|---|---|
| A | 2 | 0.011798 | 0.005898845 | 11.97587 | 0.241937 | 24.1936867 |
| B | 2 | 0.010805 | 0.005402745 | 10.96869 | 0.22159 | 22.1589676 |
| C | 2 | 0.015103 | 0.007551265 | 15.33063 | 0.30971 | 30.9709683 |
| D | 2 | 0.00958 | 0.004790058 | 9.724807 | 0.196461 | 19.6460744 |
| Error | 3 | 0.001478 | 0.000492561 | - | 0.030303 | 3.03030303 |
| Total | 11 | 0.048764 | 0.024135474 | - | 1 | 100 |

## 4.10 Confirmation Test

The performances of NMOS device is improvised by carrying out confirmation test.The optimum GRG is computed as shown.

$$\beta_{\text{opt}} = \beta_m + \sum_{i=1}^{c} (\beta_i - \beta_m) \tag{4.10}$$

[23]

where, $\beta_m$ is the total average of the GRG, $\beta_i$, is the average value of the GRG of *ith* factor at the optimum level, and c is the number of largest significant that gives impact on multiple performance characteristics.The new optimal level of a process parameter is shown in table 4.31,and the outcome of electrical characteristics with new optimal values is shown in table 4.32.

Table 4.31: Noise Factor and their Levels

| Symbol | Process Parameter | Units | Original Value |
|---|---|---|---|
| A | Halo Implant Dose | atom/cm$^{-}$3 | 2.7E+13 |
| B | Halo Implant Energy | KeV | 170 |
| C | S/D Implant Dose | atom/cm$^{-}$3 | 9.85E+13 |
| D | S/D Implant Energy | KeV | 11.5 |



Table 4.32: Result of Electrical Characteristics with New Optimal Levels

| Electrical Characteristics | Noise Factor Combinations | | | | Average |
|---|---|---|---|---|---|
| | U1V1 | U1V2 | U2V1 | U2V2 | |
| Vth (V) | 0.5597 | 0.5613 | 0.5578 | 0.5592 | 0.5595 |
| Ion ($\mu A/\mu m$) | 438.539 | 436.769 | 440.727 | 438.968 | 438.75 |
| Ioff (pA/$\mu m$) | 2.37957E-012 | 2.21868E-012 | 2.7524E-012 | 2.56711E-012 | 2.47944-12 |
| Ion/Ioff | 1.84294E+008 | 1.9686E+008 | 1.60125E+008 | 1.70997E+008 | 178.069 |
| SS (mV/dec) | 0.0744796 | 0.074445 | 0.0746945 | 0.0746464 | 74.57 |

## 4.11 Discussion

The optimum values of electrical characteristics which is Vth,Ion,Ioff,Ion/Ioff and SS for 16nm Nmos device before and after optimization are summarized as shown in table 5.1.

Table 4.33: Optimized Values of Electrical Characteristics

| Device Characteristics | Vth (V) | Ion ($\mu A/\mu m$) | Ioff (pA/$\mu m$) | Ion/Ioff | SS (mV/dec) |
|---|---|---|---|---|---|
| Before Optimzation | 0.523 | 388 | 5.52E-21 | 2.14E-14 | 7.64 |
| After Optimize Using Taguchi Method | 0.5421 | 469 | 7.75 | 6.11E+07 | 7.60 |
| After Optimize Using Taguchi GRA | 0.588 | 438 | 2.47 | 178.07E06 | 74.57 |
| ITRS Prediction | 0.530 ±12.7% | ≥422 | ≤50 | ≥8.440E06 | 70-90 |

After optimization process, the Vth value increases slightly than the ITRS prediction but its still in the prediction range of 12.7% which is between0.403V till 0.657 V and its acceptable.The taguchi optimization for Ion is higher than the prediction value whereas the taguchi GRA optimization was slightly closer to the target value which is 422$\mu$A.The SS value was achieved in the prediction range after GRA optimization.

# CHAPTER 5

# CONCLUSION AND FUTURE WORKS

Finally, the Taguchi Method was used to successfully estimate the best solution for getting the desired transistor. The fundamental factor in assessing whether or not a device is functional is the threshold voltage (Vth). To boost the device's speed and reduce the time it takes for the transistor to switch on, the leakage current was kept as low as feasible.Ion and Ion/Ioff were kept high.so that, the power consumption of transistor can be minimized.Where, it saves the time and cost in a more efficient way by the early prediction of the robust recipeTo improve the process parameters, the SILVACO TCAD programme was employed as a simulation tool.To establish a systematic experiment design, the Taguchi method is applied.It has a lot of different versions that may be used to model the device, and it can examine a lot of different input process factors.With Taguchi,the optimization of process parameter has been analyzed using fewest number of experiments.Hence,the Taguchi approach could be considered as an effective optimization tool for MOSFET device optimization [20].

## 5.1 Future Works

The recommendations for future work for 16nm NMOS is in terms of optimization.Although taguchi GRA can do optimization for multiple responses simulataneously, it is however can do optimization within specific level of process parameters.Hence, Analysis Neural Network (ANN) has been introduced to open the possibilites to further predict and tune the design parameters for robust optimization solution.With ANN, the electrical characteristics will be converted into nine GRG.Based on nine experiment, nine GRG will feed into neural network to train.Based on that training,a total of nine predictions GRG will be produced.Thus,The well-trained network will serve as a medium for fine-tuning the best process parameter that yields the best value.

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