CURRENT RATIO ANALYSIS ON DESIGN AND MODELLING A 22 NM NMOS DEVICE WITH GATE STRUCTURE OF HIGH-K/METAL GATE (TiO_2/$TiSi_X$) AND BILAYER GRAPHENE

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This report is submitted in partial fulfilment of the requirements for the degree of Bachelor of Electronic Engineering with Honours

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DECLARATION

I declare that this report entitled “Current Ratio Analysis on Design and Modelling a 22 nm NMOS Device with Gate Structure of High-k/Metal Gate (TiO_2/$TiSi_x$) and Bilayer Graphene” is the result of my own work except for quotes as cited in the references.

Signature :

Author : AZIZUL HAQEEM BIN ABD GANI

Date : 17/8/2020

APPROVAL

I hereby declare that I have read this thesis and in my opinion this thesis is sufficient in terms of scope and quality for the award of Bachelor of Electronic Engineering with Honours.

Signature : _____

Supervisor Name : DR. AFIFAH MAHERAN BINTI ABDUL HAMID

Date : 17/8/2020

DEDICATION

This dissertation is wholeheartedly dedicated to my beloved parents, who have been our source of inspiration and give us strength when I thought of giving up, who continually provide their moral, emotional, spiritual, and financial support. To my siblings, relatives, supervisor, friends and classmates who shared their knowledge and advice and encourage me until I managed to finish my study successfully.

ABSTRACT

This project is based on virtual fabrication and program code development of a 22nm NMOS device design with high-k, metal gate structure and graphene by using Silvaco software. High-k material which is Titanium Dioxide (TiO_2) is used to replace Silicon Dioxide (SiO_2). Polysilicon is also replaced with metal gate which is Titanium Silicide ($TiSi_x$). Additional of bi-layer graphene is added to complete the gate structure. This experiment reveals the general replication structure of the ATHENA and electrical characteristic analysis using ATLAS module. Such two simulators are paired with the Taguchi system to refine the threshold voltage (V_{TH}) and current leakage (I_{OFF}) electrical characteristics. The results of the device electrical characteristics after simulation obtained with V_{TH} = 0.279852V, meanwhile for I_{OFF} = 129.099 nA/μm which is near to prediction ITRS 2012 value which is 0.289 ± 12.7%. However, the optimization process by using Taguchi method is slightly incorrect for adjustment factor and dominant factor for V_{TH} optimization due to incompatible combination between high-k dielectrics with $TiSi_x$ metal gate contribute to the unsuccessful in completing Taguchi method. In conclusion, current ratio for the circuit is 15751.48.

ABSTRAK

Projek ini adalah berdasarkan fabrikasi maya dan pembangunan kod program reka bentuk peranti NMOS 22 nm dengan menggunakan struktur high-k, get logam dan graphene menggunakan perisian Silvaco. Bahan high-k iaitu Titanium Dioksida (TiO_2) digunakan untuk menggantikan Silikon Dioksida (SiO_2). Polisilikon juga digantikan dengan get logam iaitu Titanium Silicide ($TiSi_x$) dan dua lapisan graphene. Eksperimen ini mendedahkan struktur replikasi umum dengan modul ATHENA dan analisis ciri elektrik menggunakan modul ATLAS. Kedua-dua simulator ini digabungkan dengan kaedah Taguchi untuk mengkaji dan mengoptimumkan ciri elektrik iaitu ambang voltan (V_{TH}) dan kebocoran arus (I_{OFF}). Keputusan ciri elektrik bagi peranti NMOS setelah simulasi mendapati nilai V_{TH} = 0.279852V, sementara bagi arus bocor, I_{OFF} = 129.099 nA/µm yang hampir dengan nilai ramalan ITRS 2012 iaitu 0.289 ± 12.7%. Bagaimanapun, proses pengoptimuman dengan menggunakan kaedah Taguchi sedikit tidak tepat bagi faktorpenyesuaian dan faktor dominan untuk pengoptimuman V_{TH} kerana gabungan yang tidak sesuai antara dielektrik high-k dengan get logam $TiSi_x$ menyumbang kepada tidak berjaya menyelesaikan kaedah Taguchi. Kesimpulannya, nisbah arus untuk litar ialah 15751.48.

ACKNOWLEDGEMENTS

Praised be to Allah, who has given beneficence for me in finishing this thesis. Just to Allah I asks for help, so that I can finish this thesis. Without His guidance, I am completely hopeless.

With vast love and thankfulness, I am utilizing this chance to offer my most profound thanks and extraordinary gratitude to each one of the individuals who gave me the likelihood to finish this venture. My heartfelt gratitude go to my final year project's supervisor, Dr. Afifah Maheran Binti Abdul Hamid, whose contribution on explaining, guiding and encouragement has help me to get through my project as well as writing this report.

I might want to offer my thanks to my friends, Nur Dini Binti Mohd Razz Rozzfaisal and Nur Athirah Syuhada Binti Kamalrul Ariffin for their full encouragement throughout pouring and sharing new idea and spend time with many sleepless night together while trying to achieve the target to get the wanted results for this final year project.

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LIST OF SYMBOLS AND ABBREVIATIONS

SiO_2	:	Silicon Dioxide
TiO_2	:	Titanium Dioxide
$TiSi_x$	:	Titanium Silicide
FET	:	Field Effect Transistor
Si	:	Silicon
MOSFET	:	Metal-Oxide Semiconductor Field Effect Transistor
EOT	:	Electrical Oxide Thickness
V_{TH}	:	Threshold Voltage
I_{OFF}	:	Leak Current
ITRS	:	International Technology Roadmap for Semiconductor
V_{GS}	:	Gate Source Voltage
V_G	:	Gate Voltage
LPCVD	:	Low Pressure Chemical Vapor Deposition Process
BPSG	:	Borophosphosilicate Glass
PMD	:	Pre-metal dielectric
CF	:	Control Factor
I_D	:	Drain Current

CHAPTER 1

INTRODUCTION

1.1 Introduction

This chapter gives a concise presentation about the N-type Metal-Oxide Semiconductor (NMOS) with high permittivity (high-k), metal gate and furthermore with included bi-layer graphene. The background of the materials involved is first clarified. Then preceded by the project's problem statement, which would also contribute to the project's goals. The project scope will then be determined and thus the project limitation will also be discovered. Finally, a description of the report’s organization will be made.

1.2 Background

It can be said that scaling of Metal-Oxide Semiconductor or also known as MOS transistor appears to be the crucial factor in the silicon based semiconductor industry for continuous improvement. Reducing the dimension of the MOS transistor is known as scaling, a proper decrease in oxide thickness is needed to compliment the decrease in channel length. Scaling has been sought after by Moore's Law for quite a few years which gives direction to semiconductor format to expand the thickness and speed of the circuit. It permits improved circuit effectiveness and lift the chip's presentation because of the way that more semiconductors can be incorporated in one single chip [1]. However, with reduction in channel lengths, it is also necessary to reduce the oxide thickness appropriately. The thin oxide films that are exposed to quantum mechanical burrowing bring about a gate outflow current that increments exponentially as the oxide thickness is diminished [1]. Thus, it is ideal to use high-permittivity or known as high-k dielectric as a dielectric replacement for the oxide gate in any further scaling. In this research, the conventional silicon dioxide (SiO_2) and poly-silicon present in NMOS device are replaced by high-k dielectric, TiO_2 and $TiSi_X$ as metal gate respectively. The extreme measurement decrease doesn't generally satisfy with gadget execution and postures issues that still can't seem to be comprehended. High-k material will assists in solving increasing in gate dielectric capacitance in order to manage short channel effects and decrease gate leakage problems. The normal after effects of this exploration are to accomplish the targets of this task which is to structure a bi-layer graphene titanium dioxide (TiO_2) and titanium silicide ($TiSi_x$) on high-k gate 22 nm NMOS device by utilizing Silvaco programming so as to create high dependable NMOS in little scope size. Graphene is defined as a single thin layer of pure carbon atom arranged on the surface of a honeycomb

structure. It is the most slender material better-known, be that as it may, it is passing strong, light and adaptable. It lead heat better than gold and will direct power superior to silver. This one of a kind mix of properties makes graphene a perfect stage for adaptable gadgets [2].

A run of the mill silicon innovation is moving toward its nonstop balancing of critical resource and physical cutoff points, there's a developing push to appear for fresh out of the plastic new stage to configuration circuits or gadget for nanoeletronic applications. A high electrical field effect that ends up in an electrostatically tunable transporter may be one of the most critical characteristics of graphene thickness inside shift of $n < 10^{14}$ cm [3]. Regularly with high transporter versatility for the two electrons and openings (as high as 10^{14} cm^2/Vs at room temperature), this pulls in a great deal of consideration regarding graphene as a potential material for a future peak performance field effect transistor (FET) [3].

According to the dielectric input content, silicon dioxide (SiO_2) has been ingested for decades or in such a traditional way, and thus film thickness is needed for the scaling pattern of the flow device. In this case the tunneling current can increase exponentially, leading to increased dissipation of power. Expanding the power dispersal would be a fundamental issue due to the thermal guidance problems in submicron gadget structures. In addition, the utilization of flimsy oxide films not too solid [4]. In order to encounter this issue, various new high-k dielectric materials were introduced as exchange for SiO_2 dielectric film entrance. Exploration of several metal oxides (Al_2O_3, HfO_2, TiO_2, ZrO_2 and etc.) and ferroelectric content and researched as contenders to supplant SiO_2. Be that as it may, In the NMOS transistor, the mixture of polysilicon (poly-Si) and high-k gate still be considered as relevant. [4].

1.3 Problem Statement

With the rapid development trend, current semiconductor industries have balanced their creation strategy and keep developing new product to ensure they can compete and fulfill industry current needs. With regards to that, the size of the MOSFET is getting smaller over the years due to advanced technologies in scaling down the device into nanometer size. Since the smaller dimension of a scaled down MOSFET gives an advantage for its application including better performance, which resulted in reduction of the overall cost. But at the same time it is causing thickness reduction of oxide and the length of metal gate. Scaling is known as a particular property of MOSFET in light of the fact that it permits to diminish the size in nanoscale district. Scaling licenses the decrease in measurement in all perspective yet could not continue scaling until the end of time. There is a scaling limit above which the system does not integrate an unforeseen outcome [5]. The use of high-k as a substitution for silicon dioxide allows the gate efficiency to be improved, which can address the significant rise in tunneling that can lead to increased power usage and reduced device reliability. Moving a high-k material empowers the goal of the majority of the issues related with the decreased current gate leakage and the need to improve the dielectric gate ability to handle the short channel effect. Thus, it is evident that smaller transistors need to increase the dielectric ability of the gate to monitor or resolve the short channel effect [6].

1.4 Objective

The purposes of this research are:

i. To design a bi-layer graphene Titanium Dioxide (TiO_2) and Titanium Silicide ($TiSi_x$) on high-k gate 22 nm NMOS device by using Silvaco software.
ii. To analyze and optimize the electrical characteristics (V_{TH}, I_{OFF} and current ratio) of device by using Taguchi L9 orthogonal array method.

1.5 Scope of Project

In Figure 1.1, the flowchart for the scope of work for the project is shown. The execution for the analysis depends on the reenactment and program improvement of downscaled 22 nm of NMOS device execution. The features including is the substitution of silicon dioxide with high-k, replacing polysilicon with metal gate and addition of graphene layer to complete the structure. The simulation will be done by using ATHENA and ATLAS in the TCAD software. Then, the L9 experimental array of Taguchi method is used to analyze the electrical characteristics of NMOS device. ATHENA is the Silvaco process simulator used in the manufacture of devices, while the simulation for the electrical properties of the device will be performed by the simulation module of ATLAS. The use of the Taguchi L9 orthogonal array method is added to these two simulators to optimize the results and obtained an optimum V_{TH} and I_{OFF} value according to ITRS 2012 [7].

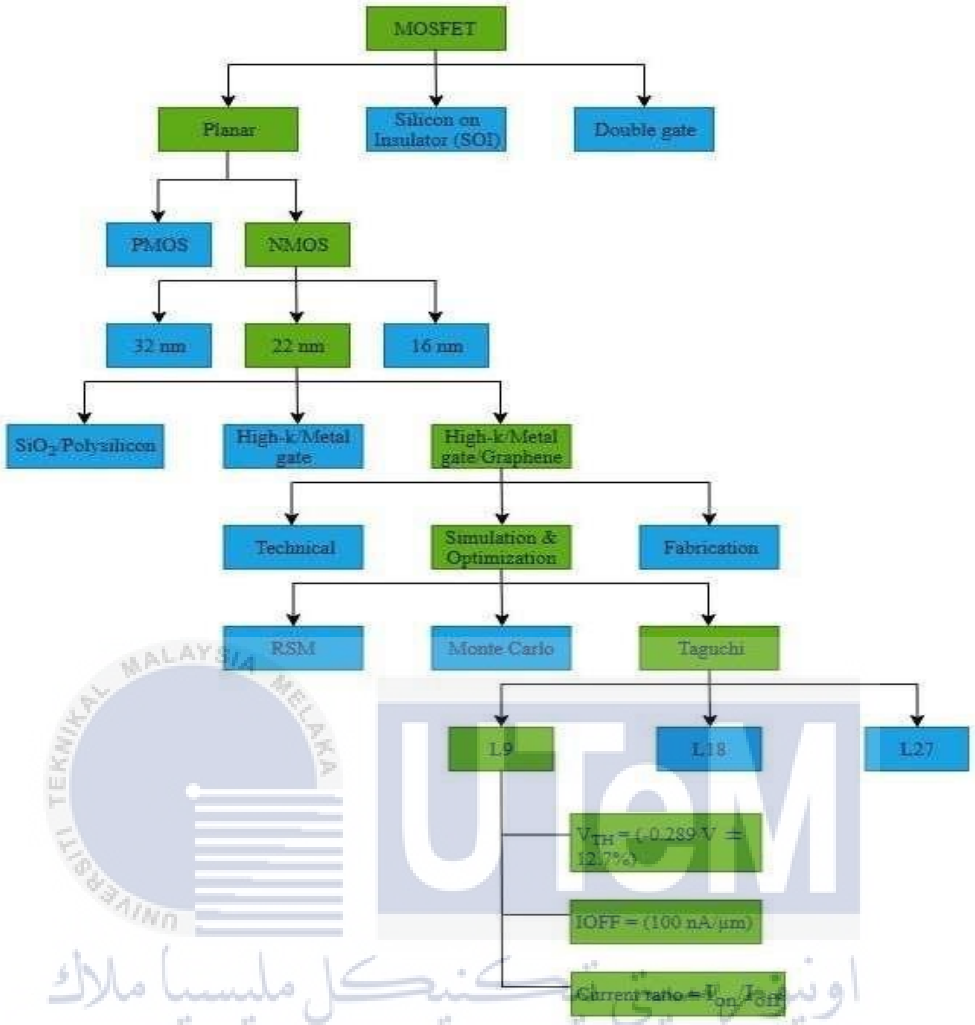

Figure 1.1: Scope of work

1.6 Organization of Report

This report comprises of five sections and starts with Chapter 1 which is the presentation of venture and end with Chapter 5 which is end and future works. Chapter 1 is basically about introduction of this project which will provide readers with early project description and concept of the whole project. Included in this chapter should explain for this project the context, issue statement, priorities, project scope and report structure.

Chapter 2 will explain about the technical parts which is cover the fundamental and basic operation of how the device works, the fabrication process and background study of all the material used for this project by referring the literature review. All related results finding from previous researchers is reviewed and studied in this chapter.

Chapter 3 is about methodology or in other words is to presents the flow of this project. In general, the work flow from beginning process of this project until the end is displayed by using flowchart. In particular, this chapter will briefly discuss regarding methods and steps involved in order to complete the project.

Chapter 4 is the results and discussion parts which will gathers the simulation result of 22 nm NMOS device structure. This chapter elaborates on the results of the NMOS performance after bi-layer graphene is added on the device. The analysis by using Taguchi method will also be explained.

The last chapter will be Chapter 5 which consists of conclusion as summarize of all the results obtained throughout this project. Recommendation and future works also provided in this part as a suggestion or improvisation that can be made in future.

CHAPTER 2

BACKGROUND STUDY

2.1 Introduction

For Chapter 2, the basic fundamental of MOSFET device and the Moore's Law which is the guideline for transistor scaling is provided in this project. In addition, this chapter has a review for every single layer material that are used to design the NMOS device.

2.2 MOSFET Transistor

Figure 2.1 shows the MOSFET structure of N-MOS and P-type Metal-oxide Semiconductor (PMOS). The metal-oxide-semiconductor field-effect transistor (MOSFET) is really comprises of four- terminal device. In addition to the drain, gate and source, there is a substrate, or body contact. Generally, for sensible applications, the substrate is connected to the source terminal. If so (and it generally is), the MOSFET might be considered as a standard three-terminal device, with the drain, gate and source the terminal of interest.

There are two sorts of MOSFET transistors that have been studied which are the NMOS transistor and the PMOS transistor, which vary in the polarity of carriers responsible for transistor current. The charge carries in NMOS transistor are electrons while charge carrier for PMOS are holes.

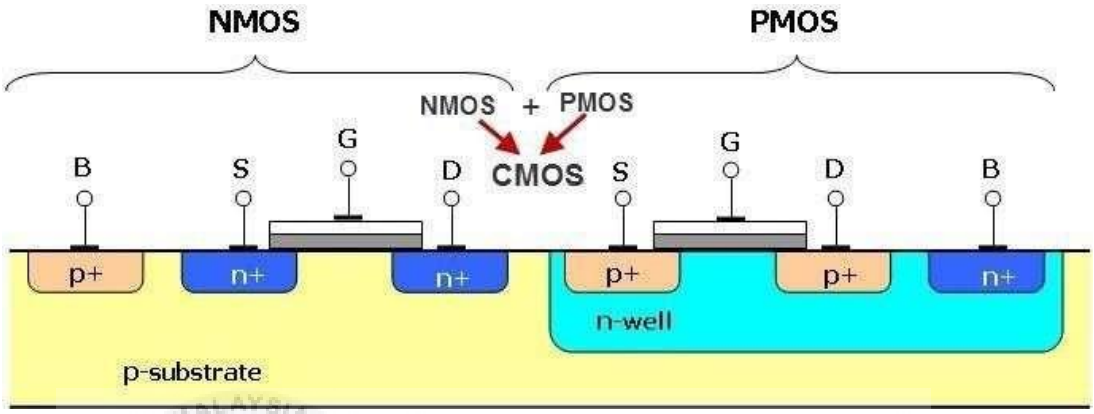

Figure 2.1: MOSFET structure for NMOS and PMOS

2.2.1 Basic Operation of MOSFET

The main structure of MOSFET device is MOS capacitor. Basically, a capacitor is formed when an insulator exists between the two voltage plates. In, MOSFET the insulator is normally form by Silicon Dioxide (SiO_2) and two voltage plate which are the top metal gate and semiconductor substrate. The following description is based on NMOS. When a small gate voltage (V_G) is applied where the positive voltage is at the gate terminal while negative voltage is at the source terminal, a depletion region is formed due to the majority carriers (holes) in the p-type substrate are repelled with the positive charge on the gate terminal. When the gate-source voltage (V_{GS}) increases, the thickness of the depletion of will also increase. This will cause the electric field to become stronger and thus begin to attract the electrons. As V_{GS} increase further, the number of electrons under the depletion region will also increase. This layer of electrons is known as an inversion layer. It will produce a channel between the source terminal and the drain terminal which will allow the current flow through it. As long

as the V_{GS} is larger than the threshold voltage (V_{TH}), there will always be a current flow through it. The same principle is applied to the PMOS. These two type of channel will be further divided as either an enhancement MOSFET or a depletion MOSFET.

2.2.2 NMOS Fabrication Process

Figure 2.2 shows the NMOS fabrication steps in which begins with oxidation method where the frequent growth around the wafer surface of a thick SiO_2 layer with 1 µm thickness. The oxide layer serves as a dopant barrier in the next step and offers an isolating layer on which other designed layers might be established [8].

In the next step, the transistor is formed in the regions specified in the surface of silicon produced in the first step. MASK 1 will then assists the photolithographic process and a junction is form as it was shaped by the wafer surface that exposed to the areas where diffusion regions in conjunction with a channel by the end of this step [8].

The transistor is created in the next step in the regions that are described within the layer of silicon dioxide formed in the first step. Silicon is then used to assist the photolithographic method and a junction transistor is formed when it was created by the wafer surface that was exposed to areas where diffusion regions were attached to a channel at the end of this phase.

Subsequently, a thin film of SiO_2 usually 0.1µm deep, mature over the entire surface of the wafer and accumulated on top of this polysilicon sheet. By using the Chemical Vapor Deposition (CVD) technique, the polysilicon layer which is 1.5 µm thickness that comprises of vigorously doped polysilicon is deposited. Exact

monitoring of thickness, concentration of impurities and resistivity is important during this phase.

Then again by exploitation the other mask or also known as MASK 2 and photographic process, the polysilicon is patterned. Poly-gate structures and poly-layered interconnections are generated using this type of technique. The thin oxide layer is extracted to reveal areas, and the n-diffusions are required as the source and drain position. The diffusion process is performed with the polysilicon and underlying thin oxide layer as the protective mask. Self-aligning is a process which shows that the source and drain are aligned automatically with the relevancy of the gate structure.

Next, a thick oxide layer is grown up everywhere once more. By undergoes the photolithographic process, the holes are created at selected areas of the polysilicon gate, drain and source regions by employing a mask known as MASK 3. Then, the aluminum layer of 1 μm thickness is deposited on the complete surface by the CVD process. With the assistance of a mask known as MASK 4, the metal layer is patterned and undergoes the photolithographic process. Necessary interconnections are provided with assistance of the metal layer.

Lastly, the entire wafer is once more lined with thick oxide layer which is known as over-glassing. The function of the oxide layer is to act as a protective layer that protects from the different elements from the environment. By using a MASK 5 mask, holes are created on this layer to allow access to bonding pads for external connections and chip testing [8].

Based on the process explained above, only the formation of NMOS enhancement-type transistor on a chip is allowed. However, the addition of an additional step is crucial if depletion-type transistor are also to be formed. Because the additional stage is critical for the development of the n-diffusion in channel regions anywhere depletion transistor is to be developed and requires a further stage between phase 2 and phase 3. Another mask will be needed to define the channel regions as the result of the diffusion process using the ion implantation technique [8].

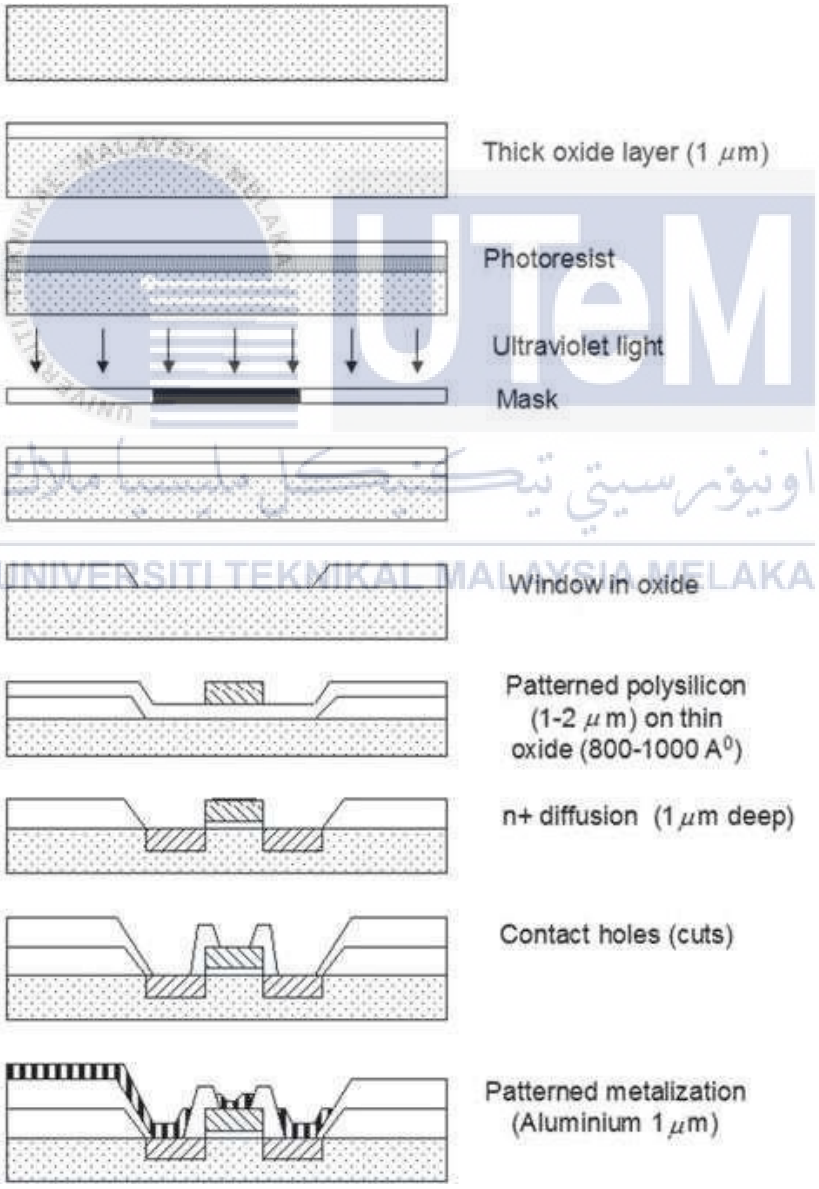

Figure 2.2: NMOS fabrication steps

2.3 Graphene

Graphene might be a molecule thick, two-dimensional (2D) material that incorporates of carbon iotas thickly sorted out into a honeycomb-like gem cross section. This can be referred to as a single layer of graphene. Bi-layer and multi-layer graphene are orchestrated inside the research facility. Unlike semiconductor materials, such as silicon, graphene do not have to be doped with impurities, which is in part the reason why graphene device show very high mobility [2]. Graphene shows very impressive electrical, mechanical, optical, thermal and alternative properties. Electrically, it is a semiconductor with zero band gap [2]. Graphene shows an awfully low resistivity, for example, only 10^{-6} W/cm at room temperature. A single later graphene film is highly not transparent, it absorbs only 2% of the white light. The mechanical properties are exceptional [2].

The technique includes creating or moving graphene on an artificial jewel or ultra-nanocystalline precious stone rather than on a customary silicon-dioxide substrate. Diamond conducts heat greater than silicon or silicon dioxide, removing additional heat off from the graphene that successively means that the surprising materials will sustain even higher current densities. The current-carrying capability of graphene will be accrued to as high as around 20 $\mu A/nm^2$ by exchange the silicon dioxide with artificial diamond or inexpensive ultranano crystalline diamond [9]. The work may encourage to create high-recurrence semiconductors, straightforward cathodes and interconnects for supplanting copper on silicon dioxide in the further MOSFET fabrication industry.

2.4 High Permittivity (high-k) Dielectric

The term high-k dielectric alludes to a material with a high dielectric constant, k (compared to silicon dioxide). In semiconductor producing processes, high-k dielectrics are used any place they are commonly acclimated supplant a silicon dioxide gate or another dielectric layer of a device. Optimum dielectric gate characteristics should have high dielectric constancy, large band gap with reasonable band orientation, low interface density and good thermal stability [10].

2.5 Metal Gate Electrode

Doped poly-silicon has been used as a gate electrode for NMOS device for past few decades. The gate electrode is made of polycrystalline silicon (poly-Si) with degenerate doping. This is often stable at high temperatures and compatible with SiO2. Poly-Si may be a sensible metal, however it is not a decent enough metal as its comparatively low carrier density provides a depletion depth of a few Å. In distinction, a good metal includes a much higher carrier density and a depletion depth of only 0.5 Å [11]. By substitute poly-Si with a standard metal, the depletion impact is expelled.

2.6 Development of Nanoscale MOSFET

Complementary metal-oxide-semiconductor (CMOS) technology has been commanding the microelectronic industry for right around fifty decades when complex semiconductor and correspondence advances begins being created. Since then, the size of CMOS semiconductor has been contracting approving through Moore's Law where highlight size of a semiconductor is scaled at a pace of roughly 0.7 occasions for every 18 months [12]. Plan decisions which considers semiconductor execution with innovation streamlining highlights alongside guaranteeing item usefulness has become the most featured angle because of the appeal for littler, quicker

and less expensive technologies. The size reduction of the MOSFET channel length often allows MOSFET activity significantly improved. Consequently, so as to keep up the recorded planar CMOS execution pattern, innovation advancements, for example, actualizing new material or new gadget structure as proposed by ITRS are required instantly to empower the rapid scaling.

2.7 Halo Implantation and Tilt Angle

Ion implantation plays an important role as a resolution for all those issues. Halo implantation process are solid possibility to remunerate varieties of different procedures since particle dosages are around simple to control inside a wafer [13].

Scaling require the use of Halo implants for control short channel effects. Halo implantation which is referred as pocket implantation is widely used in reducing the short channel effect during the downscaling. Many researchers were made to improve Halo such as junction capacitance and threshold voltage roll off. The Halo implant are frequently severally balanced for forestalling punch through. The dopant unfold within the channel frees from conventional duty of punch-through suppression and might be reduced to the body effect. A Halo implant process for the creation of halo regions of at least the first and second transistors on the same semiconductor substrates [13]. Halo implants are normally introduced once gate patterning in modern and trendy devices. A cautious tuning of pocket embed boundaries so as to acquire wanted electrical execution of nanoscale MOSFET's device is consistently essential.

Several previous works suggested that Halo with high tilt angle dramatically boosts device efficiency with reasonable off-state leakage (I_{OFF}) [14]. The exhibition furthest reaches of Halo implant and assurance of tilt edge subsequently is a basic issue and open issue. It is discovered that tilt point of Halo embed doesn't influence the last

gadget execution and (ID_{SAT} I_{OFF}) if appropriate dosage is embraced. This efficiency equivalence of tilt angle of inclination is attributed to the self-compensation between body factor and source resistance. High tilt angle due to its small junction capability should be adopted to obtain low parasitic capacitance and enhanced device performance.

2.8 Source/Drain Implantation

When device measurements of advanced CMOS technology begin to decrease, it is constantly crucial to achieve the optimum source/drain implant condition for sub-0.5 pm devices. In the case of short channel MOSFETs, unit current-voltage and capacitance-voltage (IV and CV) characteristics are prone to source/drain implant variability and annealing conditions. In order to obtain the magnificent device output and also reduce the hot-carrier effects on short-channel MOSFETs, proper selection of source/drain processing conditions is vital, particularly when the working voltage of CMOS gadgets isn't relatively scaled with device estimations. As the source/drain implant angle rises, reliability of a hot carrier for short-channel MOSFETs has been found to improve [15].

2.9 Compensation Implantation

Compensation implants are introduced into both NMOS and PMOS devices in the same lithography sequence used for source/drain implants. Normally it will be done at last process before NMOS device structure going through aluminum metallization and etching process on wafer. The purpose of compensation implantation was to reduce parasitic effects which could raise the leakage current (I_{OFF}). The effect can be seen on IV characteristic since at the I_D compensation are highly resistive diffusion in annealing process [16].

2.10 Summaries from Previous Researcher

Table 2.1: Summaries from previous researcher

No.	Reference	Author/Journal/Year	Summary
1	[3]	A. V. Klekachev, A. Nourbakhsh, I. Asselberghs, A. L. Stesmans, M. M. Heyns, and S. De Gendt, "Graphene transistors and photodetectors," Electrochem. Soc. Interface, 2013.	• Graphene has a zero-band gap and strong electric field effect. • Graphene has a high possible future in high speed FET as it has high carrier mobility for both holes and electrons.
2	[4]	A. H. Afifah Maheran, P. S. Menon, I. Ahmad, S. Shaari, H. A. Elgomati, and F. Salehuddin, "Design and optimization of 22 nm gate length high-k/metal gate NMOS transistor," J. Phys. Conf. Ser., vol. 431, no. 1, 2013.	• A 22 nm Planar PMOS transistor • Titanium Dioxide (TiO_2) and Tungsten Silicide (WSi_x) • V_{TH} = -0.29538V • ITRS = 2012
3	[5]	A. Kumar, "Leakage Current Controlling Mechanism Using High K Dielectric + Metal Gate," Int. J. Inf. Technol. Knowl., vol. 5, no. 1, pp. 191–194, 2012.	• Replacement of SiO_2 dielectric with high-k dielectric and use of metal gate instead of polygate • Aluminum Oxide (Al_2O_3) • Leakage current is minimum for Al_2O_3 (K=9)
4	[9]	N. B. Atan, I. Bin Ahmad, and B. B. Y. Majlis, "Effects of high-K dielectrics with metal gate for electrical characteristics of 18nm NMOS device," IEEE Int. Conf. Semicond. Electron. Proceedings, ICSE, pp. 56–59, 2014.	• A 18nm NMOS transistor • Combination materials of high-k and metal gate • Hafnium Dioxide (HFO_2) and Titanium Silicide ($TiSi_x$) • V_{TH} = 0.302651V and I_{OFF} = $1.9123X10^{-6}$A
5	[11]	F. Salehuddin, I. Ahmad, F. A. Hamid, and A. Zaharim, "Influence of HALO and source/drain implantation on threshold voltage in 45nm PMOS device," Aust. J. Basic Appl. Sci., vol. 5, no. 1, pp. 55–61, 2011.	• A 45nm PMOS transistor • Process parameter of HALO, Source/Drain (S/D), Oxide growth temperature and silicide anneal temperature • V_{TH} = -0.14724V and I_{OFF} = 0.190395 mA/nm

CHAPTER 3

METHODOLOGY

3.1 Introduction

This chapter will detail the project process and flow. It is including explanation about simulation of 22 nm bilayer graphene NMOS, semi analytical approach for bi-layer graphene, experimental setup for virtual transistor fabrication and the electrical properties measurement using ATHENA simulator and ATLAS simulator in the Silvaco software. Lastly, the orthogonal Taguchi L9 method is explained in last section in this chapter.

3.2 Flow of the Project

By referring to the flowchart from Figure 3.1, this project will start by designing and modeling a NMOS device with a bilayer graphene on the transistor gate. This analysis execution is based on sets of experiments, program development and physical modeling of 22 nm NMOS device performance with bi-layer of graphene using Silvaco software. The virtual fabrication of the 22 nm NMOS device is completed by using ATHENA module whereas the electrical characterization of the device has been

performed using ATLAS module from semiconductor TCAD tools. Semiconductor TCAD tools are development code programs that allow the manufacture, creation and simulation of semiconductor devices. It is always the desired simulator for complex designs realized from true industrial fabrication methods. This is because the structure that will be develop is nearer to the particular real-world device. The electrical characteristics of this device have been analyze by using L9 experimental array of Taguchi method. The value of V_{TH} and I_{OFF} after the simulation will be compared with the value based on ITRS 2012 [7].

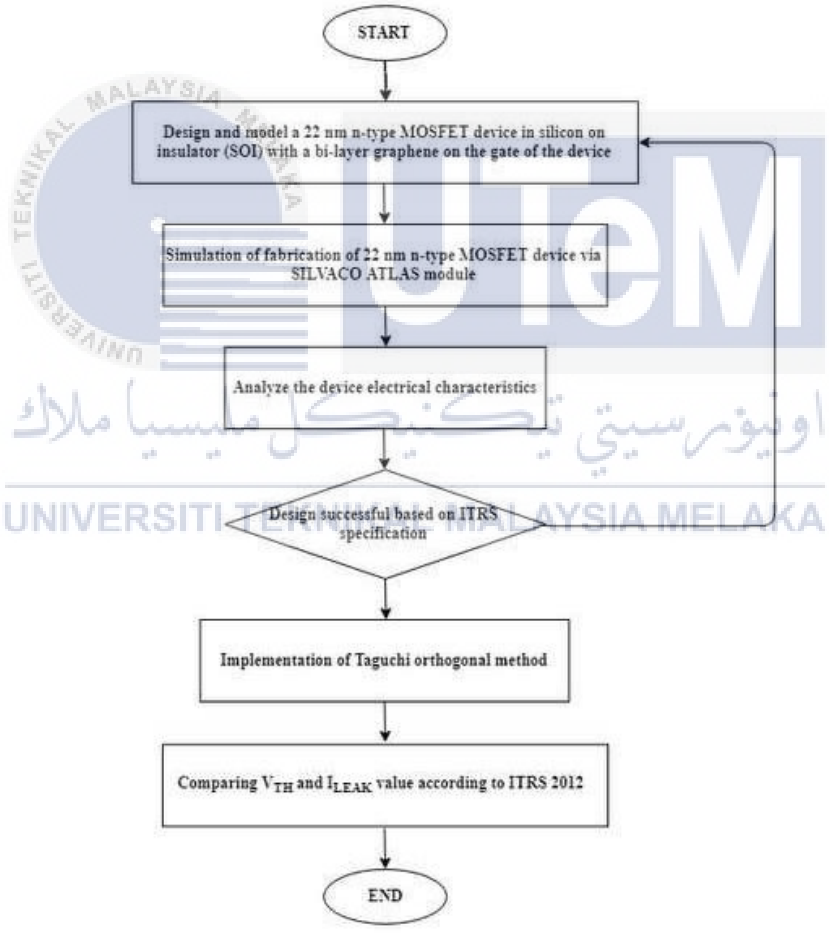

Figure 3.1: Flowchart of the project

3.3 Virtual Fabrication of 22 nm Bilayer Graphene NMOS

The fabrication of 22 nm NMOS steps are as follows. A p-type semiconductor of silicon substratum with < 100 > orientation is used and a P-well area with a dose of $3.75x10^{12}$ ions/cm^2 is formed using boron as a dopant. A Shallow Trench Isolator (STI) thickness of 130 Å is then formed by oxidizing the wafer in dry oxygen for 25 minutes, followed by an occasional low pressure chemical vapor deposition process (LPCVD) and etching process to extract surface defects. A $6.98x10^{12}$ ion/cm^2 dose of boron is implanted to the N-well active area, followed by halo implantation process by indium dose of $12.75x10^{12}$ ions/cm^2. The dosage is varied so as to induce the ideal value. The high-k material, TiO_2 (dielectric permittivity = 5.4) is then deposited for a final thickness, which is then accompanied by etching to achieve specified thickness and modified to achieve a gate length of 22 nm. $TiSi_x$ is utilized as the metal gate is then deposited on the highest part of the bulk device. Then, side wall spacers are constructed wherever it acted as a mask for the source and drain implantation. There is then implantation of source-drain when arsenic is first injected with a dose of $5.15x10^{13}$ ions/cm^2, followed by phosphorus with a dose of $1.75x10^{12}$ ions/cm^2. The next step was the creation of the 0.5μm layer of Borophosphosilicate Glass (BPSG), which functions as a dielectric pre-metal (PMD). Once BPSG deposition occurs, the wafer undergoes annealing process at a temperature of 850°C. The next step is the phosphorous compensation implantation, with a dose of $3.65x10^{13}$ ions/cm^2. Then, aluminum layer is deposited on top of the structure. Lastly, a bi-layer of graphene is added at the bottom of the metal gate ($TiSi_x$). The transistor then undergoes the cycle of electrical characteristics using ATLAS simulation module to classify the device's leakage current with respect to ITRS 2012[7].

3.4 Semi Analytical Approach for Bi-layer Graphene

The simulation of the device in this analysis reflected all the physical effects of graphene material. The whole operation is probable to operate at room temperature (T=300K) with a bandgap is set at 0.55eV, permittivity of 2.4, carrier mobility with top-gated material, an oversized value of 100 ns for radiative recombination rate of electron and holes, and the effective field E_{eff} = 0.4MV/cm while the electron and hole densities of states were calculated and is earned from [17]:

$$Nv = \frac{8\pi mnkT}{h2} \ln(1 + e^{-(Ef - Ev/kT)}) \quad (1)$$

$$Nv = \frac{8\pi mnkT}{h2} \ln(1 + e^{-(Ec - Ef/kT)}) \quad (2)$$

The effective mass of the electrons and holes of Graphene are set at me≕0.06 mo, mh≕0.03 mo and mo is the free electron mass [17].

3.5 Silvaco Software

Performing an actual Silvaco ATHENA module is an associated example of a TCAD tool that will be effectively controlled and manipulated to find out the downscaling method. It would give the traditional way of doing things an economic and speed edge [18]. Semiconductor TCAD tools are computer code programs that permits the design, manufacture and simulation of semiconductor devices. Such simulations offered an opportunity to determine the impact of various process parameters on the general output of devices [19]. All the simulation of systems has to allow improvements to recommend optimum efficiency for MOSFET technology. Optimizing manufacturing operations and products is one of the important industrial functions that similarly boosts merchandise performance on saving production costs.

There are many sub-bundles in Silvaco so as to actualize the different required strides for the Si device reproduction. These are ATHENA (for fabrication process simulation), DevEdit (for defining the structure geometry and mesh editing), DeckBuild (which shows the run time output of the simulations), ATLAS (which is a main device simulator tool in Silvaco) and TonyPlot (which can be used to visualize the simulation results). Such subsets may be used to model interface currents, functionality between specific electrodes and transient signal analysis. Further, different outer circuit components like resistor, inductor and capacitor can be associated with device anodes to copy the real estimations on devices.

3.5.1 ATHENA Simulator

ATHENA undergoes device manufacturing simulation and processing techniques such as deposition of materials, oxidation and etching. In utilization of ATHENA simulator the production of the 22 nm NMOS device begins with wafer preparation, followed by well formation, insulation, transistor production and interconnection. The technique and procedure is really comparative with the genuine fabrication process. Energy, dosage and tilt angle are parameter that need to be considered. The value of those parameters determines the value of the V_{TH}.

3.5.2 ATLAS Simulator

ATLAS give insight into the internal characteristics of semiconductor devices such as field, current densities, carrier densities and ionization/recombination rate. The ATLAS simulation module carry out equipment simulation procedures for optical, electrical and thermal properties. Electrical properties for example continuous current (DC), alternating current (AC), and V_{TH} for the manufacture of semiconductor devices can be analyzed by using this simulator. For this research and study, when the 22 nm

NMOS device is built using ATHENA simulator, then to simulate the I_D -V_{GS} and I_D -V_{DS} for the MOSFET device, ATLAS simulator will be used.

ATLAS will be used collectively of the simulators among the VWF Automation TOOLS. VWF makes extremely controlled simulation-based testing possible. VWF is employed in such a manner that experimental research and production methods are precisely replicated using divided lots. This thus strongly ties simulation with the advancement of technologies, resulting in far greater gains from simulation use.

3.5.3 Fabrication Steps

The assembly of recent MOS ICs uses a wide number and variety of simple manufacturing measures. An equivalent method can be used for the design of NMOS, PMOS and CMOS devices. The gate material is either metal or poly-silicon. The foremost ordinarily used substrate is bulk silicon or silicon-on-sapphire (SOS). In preparation for prevent the existence of parasitic transistors, the methods used to separate the system within the wafer include variations.

3.5.4 Silicon Substrate

Processing is performed on a thin wafer cut crystal of high purity silicone into which the necessary P-impurities are introduced as the crystal is fully grown. Sometimes wafers are about 15 to 75 mm in diameter and 0.4 mm thick is doped with boron to impurity concentrations of $10^{15}/cm^3$ to $10^{16}/cm^3$, giving resistivity in approximate range 2 ohms/cm to 25 ohms/cm.

3.5.5 Mesh and Substrate Material Establishment

The orientation <100> of p-type silicon is used as primary substrate for this project. The accumulated layer of Silicon Oxide (SiO_2) is the deposited on the substrate. Boron injected into the silicon substrate for approximately $7.0x10^{14}$ atom/cm^3 with the orientation <100>. Figure 3.2 shows the beginning growth of bulk silicon implanted by boron.

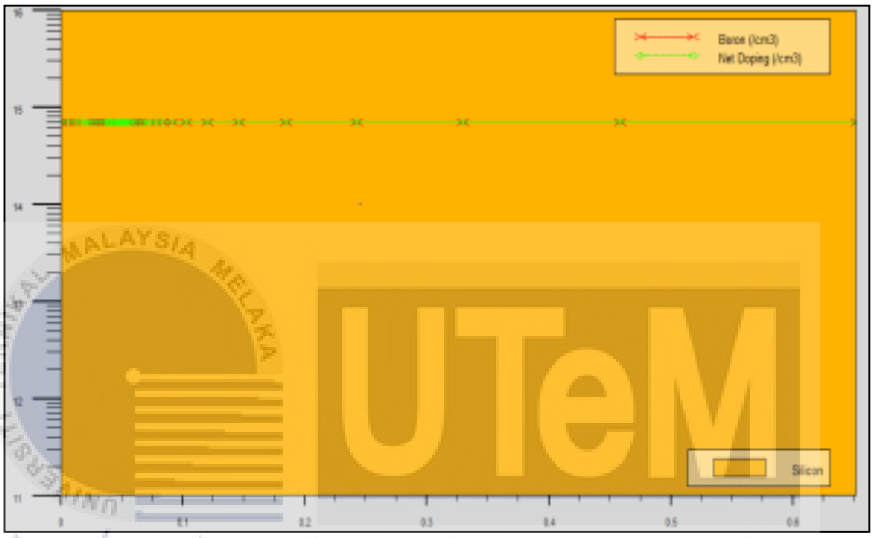

Figure 3.2: P-type substrate doping concentration

3.5.6 Well Oxidation

In advance for developing 22 nm NMOS is creating the p-well structure by developing 200 Å oxide on top of the wafer with temperature is 970°C. the mask for p-well implantation process needed the oxide layer. Figure 3.3 shows that the structure after the process of implementation boron with implant boron dose is $7.0x10^{13}$ atom/cm^3 to create p-well.

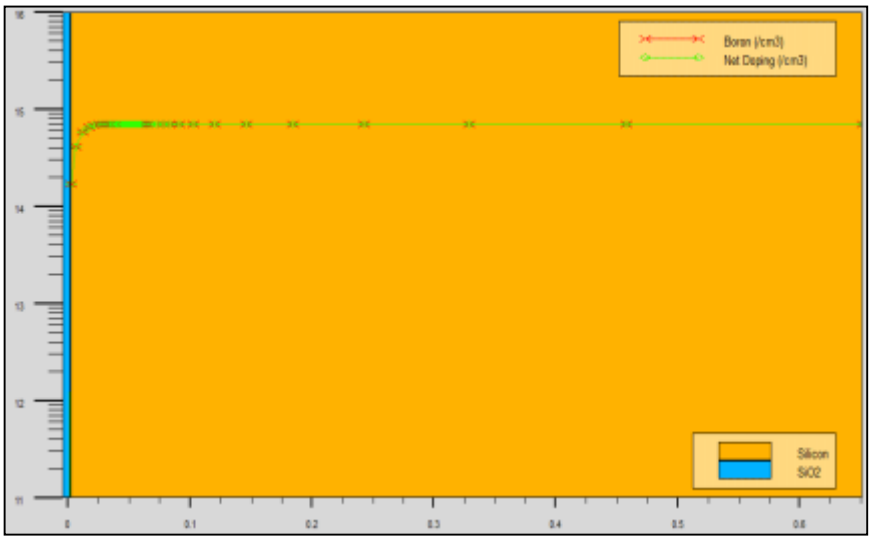

Figure 3.3: 22 nm structure after oxide deposition

3.5.7 Trenching and Gate Oxide Growth

Figure 3.4 shows the growth of gate oxide in dry oxygen at 812°C. For subsequent diffusion, the field oxide is used to trace and describe the source and drain areas. Gate oxide is considerably thinner and is constructed to have oxide of better consistency than field oxide.

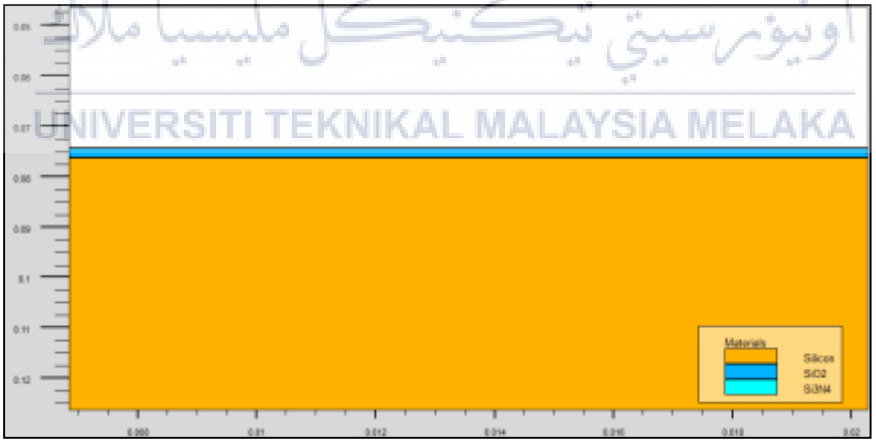

Figure 3.4: Structure after gate oxide growth

3.5.8 Threshold Voltage Adjustment Implantation

The next step is grown gate oxide and followed by a threshold voltage adjustment, which is the process is done in the channel region by using difluoride (BF_2). The 22 nm NMOS structure after threshold voltage adjustment implantation is shown as in Figure 3.5. Threshold voltage adjustment is often performed with low doses as a result of slight modification of the gate concentration has been decent and sufficient for the adjustment.

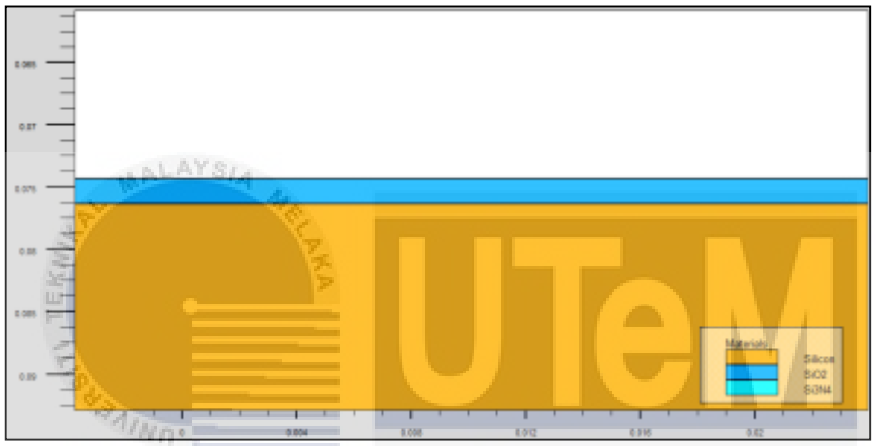

Figure 3.5: 22 nm NMOS structure after V_{TH} adjustment implantation

3.5.9 High-k Dielectric Deposition

The deposition of high-k TiO_2 process materials with oxide thickness is scaled-adjusted for this application such that they require the same EOT with SiO_2 by studying the electrical characteristics of the device. The length of the high-k material is scaled and adjusted so as to induce 22 nm same value as the gate length of the transistor. The process is done when a dose of boron is implant on N-well active area for threshold voltage adjustment process. Next, the process done for deposited Titanium Silicide ($TiSi_x$) on top high-k materials which is Titanium Dioxide (TiO_2). Figure 3.6 shows 22 nm NMOS structure after high-k deposition.

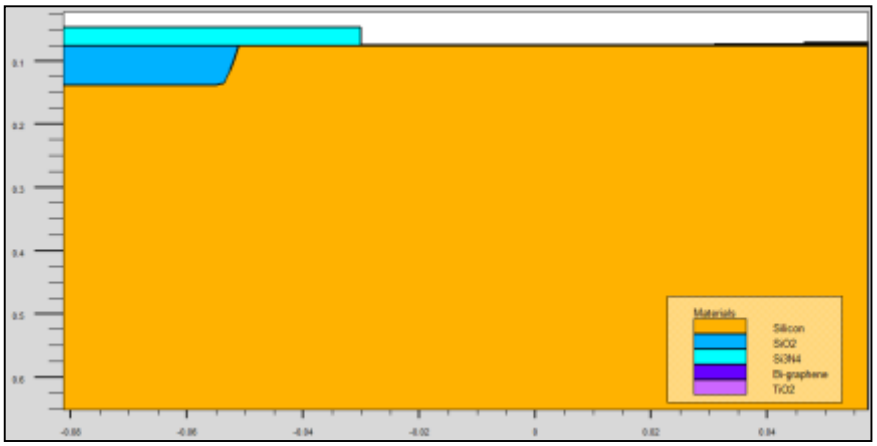

Figure 3.6: 22 nm NMOS structure after high-k deposition

3.5.10 Halo Implantation

Indium is doped in a halo implantation process to obtain optimal performance for 22 nm NMOS device. This is done by having a P-type impurity ion implanted within the NMOS substrate to the specified depth before forming an N-channel lightly doped source/drain area. The halo implantation is done by forming halo structure at the desired location to reduce channel effect. Figure 3.7 shows the structure of 22 nm NMOS device after halo implantation.

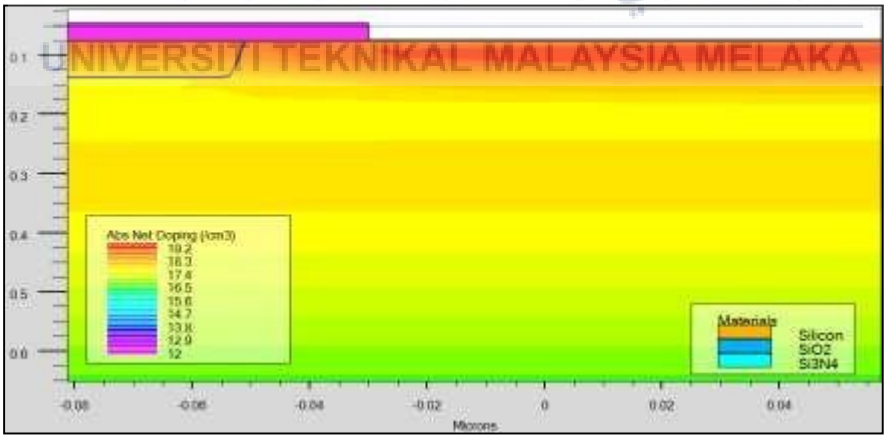

Figure 3.7: 22 nm NMOS structure after Halo Implantation

3.5.11 Sidewall Spacer

The 22 nm NMOS structure is again deposited by the nitride chemical compound after the halo implantation phase. The layer Si_3N_4 is created on the surface of silicon and polysilicon. The process known as creating sidewall spacer. Then, mask is used for source/drain implantation. The structure of 22 nm NMOS after sidewall spacer process is shown in Figure 3.8.

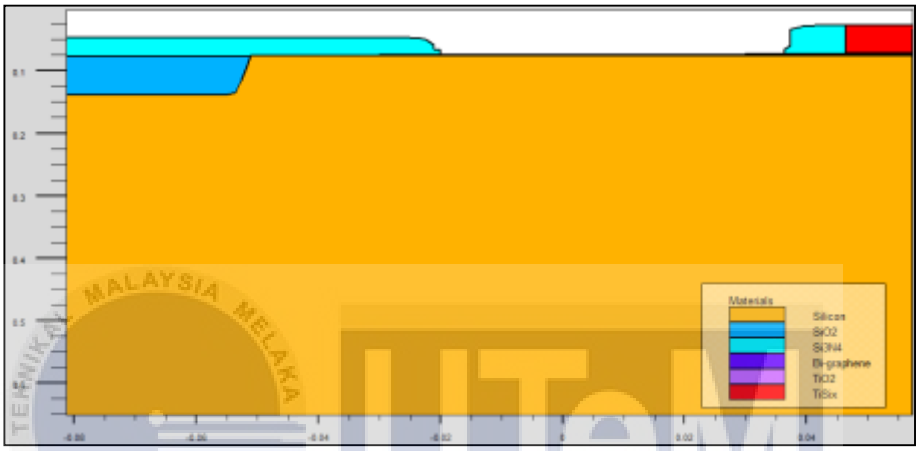

Figure 3.8: 22 nm NMOS structure after sidewall spacer applied

3.5.12 Source/Drain Implantation

The arsenic atom is injected into the p-type substratum to show the highly n-type doped area. This region is employed to ensure the smooth surface current flow in 22 nm NMOS device. The structure of 22 nm NMOS device after source/drain implantation is shown in Figure 3.9.

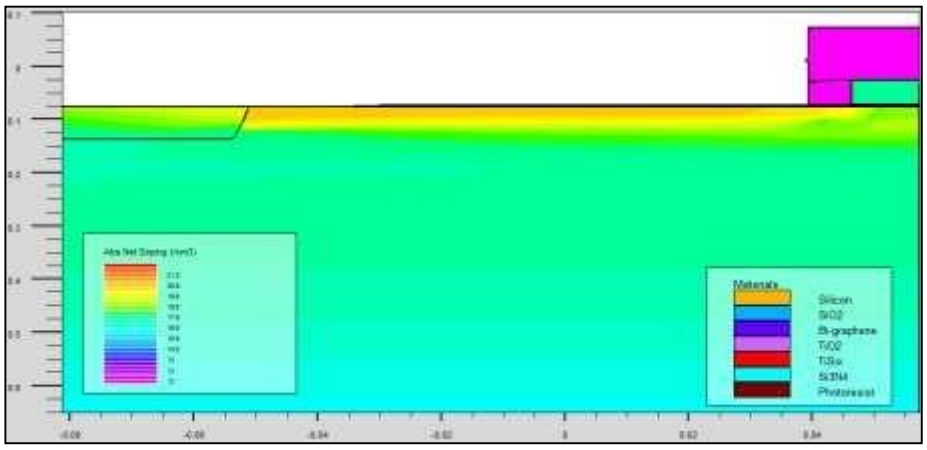

Figure 3.9: Structure after source/drain implantation

3.5.13 Pattern Source and Drain Contact and Compensate Implantation

Furthermore, the source/drain contact is patterned as shown in Figure 3.10. The contact is really to permit current move through the source and channel. After that, compensate implantation process is carried out. Compensate implantation is performed to reduce side capacitance effect.

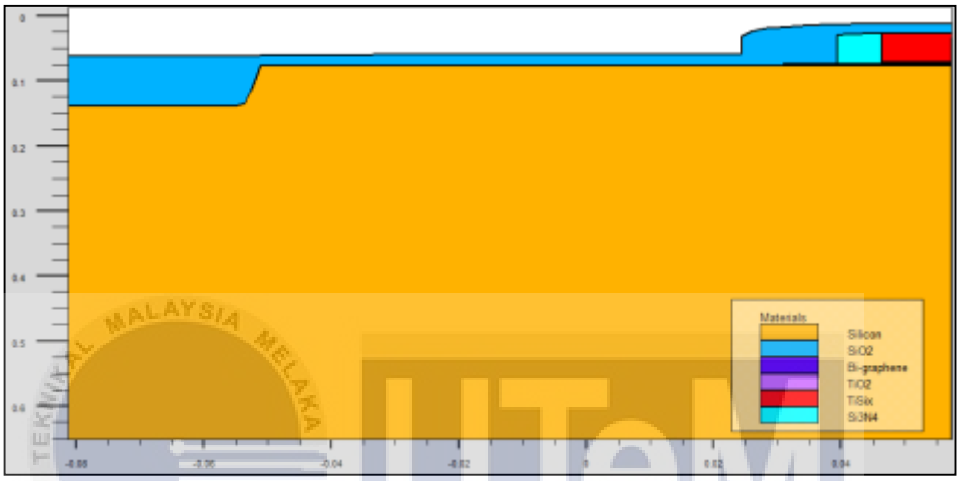

Figure 3.10: After source and drain contact and compensate implantation process

3.5.14 Aluminum Metallization

The 22 nm NMOS structure is connected with aluminum metal followed by depositing the second aluminum layer on top of the Intel-Metal dielectric which the structure is shown on Figure 3.11. Aluminum layer if functional for easy wire bonding attachment in packaging semiconductor process.

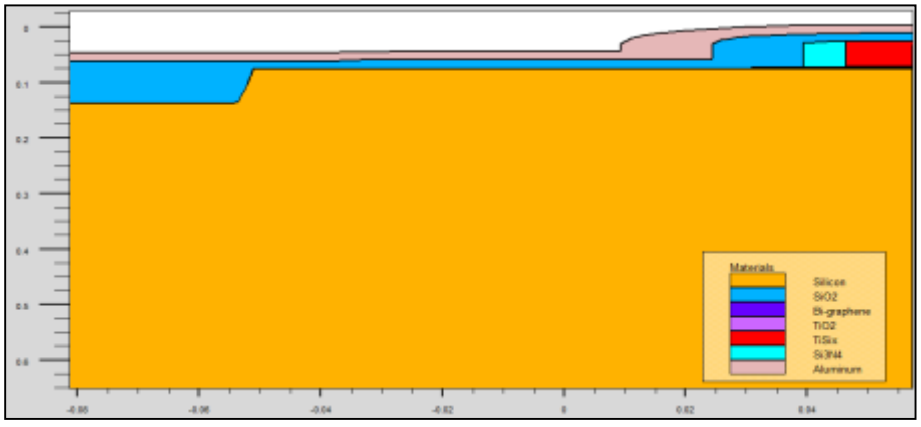

Figure 3.11: Structure after aluminum metallization

3.5.15 Aluminum Etching

Any unwanted aluminum is etched to develop the contacts. Aluminum etching is highly exothermic an under etching of the resist mask causes local heating, agitation is performed if no local heating occurred. The 22 nm NMOS structure after etched the excessive aluminum area is shown in Figure 3.12.

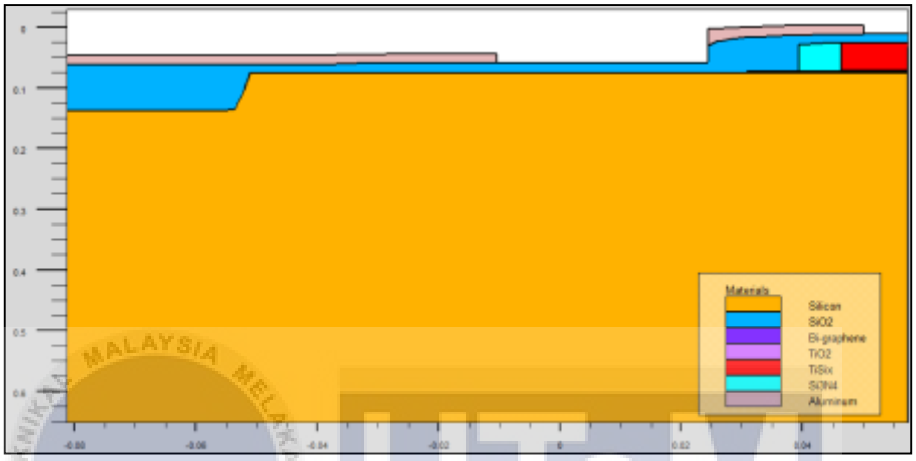

Figure 3.12: Structure after etching excess aluminum

3.5.16 Adding Bi-layer Graphene

Lastly, the permittivity of graphene is adjusted to 2.4. Then, a bi-layer of graphene is added at the bottom of the metal gate ($TiSi_x$) as shown in Figure 3.13.

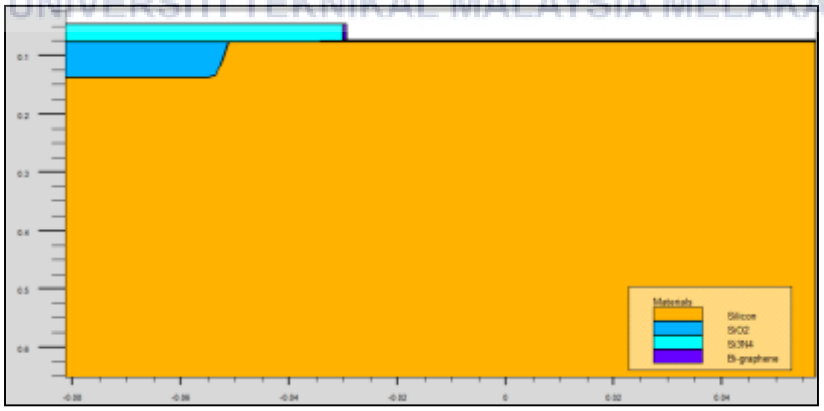

Figure 3.13: Bi-layer graphene on NMOS structure

3.6 Taguchi Method

An orderly and productive approach to accomplish this is regularly utilize a streamlining strategy for arranging tests dependent on Taguchi Method [20]. Taguchi strategy give the preeminent prudent and practical arrangement in such cases with insignificant test preliminaries.

L9 Taguchi approaches are presented to withdraw maximum significant data with least number of experiments. It is an experimental design optimization which utilizes Orthogonal Arrays (OA) for creating a matrix of experiments without violating some limitation [21]. The goals are to help inventors to learn and analyze the impact of different manageable factors on the normal of quality characteristics and the distinctions efficiently. In the research, four control factors (CF) and two noise factor (NF) were chosen based on established research papers in. The factors are identified as the most influential parameters for V_{TH} and I_{OFF} [22].

Table 3.1: Standard L9 Orthogonal Array

Experiment No.	Factor A	Factor B	Factor C	Factor D
1	1	1	1	1
2	1	2	2	2
3	1	3	3	3
4	2	1	2	3
5	2	2	3	1
6	2	3	1	2
7	3	1	3	2
8	3	2	1	3
9	3	3	2	1

CHAPTER 4

RESULTS AND DISCUSSION

4.1 Introduction

This chapter reveals general structure of the simulation for NMOS device. This chapter will explains the results of adding a bi-layer of Graphene on 22 nm NMOS device after simulated by ATHENA and ATLAS module of Silvaco software. Basically, the results will be discussed in depth in this chapter.

4.2 Simulation Result of Structure

Both ATLAS and ATHENA have done by using simulation. ATHENA is used to initiate 22 nm gate length NMOS structure with additional of bi-layer graphene. Graph for displaying the values of threshold voltage (V_{TH}) and leakage current (I_{OFF}) is obtained from ATLAS.

4.2.1 Structure of 22 nm NMOS with Bi-layer Graphene

Overall device structure with enlarge figure of a 22 nm gate length of the high-k/metal gate NMOS transistor are shows in Figure 4.1. The body dimension and also for the S/D electrode is shown on the figure below. The structure is designed by using mirroring technique, which is the structure is design only half-cell on the left side and then mirrored it on the right side to get full structure of the MOSFET. Meanwhile, Figure 4.2 displays the NMOS structure applied with bi-layer graphene to it. Figure **4.3** shows the doping profile of 22 nm NMOS device.

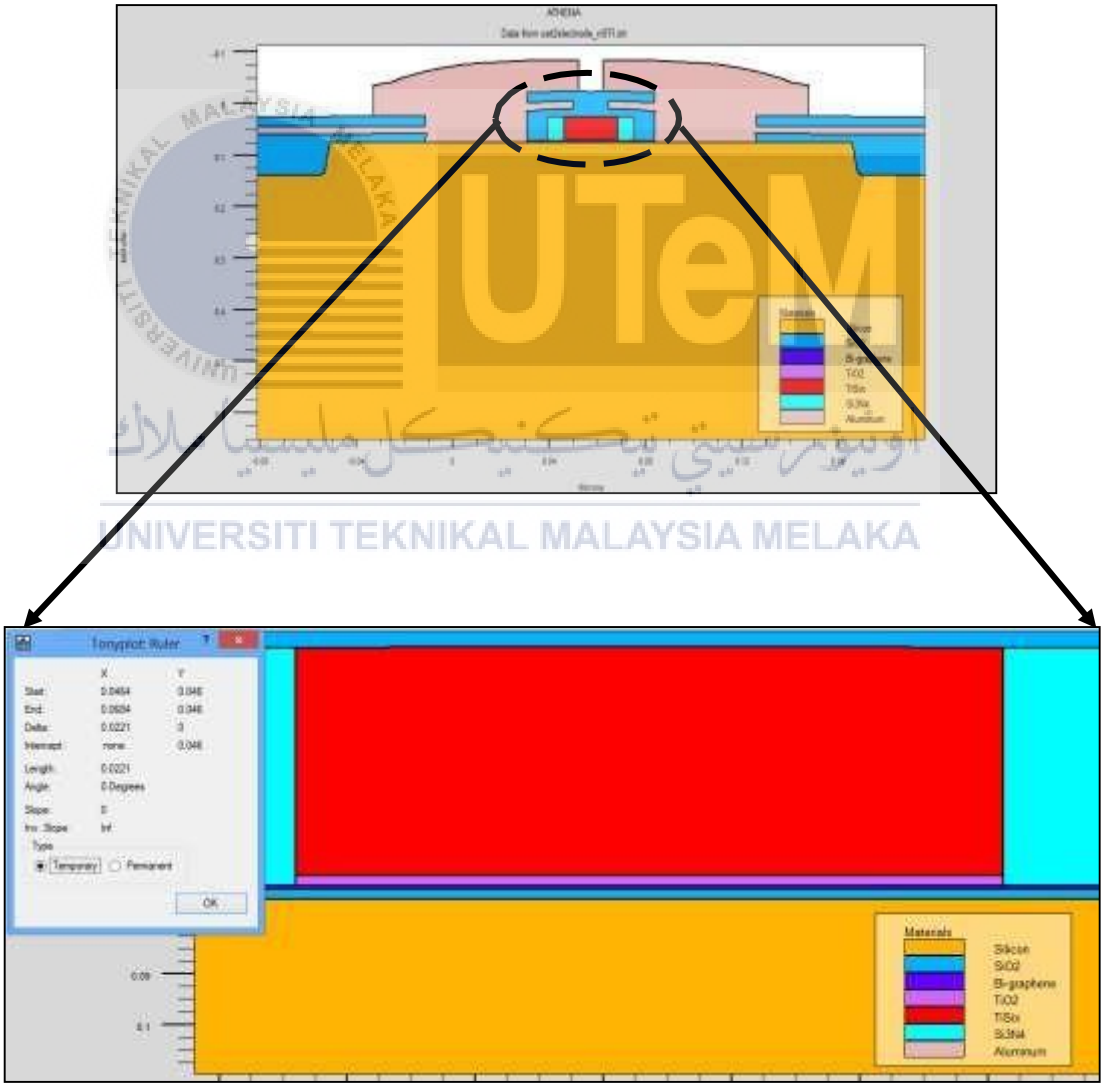

Figure 4.1: Completed NMOS transistor with 22 nm gate length

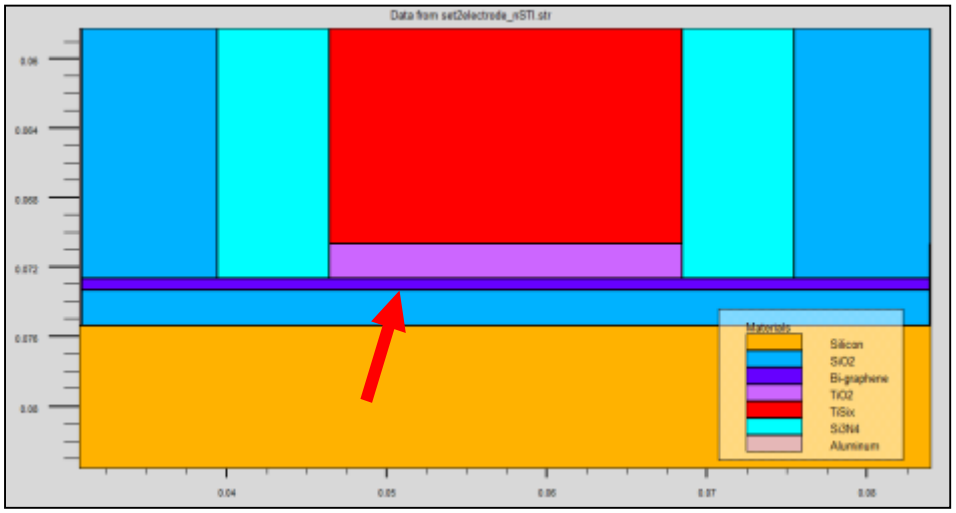

Figure 4.2: Additional of bi-layer graphene on MOSFET structure

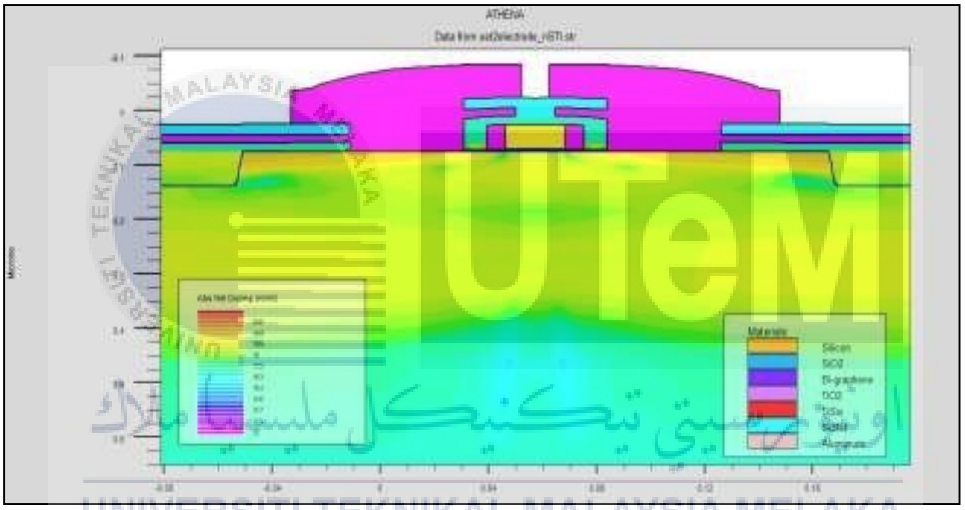

Figure 4.3: The doping profile on the 22 nm NMOS transistor

Figure 4.4 shows the chart of channel current, I_D (An) against channel voltage, V_{DS} (V), while Figure 4.5 shows the diagram of I_D-V_G for 22 nm NMOS device. Drain leakage current (I_{OFF}) or sub-threshold current leakage occurs when the voltage at the gate is lower than the voltage threshold. Ideally, if the transistor is in "OFF" state, V_{GS} = 0 volt and V_{DS} = V_{DD} (voltage supply), no current will flow through the channel (I_{OFF} = 0). The great performance of MOSFET design is when I_{OFF} is equal to zero and the I_{ON} value higher. As device dimensions are getting smaller, leakage current are becoming as one of the major parameter which needs to be emphasize.

Voltage V_{DS} = 1.1 V is applied for $I_D - V_{DS}$ graph with discrete voltage of V_{DS}. While V_{GS} = 0.5 V is supplied for with different voltage V_{GS}. The threshold voltage (V_{TH}), state on current (I_{ON}) can be extract and current leakage (I_{OFF}) can be extracted from $I_D - V_{GS}$ curve. The value of voltage threshold is determined by voltage threshold adjustment equal to 0.4V since the gate voltage starts to rising up at 0.5V. When V_{GS} is equal or less than $V_{TH,}$ the drain current will always remain to zero even the voltage drain-source (V_{DS}) increase.

To define the various points in I_D - V_{GS} on the transfer characteristic, only V_{DS} saturation is employed. In order to plot the curve, the condition for saturation region can be expressed as:

$$V_{DS_{sat}} = V_{GS} - V_T$$

Or

$$V_{DS} \geq V_{GS} - V_T$$

The threshold voltage is a very important device parameter to design, model, simulate and utilize MOSFET. Traditionally, the threshold voltage of MOSFET was known as the gate voltage needed to ensure that the surface potential in the bulk of the semiconductor is equal to twice the Fermi.

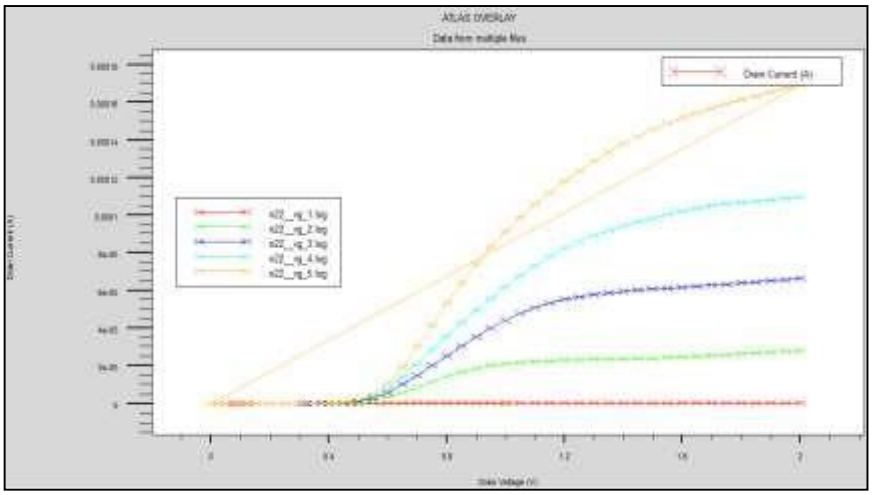

Figure 4.4: Graph of drain current, I_D (A) against drain voltage, V_{DS} (V)

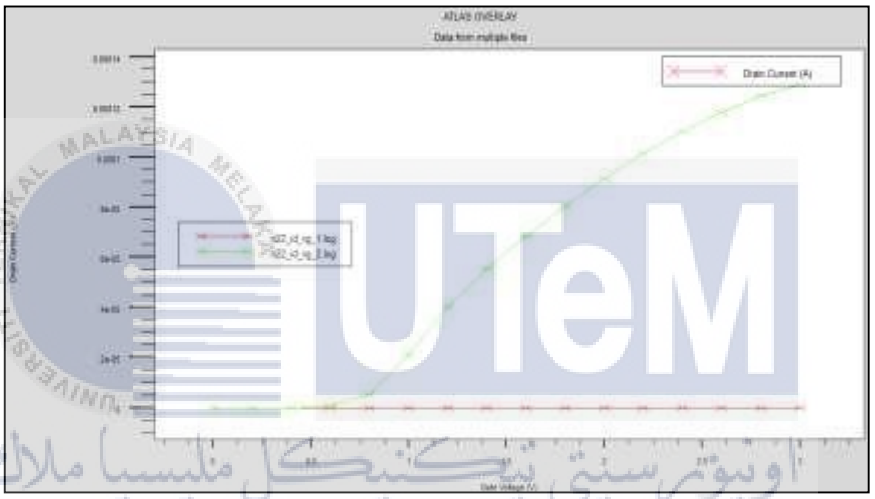

Figure 4.5: Graph of I_D – V_G for 22 nm NMOS device

The consequences of the gadget qualities for the 22 nm NMOS gadget with additional of bi-layer graphene is appeared in Table 4.1. The device is suitable for high power application because it displays low I_{OFF} ratio in the sub threshold region of operation.

Table 4.1: Results of device characteristics for 22 nm NMOS device

Parameter	Device (simulation) $TiO_2/TiSi_x$ with bi-layer graphene	ITRS 2012
V_{TH} (V)	0.279852	0.289
I_{OFF} (nA/μm)	129.099	100
I_{ON} (A/μm)	0.000129099	1.0×10^{-7}
I_{ON}/I_{OFF}	15751.48	16000

4.3 Taguchi Orthogonal L9 Array Method

The L9 Taguchi symmetrical cluster technique is utilized to decide the streamlining of the gadget's procedure boundary so as to accomplish the best blends of procedure boundaries bringing about high device execution through various analysis. Although it seems to have the same concept of fractional factorial designs, it differs as it has an additional Parameter Design and Tolerance Design. A total of 36 running simulations was performed while taking into consideration of the three leveled, four control factors and two noise factors which will be the basis of the Taguchi L9 orthogonal array method. The control factor consists of Factor A which is the Halo Implantation, Factor B, which is the Halo Tilt Angle, Factor C which is the Source/Drain (S/D) Implantation and Factor D which is the Compensation Implantation. Then the two noise factors that are involved in this process are the Factor X and Factor Y which are the Sacrificial Oxide Layer (PSG) and P well implantation/ BPSG Oxide Temperature respectively [3]. The process parameter and noise factors are as shown below in Table 4.1 and Table 4.2 respectively.

Table 4.2: Process Parameter and Their Levels

Factor	Process Parameter	Unit	Level		
			1	2	3
A	Halo Implantation Dose	Atom/cm^2	1.170 x 10^{13}	1.175 x 10^{13}	1.180 x 10^{13}
B	Halo Tilting Angle	Degree	28	30	32
C	S/D Implantation Dose	Atom/cm^2	2.550 x 10^{13}	2.600 x 10^{13}	2.650 x 10^{13}
D	Compensation Implantation Dose	Atom/cm^2	1.450 x 10^{13}	1.500 x 10^{13}	1.550 x 10^{13}

Table 4.3: Noise Factor and Their Levels

Factor	Noise Factor	Temperature, °C	
		Level 1	Level 2
X	Sacrificial Oxide Layer (PSG)	950 (X0)	954 (X1)
Y	P-well implantation/BPSG Oxide	920 (Y0)	924 (Y1)

4.3.1 Analysis Signal-to-Noise (S/N) Ratio for V_{TH} and I_{OFF}

Nine sets of experiments which consist of 36 simulations were done utilizing the four level of Control Factor (CF) and two level of Noise Factor (NF). The simulation results for V_{TH} and I_{OFF} are shown Table 4.3 and Table 4.4 respectively.

Table 4.4: V_{TH} Results for Bi-Layer Graphene NMOS Device

Exp. No.	V_{TH}(V)			
	X0Y0	X0Y1	X1Y0	X1Y1
1	0.300144	0.269542	0.314468	0.286283
2	0.277173	0.23435	0.292506	0.252891
3	0.248324	0.201618	0.265998	0.208276
4	0.290515	0.25836	0.30538	0.275883
5	0.257148	0.204907	0.273703	0.219257
6	0.289656	0.254132	0.304515	0.272069

7	0.273469	0.227049	0.289452	0.24669
8	0.304007	0.27525	0.317333	0.290842
9	0.269946	0.220251	0.286211	0.240426

Table 4.5: I_{OFF} Results for Bi-Layer Graphene NMOS Device

Exp. No.	I_{OFF} (nA/μm)			
	X0Y0	**X0Y1**	**X1Y0**	**XIY1**
1	8.14499	8.23367	8.35027	8.44448
2	8.20403	8.31148	8.41484	8.52302
3	8.28805	8.40518	8.4986	8.61001
4	8.16468	8.2583	8.37217	8.46901
5	8.25914	8.36472	8.47178	8.57372
6	8.16261	8.27149	8.36808	8.481
7	8.2177	8.32355	8.42867	8.5342
8	8.11233	8.21131	8.3171	8.42184
9	8.22584	8.33836	8.43551	8.54767

The results are used to verify the factor that provide with the most significant effect on the device performance through Signal-to-Noise (S/N) ratio calculation. The V_{TH} investigation has a place with the ostensible the-best quality attributes while its I_{OFF} has a place with the littler the-best quality trademarks. The statistical method is used to get the nominal value of V_{TH} as well as the lowest possible value for I_{OFF}. The S/N ratio of nominal-the-best, ŋNTB can be expressed as:

$$\eta NT = 10 \log 10 \left[\frac{\mu^2}{\sigma^2} \right]$$

and

$$\boldsymbol{u} = \frac{\boldsymbol{Yi} + \cdots + \boldsymbol{Yn}}{\boldsymbol{n}}$$

$$\boldsymbol{\sigma^2} = \frac{\sum_{\boldsymbol{i}}^{\boldsymbol{n}} (\boldsymbol{Yu} - \mu)^2}{\boldsymbol{n} - \boldsymbol{1}}$$

Where n indicates the number of experiments, Yi is the experimental value of V_{TH}, μ is mean and σ is variance. The S/N ratio of smaller-the-best for I_{OFF}, ηNTB can be expressed as:

$$\eta STB = -10 \log 10 \left[\frac{1}{2} \sum Y_1^2 + Y_2^2 + Y^2 \right]$$

Where n is the number of experiments, Yi is the experimental value of I_{OFF}. The η (S/N ratio) of every simulation for V_{TH} and I_{OFF} are measured by applying the formula in Equation (4.1) and Equation (4.4). In this calculation, the effect of S/N ratio can be parted out at every level the fact that the test configuration is symmetrical.

The S/N ratio of each level of Control Factor (CF) for V_{TH} and I_{OFF} and the calculation of the overall mean of S/N ratio are summarized in Table 4.6 and Table 4.7 respectively. The value of S/N ratio specifies the significance of a CF to lessen the variation. The higher the value of ratio, the better the characteristic quality of V_{TH} and I_{OFF}, hence, the greater the impact on the device performance.

Table 4.6: S/N response for V_{TH}

Factor	S/N Ratio (Mean)			Total mean S/N ratio
	Level 1	Level 2	Level 3	
A	20.43	20.85	20.82	
B	22.00	20.67	19.43	20.7
C	23.39	20.63	18.09	
D	19.93	20.60	21.57	

Table 4.7: S/N response for I_{OFF}

Factor	S/N Ratio (Mean)			Total mean S/N ratio
	Level 1	Level 2	Level 3	
A	161.55	161.56	161.57	
B	161.59	161.57	161.53	161.56
C	161.62	161.56	161.50	
D	161.55	161.56	161.57	

4.3.2 Analysis of Variance (ANOVA) for V_{TH} and I_{OFF}

The most widely recognized factual examination to gauge the level of commitment of a factor that fundamentally influences the device execution is the investigation of analysis of variance (ANOVA). The analysis also includes the sum of square (SS), the degree of freedom (DF), the mean square and the percentage of factor effect of the S/N ratio. As seen in Table 4.8 and Table 4.9 respectively, ANOVA findings for V_{TH} and I_{OFF} are displayed. As notice previously, the most elevated estimation of S/N proportion of a factor demonstrates that the factor has the most predominant impact on the device execution.

Based on the result of ANOVA for $V_{TH,}$ S/D implantation dose factor scored the highest value on S/N ratio with 74.65% contribution and thus is set as the dominant factor. On the other side, the Halo implantation dosage is set as an adjustment factor as it received 0.58% in the lowest S/N ratio.

Table 4.8: Results of ANOVA for V_{TH}

Performance Parameter	Control Factor	DF	SS	Mean Square	Factor Effect (%)	
					S/N Ratio	Mean
V_{TH}	Halo Implantation Dose	2	0	0	0.58	2.26
	Halo Tilting Angle	2	10	5	17.59	18.85
	S/D Implantation Dose	2	42	21	74.65	76.44
	Compensation Implantation Dose	2	4	2	7.18	2.46

The investigation of ANOVA for I_{OFF} reveals that S/D Implantation factor is the most dominant factor with 76.22% of contribution followed by Halo Tilting Angle factor at 17.60%, Halo Implantation dose at 3.67% and Compensation Implantation dose at 2.51%. This means a small change in S/D implant dopant will either increase or reduce the leakage current significantly.

Table 4.9: Results of ANOVA for I_{OFF}

Performance Parameter	Control Factor	DF	SS	Mean Square	Factor Effect (%)
I_{OFF}	Halo Implantation Dose	2	0	0	3.67
	Halo Tilting Angle	2	0	0	17.60
	S/D Implantation Dose	2	0	0	76.22
	Compensation Implantation Dose	2	0	0	2.51

4.3.3 Justification of Dominant and Adjustment factor

From the results obtained and analysis for ANOVA V_{TH} and $I_{OFF,}$ the adjustment of the process parameters for a NMOS device that impacts the V_{TH} is recommended after Taguchi process is finished. However, the results in ANOVA for V_{TH} clearly shown there have two adjustment factors which is Halo Implantation dose and Halo Tilt angle since both of the parameters have less percentage in nominal-the-best and high percentage in mean. It should be only one parameter that can be adjustment factor and dominant factor. The same parameter cannot be dominant and adjustment factor at the same time. To verify the results, the parameter values of four process parameters has been changed repeatedly to get the best adjustment factor. The results obtained from the 36 simulations still showing the same results. By considering this case, the confirmation of optimum factor for NMOS device cannot be done.

Another factor that may encounter is the combination of the high-k material with the metal gate used in this experiment are less suitable since there are other high-k material which can be a good combination with silicon such as hafnium dioxide (HfO_2) and Aluminum Oxide (Al_2O_3). Based on the previous researcher experiment, "EFFECTS OF HIGH-K DIELECTRICS WITH METAL GATE FOR ELECTRICAL CHARACTERISTICS OF 18 NM NMOS DEVICE" by N.B. Atan, I. Ahmad and B.Y. Majlis, where in their research regarding designing a 18 nm gate length NMOS device by comparing three types of high-k materials and pair with titanium tilicide ($TiSi_x$). It is proven that hafnium dioxide is the best high-k material to be pair with titanium silicide. The reason of hafnium dioxide be the most ideal decision material as the dielectric of transistor is on the grounds that it has sufficiently high dielectric consistent, sufficiently high band-hole and band balances with silicon. Besides, it likewise has great versatility and low spillage current contrast with TiO_2 [10].

In Figure 4.6 shows the plotted graph of I_{ON}/I_{OFF} for three different high-k materials. It demonstrated that HfO_2 dielectric produce the most elevated I_{ON}/I_{OFF} proportion contrasted and Al_2O_3 and TiO_2. Therefore, better device performance can be acquire by using the dielectric HfO_2 as a gate. This device displays the higherratio of I_{ON} and I_{OFF} at operating area sub-threshold. So, combination of HfO_2 and $TiSi_x$ is suitable for low power application [10].

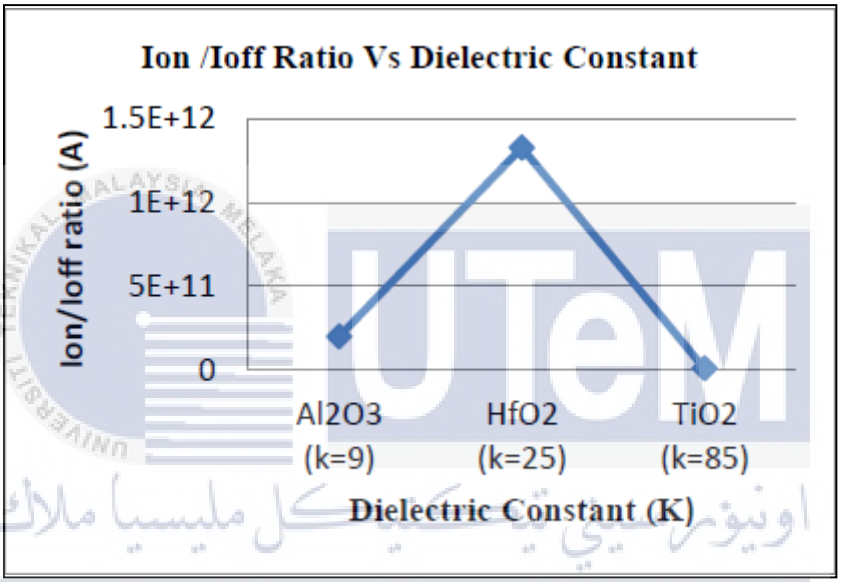

Figure 4.6: I_{ON}/I_{OFF} current for Al_2O_3, HfO_2 and TiO_2

In Table 4.6, indicating the reenacted outcomes for HfO_2, Al_2O_3 and TiO_2 of three dielectric materials with $TiSi_x$ as the metal gate for 18 nm NMOS. The great execution of plan MOSFET is when $I_{OFF} = 0$ and higher of I_{ON} esteem. It is obviously shows that HfO_2 has a higher I_{ON}/I_{OFF} proportion contrasted withTiO_2.

Table 4.10: Simulated Results of Various Dielectric Material with ITRS 2011 Prediction

Parameter	Simulation			ITRS 2011 Prediction
	Al_2O_3	HfO_2	TiO_2	
V_{TH} (V)	0.302651	0.302651	0.302651	0.302
I_{ON} (A/µm)	$4.721x10^{-4}$	$2.536x10^{-4}$	$1.934x10^{-4}$	$1.0x10^{-7}$
I_{OFF} (A/µm)	$2.365x10^{-15}$	$1.912x10^{-16}$	$2.432x10^{-14}$	$1.496x10^{-6}$
I_{ON}/I_{OFF} ratio	$1.996x10^{11}$	$1.326x10^{12}$	$7.952x10^{9}$	$6.685x10^{-2}$

CHAPTER 5

CONCLUSION AND FUTURE WORKS

5.1 Conclusion

By and large, the plan of a bi-layer graphene TiO_2 and $TiSi_x$ on a high-k dielectric material 22 nm NMOS device by utilizing Silvaco programming was accomplished. Then, the electrical characteristics, V_{TH} and I_{OFF} of device was analyzed and optimized using Taguchi L9 orthogonal array method. However, the optimization process by using Taguchi method is unsuccessful due to incompatible materials. The adjustment factor and dominant factor for V_{TH} is not valid since both of the factors have same process parameter. Hence, the optimization process cannot be completed. It can be conclude that TiO_2 as a high-k material with metal gate, $TiSi_x$ is not the best combination for NMOS device with 22 nm gate length. Since there are a few high-k materials more suitable to be combine with metal gate, $TiSi_x$, a few criteria should be considered before starts designing a MOSFET. The high-k material ought to have enough dielectric steady, sufficiently high band-hole and band counterbalances with silicon. One of the most dominant factors in determining the performance and

application of nano-scaled device is the threshold voltage (V_{TH}). Also in order to increase the performance of the device, the current leakage (I_{OFF}) ought to likewise be kept as low as conceivable by decreasing the time taken by charge to collect inside the channel for the transistor to turn on. Even though the optimization process by using Taguchi method is almost accurate, but it is affected by incompatible high-k material which is titanium dioxide in the device.

5.2 Sustainability and Environmental Friendly

This project will always be relevant in future, as planar is still used in the manufacturing for sensor and semiconductor fabrication industry. Graphene has also gained popularity in the design of planar MOSFET due to its excellent properties. The gate structure designed with high-k, titanium dioxide (TiO_2) and metal gate, titanium silicide ($TiSi_x$) with 22 nm gate length is a structure that is not too common due to the disproportionate volume of high-k material that can be pair with titanium silicide. This project is environmental sustainable, because it performs the simulation needed for the designed NMOS product without waste of any materials by only using Silvaco TCAD software. It will be advantageous in the sectors for the semiconductor processing process as it will not waste resources and would be more cost-effective.

5.3 Future Works

As per the reenactment results acquired, survey and finish of the examination, persistent work is required to be completed so as to consistently improve the current leakage (I_{OFF}) at the gate and the threshold voltage (V_{TH}) of NMOS transistor. As a result, this research can be strengthened to be better and to cover more scope in order to improve the leakage current and threshold voltage. Scaling down the gate oxide thickness can provide an increased drive current and an improvement in short-channel

effects. Besides, by adding Silicon on Insulator (SOI) layer also can give a different results in terms of electrical characteristic. SOI is typically situated on head of a silicon dioxide layer and viably in tackling parasitic impacts present in mass silicon transistors.

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