CURRENT RATIO ANALYSIS ON DESIGN AND MODELLING A 22 NM BILAYER GRAPHENE AND HIGH-K/METAL GATE (TiO_2/WSi_x) NMOS DEVICE

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CURRENT RATIO ANALYSIS ON DESIGN AND MODELLING A 22 NM BILAYER GRAPHENE AND HIGH-K / METAL GATE (TiO_2 / WSi_x) NMOS DEVICE WHICH HAS BEEN APPROVED BY FACULTY OF ELECTRONIC AND COMPUTER ENGINEERING

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This report is submitted in partial fulfilment of the requirements for the degree of Bachelor of Electronic Engineering with Honours

Faculty of Electronic and Computer Engineering
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DECLARATION

I declare that this report entitled “Current Ratio Analysis on Design and Modelling a 22 nm Bilayer Graphene and High-k/Metal Gate (TiO2/WSix) NMOS Device” is the result of my own work except for quotes as cited in the references.

Signature :

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Date : 2 JULY 2020

APPROVAL

I hereby declare that I have read this thesis and in my opinion this thesis is sufficient in terms of scope and quality for the award of Bachelor of Electronic Engineering with Honours.

Signature :

Supervisor Name : R ATIFAH MAHERAN

Date : 2/7/2020

DEDICATION

In this section is especially dedicated to express my highest gratitude to my beloved parents and siblings for endless love and support. To my lecturers and fellow friends, thank you for the guidance and help that were shared and discuss together till finished this report.

ABSTRACT

A 22nm of a bilayer Graphene NMOS transistor was designed and modeling based on virtual fabrication using Silvaco Software besides optimized current ratio using Taguchi L9 orthogonal array method. In this project, the materials used are high permittivity material (high-K) which is Titanium Dioxide (TiO_2) and metal gate which is Tungsten Silicide (WSi_x). There are four Control Factor (CF) and two Noise Factor (NF) which have been considered to get a good result for threshold voltage and leakage current. As the result of V_{TH} optimization, Halo Tilt angle is the adjustment factor while Compensation Implant was selected as dominant factor. Meanwhile, the dominant factor for I_{LEAK} optimization is Compensation Implant. From L9 Taguchi, the V_{TH} value of 0.289433V and I_{LEAK} value of 5.61104 nA/µm were achieved which closer to the ITRS 2012 prediction which is 0.289 V ± 12.7% for threshold voltage and lower than 100nA/µm for leakage current. Finally, the value of current ratio obtained is 4.4822×10^4.

ABSTRAK

22nm transistor graphene NMOS dibentuk dan dimodelkan berdasarkan fabrikasi maya menggunakan Perisian Silvaco selain nisbah arus yang dioptimumkan menggunakan kaedah Taguchi L9 ortogonal array. Dalam projek ini, bahan yang digunakan adalah bahan permitiviti tinggi (high-K) yang merupakan Titanium Dioksida (TiO_2) dan gerbang logam yang merupakan Tungsten Silicide (WSi_x). Terdapat empat Faktor Kawalan (CF) dan dua Faktor Kebisingan (NF) yang berbeza-beza dalam menentukan nilai terbaik untuk voltan ambang dan arus kebocoran. Hasil pengoptimuman V_{TH}, sudut Halo Tilt adalah faktor penyesuaian manakala Implan Kompensasi dipilih sebagai faktor dominan. Sementara itu, faktor utama pengoptimuman I_{LEAK} adalah Implan Kompensasi. Pengoptimuman Taguchi juga mencapai nilai min V_{TH} 0.289433V dan nilai min I_{LEAK} minimum 5.61104 nA/µm yang lebih dekat dengan nilai ramalan yang diberikan dalam ITRS 2012 iaitu 0.289 V ± 12.7% untuk voltan ambang dan lebih rendah daripada 100nA/µm untuk arus kebocoran. Akhir sekali, nilai nisbah arus yang diperoleh adalah 4.4822 x 104.

ACKNOWLEDGEMENTS

Foremost, I wish my sincere gratitude to my supervisor, Dr. Afifah Maheran binti Abdul Hamid for the continuous support of my FYP project and helped in writing of this thesis. I would like to express my appreciation to the master student, Amer who helped me to install and introduce this software to me.

Sincere thanks to all friends especially Azizul Haqeem bin Abd Gani, Nur Dini binti Razz Rozzfaisal and others for their moral support and encouragement during preparing my project and thesis.

Last but not least, my sincere gratitude goes to my beloved parents; Kamalrul Ariffin bin Mohd. Yusof and Noriah binti Hussain and also to my siblings for their support throughout my life.

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LIST OF SYMBOLS AND ABBREVIATIONS

SCE	:	Short Channel Effect
MOSFET	:	Metal Oxide Semiconductor Field Effect Transistor
ITRS	:	International Technology Roadmap for Semiconductor
Poly-Si	:	Poly-Silicon
SiO_2	:	Silicon Dioxide
$Ti0_2$	:	Titanium Dioxide
WSi_x	:	Tungsten Silicide
HfO_2	:	Hafnium Dioxide
FET	:	Field-Effect Transistor
High-K	:	High Permittivity
EOT	:	Equivalent Oxide Thickness
V_{TH}	:	Threshold Voltage
V_{GS}	:	Gate Voltage
V_{DS}	:	Drain-Source Voltage
TSMC	:	Taiwan Semiconductor Manufacturing Company
UHD	:	Ultra High Definition

LPP	:	Low Power Plus
PPA	:	Power Performance Area
STI	:	Shallow Trench Insulator
LPCVD	:	Low Pressure Chemical Vapour Deposition
BPSG	:	Borophosphosilicate Glass
STB	:	Smaller-the-Better
NTB	:	Nominal-the-Best
ANOVA	:	Analysis of Variance
ITRS	:	International Technology Roadmap for Semiconductors

LIST OF APPENDICES

CHAPTER 1

INTRODUCTION

1.1 Background

The activity of scaling down of gate length had been increases by years to create devices much thin so as to fabricate high density chips. As MOSFET is downscaled it gives more difficulties and worsens when it comes to the nanometer dimensions for example, SCE [11].

Sustaining Moore's Law while satisfying the needs for low power high performance in electronic systems have prompted an innovation of a device structures and implementation the materials. This creation has been exhorted by the ITRS for the efficient scaling of the devices in the following 15 years. As far as a planar geometry, MOSFET device has transformed from a traditional SiO_2 / Poly-silicon (Poly-Si) MOSFET to a high-K / metal gate. Due to its excellent properties, single layer and bilayer graphene have been applied as the channel material for transistor device. Next, bilayer graphene was implemented along by pairing High-K / metal gate and replaced with SiO_2 / Poly-Si as the top gate so that it will create the band gap, regulates the current in drain region, I_D and will restrict the carrier mobility into the channel. Thus, the 22nm bilayer graphene will be virtual fabricates in Silvaco Software to analyze the performance and next, will be optimized using the Taguchi method analysis [13]. For this project, the virtual fabrication was simulated and electrical characteristics in Silvaco Software for designing and optimization of the semiconductor device parameter. The L9 Taguchi Array was utilized as a part of the optimization process to evaluate variance and mean effect. [20]. TiO_2 and WSi_x were selected as high-K and metal gate in this project. The electrical characteristics of this NMOS device prediction made by the ITRS 2012 was used as a useful approach for next research in exploring and enhances the efficiency of the devices.

1.2 Problem Statement

From theory Moore's law, many researchers applied this law as the guidance in semiconductor technology to enhance the performance of the materials. However, this trend will make the manufacturing cost per device increases. Thereby, the production will must to downscale the geometry of the MOSFET [26].

Scaling down of the device will reduce the gate length, resulting in a closer gap between the drain and the source thus SCE occur [10]. When SCE happened, the devices will have some problems to produce and fabricate. For many years, SiO_2 layer was chosen as the high-K in devices but more disadvantages than the benefits. The silicon dioxide layer will crack and make current leakage rise up. Thus, excessive dissipation of power in the device and make the production cost become higher. When the high-K was introduced together with Poly-Si, they cannot be unite as the both materials give a reaction and this shows that the metal gate and high-K must be in sync.

Thus, the solution of the previous researcher for these issues of gate leakage current are being resolved by applying a new method which is combining a high-K dielectrics and metal gate for replacing the traditional SiO_2 and Poly-Si.

1.3 Objectives

There are two objectives in this project. The objectives are:

i. To design a 22 nm NMOS device with Graphene, Titanium Dioxide (TiO_2) and Tungsten Silicide (WSi_x) using Silvaco TCAD Software.

ii. To analyze electrical characteristics and optimize current ratio using Taguchi L9 orthogonal array method.

1.4 Scope of Work

Figure 1.1 indicates the flowchart of this scope of the project. The existing device structures are the high-k is Titanium Dioxide (TiO_2) and Tungsten Silicide (WSi_x) which is a metal gate. The Silvaco software will be apply to virtually fabricate the device. The ATHENA in Silvaco software will be used to simulate the virtual fabrication of the N-type device while for the ATLAS is for the electrical characteristic's properties. Next, the L9 Taguchi array was used to analyze the electrical characteristics from the current ratio and to optimize the best combination to produce a device with better performance. This method also to analyze the V_{TH}, I_{ON}, I_{OFF} and current ratio refer ITRS 2012 and compare with previous researcher.

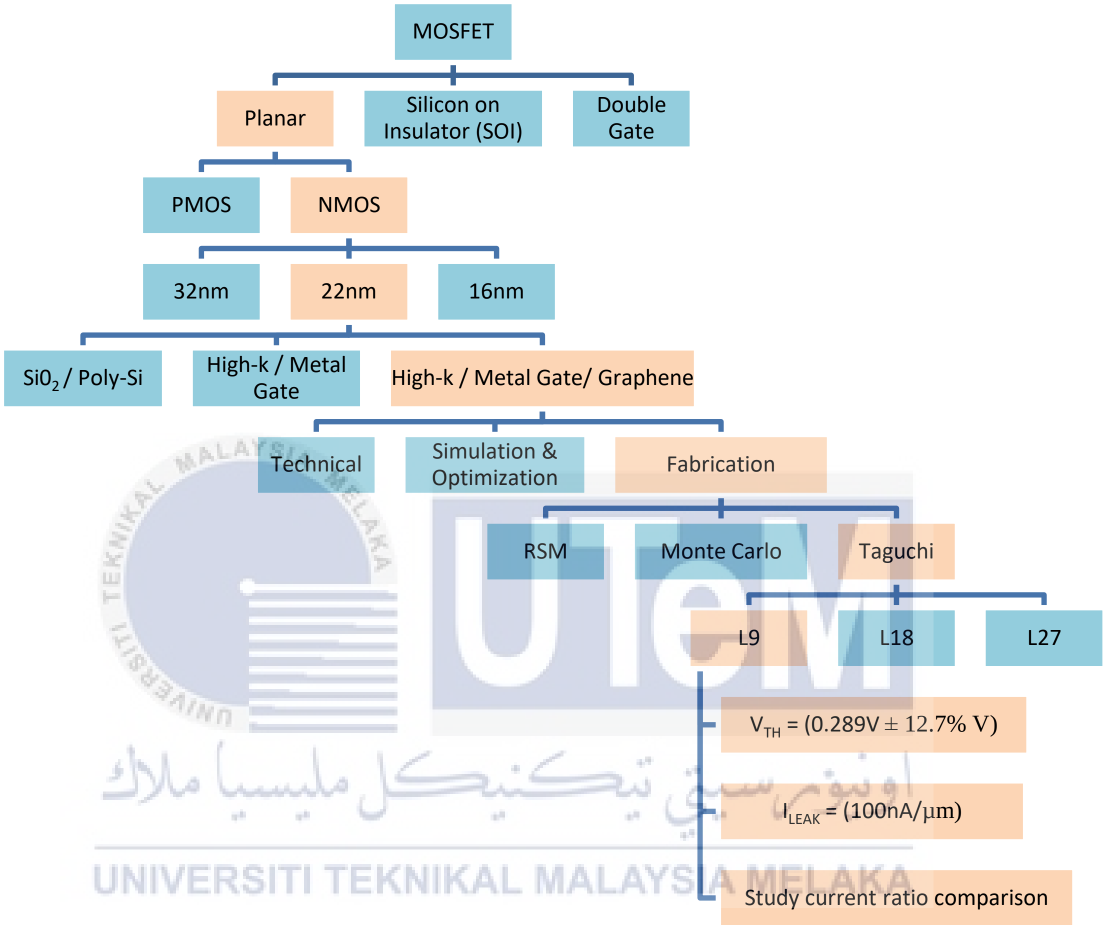


Figure 1.1: Flowchart of the Scope of Work

1.5 Report Structure

This report aims on a current ratio analysis on 22 nm NMOS device with graphene / high-K and metal gate using Silvaco Software. This report is classified into five major chapters which are introduction, background study, methodology, results and discussion, and also conclusion and future works. For Chapter 1 will review about the background of the project, problem statement, objectives of the project, scope of work and the report structure. Chapter 2 discuss on the literature review which contain the introduction, and other studies that relates to this project from different researcher which are MOSFET fundamental, Moore's Law, High-K / Metal Gate, graphene properties and summary from previous study. Next, Chapter 3 reviews about the methodology used in this project. The introduction, flowchart of the project and experimental setup will be analyzed. Chapter 4 reviews about the results obtained and discussions of the device. In this chapter, fabrication using Silvaco software, virtual transistor in Silvaco ATHENA, transistor electrical characteristic in Silvaco ATLAS and Taguchi Orthogonal L9 Array method are reviewed. Chapter 5 reviews about the conclusion which can conclude the whole project from the results to the future works.

CHAPTER 2

BACKGROUND STUDY

2.1 MOSFET Fundamental

Lilienfeld and Heil was the first researchers in conceived the insulated gate field effect transistor (FET) in 1926 [15]. These insulated-gate FET have been used widely in semiconductor industry and now named as MOSFET. The MOSFET is a semiconductor device which the function are for switching and amplifying electronic signals thus beneficial for the device functionality. Due to its size which is smaller, it is suitable to design and fabricates in this semiconductor devices such as switch [16].

MOSFET can be divided into two which are Depletion Type and Enhancement Type. For Depletion type, the drain current, I_D can flow at zero gate bias while for Enhancement type, zero I_D can flow at zero gate bias and has no conducting channel region. In that both types, there are four terminal devices in MOSFET which are Source, Gate, Drain and Body terminals [10].

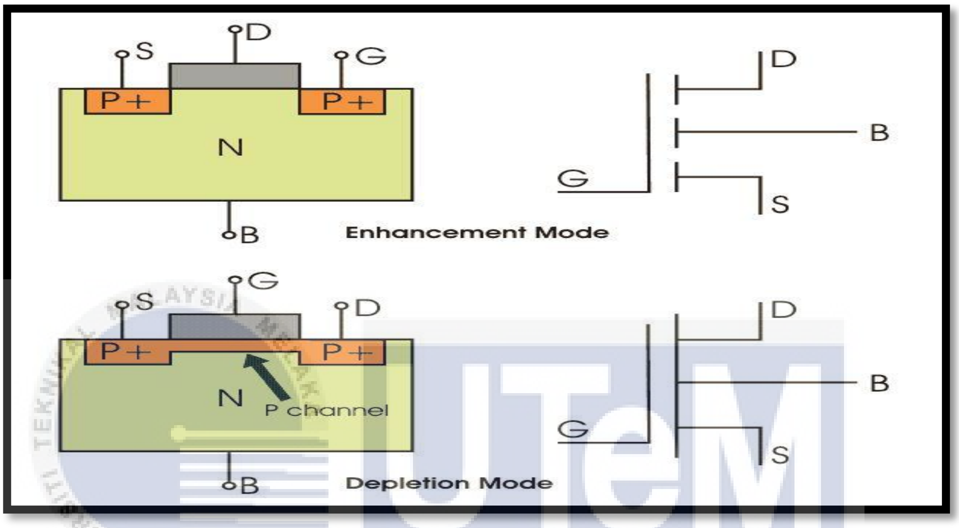


Figure 2.1: The diagram and symbol of MOSFET

2.1.1 MOSFET Operation

MOSFET works as a capacitor. Firstly, the gate length whether used positive or negative voltages are applied thus it can be set up into N-type in depletion region .When the holes present with a repulsive force which populated by negative charges and associated with acceptor atoms is known as positive gate voltage. While, the negative voltage is applied when the holes present and filled by positive charges and allied with donor atom [16]. Thus the current can freely flow and the gate voltage $V_{G,}$ will control the electrons in the channel.

2.1.2 N-Channel MOSFET

This type of MOSFET is located between source and drain which is heavily doped N+ region which the highest number of electrons as current carriers [16]. The negatively charged electrons will caused the current to flow in this type of MOSFET.

2.2 Scaling MOSFET

MOSFET scaling is the reduction in parameters with technological advancement. The semiconductor industry has benefited enormously from the MOSFET miniaturization over the last decades. Reducing transistors to dimensions below 100 nm will allow a lot of transistors to be implemented on a high density chip. The benefits of downscaling of the devices such as increased functionality, reduces power dissipation and reduces cost of manufacturing a wide range of integrated circuits and systems to the users and especially for semiconductor technology in creating a smaller devices with a greater performances [14]. When the MOSFET transistors in size are reduced, the chip area will lessen. So that, more single chips per wafer can be designed and produced. Besides, the downsides of scaling the devices are causes noise problem. This is because when there are problem in noise when the scaling process takes step thus the efficacy of the devices will low [17].

2.2.1 Moore's Law

In 1965, Gordon Moore has an insight in the semiconductor industry which is a revelation which revolutionized the technology industry and devote in semiconductor technology. With applying Moore's Law, many companies can have preparation for the future in down-scaling the devices and upgrade the production to achieve the advancement of technology [18].

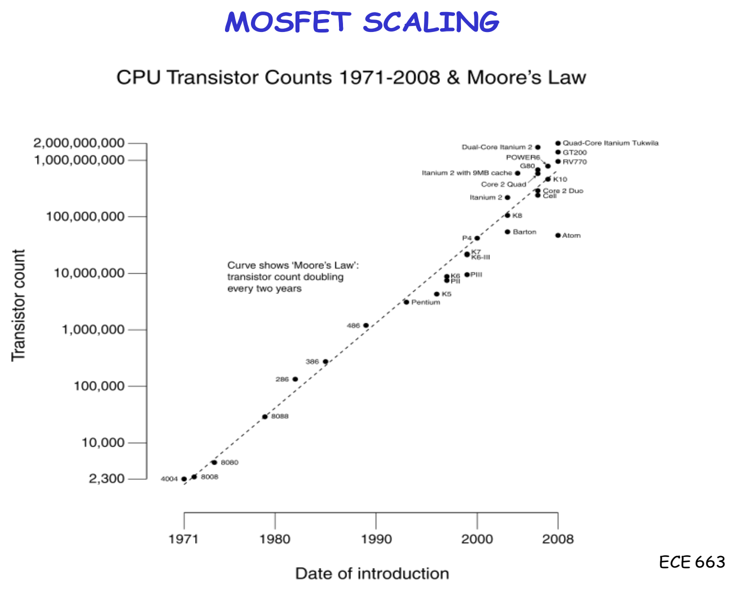


Figure 2.2: Graph of CPU transistor counts from 1971-2008 & Moore's Law

Currently, Taiwan Semiconductor Manufacturing Company (TSMC) produced the smallest process node is 7nm. And besides, Samsung built the transistor into 3nm and TSMC is approved to begin the production at the end of 2022 or the beginning of 2023 [17].

Moore's law will possibly continued by Samsung. The Samsung will make their evolution by focusing on device performance or active diff lines or cell comparison. Along with the downscale, it will have better power performance area (PPA) per cell [18]. Besides, the Intel® 14 nm technology offer better the dimensions scaling of transistors from 22 nm. The transistor fins build to enhance their density and lower the capacitance of the devices [31]. Next, the 14 nm process and the main system-on-a-chip (SoC) product are eligible and manufactured in volume, with fabs throughout Oregon (2014), Arizona (2014), and Ireland (2015).

2.2.2 High Permittivity (High-K) Dielectric

In this semiconductor technology, High-K is one of the focus in extensive studies recently [19]. Silicon Dioxide, SiO_2 gate widely used in fabricating process were replaced with High-K dielectric because of their weaknesses which is SiO_2 have larger high-K thus can produce a short channel effect [19]. High-K materials were introduced to produce a higher permittivity and band gap. Not just that, these materials also can improve the capacitance and obtain the minimum current leakage.

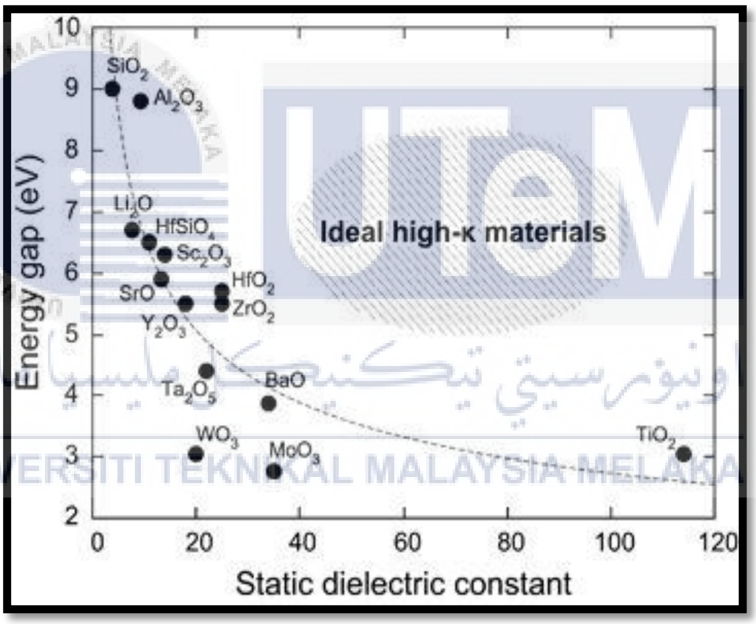


Figure 2.3: The graph of the ideal High-K materials.

2.2.3 Metal Gate

A metal gate is located at the upper part of the high-K and silicon substrate in MOSFET transistor and operates for controlling the resistance in the regions.

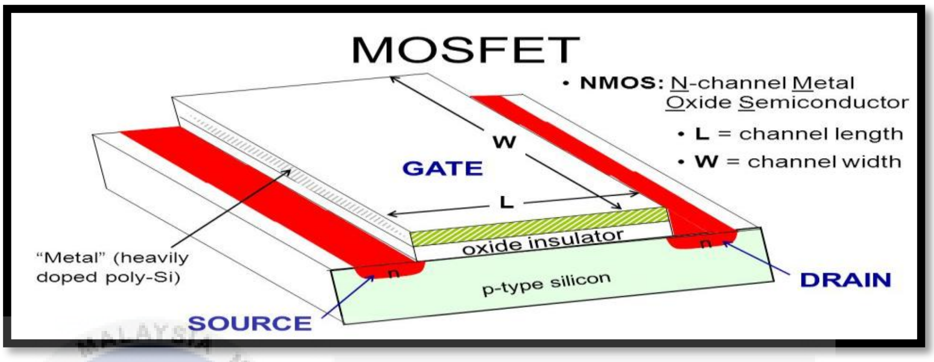


Figure 2.4: The structure of Metal Gate in MOSFET

There are a few reasons that poly-Si was the preferred material for the past decade are metal gates were used when operating voltages were 3V to 5V. As operating voltages lowered, manufacturers transitioned to using poly-silicon as the gate material. Recently, after 45nm (for Intel) and 28nm (for TSMC), gates are again made with metal in conjunction with high-k insulators [12]. Poly-Si gates were favored because the material could be easily matched to the SiO_2 lattice constant, creating a no-strain, reliable structure. This structure has fallen into disfavour because it is slow and can toggle unexpectedly, as in time it alter the shape of the SiO_2 layer by itself.. Because high-k means high dielectric constant thus make a choice for a thinner gate size and put the contact on top [11].

2.3 Graphene

Graphene is a purely two-dimensional (2D) material and graphene's atom are tightly bound in a hexagonal honeycomb lattice [19]. The characteristics of graphene are they high electron mobility at room temperature which enables the electrons in the layer to flow faster. Besides, this material are cheap to produce compared to other material in marketplace thus many devices used their materials in fabrication process. Besides, they can conduct electricity and heat which is more behavior like a metal. Then, the carbon atoms within the layers are tightly bounded and remarks as stiff material.

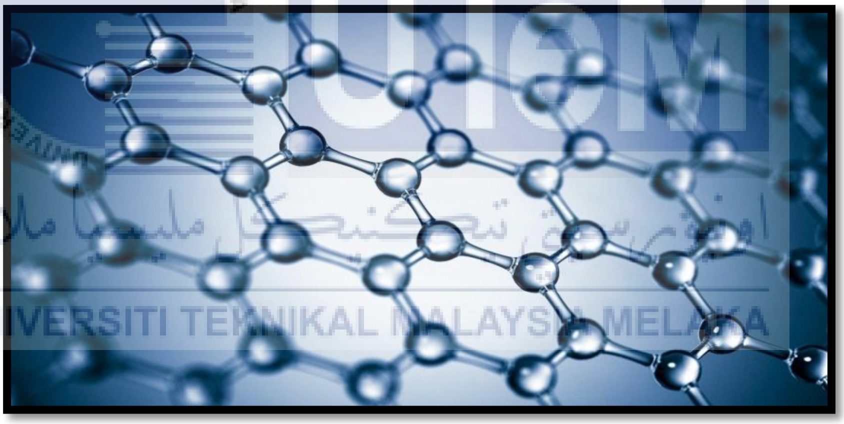


Figure 2.5: The structure of Graphene

2.3.1 Graphene Bandgap

To ensure the currents switched on and off, therefore the movement of electrons into conduction bands are required. Since they have a zero-bandgap regarding their characteristics that is mass-less electrons, thus the current flows within the bands cannot be stop [20]. This zero-bandgap makes the graphene to conduct like a metal which is cannot control and stop the electrons of this material.

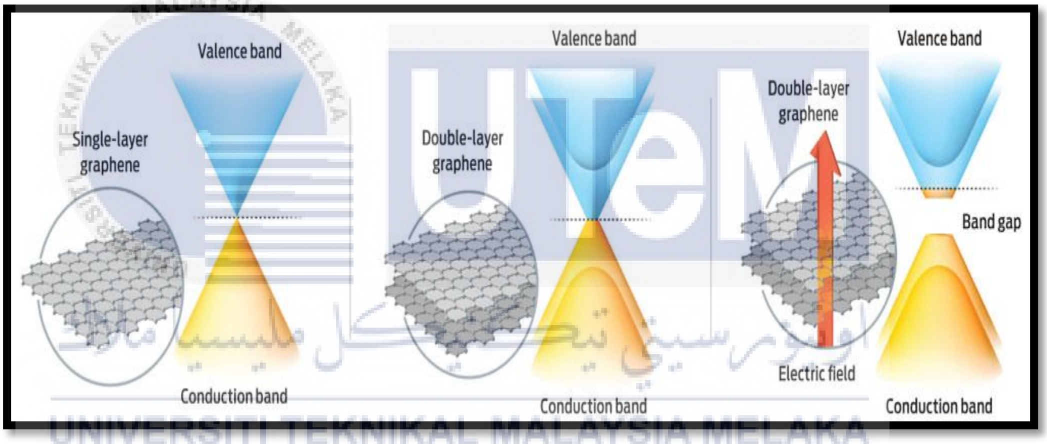


Figure 2.6: The diagram of bandgap in Graphene.

2.4 Summary from Previous Research

Table 2.1: Summary from Previous Research

No	Author/Journal/Year	Summary
1	N.F. Z.A, I. Ahmad, P.J. Ker, Siti Munirah Y, Mohd Firdaus R, S.K. Mah and P.S. Menon. (2016). Process Parameters Optimization of 14 nm p-Type MOSFET using 2-D Analytical Modeling, vol. 8, No.4, Page 97-100.	• This paper presents the modeling and optimization of 14nm gate length CMOS transistor which is downscaled from previous 32nm gate length. • Hafnium Dioxide (HfO_2) and Tungsten Silicide (WSi_2) • V_{TH} and I_{OFF} are 0.248635±12.7%V and 5.26x10-12 A/um • (ITRS 2013)
2	Noor Faizah Zainul Abidin, Ibrahim Ahmad, Pin Jern Ker & P. Susthitha Menon. (2017). Performance Characterization of Schottky Tunneling Graphene Field Effect Transistor at 60 nm Gate Length.	• A planar Graphene Field-Effect Transistor GFET performance • Gate length of 60 nano-meter was evaluated in exploring new material to meet the relentless demand for increasing the performance- power saving features.

3	Z. A. Noor Faizah, I. Ahmad, P. J. Ker, P. Susthitha Menon N V Visvanathan, A. H. Afifah Maheran. (2017). VTH and ILEAK Optimization using Taguchi method at 32nm bilayer graphene PMOS.	• A 32nm top-gated bilayer Graphene PMOS transistor • Titanium Dioxide ($Ti0_2$) and Tungsten Silicide (WSi_X) • V_{TH} = -0.10299V and I_{LEAK} = 0.05545673nA/um • (ITRS 2011)
4	Afifah Maheran, A. H.a, Menon, P. S.a , I. Ahmadb, S. Shaaria. (2014). Optimisation of Process Parameters for Lower Leakage Current in 22 nm n-type MOSFET Device using Taguchi Method	• In this article, Taguchi orthogonal array method was used to optimize the process parameters during the design of a 22nm n-type Metal Oxide Semiconductor Field Effect Transistor (MOSFET) in order to decrease the leakage current (I_{LEAK}) of the device.
5	K.E. Kaharudin, F. Salehuddin, A.S.M. Zain, 4m.N.I.A. Aziz.(2016). Taguchi Modeling With The Interaction Test For Higher Drive Current In Wsix/Tio2 Channel Vertical Double Gate Nmos Device.	• This paper presents a study in which Taguchi method has been utilized to increase the drive current (I_{ON}) in the WSi_x / TiO_2 Vertical Double Gate NMOS Device

6	F.Salehuddin, Ameer F.Roslan, A.E.Zailan, K.E.Kaharudin, A.S.M.Zain, Afifah Maheran A.H., A.R.Hanim, H.Hazura, S.K.Idris, Wira Hidayat Mohd Saad.(2018). Analyze of Process Parameter Variance In 19nm Wsi2/Tio2 NMOS Device Using 2k-Factorial Design.	• This paper investigates and analyzes the impact of process parameter variance on the drive current (I_{ON}) and leakage current (I_{OFF}) for 19 nm WSi_2/TiO_2 NMOS device using 2k-factorial design
7	M. Zabeli, N. Caka, M. Limani, Q. Kabashi. (2016). Impact of MOSFET's Structure Parameters on its Overall Performance Depending to the Mode Operation.	• The objective of this research is to analyze the impact of the main electrical and physical parameters in characterized the MOSFET.
8.	Eliya Firhat. (2019). Minimum Leakage current optimization on 22nm Hafnium Dioxide ($Hf0_2$)/ Tungsten Silicide (WSI_x) / Graphene with Silicon on Insulator (SOI) using Taguchi Method.	• This paper is to design and simulate a bilayer graphene on hafnium dioxide ($Hf0_2$) / Tungsten silicide (WSI_x) with SOI on 22nm NMOS device using Silvaco Software.

9	Savita Maurya. (2016). Challenges Beyond 100 nm MOS Devices.	• This paper deals with challenges and limits of beyond 100nm technology. • Possible limiting factors for the scaling of devices have also been elaborated.
10	S. K. Mah, I. Ahmad, P. J. Ker, Noor. (2016). Faizah Z. A. Modelling of 14NM Gate Length La_2O_3-based n-Type MOSFET.	• In this paper, a 14nm silicon based n-type MOSFET was virtually fabricated using Lanthanum Oxide (La_2O_3) on Titanium Silicide ($TiSi_2$).

CHAPTER 3

METHODOLOGY

3.1 Flowchart of the project

Figure 3.1 indicates the flowchart of the project which is firstly, design and modeling a 22nm NMOS device with a bilayer of Graphene. The result was simulated via ATHENA and ATLAS in Silvaco Software and analyzed by referring ITRS 2012. The ATHENA in Silvaco software will be used to simulate the virtual fabrication of the NMOS devices in the software while for the ATLAS is for the electrical characteristic's properties. If the electrical characteristics are fulfilled, it is considered successful. Then, the Taguchi method are applied for analyzing the electrical characteristics of current ratio and to optimize the best combination to produce a device with better performance. The results obtained will compare with the previous researcher and literature to determine whether the downscaling the device can reduces the leakage current, I_{LEAK} and achieve an optimum threshold voltage, V_{TH}.

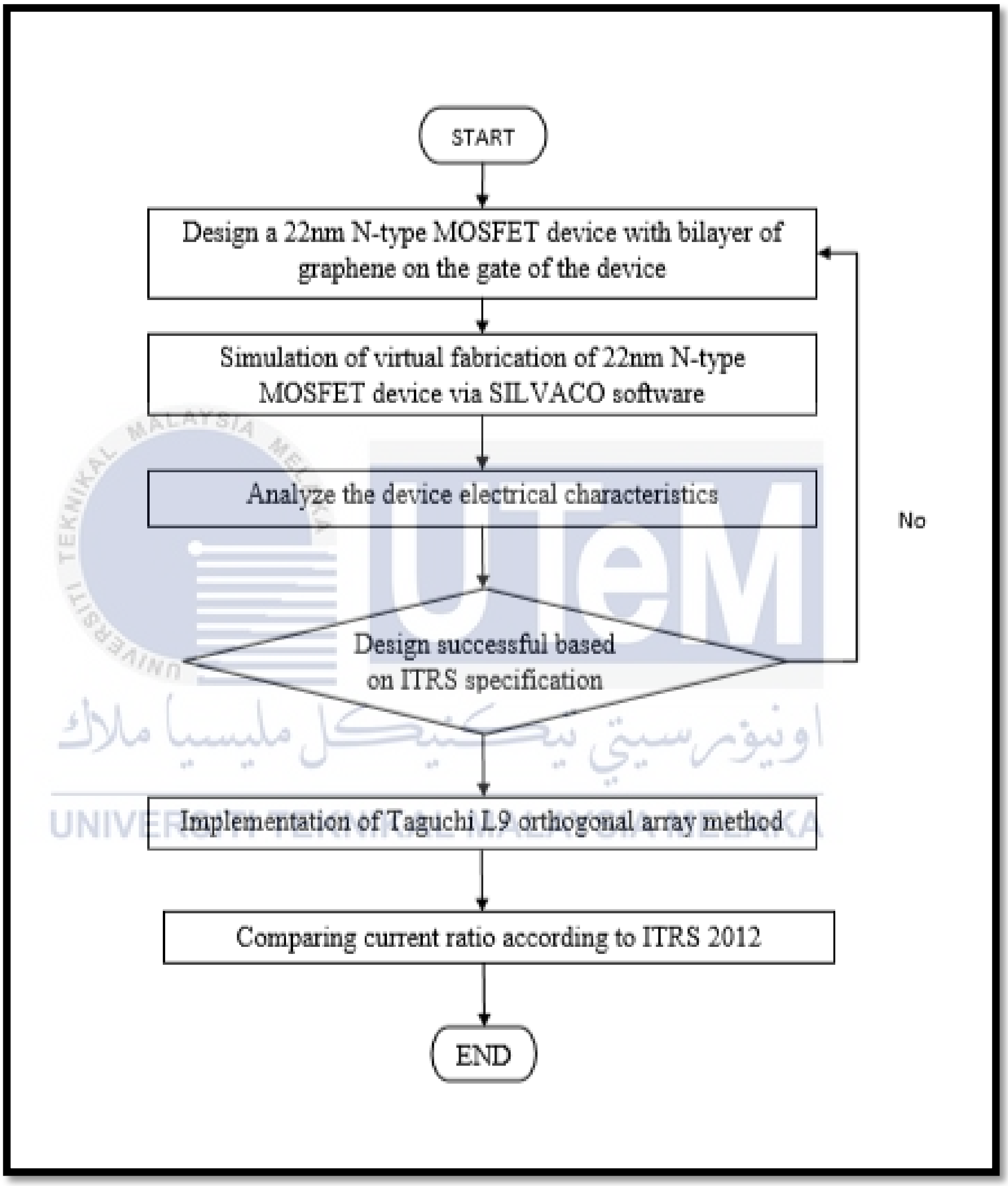


Figure 3.1: Flowchart of the project

3.2 Experimental Setup

A current ratio analysis on design and modeling a 22nm Graphene / High-K and metal gate was simulated to fabricate using ATHENA and optimize electrical characteristic using ATLAS module in Silvaco software. The fabrication step takes after the same regular top-down transistor well-matched process flow with a variety of a few process parameters which exists in doping density and annealing temperature to get the outcome as the standard by ITRS specification. The substrate is prepared for similarly in this procedure. The MOSFET device process simulation entails a sequence of processing steps known as the process flow. The process started with wafer preparation, followed by well formation, isolation, transistor and interconnection as shown in the Table 3.1.

Table 3.1 Fabrication step of NMOS device

Process Step	n-type MOSFET parameters
Substrate	• Silicon • <100> orientation
Retrogade well implantation	• 200 Å oxide screen by 870℃, 20 min of dry oxygen • $1x10^{16}$ ions/cm^2 phosphorus • 30 min, 900℃ diffused in nitrogen • 36 min, dry oxygen
STI isolation	• 130 Å stress buffer by 900℃, 20 min of dry oxygen • 1500 Å Si_3N_4 applying LPCVD • 1.0 µm photoresist deposition • 15 min annealing at 900℃
Gate oxide	• Diffused dry oxygen for 0.001 min, 805℃
Vt adjust implant	• $9.15x10^{11}$ions/cm^3 Boron difluoride • 5.5KeV implant energy, 7˚ tilt • 20 min annealing at 800℃
Graphene layer	• 0.00068 µm graphene

High-K/ Metal Gate deposition	• 0.002 µm High-K dielectric • 0.0464 µm WSi_x • 3.5 min, 850°C annealing
Halo implantation	• 1.825x10^{13} ions/cm^3 indium • 35˚ tilt
Sidewall spacer deposition	• 0.0404 µm Si_3N_4
S/D implantation	• 9.78x10^{14} ions/cm^3 arsenic • 8 KeV implant energy • 5˚ tilt
PMD deposition	• 0.015 µm BPSG • 20 min, 855°C annealing • 1.435x10^{14} ions/cm^3 phosphor • 160KeV implant energy • 7˚ tilt
Metal 1	• 0.015 µm aluminum
IMD deposition	• 0.05 µm BPSG • 15 min, 950°C annealing
Metal 2	• 0.12 µm aluminum

3.2.1 Virtual Fabrication of 22nm Bilayer Graphene NMOS

The virtual fabrication steps are as mentioned in this part. The first step is use p-type silicon as a substrate (100) and p-well implantation was produced and the Boron as a dopant will well spread in the wafer. Next a Shallow Trench Isolator (STI) processes occur when oxidized in dry oxygen for 20 minutes to build the STI layer. For depositing the Nitride layer, the wafer have to undergo the low pressure chemical vapour deposition process (LPCVD). Then, a photo resist was deposited with a thickness of 1.0µm before developing the Nitride layer and trench is produced. Next, it followed with etching process. The next step was to implant the gate length of 22nm bilayer graphene in the wafer with the thickness of 0.00068 µm. Later on, the high-k dielectrics, TiO_2 and metal gate, WSi_X was deposited on the top of the bilayer layer with thickness of 0.002 µm and 0.0464 µm.

Then, halo implantation were formed which is the dosage of Indium $1.825x10^{13}$ ions/cm^3 for producing the good performance of N-type MOSFET. Then, side wall spacers was deposited with a thickness of Si_3N_4 which is 0.0404 µm. S/D Implantations using Arsenic was deposited with a dosage of $9.78x10^{14}$ ions/cm^2. It is followed with PMD deposition using phosphorous with a dose of $1.435x10^{14}$ ions/cm^3. Next, placing with aluminium layer as the first step of metallization with the thickness of 0.015 µm. The next process was takes place is IMD Deposition by placing BPSG layer at 950°C temperature. Then finally, the second metallization of the aluminium layer with thickness of 0.12 µm was deposited onto of the structure.

Figure 3.1 and Figure 3.2 indicates the complete 22nm NMOS device structure and the enlarged figure of the 22 nm gate length and for Figure 3.3 represents the doping profile of the device. Then, the device will simulate and optimize the electrical characteristics through ATLAS [10].

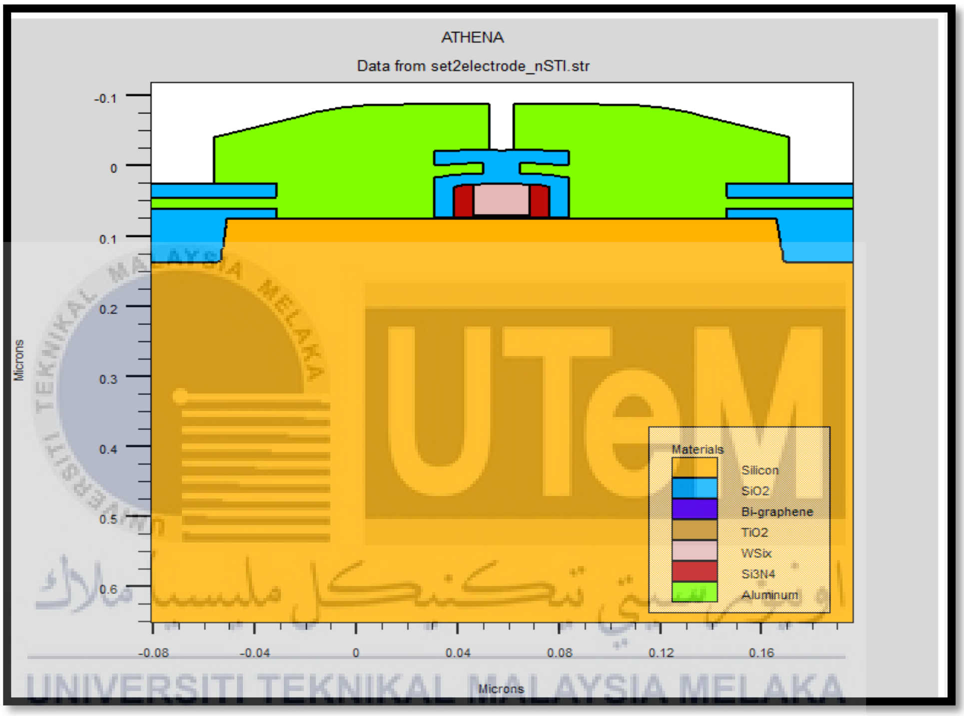


Figure 3.2: The complete 22nm NMOS device structure

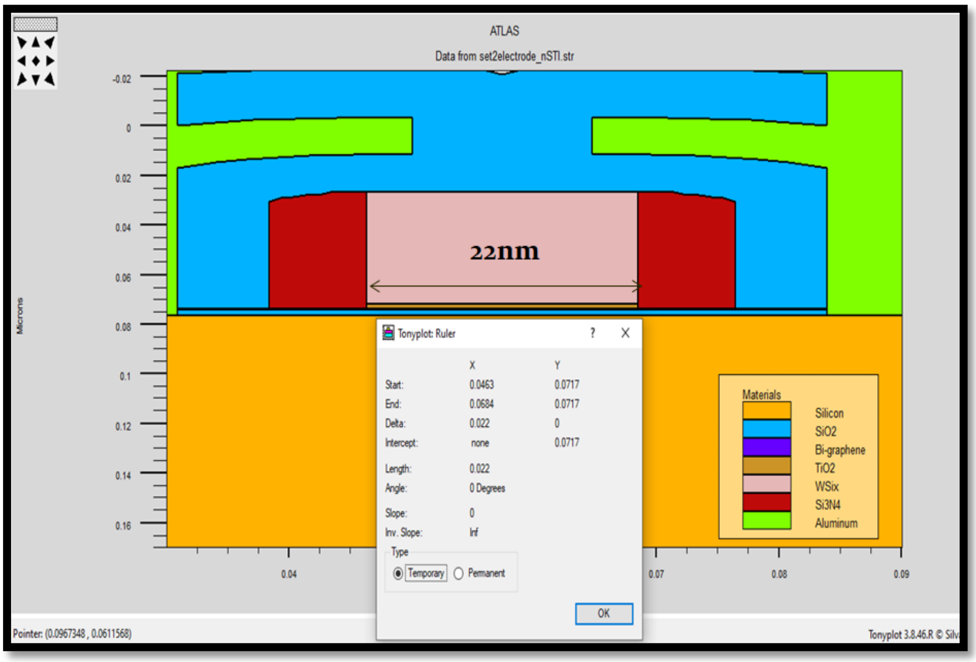


Figure 3.3: The enlarged figure of the 22 nm gate length

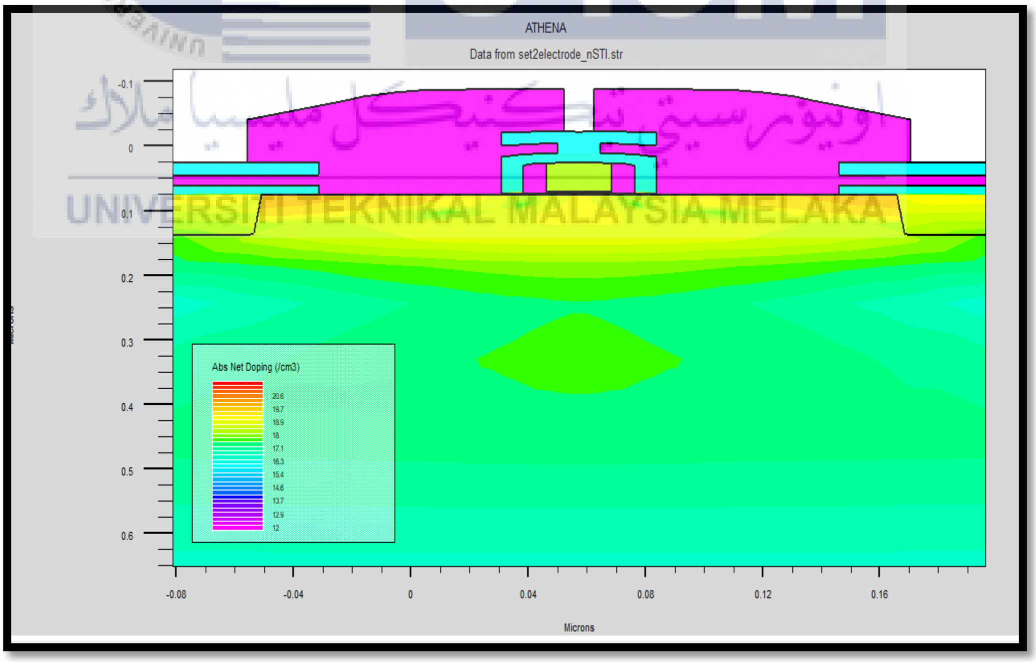


Figure 3.4: Doping profile of 22nm NMOS transistor

3.2.2 Semi Analytical Approach for Bilayer Graphene

In this project, the device performances were characterized into threshold voltage (V_{TH}) and leakage current (I_{LEAK}) which reference to ITRS 2012. The bilayer graphene was designed with a bandgap is set at 0.55eV, permittivity of 2.4, carrier mobility of top-gated graphene, a large value of 100 ns for radiative recombination rate of electron and holes [14], and the effective field of E_{eff} = 0.4MV/cm while the electron and hole densities of states at room temperature (300K) were measured from equation 3.1 and 3.2 below:

$$Nc = \frac{8\pi m_e kT}{h^2} \ln\left(1 + e^{-(Ec-Ef)/kT}\right) \quad (3.1)$$

$$Nv = \frac{8\pi m_h kT}{h^2} \ln\left(1 + e^{-(Ef-Ev)/kT}\right) \quad (3.2)$$

where the effective mass of the electrons and holes of graphene were set at $m_e \approx 0.06$ m_o and $m_h \approx 0.03 m_o$ which is m_o is the free electron mass.

3.3 Taguchi Method to Parameter Design

Taguchi array approach were implemented to achieve maximal data with fewer experiments. The goals are to analyze the control factors in designing and modeling a 22 nm NMOS device to attain the value of threshold voltage ($V_{TH)}$ and a lowest leakage current (I_{LEAK}).

The optimizations of this transistor were performed using Taguchi L9 method, where 36 simulations of four Control Factors and two Noise Factors are applied to get the optimized V_{TH} and I_{LEAK}. The noise factors are applied to achieve a more reliable design and resistant to variance and mean. The control factors and noise factors with values of each levels are listed in Table 3.2 and Table 3.3 respectively.

Table 3.2: Control Factor and their levels

Symbol	Control Factor	Unit	Level 1	Level 2	Level 3
A	HALO Implantation ($X10^{13}$)	Atom/cm^3	2.61	2.905	3.25
B	HALO Tilt	Degree	30	35	40
C	S/D Implantation ($X10^{13}$)	Atom/cm^3	4.7	4.8	4.9
D	Compensation Implantation ($X10^{12}$)	Atom/cm^3	2.35	2.391	2.6

Table 3.3: Noise Factor and their levels

Symbol	Noise Factor	Unit	Level 1	Level 2
X	Sacrificial Oxide Layer PSG	°C	950 (X0)	960 (X1)
Y	P well implantation/ BPSG Oxide temp	°C	920 (Y0)	930 (Y1)

Table 3.4: Orthogonal Array L9 Taguchi

Expt. No.	A	B	C	D
1	1	1	1	1
2	1	2	2	2
3	1	3	3	3
4	2	1	2	3
5	2	2	3	1
6	2	3	1	2
7	3	1	3	2
8	3	2	1	3
9	3	3	2	1

CHAPTER 4

RESULTS AND DISCUSSION

4.1 Virtual Fabrication for 22nm NMOS Device

This part represents the electrical characteristics NMOS transistor obtained from the ATLAS in Silvaco Software were analyzed in Figure 4.1 and Figure 4.2. Figure 4.1 shows the graph of I_D-V_D and Figure 4.2 shows the graph of I_D-V_G for 22nm NMOS device. In this part, the performances of NMOS device were followed as ITRS 2012 at threshold voltage, V_{TH} = 0.289 ± 12.7% and the leakage current (I_{LEAK}) must be lower than 100 nA/µm.

Figure 4.1 demonstrates the electrical characteristics graph of the drain current (I_D) versus drain voltage (V_D) of NMOS devices. This figures shown that different gate voltage (V_G) was applied which are 1.0 V, 2.0 V and 3.0 V. When gate voltage is equal to 1.0 V, the device reaches the saturation region because once V_D is greater than 0.4V. This is because of high electron mobility in the gate channel.

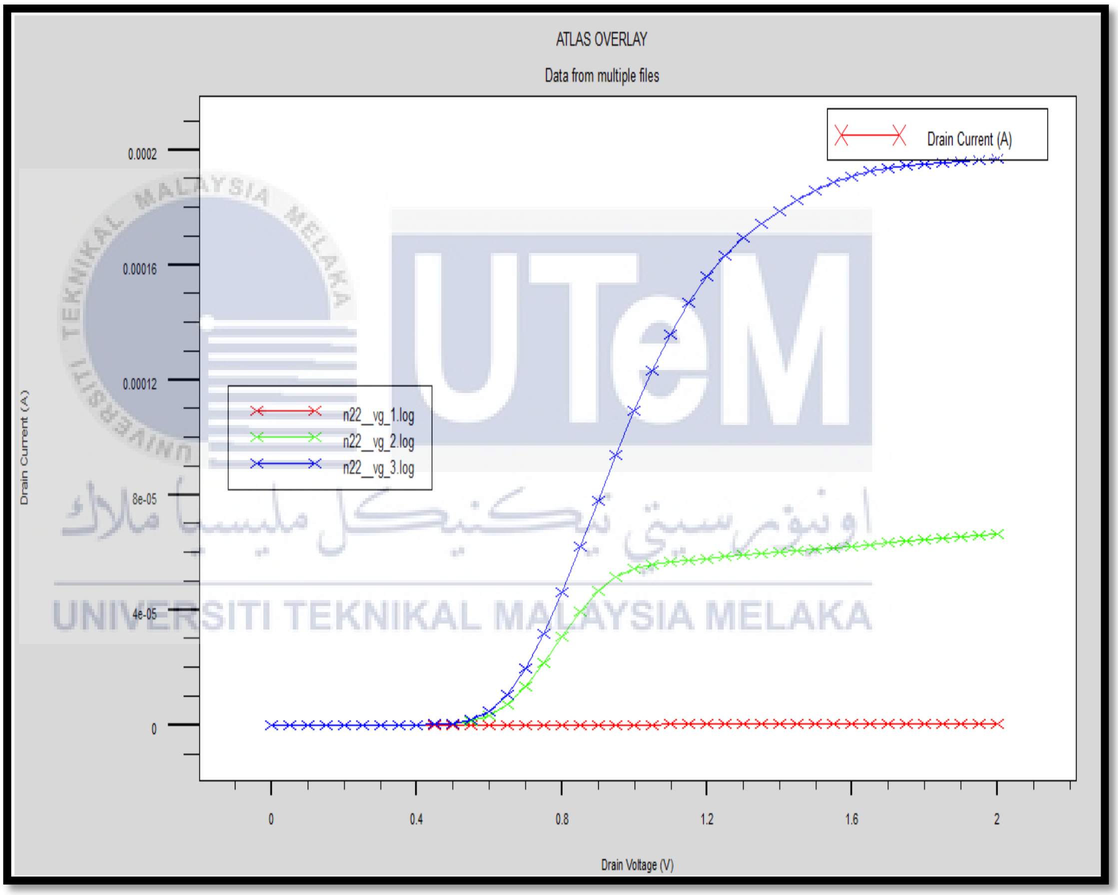


Figure 4.1: Graph of I_D-V_D for 22nm NMOS device

Figure 4.2 illustrates the characteristic curve of drain current, I_D against gate voltage, V_G. The graphs were analyzed on drain voltage, V_D which are 1.0 V and 2.0 V. So as to support the results and discussions obtained, besides validate the performance of device, the threshold voltage (V_{TH}) was fixed with predicted value of 0.289 V in this device.

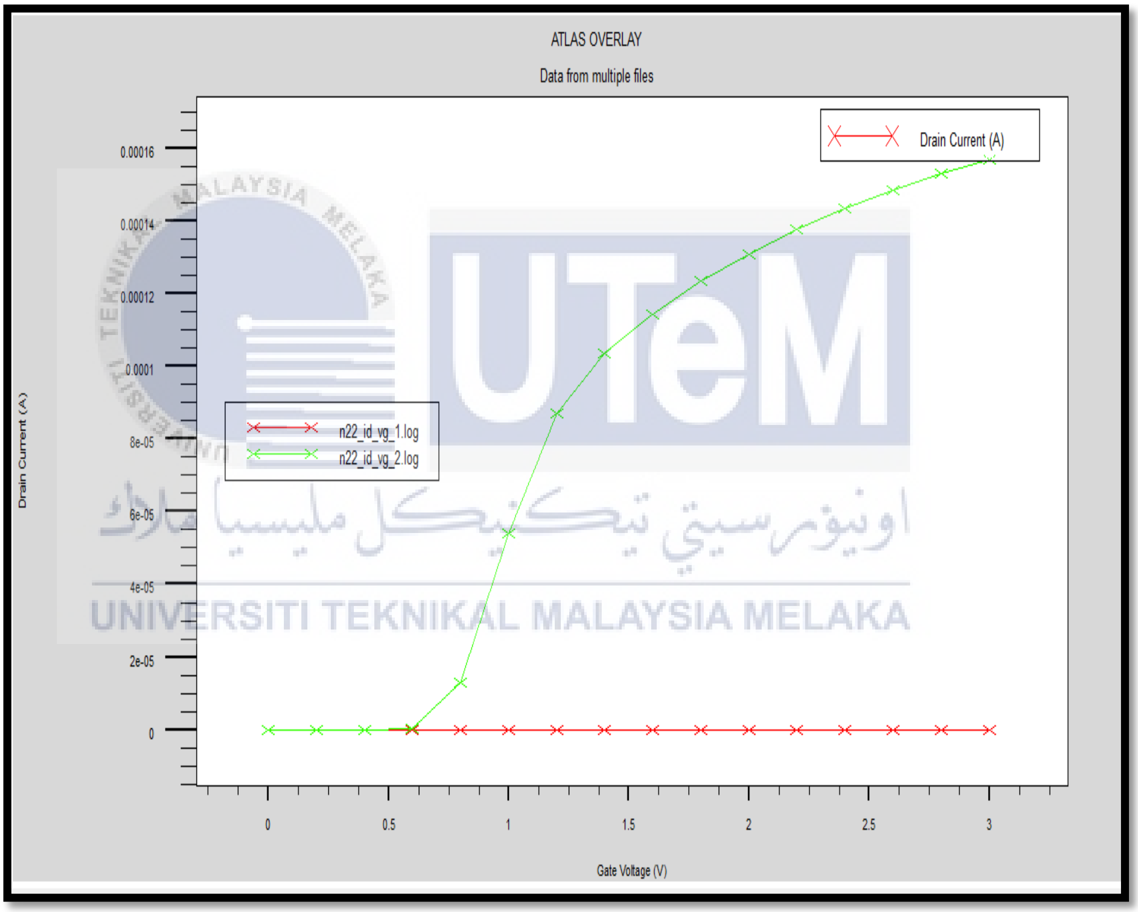


Figure 4.2: Graph of I_D-V_G for 22nm NMOS device

4.2 Optimization analysis of L9 Taguchi Array method

The Taguchi approach were applied to obtain the optimized value in achieving the optimal design of devices. The threshold voltage (V_{TH}) and leakage current (I_{LEAK}) were analyzed and interpreted [1]. In this part, V_{TH} refers to Nominal-the-Best while I_{LEAK} refers to Smaller-the-Better. Analysis from Taguchi approach consisting of nine experiments and four parameters were simulated and placed on the table given. The completed response for V_{TH} and I_{LEAK} data are as shown in Table 4.1.

Table 4.1: The completed response for V_{TH} and I_{LEAK} data

Exp No.	Threshold Voltage, V_{TH} (V)				Leakage Current, I_{LEAK} (nA/um)			
	(X0,Y0)	(X0,Y1)	(X1,Y0)	(X1,Y1)	(X0,Y0)	(X0,Y1)	(X1,Y0)	(X1,Y1)
1	0.271741	0.231208	0.271835	0.231321	7.14814	7.61868	6.98839	7.3911
2	0.239306	0.185578	0.23938	0.18568	6.66707	6.05098	6.53284	5.98828
3	0.190735	0.103545	0.190803	0.103668	5.61116	5.62019	5.58367	5.59138
4	0.394981	0.284218	0.392789	0.284275	7.33766	8.09594	7.3284	7.84204
5	0.286144	0.237084	0.28624	0.237187	7.05655	7.58115	6.89065	7.35649
6	0.258919	0.217591	0.259001	0.217698	7.07842	6.83615	6.96764	6.69271
7	0.736262	0.475019	0.732031	0.473669	5.40471	6.69977	5.40575	6.69887
8	0.657571	0.423804	0.654988	0.421984	5.72658	7.06991	5.72867	7.06543
9	0.356607	0.258991	0.356602	0.25911	7.66514	7.61183	7.65037	7.42241

The S/N Ratio for each level of process parameters is intended to produce the device which is more precise. The greater S/N Ratio values, the better the electrical characteristics for V_{TH} and I_{LEAK}. Hence, impact on the performance of the devices became higher [3]. Next, this process parameter was chosen to obtain a threshold voltage, V_{TH} value at (0.289 V ± 12.7%) guided by ITRS 2012 specification. The S/N ratio of Nominal-the-Best, ŋNTB can be demonstrated as [3]:

$$\eta NTB = 10 \log 10 \left(\frac{\mu^2}{\sigma^2}\right) \quad (4.1)$$

$$\mu = \frac{Y_i + \cdots + Y_n}{n} \quad (4.2)$$

$$\sigma^2 = \frac{\sum_{i=1}^{n} (Y_i - \mu)^2}{n-1} \quad (4.3)$$

where n is the number of experiments, Y_i is the experimental value of V_{TH}, μ is mean and σ is variance. The S/N ratio for I_{LEAK}, ŋSTB can be displayed as [3]:

$$\eta STB = -10 \log 10 \left[\frac{1}{n} \sum [Y_1^2 + Y_2^2 + \cdots Y_n^2]\right. \quad (4.4)$$

where n is the number of experiments, Y_i is the experimental value of I_{LEAK}. The ŋ (S/N Ratio) of each simulation for V_{TH} and I_{LEAK} were then measured using the formula in Equation.

Table 4.2: S/N Ratio for Nominal-the-Best

Expt. No.	Mean	Variance	S/N Ratio (Mean)	S/N Ratio (Nominal-the-Best)
1	2.52E-01	5.4739E-04	-1.20E+01	20.63
2	2.12E-01	9.6173E-04	-1.35E+01	16.72
3	1.47E-01	2.5324E-03	-1.66E+01	9.32
4	3.39E-01	4.0077E-03	-9.39E+00	14.58
5	2.62E-01	8.0218E-04	-1.16E+01	19.31
6	2.38E-01	5.6899E-04	-1.25E+01	19.99
7	6.04E-01	2.2502E-02	-4.38E+00	12.10
8	5.40E-01	1.8158E-02	-5.36E+00	12.05
9	3.08E-01	3.1723E-03	-1.02E+01	14.75

According to Table 4.2, S/N Ratio for Nominal-the-Best (NTB) value at rows 1, 5 and 6 given 20.63 dB, 19.31 dB and 19.99 dB respectively offer the great intolerance to the characteristics of devices. As orthogonal design is used, the impact on process parameter of S/N Ratio can be distinguished at various levels. In addition, the S/N Ratio for NTB are summarized in Table 4.2. By referring Table 4.3, the overall mean on S/N Ratio for the V_{TH} were tabulated.

Table 4.3: S/N Response for V_{TH}

Symbol	Control Factor	S/N Ratio (dB)			Overall Mean S/N	Max-Min
		L1	L2	L3		
A	Halo implant dose	15.56	17.96	12.97	15.49	4.99
B	Halo tilt angle	15.77	16.03	14.69		1.34
C	S/D Implantation	17.56	15.35	13.58		3.98
D	Compensation implant	18.23	16.27	11.98		6.25

Figure 4.1 indicates the factor effect graph on S/N Ratio for V_{TH}. The line graphs at the top and bottom represents the S/N Ratio of Nominal-the-best and also for Mean. When the S/N Ratio became higher, the electrical characteristics properties for the threshold voltage will became better. According the Figure 4.3, the graph is shown the Halo Implant Dose (Factor A) at first, following the Halo Tilt Angle (Factor B), the S/D implantation (Factor C) and the Compensation Implant (Factor D). The graph reveals the dosage of the Compensation Implant (Factor D) which is dominant factor since the maximum S/N ratio due to the slope in the graph was resulted the highest results as compared to the others process parameters. Whereas the Halo Tilt angle (Factor C) was considered as the adjustment factor because it had a low impacts on Nominal-the-best but had a greater effect on Mean.

Figure 4.3: Factor effect graph for the S/N Ratio for V_{TH}

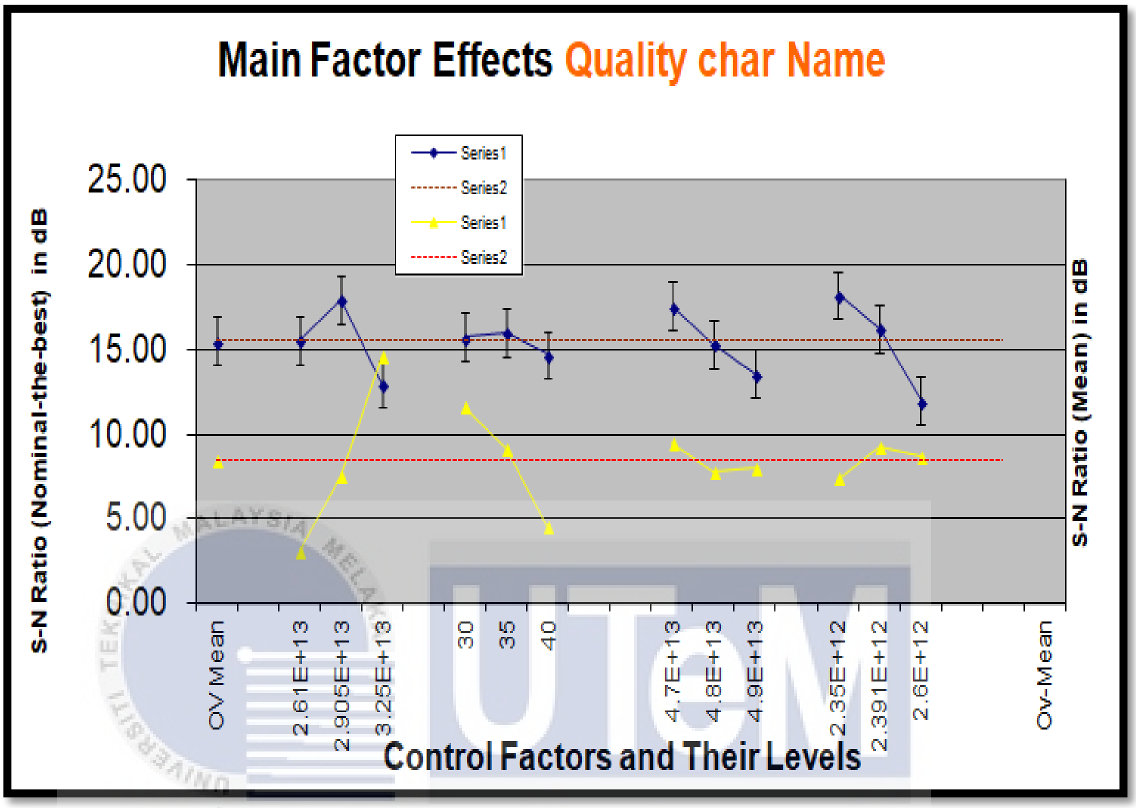


Table 4.4: S/N Ratio for Smaller-the-Better

Expt. No.	**S/N Ratio (Smaller-the-Better)**
1	162.74
2	163.99
3	165.03
4	162.32
5	162.82
6	163.23
7	164.31
8	163.83
9	162.40

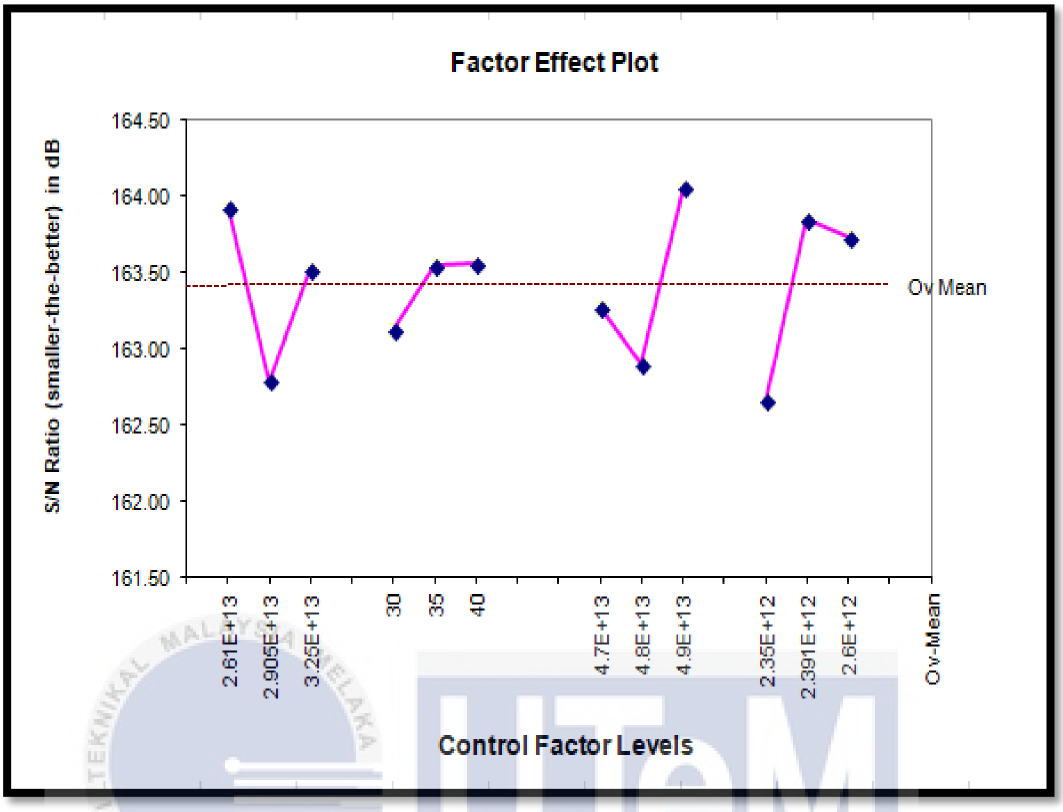
Stated in Table 4.4, the highest STB which is in row 3 has value of 165.03 dB. The higher value of STB shows in row 3 provides the best in sensitivity for the response characteristics. The S/N Response and overall mean for I_{LEAK} are tabulated in Table 4.5.

Table 4.5: S/N Response for I_{LEAK}

Symbol	Control Factor	S/N Ratio (dB)			Overall Mean S/N	Max-Min
		L1	L2	L3		
A	Halo implant dose	163.92	162.79	163.51	163.41	1.13
B	Halo tilt angle	163.12	163.55	163.55		0.43
C	S/D Implantation	163.27	162.90	164.06		1.16
D	Compensation implant	162.65	163.84	163.73		1.01

Factor effect graph on S/N Ratio for I_{LEAK} are as shown at Figure 4.4. The horizontal lines in the graph represent the results on overall mean for S/N Ratio of the I_{LEAK} which is 163.41 dB. Based on Figure 4.4, Halo Implantation (Factor A), following with Halo Tilt angle (Factor B), S/D Implantation (Factor C) and finally, Compensation Implant (Factor D) respectively. The graph demonstrates which Compensation Implant (Factor D) dose has been observed as a dominant factor since this factor has the highest S/N ratio values compared to other values.

Figure 4.4: Factor effect graph for the S/N Ratio for I_{LEAK}



4.3 Analysis of Variance (ANOVA) for V_{TH} and I_{LEAK}

Process parameters in V_{TH} and I_{LEAK} was examined in order to provide the great results for threshold voltage and leakage current and get the accurate value for current ratio. Thus, the outcome for ANOVA of the V_{TH} values is demonstrated in Table 4.6. The higher the factor effect on Anova-mean it will also gives the higher impacts on the reability of V_{TH} added with noise factor.

Table 4.6: Results of ANOVA for V_{TH}

Expt. No.	Control Factor	DF	SS	Mean Square	Factor Effect (%)	
					Anova-Nominal	Anova-Mean
V_{TH}	Halo Implant Dose	2	37	19	29.79	69.69
	Halo tilt angle	2	3	2	2.41	26.64
	S/D Implantation	2	24	12	18.99	1.78
	Compensation Implant	2	61	31	48.81	1.88

From Table 4.6, the ANOVA values for V_{TH} clearly show that the Compensation Implant with a percentage of 48.81 % provide greater effect on threshold voltage (V_{TH}), followed by Halo implant dose at 29.79 %, whereas the percentage of 18.99 % and 2.41 % is owned by S/D implantation and lastly the Halo Tilt angle respectively. While, the parameter of Halo Tilt angle acted as adjustment factor because of the percentage of factor effect in Anova-Nominal is higher than Anova-Mean.

The outcome of ANOVA for I_{LEAK} is tabulated as shown at Table 4.7. The factor effect (%) on STB indicates the higher factor effect (%) on STB affected to the result on the I_{LEAK}. The factor effect on the STB indicates the Compensation Implant dose as Dominant Factor in findings the lowest I_{LEAK} with 36.82 %, followed by the S/D Implantation with 29.79% and Halo Implant Dose with 28.22 %. The factor effect for the STB for the Halo Tilt angle was much lower, being 5.18 %.

Table 4.7: Results of ANOVA for I_{LEAK}

Expt. No.	Control Factor	DF	SS	Mean Square	Factor Effect (%)
V_{TH}	Halo Implant Dose	2	2	1	28.22
	Halo tilt angle	2	0	0	5.18
	S/D Implantation	2	2	1	29.79
	Compensation Implant	2	3	1	36.82

4.4 Confirmation of Optimum Run

The best combination factors were chosen given by the highest values on S/N ratio which can be refers in Table 4.3 and Table 4.4. For lowest I_{LEAK}, the highest score of S/N ratio for Factor A is level 1 (163.92 dB), Factor B is level 2 and 3 (163.55 dB), Factor C is level 3 (164.06 dB), and Factor D is level 2 (163.84 dB). Since Factor B was set as an adjustment factor in ANOVA, the dopant value was swept. Hence, the best combination factor for optimum I_{LEAK} is A1, B (sweep), C2, and D2. While for, the best combination factor for the V_{TH} was A2, B2, C1, and D1 as the factors score highest at level 2 (17.96 dB) for Factor A, level 2 (16.03 dB) for Factor B, while for Factor C is level 1 (17.56 dB) and Factor D which is in level 1 (18.23 dB). The best setting parameter which were determined by Taguchi method are as tabulated as stated at Table 4.8. Table 4.9 indicates the results of confirmation for V_{TH} and I_{LEAK}.

Table 4.8: Best Setting Parameter for V_{TH} and I_{LEAK}

Symbol	Control Factor	Unit	Best Values	
			V_{TH}	I_{LEAK}
A	Halo implant dose	Atom/cm^3	2.905×10^{13}	2.61×10^{13}
B	Halo tilt angle	Degree	Sweep (30 to 40)	35
C	S/D Implantation	Atom/cm^3	4.7×10^{13}	4.9×10^{13}
D	Compensation Implant	Atom/cm^3	2.35×10^{12}	2.391×10^{12}

Following the best setting parameter stated in Table 4.8, this simulation was applying in verified with the prediction values. For V_{TH}, the Halo Implantation was set up at Level 2, Halo Tilt angle was sweep to be between the value of 30˚ to 40˚. To obtain a V_{TH} final results which is applying the best setting parameter which is 37.5˚, the S/D Implantation dose set into Level 1 and lastly the value of compensation implantation adjust to Level 1. These final parameters will be simulates to achieve the optimal and best result as stated in Table 4.9.

Table 4.9: Results of Confirmation Experiment

Device	Performance Parameter	(X0,Y0)	(X0,Y1)	(X1,Y0)	(X1,Y1)	Best Values
NMOS	V_{TH} (V)	0.289433	0.236786	0.289505	0.2369	0.289433
	I_{LEAK} (nA / µm)	5.61104	8.04628	7.1459	7.77905	5.61104

Finally, the experiment resulted of V_{TH} value of 0.289433 V and an I_{LEAK} value with the 5.61104 nA/µm. The optimization results obtained for threshold voltage (V_{TH}) and leakage current (I_{LEAK}) are nearest with prediction by International Technology Roadmap for Semiconductors (ITRS 2012). The value of current ratio analysis is 4.4822 x 10^4 as stated in Table 5.0.

Table 5.0: ITRS Prediction vs. Optimization Results

Device	**Performance Parameter**	**ITRS Prediction**	**Optimization Results**
NMOS	V_{TH} (V)	0.289 ± 12.7%	0.289433
	I_{LEAK} (nA/µm)	100	5.61104

CHAPTER 5

CONCLUSION AND FUTURE WORKS

The designing and modeling of 22nm bilayer Graphene and High-K / Metal Gate (TiO_2 / WSi_X) NMOS transistor has been successfully delivered. The optimization of the threshold voltage (V_{TH}) and leakage current (I_{LEAK}) through L9 Taguchi Array analysis was also completely exploited along with Silvaco TCAD Tools for virtual fabrications and also for the electrical characteristics of the MOSFET. In this project, Compensation Implant was recognized as the Dominant Factor for V_{TH} and I_{LEAK} respectively while the Halo Tilt angle as an Adjustment Factor in V_{TH}. The project has resulted in a mean of V_{TH} value of 0.289433 V and the mean of leakage current of 5.61104 nA/µm. The values are closer with ITRS 2012 predictions. The minimum leakage current, I_{LEAK} was used to improve the speed efficiency of the device. Optimization using L9 Taguchi Array method, the great combination of control factors and noise factors results in a current ratio analysis of 4.4822×10^4. Recently, the vertical transistors evolves as a very attractive device design option to implement the double-gate and the cylindrical surrounding MOSFET's. Hence modeling and numerical analysis of the vertical transistors needs to be considered as an extension of this work.

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