DESIGN AND ANALYSIS OF 18NM GRAPHENE/TIO2/TISIX NMOS DEVICE USING TAGUCHI METHOD

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This report is submitted in partial fulfilment of the requirements for the degree of Bachelor of Electronic Engineering with Honours

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Universiti Teknikal Malaysia Melaka

2022

DECLARATION

I declare that this report entitled “Design and Analysis of 18nm Graphene/TiO2/TiSix NMOS Device Using Taguchi Method” is the result of my own work except for quotes as cited in the references.

Signature : ……..

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Date : 11 JANUARI 2022

APPROVAL

I hereby declare that I have read this thesis and in my opinion this thesis is sufficient in terms of scope and quality for the award of Bachelor of Electronic Engineering with Honours.

Signature : ……..

Supervisor Name : DR. AFIFAH MAHERAN BINTI ABDUL HAMID

Date : 11 JANUARI 2022

DEDICATION

To my wonderful and devoted father and mother, who have supported me since I was a youngster and are the reason for who I am now, Ahmad Fairuz bin Muhd Amin and Salbiah Binti Othman

ABSTRACT

Metal Oxide Semiconductor Field Effect Transistor (MOSFET) has been steady growth in high-speed switching applications in the semiconductor industry. As shrinking of the transistor size will enable a greater number of transistors to be placed in a chip. However, the conventional combination of regular Silicon Dioxide (SiO_2) and Polysilicon will be replaced with high-k materials which is Titanium Dioxide (TiO_2) as metal gate and Titanium Silicide ($TiSi_x$) as a gate dielectric. The main objectives of this project are to reduce the leakage current (I_{OFF}) and to obtain optimum threshold voltage (V_{TH}) for the NMOS device. The designed NMOS device are implemented using Silvaco software with ATHENA tool as a virtual fabrication process and ATLAS tool as an analyzing process for the device's electric properties. The results will be analyzed using Taguchi L9 orthogonal array method to obtain nominal values of threshold voltage and leakage current. The initial results before optimizing with the Taguchi Method are 0.500061 V for V_{TH} and 13.2042 pA/μm for I_{OFF}. Once the device is optimized with Taguchi Method, the optimum value for V_{TH} is 0.540576 V and 12.9181 pA/μm for I_{OFF}. These values are met with the targeted values based on International Technology Roadmap for Semiconductors (ITRS) 2013.

ABSTRAK

Transistor Kesan Medan Semikonduktor Oksida Logam (MOSFET) telah berkembang pesat dalam aplikasi berkelajuan tinggi dalam industri semikonduktor. Saiz transistor yang kecil akan membolehkan bilangan transistor yang lebih banyak diletakkan di dalam cip. Walau bagaimanapun, gabungan konvensional Silikon Dioksida (SiO_2) dan Polisilikon akan digantikan dengan bahan tinggi-k iaitu Titanium Dioksida (TiO_2) dan Titanium Silisid ($TiSi_x$). Objektif utama projek ini adalah untuk mengurangkan kebocoran arus (I_{OFF}) dan mengoptimumkan voltan ambang (V_{TH}) untuk peranti NMOS. NMOS yang direka akan ditunjukkan dalam perisian Silvaco dengan ATHENA sebagai proses fabrikasi maya dan ATLAS sebagai menganalisis sifat elektrik peranti tersebut. Keputusan akan dianalisis menggunakan kaedah tatasusunan ortogonal Taguchi L9 untuk mendapatkan nilai nominal voltan ambang dan kebocoran arus. Keputusan awal sebelum dioptimumkan dengan kaedah Taguchi ialah 0.500061 V untuk V_{TH} dan 13.2042 pA/μm untuk I_{OFF}. Setelah peranti dioptimumkan dengan kaedah Taguchi, nilai optimum bagi V_{TH} ialah 0.540576 V and 12.9181 pA/μm untuk I_{OFF} . Nilai-nilai ini memenuhi sasaran yang diterbitkan oleh Pelan Hala Tuju Teknologi Antarabangsa untuk Semikonduktor (ITRS) 2013.

ACKNOWLEDGEMENTS

Be grateful, I would like to express my highest gratitude to Allah for His guidance, which I have an opportunity to complete Bachelor Project Degree title of Design and Analysis of 18nm Graphene/TiO_2/$TiSi_x$ NMOS Device Using Taguchi Method, blessing and for giving me strength to perform my responsibilities as a student and complete this thesis within time.

A huge appreciation goes to the contribution of Faculty of Electronics & Computer Engineering. My dearest thanks to my lecturer and supervisor Dr. Afifah Maheran Binti Abdul Hamid who had assisted and supported me throughout this project. Not to be forgotten, to my other lecturers that always have supported and motivated me to undergo this degree.

Meanwhile, I am grateful to have a very understanding family member who always supports and is a concern in my studies. Also, a special word of appreciation goes to all individuals and my friends, especially Safiq Sar who were involved directly and indirectly in giving useful information and valuable comments for me completing my thesis. Thank you.

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LIST OF SYMBOLS AND ABBREVIATIONS

BPSG	:	Boron Phosphorus Silicate Glass
CVD	:	Chemical Vapor Deposition
FET	:	Field-Effect Transistor
HF-FOM	:	High-Frequency Figure of Merit
IC	:	Integrated Circuit
IoT	:	Internet of Things
ITRS	:	International Technology Roadmap for Semiconductor
I-V	:	Device Current-Voltage Characteristic
L9	:	Level 9
MOSFET	:	Metal Oxide Semiconductor Field Effect Transistor
NMOS	:	N-channel Metal Oxide Semiconductor
PECVD	:	Plasma Enhanced Chemical Vapor Deposition
PMD	:	Pre-Metal Dielectric
PMOS	:	P-channel Metal Oxide Semiconductor
P-Well	:	P-type diffusion is done over N-type substrate
SMIC	:	Semiconductor Manufacturing International Corporation
SOI	:	Silicon on Insulator
SDG	:	Split Dummy Gate

°C	:	Celcius
I_D	:	Drain current
I_{OFF}	:	Leakage current
keV	:	kilo-electronvolts
pA	:	picoampere
SiO_2	:	Silicon Dioxide
TiO_2	:	Titanium Dioxide
$TiSi_x$	:	Titanium Silicide
V_D	:	Drain voltage
V_{DS}	:	Drain to Source voltage
V_{GS}	:	Gate to Source voltage
V_{TH}	:	Threshold voltage
μm	:	micrometer

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CHAPTER 1

INTRODUCTION

1.1 Project Overview

Metal Oxide Semiconductor Field Effect Transistor (MOSFET) has been steady growth in high-speed switching applications in the semiconductor industry and also in IoT devices [1,2]. As shrinking of the transistor size will enable a greater number of transistors to be placed in a chip [3]. This will benefit to the low cost of manufacturing, increase in data speed and the ability to finish multiple tasks computing simultaneously in a shorter time [4]. In this project, the combination of regular Silicon Dioxide (SiO_2) and Polysilicon will be replaced with high-k materials. The main objectives of this project are to reduce the leakage current (I_{OFF}) and optimum threshold voltage (V_{TH}) for the NMOS device. The designed and analyzed NMOS will be demonstrated in Silvaco software with ATHENA as a virtual fabrication process

and ATLAS as analyzing the electric properties of the device. The results will be analyzed using Taguchi L9 orthogonal array method to obtain nominal values of threshold voltage and leakage current by following to an ITRS 2013 specification (V_{TH} = 0.54 V ± 12.7% and I_{OFF} < 20pA/μm).

1.2 Objectives

1. To design an 18nm NMOS device with low leakage current and acceptable threshold voltage using Silvaco software.
2. To analyze and optimize the V_{TH} and I_{OFF} using the Taguchi statistic method that is in line with ITRS 2013 prediction.

1.3 Problem Statement

In modern semiconductor industries, scaling down MOSFET will create a more beneficial and economical even to the consumers. This means the thickness of oxide and length of the gate must reduce to a smaller size. Shrinking down the dimension of a transistor is now already hit the limit [5,6]. Unforeseen results will occur when keep scaling down the transistors. The substitution of high-k materials Over SiO_2 will allow minimizing the leakage current and increase capacitance to prevent the short channel effect. Besides, the addition of graphene is required to the transistor because it has high carrier mobility. After all, electrons can move easily through graphene without resistance. Therefore, this project is proposed to solve those problems.

1.4 Scope of Work

The project scope is to design an 18nm planar NMOS device in simulation software and statistical method. The silicon dioxide and polysilicon will be substituted with high-k materials with the addition of Graphene. Silvaco software will be used where ATHENA conducts virtual fabrication and ATLAS as analyzing electrical properties. Taguchi method L9 orthogonal array is used as analyzing the electrical properties of the NMOS. This statistical method will get an optimized value for threshold voltage and current leakage that follows the ITRS 2013 standard.

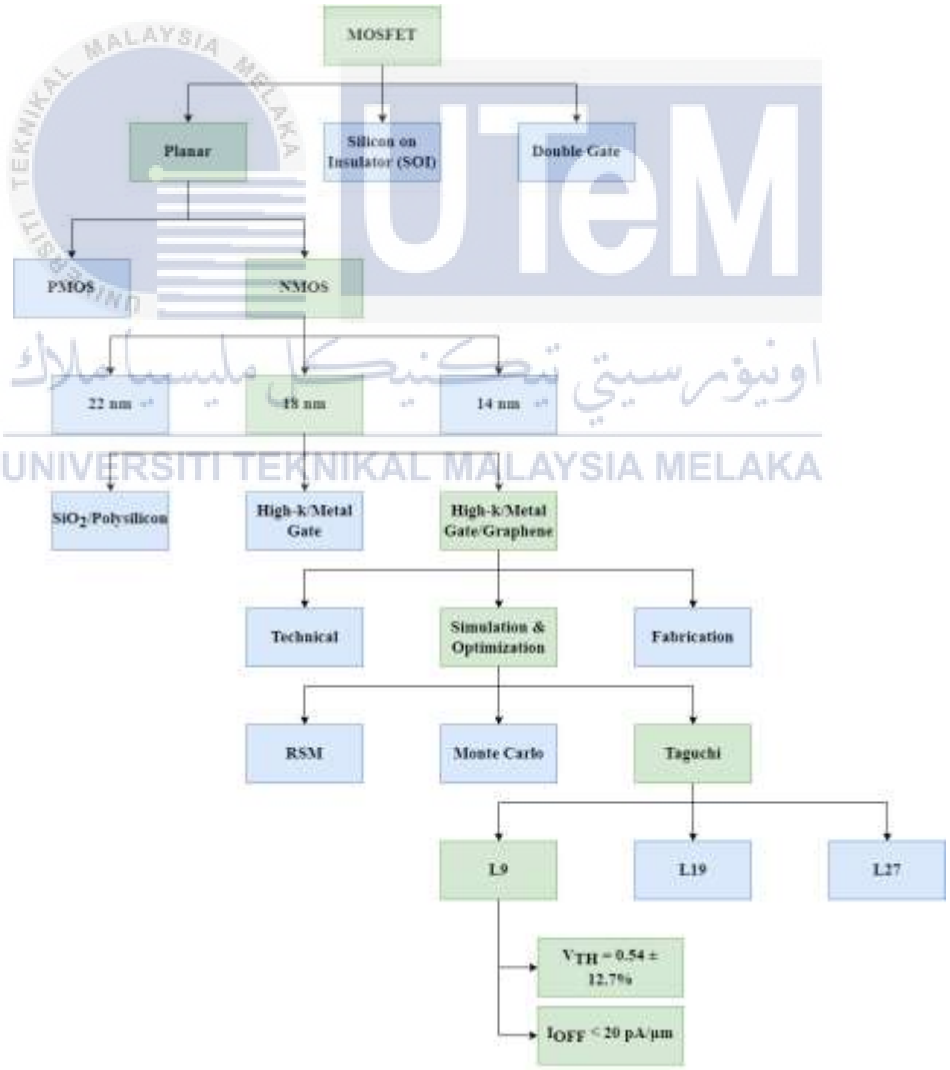

Figure 1.1: Scope of Project on designing and analysis 18nm NMOS device

1.5 Thesis Structure

The structure of this thesis is arranged into FIVE (5) main chapters excluding their subs. There are Chapter I Introduction, Chapter II Literature Review, Chapter III Research Methodology, Chapter IV Results and Discussion and Chapter V Conclusion and Recommendation.

Chapter I is an introduction to this thesis. This chapter acts as the first connection of this thesis that explains the project overview, the objective of this project, problem statement and scope of work.

Chapter II is about the Background Study which is an important part of this project. It discusses the previous work that had been done in the same field and the improvement towards the project. The background study covers the reviewed journals and also some theories that are required in supporting the research of this project.

Chapter III discusses the Research Methodology. This chapter explains the procedures that have been conducted in order to complete this project. This chapter also briefly discusses the flow of this project and system overview to give more understanding of the design and development concept of the project.

CHAPTER 2

BACKGROUND STUDY

2.1 Introduction

This chapter will give an introduction of the basic configuration of MOSFET and the relationship between Moore's Law. Besides, this chapter consists of materials overview that are being used in designing 18nm NMOS device with planar.

2.2 Basic Understanding of MOSFET

MOSFET or known as Metal Oxide Semiconductor Field Effect Transistor is a transistor that is widely used as switching and amplifying electronic signals in electronic devices [7]–[9]. MOSFET device usually consists of three main terminals: source, drain and gate terminal. Then, there is a substrate underneath it. Based on Figure 2.1, MOSFETs are divided into two types, PMOS where uses n-type substrate and NMOS uses p-type substrate. The majority of carriers for PMOS are holes while in NMOS are electrons. Therefore, NMOS is being used more compared to PMOS because of electrons move faster than holes which means have better velocity.

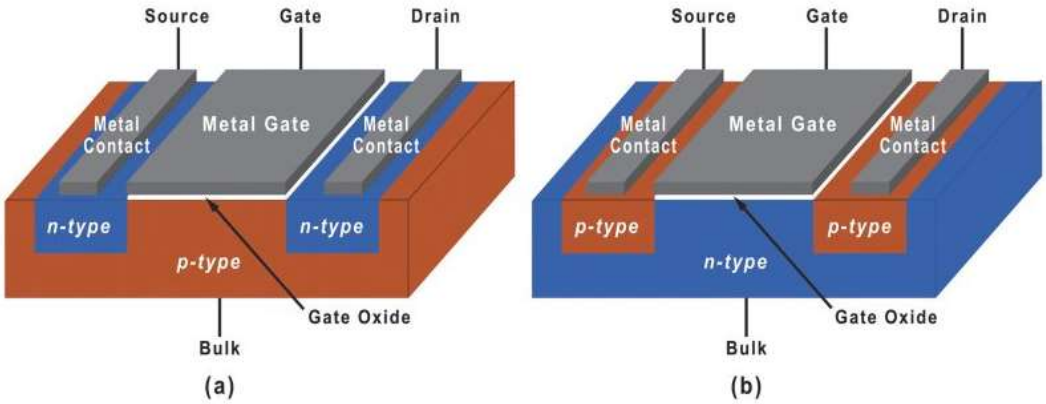

Figure 2.1: NMOS (a) device and PMOS (b) device [10]

In general, when a drain-source voltage (V_{DS}) is linked between the drain and the source, the drain receives a positive voltage while the source receives a negative value. The PN junction at the drain is reverse biased, while the PN junction at the source is forward biased in this example. There will be no current flow between the drain and the source at this point.

When the V_{GG} is supplied with positive voltage to the gate terminal, the minority charge carriers (electrons) in the P substrate begin to gather on the gate contact, forming a conductive bridge between the two n+ areas due to electrostatic attraction. The strength of the provided positive voltage determines the number of free electrons accumulated at the gate contact. The wider the n-channel generated by electron accumulation, the higher the applied voltage; this finally increases the conductivity, and the drain current (I_D) begins to flow between the Source and Drain.

There will be no current flow if no voltage is given to the gate terminal, except for a little amount of current due to minority charge carriers. The threshold voltage is the lowest voltage at which the MOSFET begins to conduct.

Two operations of MOSFET are applied between NMOS and PMOS: (i) Depletion mode and (ii) Enhancement mode. Depletion is accomplished in a variety of ways. Because they are normally in the closed state when no bias voltage is provided to the gate terminal, MOSFETs are commonly referred to as "Switched ON" devices. The channel width is increased in depletion mode by increasing the applied voltage to the gate in the positive direction. As a result, the channel's drain current I_D will be increased. Meanwhile, the enhancement mode is identical to the open switch mode, where it starts to conduct when the V_{GS} is applied with positive voltage and drain current starts flowing through the device. The width and drain current increase directly proportional to the bias voltage is increase. The transistor, however, will remain in the OFF state if the supplied bias voltage is zero or negative.

2.3 Graphene

Graphene is a two-dimensional carbon allotrope that may be considered as a solid as well as a macromolecule, having molecular weights of more than 10^6-10^7 g/mol [11]–[13]. It is a one-atom-thick organic crystal made up of a single sheet of carbon atoms [13,14]. Companies from a variety of industries are salivating over graphene's features: its mobility is predicted to be 250 times that of silicon, and its flexibility and other properties make it perfect for a variety of applications, from battery technology to optoelectronics like touch screens [16]. This means that Graphene has great material properties. Table 2.1 shows the comparison of characteristic of Silicon, Germanium, Gallium Arsenide and Graphene.

Table 2.1: Properties of Si, Ge, GaAs and Graphene [17,18]

Property	Symbol	Units	Si	Ge	GaAs	Graphene
Mobility: a. Electron	μ_e	$cm^2V^{-1}s^{-1}$	1417	3900	8800	100.000
b. Holes	μ_h		471	1900	400	100.000
Thermal Conductivity	κ	$cm^2V^{-1}s^{-1}$	141	61	46	~600

Graphene is one of the important materials on designing the NMOS device because it is capable to operate at low voltage with high sensitivity [19,20]. These characteristics distinguish graphene-based transistors are better compared to silicon-based transistors [8,20]. Furthermore, due to graphene's inherent characteristics, such transistors are very flexible and bendable [18,19]. Electrons move 1000 to 10,000 times quicker through graphene than they do in silicon [23]. As a result, in terms of electron mobility, it outperforms silicon. However, because of the bandgap problem, graphene cannot be utilized as a silicon substitute.

2.4 Literature Review

This section will review the previously developed by [24] of NMOS device where the simulated device performance obtained was I_{OFF} = 9.29746 nA/μm which is indicated below than ITRS prediction value. The process of optimizing the device was applied with Taguchi L9 orthogonal array method. Four parameters were used to

control in Taguchi orthogonal method: (i) Halo Implantation, (ii) Halo Tiling Angle, (iii) S/D Implantation and (iv) Compensation Implant. The researcher mentioned that tiling the angle is the dominant factor for this NMOS device. In another research paper proposed by [25], the 19nm NMOS device was designed 2k-factorial design. Parameter (i) and (v) were also being adjusted with Halo implant energy and S/D implant energy in order to get optimized values for the NMOS device. The results obtained are also meet the ITRS standard at I_{OFF} = 2.217 pA/μm. Halo Implant dose and S/D implant were recognized as dominant process parameters that affect the characteristics of the NMOS device.

By referring to Moore's Law, he stated that the number of transistors in a dense integrated circuit doubles approximately every two years [26]. This means that as transistors continue to shrink, SiO_2 or Polysilicon gate has to be replaced with high-k/metal gate to facilitate further scaling. The main reason for choosing high-k over polysilicon as the metal gate is the high bandgap in polysilicon. Figure 2.2 shows that polysilicon has the highest voltage bandgap with the lowest number of dielectric constant. Then, the metal gate enables more precise threshold voltage adjustment, gate resistance and removes any implants that are no longer required by the device.

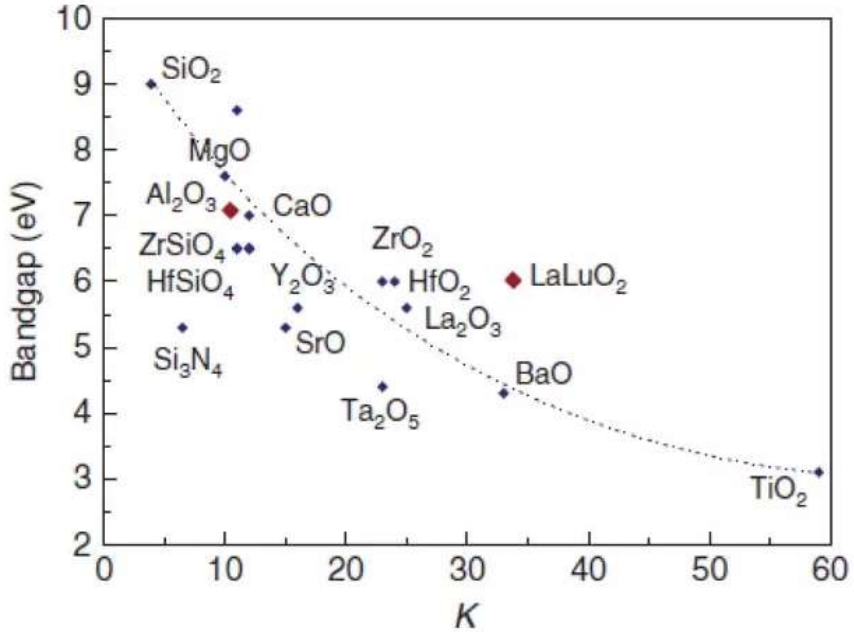

Figure 2.2: Band Diagram between polysilicon and other high-k material [27]

In obtaining of an optimized NMOS device, the ionizing dose is one of the parameters to exhibit a better device. This is because ion implantation provides a steadily shifting junction depths and dopant concentration in lateral device dimensions was scaled to be used in the next generation of transistors design and fabrication process.

2.5 Summary of Previous Research

Table 2.2 shows some research on the modelling, characterization and simulation of NMOS the device using real fabrication lab and also virtual fabrication such as in Silvaco software.

Table 2.2: Summaries of the fabrication NMOS device

No.	Reference	Author/Journal/Year	Summary
1.	[24]	A. H. Afifah Maheran *et al.*, "Minimum leakage current optimization on 22 nm SOI NMOS device with HfO2/WSix/Graphene gate structure using Taguchi method, 2020	• 22nm SOI NMOS • Hafnium Dioxide (HFO_2) and Tungsten Silicide (Wsi_x) • I_{OFF} = 9.29746 nA/µm
2.	[25]	F. Salehuddin *et al.*, "Analyze of process parameter variance in 19nm Wsi2/Tio2 NMOS device using 2k-factorial design, 2018	• 19nm NMOS • Tungsten Disilicide (WSi_2) and Titanium Dioxide (TiO_2) • I_{ON} = 591.38 µA/µm • I_{OFF} = 2.217 pA/µm
3.	[28]	H. Magenthiran and A. M. A. H, "DESIGN AND ANALYSIS OF 18nm GRAPHENE / HfO 2 / WSi x NMOS DEVICE USING TAGUCHI METHOD, 2021	• 18nm NMOS • Graphene, Hafnium Dioxide (HfO_2) and Tungsten Silicide (WSi_x) • V_{TH} = 0.549704 V • I_{OFF} = 0.531801 nA/µm
4.	[29]	P. Mogan and A. M. A. H, "Taguchi Method Analysis in Designing an 18nm Graphene / TiO_2 / WSi_x NMOS Device, 2021	• 18nm NMOS • Graphene, Titanium Dioxide (TiO_2) and Tungsten Silicide (WSi_x) • V_{TH} = 0.5335519 V • I_{OFF} = 6.07587 nA/µm
5.	[30]	D. Mohanta and S. S. Singh, "Effect of using High-k Dielectric Material on Transconductance of a Strained-Si PMOS, 2021	• Effect of high-k on strained silicon PMOS • Arora model • 80% enhancement of transconductance
6.	[31]	S. K. Mah, I. Ahmad, P. J. Ker, K. P. Tan, and Z. A. N. Faizah, "Modelling, simulation and optimization of 14nm high-K/metal gate NMOS with taguchi method," 2018	• 14nm NMOS • Lanthanum oxide (La_2O_3) and Tungsten Disilicide (WSi_2) • V_{TH} = 0.233321 V • I_{OFF} = 47.32375 pA/µm
7.	[32]	A. Siddiqi, N. Jain, and M. Rashed, "Back-bias generator for post-fabrication threshold voltage tuning applications in 22nm FD-SOI process," 2018	• Back-Bias Generator for for Forward-Back-Bias in 22nm FD SOI • 33-40% RO f_{max} improvement

8.	[33]	M. S. Kim *et al.*, "12-EUV Layer Surrounding Gate Transistor (SGT) for Vertical 6-T SRAM: 5-nm-class Technology for Ultra-Density Logic Devices," 2019	• EUV 6T SRAM with 5nm • 0.0205 μm^2 unit cell area
9.	[34]	C. Luo, Z. Li, T. T. Lu, J. Xu, and G. P. Guo, "MOSFET characterization and modeling at cryogenic temperatures," *Cryogenics (Guildf).*, vol. 98, pp. 12–17, 2019	• Performance of SMIC 0.18 μm / 1.8 V CMOS • Model based on BSIM3v3 • Optimization approach using temperature-dependent parameters
10.	[35]	P. Vudumula and S. Kotamraju, "Design and Optimization of 1.2-kV SiC Planar Inversion MOSFET Using Split Dummy Gate Concept for High-Frequency Applications," *IEEE Trans. Electron Devices*, 2019	• 1.2-kV SiC planar MOSFET • Split dummy gate (SDG) • 0.2 μm dummy gate has best HF-FOM

CHAPTER 3

METHODOLOGY

3.1 Project Flow

Based on Figure 3.1 and Figure 3.2, the designing and modelling an NMOS device is start with a bilayer planar on the transistor gate. The analysis will be carried out using Silvaco software and will be based on a set of experiments, device construction, and structural modelling of 18nm planar NMOS device performance using bi-layer graphene. 18nm NMOS devices are using the ATHENA module as virtual fabrication and ATLAS module as electrical properties in the semiconductor that will be designed. Semiconductor TCAD tools are one of the biggest key components of designing an NMOS device because it is able to design a complex semiconductor that is being used by industrial fabrication software. As a result, the semiconductor is designed as a specific real-world device. The electrical characteristics of the NMOS device will be analyzed by using the L9 experimental array of the Taguchi method. The results will be compared to the value of the ITRS 2013 standard.

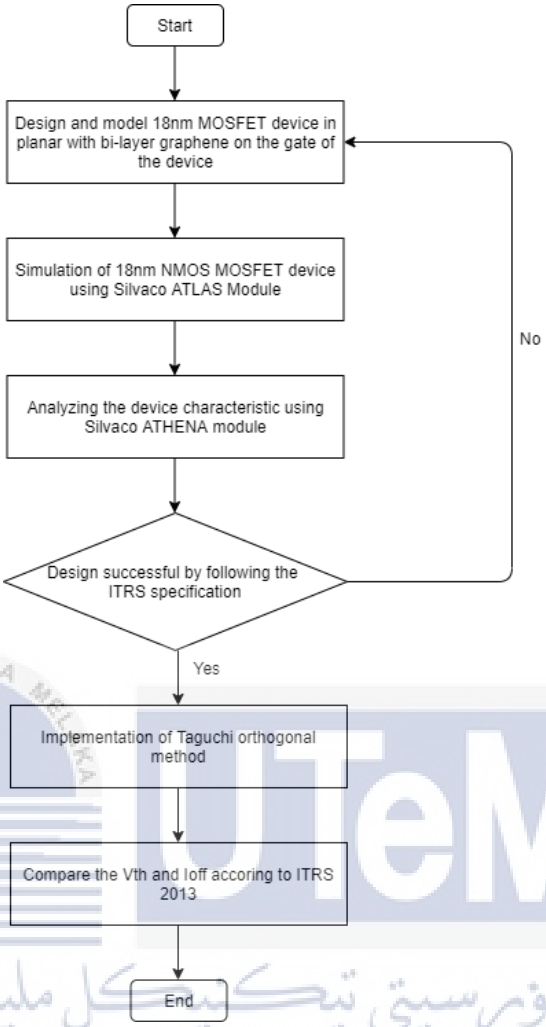

Figure 3.1: Project Flowchart

3.2 Silvaco Software

Silvaco ATHENA and ATLAS module are both TCAD tools which used as controlling and utilizing the downscaling of MOSFET. TCAD has become an important and powerful tool to improve the efficiency of the power device design and its optimization [36]. In terms of designing, fabricating, and simulating semiconductor devices, semiconductor TCAD tools are at the forefront. MOSFET technology needs an optimization strategy in device modelling to get optimal performance. Instead of

fabrication in a clean room, this software will save the manufacturing cost, which is critical in the industry to perform the optimization of the manufacturing operation of the product.

The packages that will be used in Silvaco is Deckbuild, ATHENA, ATLAS and Tonyplot. Deckbuild, ATHENA and ATLAS software that can perform fabrication process simulation and display the output of the run-time simulation. Meanwhile, Tonyplot is used to analyze and visualize the simulated results from those three packages in Silvaco. The International Technology Roadmap for Semiconductors (ITRS) confirms the worldwide manufacturing industry, predicting a 40% decrease in development costs in 2016 due to TCAD deployment [37]. This means that many types of circuit elements such as capacitors that are connected to the device electrode can resemble the actual measurement on the device. Figure 3.2 shows on project planning of designing an 18nm planar NMOS device by referring to ITRS 2013 standard.

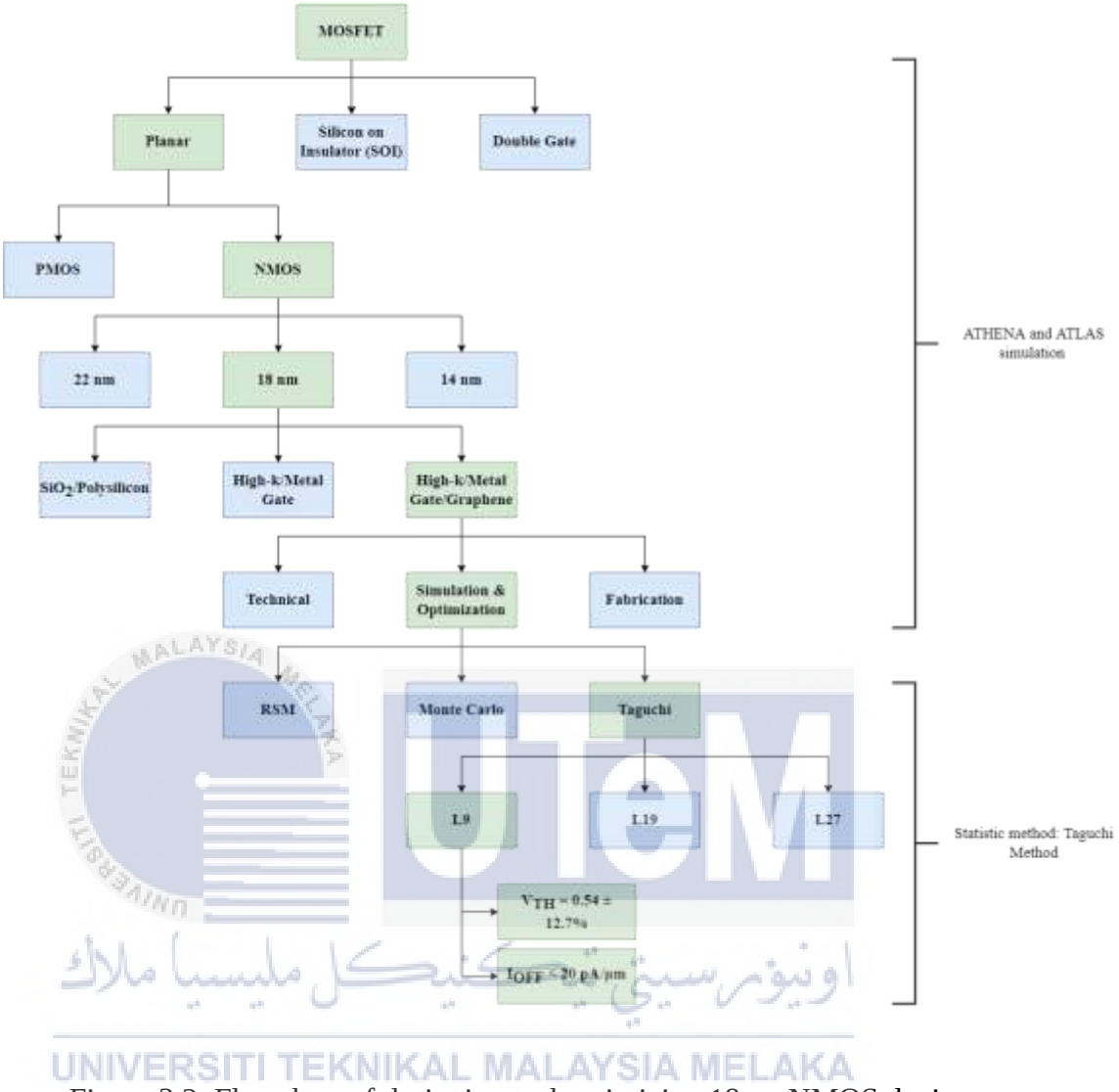

Figure 3.2: Flowchart of designing and optimizing 18nm NMOS device

3.2.1 Fabrication Process (ATHENA)

Figure 3.3 shows the fabrication process that is summarized into a flowchart that follows from the start to the end process.

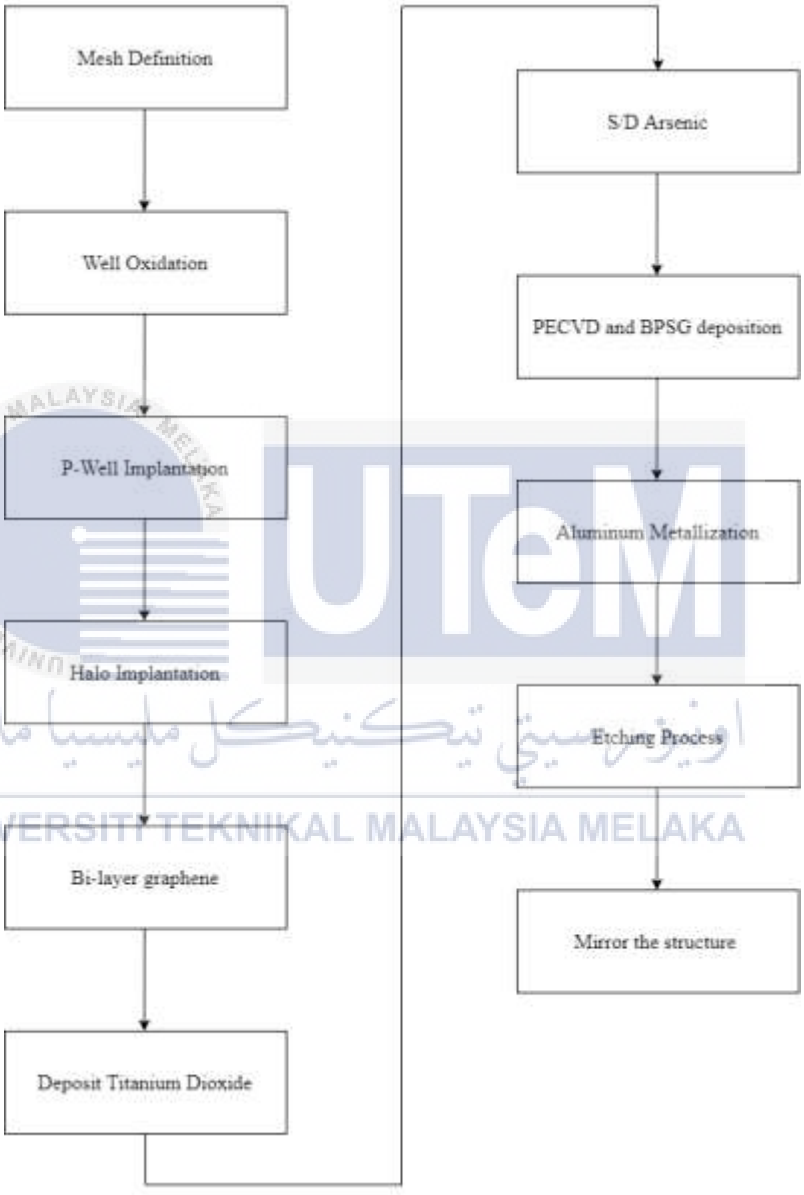

Figure 3.3: Fabrication Process in ATHENA

3.2.1.1 Meshing

The device started with meshing <100> oriented of p-type silicon. SiO2 deposited in the substrate and pre-deposition of boron at 7.0 x 10^{14} atom/cm^3 as in Figure 3.4.

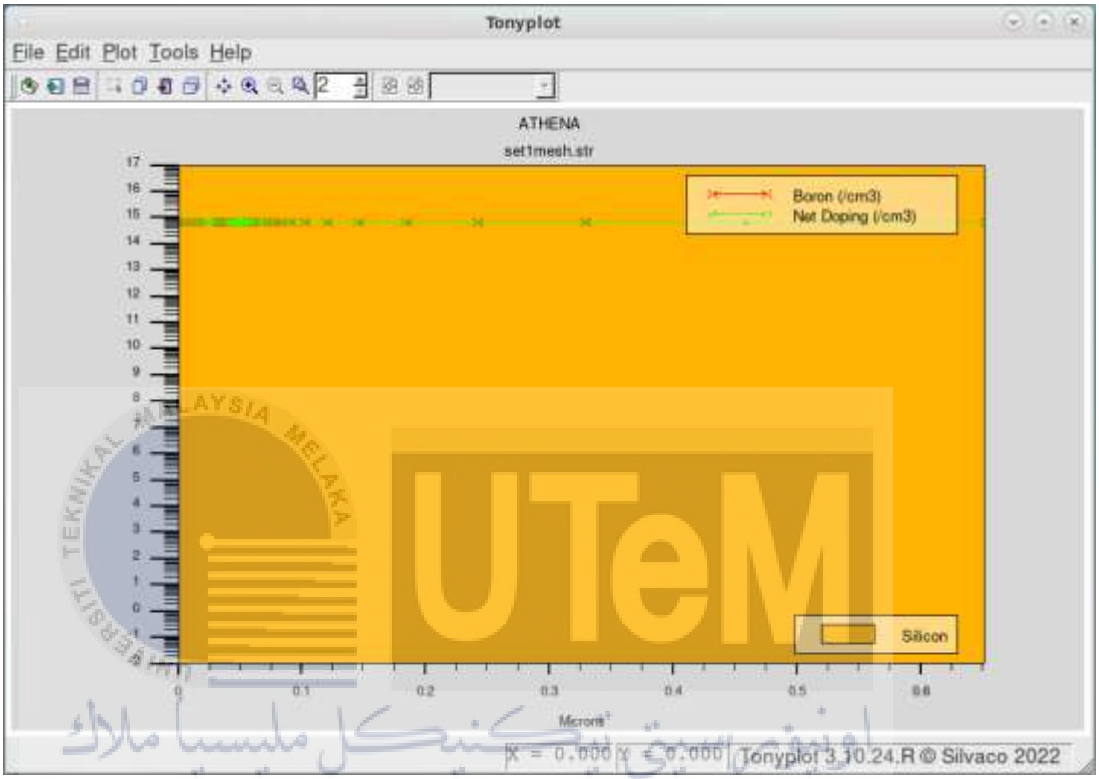

Figure 3.4: Defines silicon as the mesh's primary material

3.2.1.2 Well Oxidation

Create well oxidation by using 200A SiO2 on the top layer of the substrate. Figure 3.5 shows the structure after the process of diffusing dry oxygen with 870° Celsius at 20 minutes.

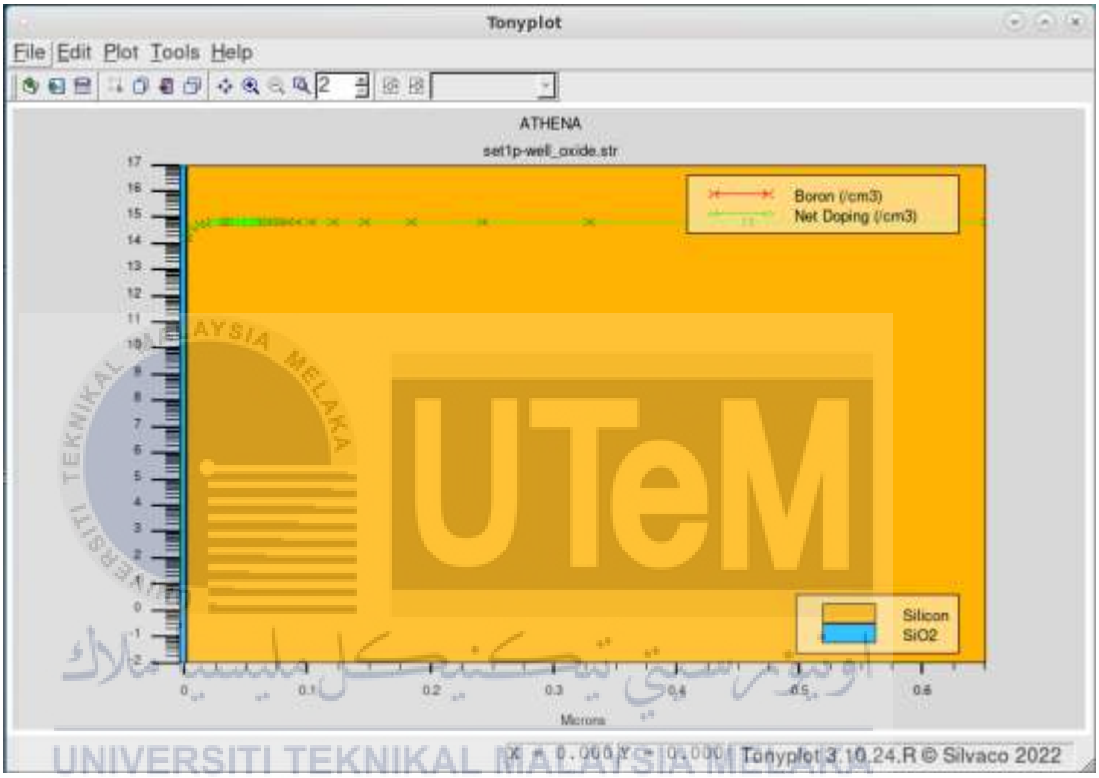

Figure 3.5: Process of Well Oxidation in 18nm NMOS device

3.2.1.3 P-Well Implantation

Then, the device is implant dose with boron at 3.75 x 10^{12} atom/cm3 with 100 KeV of implant energy, tilting the angle in 7 degrees and rotating at 30 degrees, 120, degrees, 210 degrees and 300 degrees respectively and then diffused with 30 minutes, 900° Celsius and 1atmosphere gas pressure as shown in Figure 3.6.

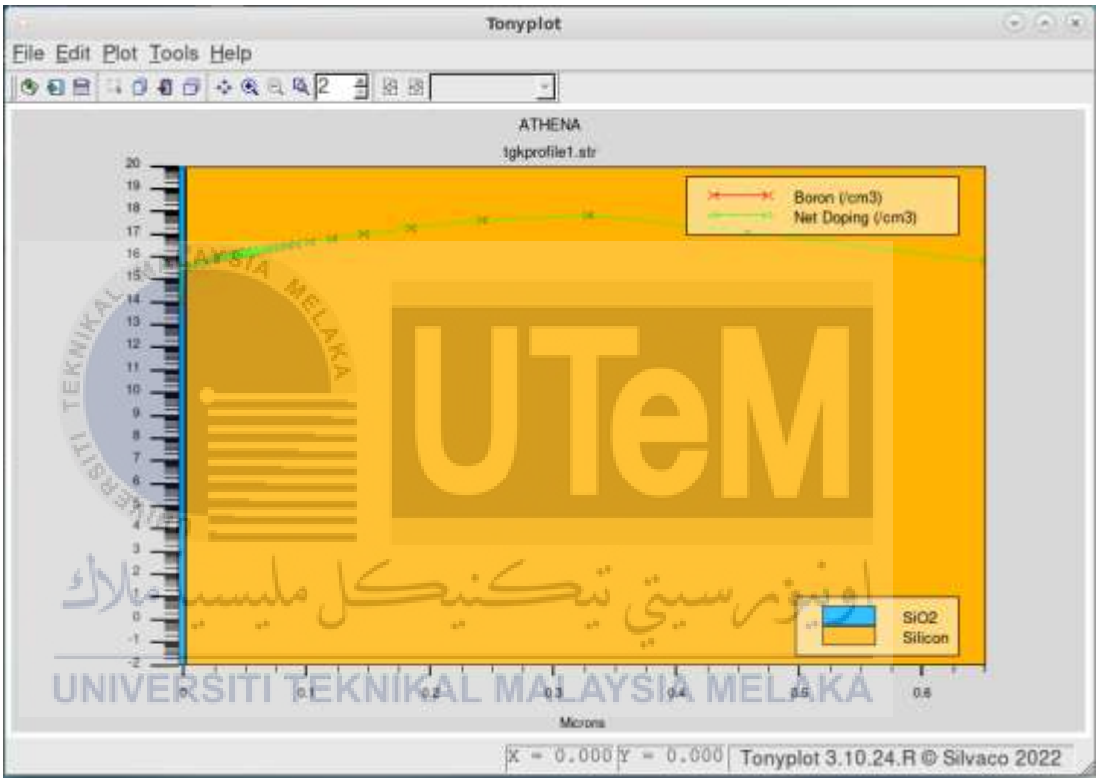

Figure 3.6: Process of P-well Implantation in 18nm NMOS device

3.2.1.4 Bi-layer graphene

Next, the graphene is deposited with a thickness of 680 x 10-^{5} um/cm^{3} and etched started from 0.03um/cm^{3} to the left side of the device as shown in Figure 3.7.

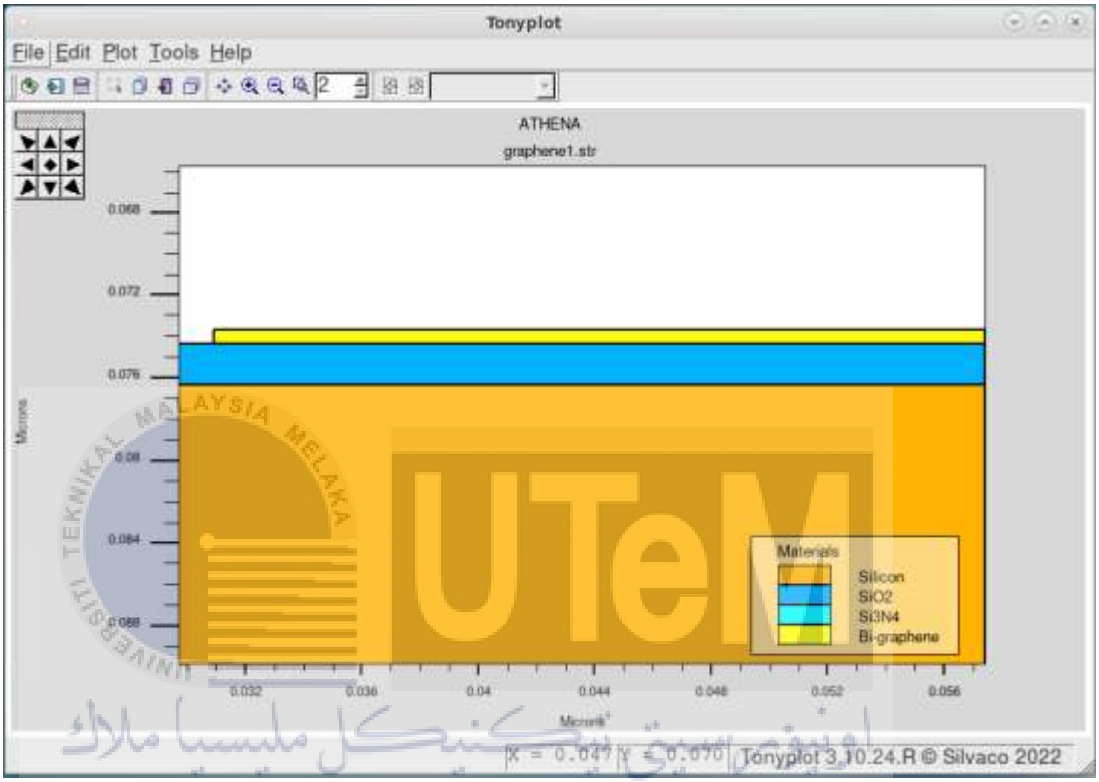

Figure 3.7: Process of adding bilayer of graphene

3.2.1.5 High-K Material

The high-k material for this NMOS device is titanium dioxide (TiO_2) which is deposited with a thickness of 0.002um/cm^3. The material is etched and scaled into 18nm metal gate dielectric of the transistor. This process then continued with depositing titanium silicide ($TiSi_x$) at thickness 0.045um/cm^3 on top of the TiO_2 and etched at the same length as shown in Figure 3.8.

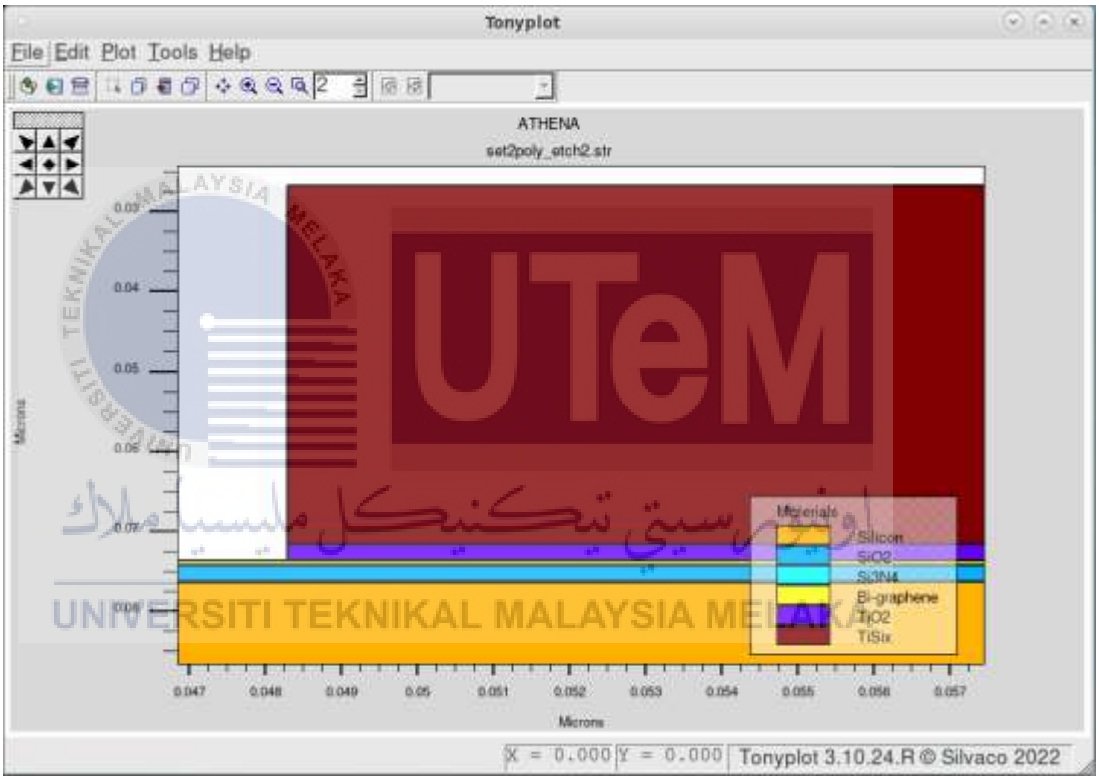

Figure 3.8: Process of etching 18nm material gate dielectric and metal gate

3.2.1.6 Source and Drain Arsenic

The substantially n-type doped region within the p-type substrate is presented by implanting an arsenic atom. This is to ensure that the device's surface current flow is smooth. Figure 3.9 shows before and after the implantation of arsenic dose into the device.

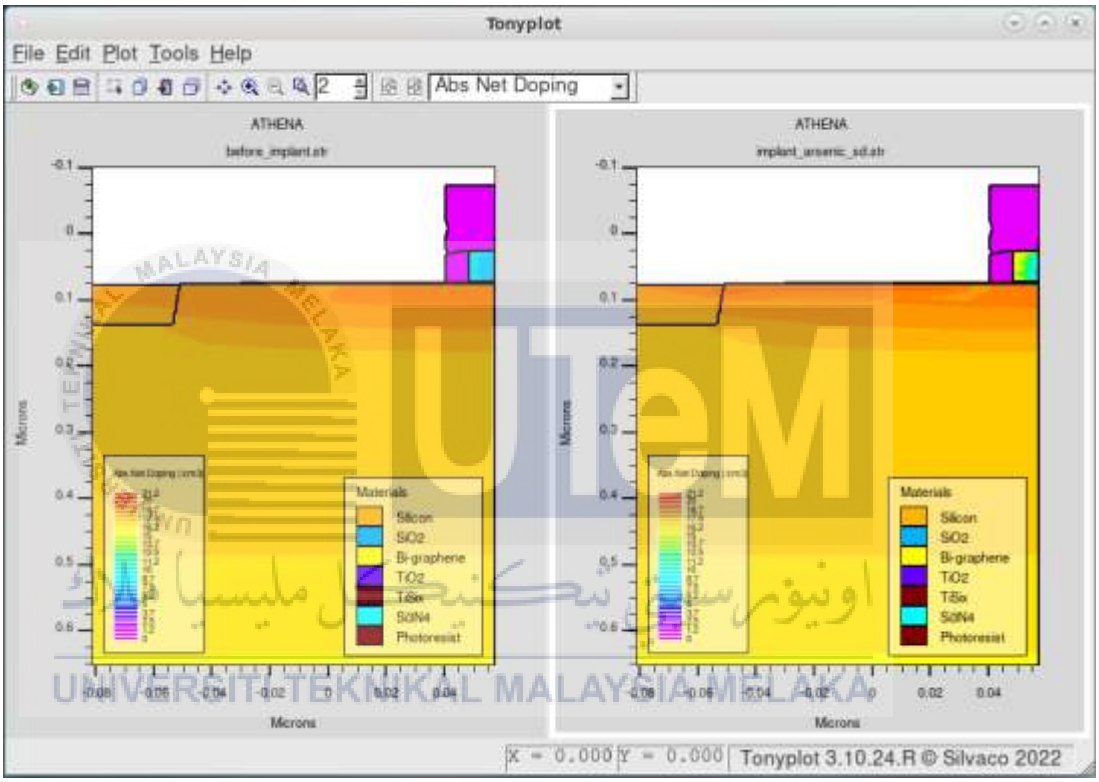

Figure 3.9: Arsenic Implantation

3.2.1.7 PECVD and BPSG

Plasma Enhanced Chemical Vapor Deposition (PECVD) and Boron Phosphorus Silicate Glass (BPSG) are used to establish the process of condition to increase film quality and deposition rate by establishing process conditions. Besides, those methods are used as a low-temperature flow-able PMD that ensures enough metal coverage across steps and into contact, preventing metal discontinuities or local regions with thin metal over steps. Figure 3.10 shows before and after the deposition of the BPSG.

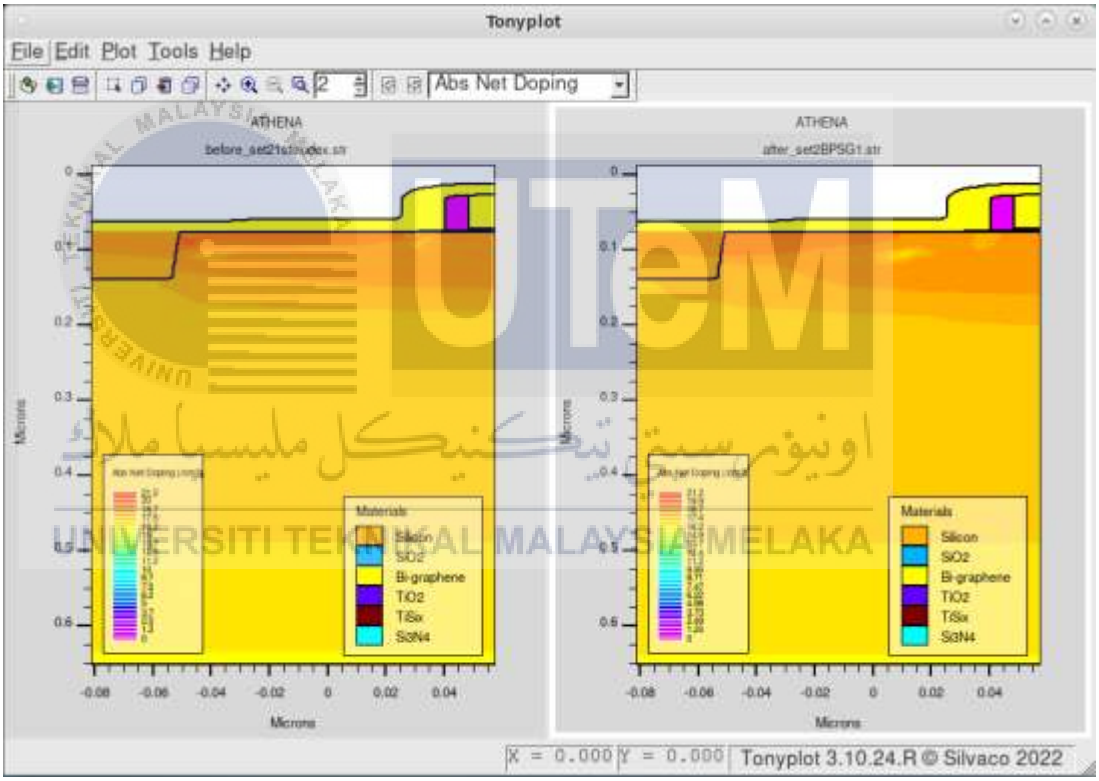

Figure 3.10: BPSG Process

3.2.1.8 Patterning Source and Drain Contact

This patterning process is to create a current flow to move through source and drain and followed with implant phosphorus which to reduce the side capacitance as shown in Figure 3.11.

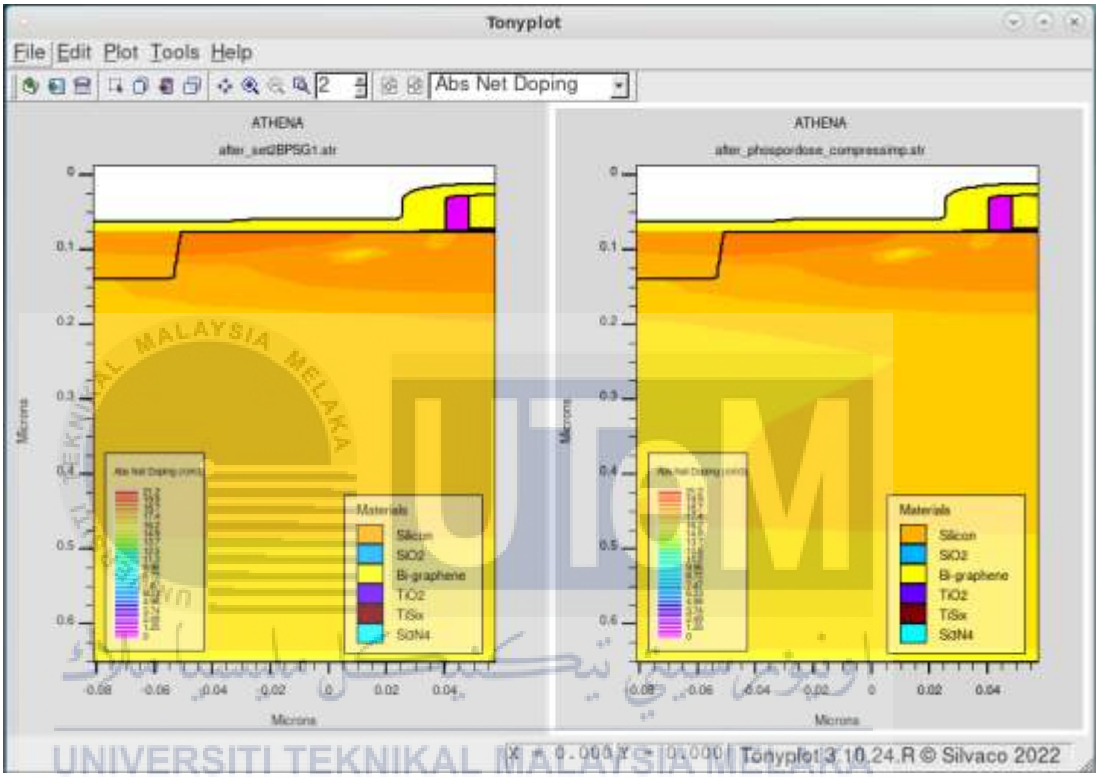

Figure 3.11: Before and after implant phosphorus/compensation

3.2.1.9 Aluminium Metallization and Etching

Lastly, the aluminium is being etched within a range of size were to create metal contact between source and drain. The 18 nm NMOS device is etched as shown in Figure 3.12.

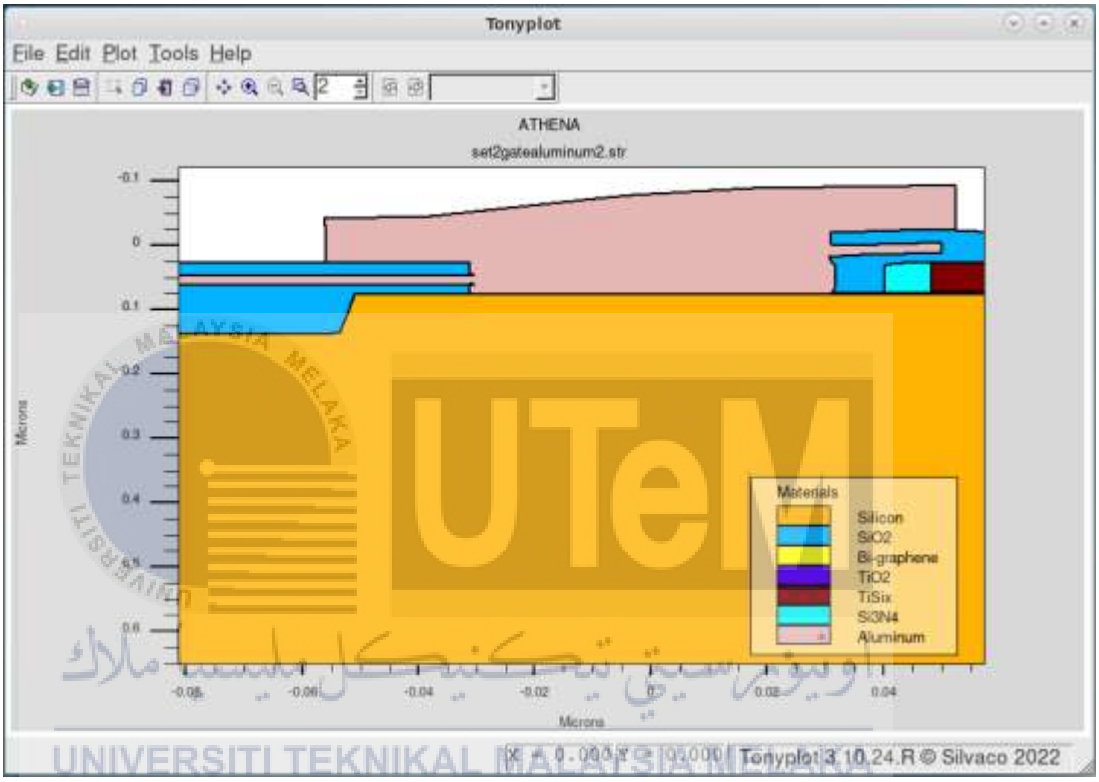

Figure 3.12: Process of Aluminium Etching

3.2.2 Device Simulation (ATLAS)

The flowchart shown in Figure 3.13 is a summarization of processes that are done for the device within the simulation in the ATLAS program from beginning to the parameter extraction. The simulation is simulated the IV characteristic and electrical properties of the device.

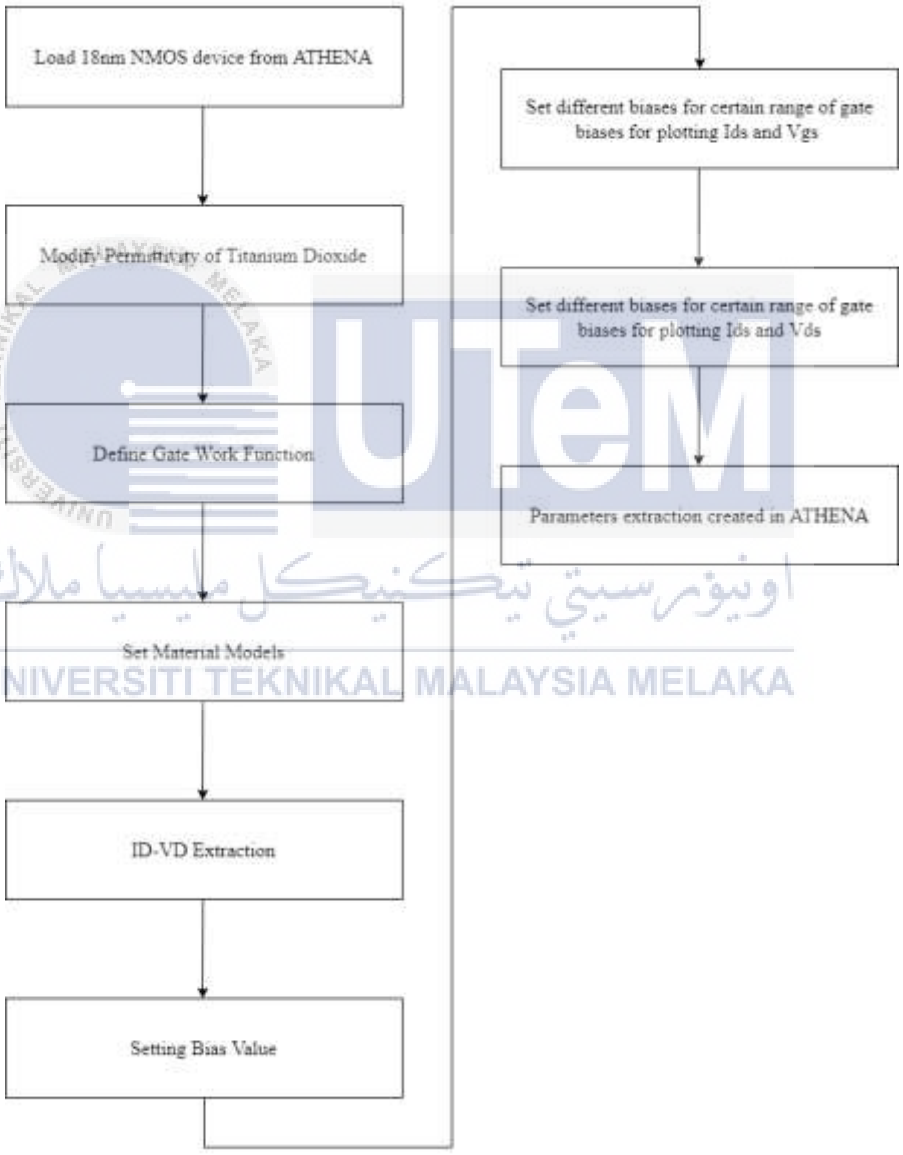

Figure 3.13: Flowchart of device simulation in ATLAS

CHAPTER 4

RESULTS AND DISCUSSION

4.1 Introduction

18nm NMOS device is fabricated virtually in ATHENA and analyzed the electrical properties through ATLAS. In this chapter, the results will be shown and followed by discussions. The simulation will be compared before and after the fabricated virtual 18 NMOS device using Taguchi Orthogonal Array.

4.2 Simulation Result of the Device

ATHENA and ATLAS were done using Silvaco simulation software. The I_D-V_{DS} and I_D-V_{GS} characteristic of the 18nm device was plotted in ATLAS. ATHENA is used virtually fabricated 18nm NMOS device.

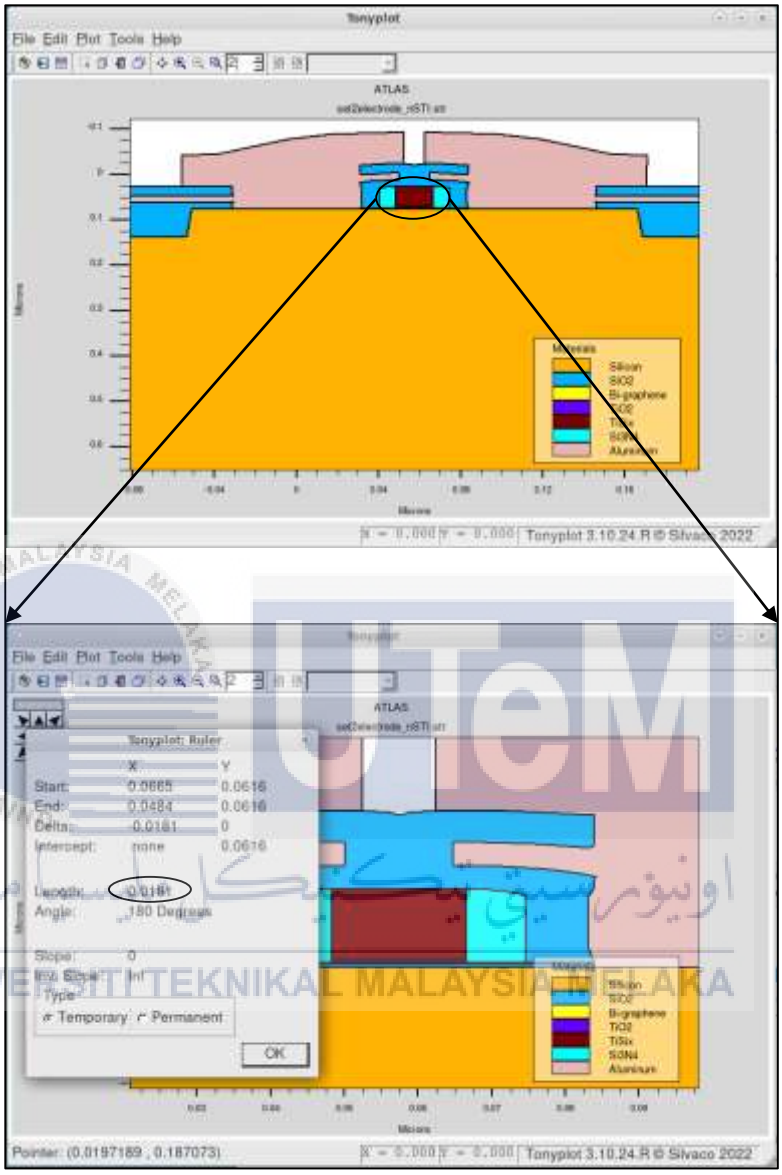

Figure 4.1: Close-up of 18nm gate length

Figure 4.1 shows a completed structure of planar NMOS device with the value length of the gate length in micron which is equivalent to 18nm. The fabricated NMOS device in ATHENA was mirrored to the right side of the MOSFET.

Figure 4.2 below shows the doping profile of the 18 nm NMOS device. It shows that the highly doped area seems under source and drain region.

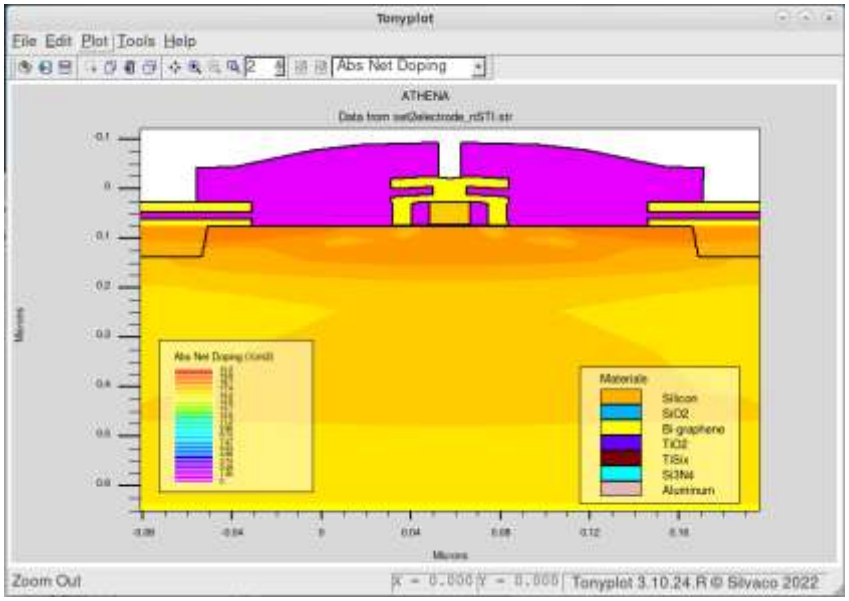

Figure 4.2: Doping profile of 18nm NMOS MOSFET

In Figures 4.3 and 4.4, the graph shows the characteristic of the NMOS device, which are I_D-V_{DS} and I_D-V_{GS} characteristics.

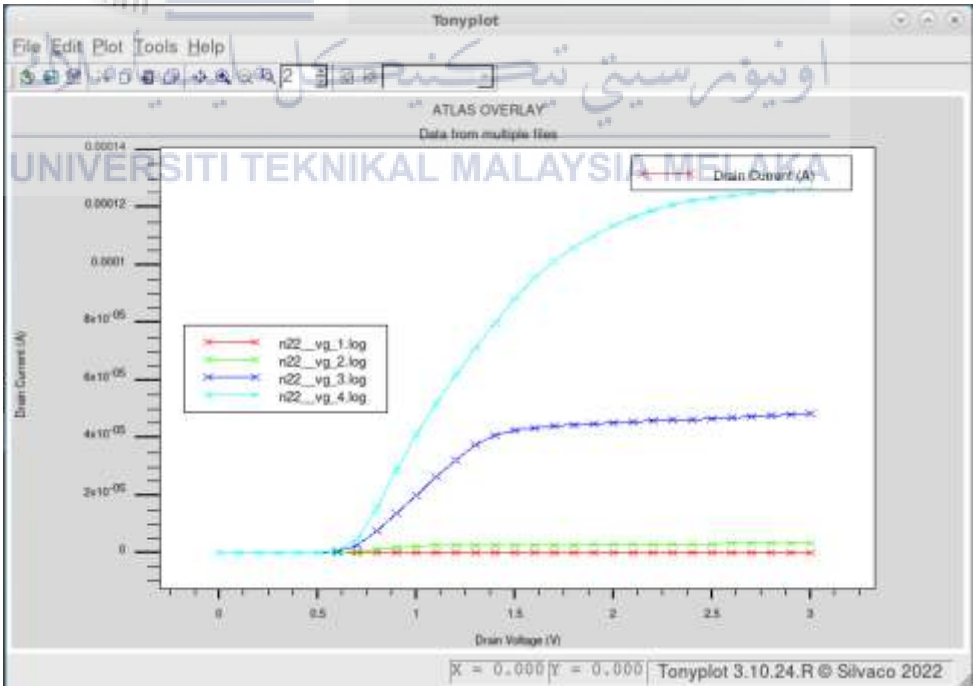

Figure 4.3: I_D-V_{DS} characteristic of the 18nm NMOS device

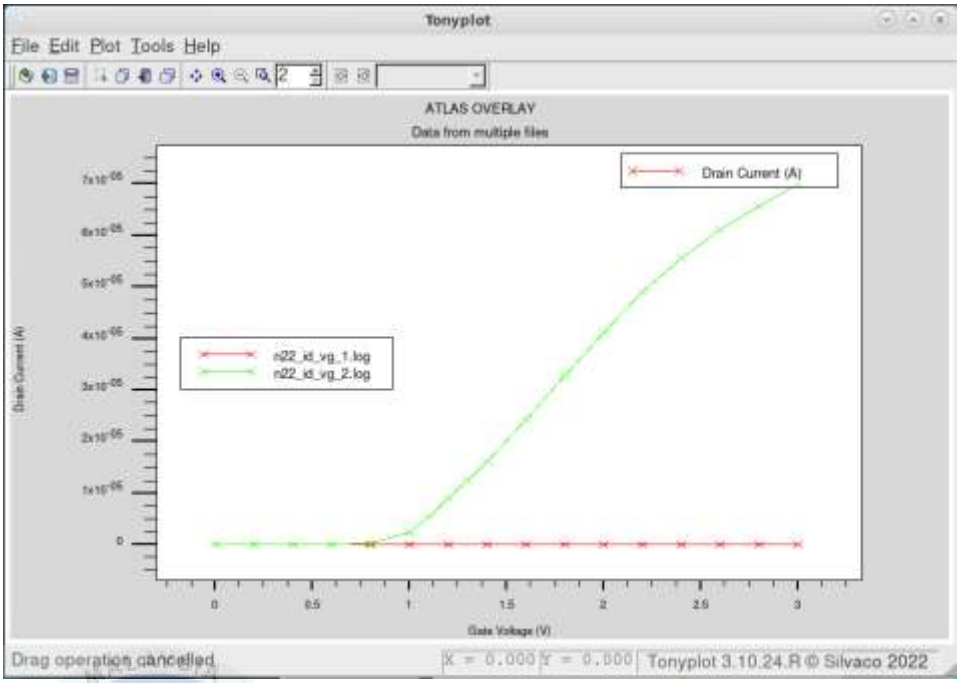

Figure 4.4: I_D-V_{GS} characteristic of the 18nm NMOS device

The threshold voltage of a MOSFET is important because it is defined when the gate voltage will start to turn on. This is because to predict correct circuit behavior from a circuit simulator where accurate threshold voltage modelling is required. Table 4.1 shows the initial result of the threshold voltage and leakage current for the 18nm NMOS device that uses $TiO_2/TiSi_x$ which will be analyzed using the Taguchi method to obtain a better result.

Table 4.1: Initial value of V_{TH} and I_{OFF} 18nm NMOS device

Parameter	Value	ITRS 2013
V_{TH} / V	0.500061	0.540 ± 12.7%
I_{OFF} / pA/μm	13.2042	<100

4.3 Taguchi Orthogonal L9 Array (Statistical Method)

The L9 Taguchi orthogonal array is used to obtain optimized process parameters for the simulation device which are the best combination that will gain high performance of device through a set number of experiments. It contains about 36 running experiment simulations which consist of 4 control factors and 2 noise factors in the Taguchi L9 orthogonal array. The process parameters are selected based on the reading which is the most major factor that will give more alter values to the device. The control factors are Factor A as Halo Implantation, Factor B as Halo Title Angle, Factor C as S/D Implantation and Factor D as Compensation Implantation. Two noise factors are involved in the experiments which are Factor X as Sacrificial Oxide Layer (PSG) and Factor Y BPSG Oxide Temperature. Table 4.2 and Table 4.3 shows the values that will be used in the experiment.

Table 4.2: Process Parameters

Symbol	Process Parameter	Unit	Level 1	Level 2	Level 3
A	Halo Implantation dose	$Atom/cm^3$	$2.852x10^{13}$	$2.857x10^{13}$	$2.862x10^{13}$
B	Halo Implantation Tilt angle	degree	33	35	37
C	S/D Implantation dose	$Atom/cm^3$	$4.77x10^{13}$	$4.8x10^{13}$	$4.83x10^{13}$
D	Compensation Implantation	$Atom/cm^3$	$23.43x10^{13}$	$23.93x10^{13}$	$24.43x10^{13}$

Table 4.3: Noise Factors

Symbol	Noise Factor	Unit	Level 1	Level 2
X	Sacrificial Oxide Layer PSG	°C	950	953
Y	BPSG	°C	920	923

4.3.1 Analyze the (S/N) Ratio for V_{TH} and I_{OFF}

Nine sets of tests, totaling 36 simulations, were carried out with four control factors and two levels of noise. Table 4.4 and Table 4.5 shows simulation results by using process parameters and noise factors values from Table 4.2 and Table 4.3.

Table 4.4: V_{TH} results for 18nm Bi-Layer Graphene NMOS device

Expt. No.	Vth1 (X0,Y0)	Vth2 (X0,Y1)	Vth3 (X1,Y0)	Vth4 (X1,Y1)
1	0.679958	0.549870	0.548337	0.428199
2	0.490292	0.396658	0.413862	0.391097
3	0.389893	0.362519	0.383829	0.355165
4	0.652721	0.523257	0.524400	0.421650
5	0.461356	0.392629	0.409498	0.386703
6	0.402844	0.378700	0.397425	0.361534
7	0.620077	0.495027	0.495027	0.413796
8	0.545756	0.428467	0.432166	0.399982
9	0.398750	0.373752	0.393331	0.366571

Table 4.5: I_{OFF} results for 18nm Bi-Layer Graphene NMOS device

Expt. No.	Ioff1 (X0,Y0)	Ioff 2 (X0,Y1)	Ioff 3 (X1,Y0)	Ioff 4 (X1,Y1)
1	12.8×10^{-12}	13.0×10^{-12}	25.6×10^{-12}	26.5×10^{-12}
2	13.2×10^{-12}	13.5×10^{-12}	27.5×10^{-12}	28.5×10^{-12}
3	13.7×10^{-12}	13.9×10^{-12}	29.9×10^{-12}	31.1×10^{-12}
4	12.8×10^{-12}	13.1×10^{-12}	25.9×10^{-12}	26.7×10^{-12}
5	13.3×10^{-12}	13.5×10^{-12}	27.9×10^{-12}	28.9×10^{-12}
6	13.5×10^{-12}	13.7×10^{-12}	28.8×10^{-12}	29.8×10^{-12}
7	12.9×10^{-12}	13.2×10^{-12}	13.2×10^{-12}	27.1×10^{-12}
8	13.1×10^{-12}	13.3×10^{-12}	26.9×10^{-12}	27.8×10^{-12}
9	13.6×10^{-12}	13.8×10^{-12}	29.2×10^{-12}	30.2×10^{-12}

Through S/N ratio calculation, the results are utilized to verify the factor that has the most significant effect on the device. The V_{TH} analysis is associated with the nominal-the-best quality feature, whereas I_{OFF} is linked with the smaller-the-best quality characteristic. To obtain the nominal value of V_{TH} as well as the lowest possible value for I_{OFF}, the statistical technique is applied. The S/N ratio for nominal-the-best can be expressed as Equation 4.1. Besides, the S/N ratio for smaller-the-best can be expressed as Equation 4.2.

$$\eta_{NTB} = 10\log_{10}\left(\frac{\mu^2}{\sigma^2}\right) \tag{4.1}$$

$$\eta_{STB} = -10\log_{10}\frac{1}{n}\left(\sum_{i=1}^{n} y_i^2\right) \tag{4.2}$$

Both V_{TH} and I_{OFF} are calculated the mean and variance using Equation 4.3 and Equation 4.4.

$$\mu = \frac{Y_i + \ldots + Y_n}{n} \tag{4.3}$$

$$\sigma^2 = \frac{\sum_i^n \left(Y_i - \mu\right)^2}{n-1} \tag{4.4}$$

Because the experimental design is in orthogonal, the influence of the S/N ratio can be separated at every level in the computation. The S/N ratio of each level for V_{TH} and I_{OFF} is calculated in Table 4.6 and Table 4.7 respectively. The higher the ratio value, the better the characteristic of V_{TH} and I_{OFF}. Therefore, device performance will be better.

Table 4.6: S/N ratio for V_{TH}

Factor	S/N Ratio (Mean) (Nominal-the-Best)			Total mean S/N Ratio
	Level 1	Level 2	Level 3	
A	20.30	20.96	20.11	20.45
B	15.01	19.30	27.05	
C	19.24	20.73	21.39	
D	21.4	20.33	19.63	

Table 4.7: S/N ratio for I_{OFF}

Factor	S/N Ratio (Mean) (Smaller-the-Better)			Total mean S/N Ratio
	Level 1	Level 2	Level 3	
A	213.14	213.19	213.72	213.35
B	214.16	213.20	212.68	
C	213.31	213.19	213.55	
D	213.18	213.69	213.18	

4.3.2 Analysis of Variance (ANOVA) for V_{TH} and I_{OFF}

The most widely used statistical analysis is the analysis of variance (ANOVA)., which is used to calculate the percentage of the contribution factor that has a significant impact on device performance. The ANOVA results are shown in Table 4.8 and Table 4.9. As mentioned earlier, the highest value of the S/N ratio will contribute as the most dominant factor which affects the device performance. Table 4.8 shows that Halo Tilt Angle is the most dominant factor for the threshold voltage. Besides, the dominant factor for leakage current is Halo Tilt Angle, which is the same as the process parameter for the threshold voltage.

Table 4.8: ANOVA Analysis for V_{TH}

Symbol	Process Parameter	Factor Effect	
		NTB	Mean
A	Halo Implantation	0.51	0.16
B	Halo Tilt Angle	94.39	95.06
C	S/D Implantation	3.08	4.14
D	Compensation Implantation	2.02	0.64

Table 4.9: ANOVA Analysis for I_{OFF}

Symbol	Process Parameter	Factor Effect
		STB
A	Halo Implantation	13.06
B	Halo Tilt Angle	71.55
C	S/D Implantation	4.41
D	Compensation Implantation	10.98

4.3.3 Confirmation of Optimum Factor

Several simulations are run with various Halo title angle values in order to get the threshold voltage as close to the desired value as possible. The S/D Implantation dose is changed from $4.8x10^{13}$ into $4.7x10^{13}$ until which the threshold voltage reaches 0.54V, which is close to ITRS 2013. The optimal angle for fabricating an 18nm NMOS device, according to the experiments, is $4.65x10^{13}$. Table 4.10 shows the Taguchi method's best-projected setting for the device's process parameters. The final

parameters are simulated with noise factor to get the optimal result and confirmation experiment with added noises factor in Table 4.11. Therefore, the new threshold voltage for the 18nm NMOS device after optimization is 0.540576 V. It is within the ITRS 2013 value (0.540V ± 12.7%).

Table 4.10: Best Setting simulation for V_{TH}

Factor	Process Parameter	Unit	Level	Best Value
A	Halo Implantation dose	Atom/cm^3	2	2.857x10^{13}
B	Halo Implantation Tilt angle	^{o}	3	37
C	S/D Implantation dose	Atom/cm^3	Sweep	4.65x10^{13}
D	Compensation Implantation	Atom/cm^3	1	23.43x10^{13}

Table 4.11: Confirmation test result for V_{TH}

V_{TH1}(X0,Y0)	V_{TH2}(X0,Y1)	V_{TH1}(X1,Y0)	V_{TH1}(X1,Y1)
0.540576	0.423995	0.428754	0.397208

Meanwhile for leakage current, the best combination factor is shown as in Table 4.12. The lowest value leakage current can be obtained is 12.9181 pA/μm which is lower than the ITRS 2013 prediction, which is below 20 pA/μm.

Table 4.12: Best Setting simulation for I_{OFF}

Factor	Process Parameter	Unit	Level	Best Value
A	Halo Implantation dose	Atom/cm^3	3	2.862x10^{13}
B	Halo Implantation Tilt angle	degree	1	33
C	S/D Implantation dose	Atom/cm^3	3	4.83x10^{13}
D	Compensation Implantation	Atom/cm^3	2	23.93x10^{13}

Table 4.13: Confirmation test result for I_{OFF}

I_{OFF1}(X0,Y0)	I_{OFF2}(X0,Y1)	I_{OFF3}(X1,Y0)	I_{OFF4}(X1,Y1)
12.9181x10^{13}	13.1535x10^{13}	26.1889x10^{13}	27.0571x10^{13}

Table 4.14: Comparison V_{TH} and I_{OFF} 18nm NMOS device

Parameter	Value	ITRS 2013
V_{TH} / V	0.540576	0.540 ± 12.7%
I_{OFF} / pA/μm	12.9181	<20

CHAPTER 5

CONCLUSION AND FUTURE WORKS

5.1 Conclusion

In conclusion, the designed NMOS device by using bi-layer graphene, TiO_2 and $TiSi_x$ as a high-k gate by using Silvaco TCAD was achieved. The electrical properties such as V_{TH} and I_{OFF} of the device were analyzed and optimized using the Taguchi L9 orthogonal array. The main parameter for designing on the small-scaled device is the threshold voltage, V_{TH}. The leakage current, I_{OFF} must be kept as slow as possible to minimize the amount of static power consumed by a circuit while it is in standby mode. The optimum value of V_{TH} and I_{OFF} in this research can be concluded that it was following the prediction of ITRS 2013 and achieved the objective that was pointed out in the early chapter. It is important to select which material that is suitable for designing a small-scale device that can achieve the target value of V_{TH} and I_{OFF} of the NMOS MOSFET device. Based on the experiments that have been conducted, the

Halo tilt angle was determined as the most dominant factor that contributed to the changes of V_{TH} and I_{OFF}. Besides, the S/D Implantation dose was identified as an adjustment factor in the device. The reason why one of the process parameters has to be considered as an adjustment factor is that to obtain threshold voltage and leakage current that is close to the ITRS 2013 standard, which is 0.54 V and below 20 pA/μm. It was found out that the V_{TH} value was 0.540576 V where is in between the tolerance standard, 12.7% and also acceptable leakage current at 12.9181 pA/μm.

5.2 Sustainability and Environmental Friendly

This project is still relevant because the planar process is a popular method in the semiconductor industry to build transistors, especially in high nodes [38]. Plus, developing planar transistors are much cheaper compared to finFET transistors. In addition, the approach of developing the device was carried out entirely in simulation, using Silvaco TCAD software, this project is environmentally benign. As a result, the device was created virtually, so no materials were wasted. This will be a great starter or as planning on fabricating the semiconductor device in the future.

5.3 Future Work

According to the acquired simulated findings, analysis, and research conclusion, this should be a continuous research project to achieve the best performance with low leakage current gate of the NMOS device. Some of the recommendations include improving the simulation of the NMOS device by shrinking the MOSFET size, which will be in line with the semiconductor industry's trend.

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APPENDIX A

Table PIDS3a Low Power (LP) Technology Requirements - TCAD

Year of Production	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028
Logic Industry "Node Range" Labeling (nm) [based on 0.7 in reduction per "Node Range" ("Node" = ~2x hp)]	"16/14"		"11/10"		"8/7"		"6/5"		"4/3"		"3/2.5"		"2/1.5"		"1/0.75"	
MPU/ASIC Metal 1 (M1) ½ Pitch (nm) (contacted)	40	32	32	28.3	25.3	22.5	20.0	17.9	15.9	14.2	12.6	11.3	10.0	8.9	8	7.1
L_g: Physical Gate Length for HP Logic (nm)	25	21	19.0	18.0	16.0	14.6	13.3	12.2	11.1	10.1	9.3	8.5	7.7	7.0	6.4	5.9
L_{ch}: Effective Channel Length (nm) [1]	18.4	16.8	15.2	14.4	12.8	11.7	10.6	9.8	8.9	8.1	7.4	6.8	6.2	5.6	5.1	4.7
V_{dd}: Power Supply Voltage (V)																
Bulk/SOI/MG	0.86	0.85	0.83	0.81	0.80	0.78	0.77	0.75	0.74	0.72	0.71	0.69	0.68	0.66	0.65	0.64
EOT: Equivalent Oxide Thickness																
Bulk/SOI/MG (nm)	0.80	0.77	0.73	0.70	0.67	0.64	0.61	0.59	0.56	0.54	0.51	0.49	0.47	0.45	0.43	0.41
Dielectric constant (K) of gate dielectrics	12.5	13.0	13.5	14.0	14.5	15.0	15.5	16.0	16.5	17.0	17.5	18.0	18.5	19.0	19.5	20.0
Physical gate oxide thickness (nm)	2.56	2.57	2.53	2.51	2.49	2.46	2.42	2.42	2.37	2.35	2.29	2.26	2.23	2.19	2.15	2.10
Channel Doping (10^{18}/cm^3) [4]																
Bulk	5.0	6.0	7.0	7.7	8.4											
SOI/MG	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1
Body Thickness (nm) [5]																
SOI																
MG	7.4	6.7	6.1	5.8	5.1	4.7	4.3	3.9	3.6	3.2	3.0	2.7	2.5	2.2	2.0	1.9
T_{BOX}: Buried Oxide Thickness for SOI (nm) [6]																
SOI																
CET: Capacitance Equivalent Thickness (nm) [7]																
Bulk/SOI/MG	1.10	1.07	1.03	1.00	0.97	0.94	0.91	0.89	0.86	0.84	0.81	0.79	0.77	0.75	0.73	0.71
C_{ox} intrinsic (fF/μm) [8]																
Bulk/SOI/MG	0.577	0.542	0.509	0.497	0.455	0.429	0.404	0.379	0.356	0.332	0.317	0.297	0.278	0.256	0.242	0.229
Mobility (cm^2/V-s)																
Bulk	400	400	400	400	400											
SOI																
MG	375	375	375	375	375	375	375	300	300	300	300	300	225	225	225	225
I_{off} (nA/μm) [9]																
Bulk	10	10	20	20	50											
SOI																
MG	10	10	10	10	10	10	10	20	20	20	20	20	30	40	40	50
I_{dsat}: NMOS Drive Current (μA/μm) [10]																
Bulk	490	459	456	485	422											
SOI																
MG	643	610	608	589	574	556	550	533	537	461	458	395	396	337	334	295
$V_{th,lin}$ (V) [11]																
Bulk	0.619	0.639	0.636	0.670	0.647											
SOI																
MG	0.483	0.492	0.492	0.496	0.507	0.507	0.510	0.501	0.507	0.521	0.511	0.520	0.507	0.514	0.508	0.519
$V_{th,sat}$ (V) [12]																
Bulk	0.528	0.543	0.533	0.540	0.530											
SOI																
MG	0.446	0.453	0.453	0.454	0.461	0.459	0.461	0.447	0.446	0.454	0.453	0.460	0.454	0.459	0.461	0.468
R_{sd}: Total Parasitic Series Source/Drain Resistance (Ω-μm) [13]																
Bulk	188	179	171	162	156											
SOI																
MG	128	146	130	126	124	117	120	116	112	111	113	123	129	131	126	128
Gate Fringing Capacitance (fF/μm) [14]																
Ratio of fringing capacitance to intrinsic	1.1	1.2	1.3	1.4	1.5	1.6	1.7	1.8	1.9	2.0	2.0	2.0	2.0	2.0	2.0	2.0
Fringing capacitance Bulk/SOI/MG	0.64	0.65	0.66	0.70	0.68	0.69	0.69	0.68	0.68	0.66	0.63	0.59	0.55	0.52	0.48	0.46
C_{gate}: Total Gate Capacitance (fF/μm) [15]																
Bulk/SOI/MG	1.21	1.19	1.17	1.19	1.14	1.12	1.09	1.06	1.03	1.00	0.95	0.89	0.83	0.77	0.73	0.69
CV^2: NMOSFET Dynamic Power Indicator (fJ/μm) [16]																
Bulk/SOI/MG	0.90	0.86	0.81	0.78	0.73	0.68	0.65	0.60	0.57	0.52	0.48	0.42	0.38	0.34	0.31	0.28
τ =CV/I: NMOSFET Intrinsic Delay (ps) [17]																
Bulk	2.120	2.208	2.132	1.992	2.159											
SOI																
MG	1.622	1.661	1.573	1.640	1.587	1.564	1.525	1.491	1.426	1.556	1.474	1.557	1.422	1.514	1.413	1.493
FCV (1-ps) [18]																
Bulk	0.47	0.45	0.47	0.50	0.46											
SOI																
MG	0.62	0.60	0.64	0.61	0.63	0.64	0.66	0.67	0.70	0.64	0.68	0.64	0.70	0.66	0.71	0.67
I_{dsat} (n-channel)/I_{dsat} (p-channel) [19]	1.27	1.26	1.25	1.24	1.22	1.21	1.20	1.19	1.18	1.16	1.15	1.14	1.13	1.12	1.11	1.10

Manufacturable solutions exist, and are being optimized

Manufacturable solutions are known

Interim solutions are known

Manufacturable solutions are NOT known

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APPENDIX B

ACTIVITIES	WEEK														
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Project proposal preparation	X	X	X	X											
Literature review			X	X	X	X	X	X	X	X		X	X	X	X
Design 18nm NMOS MOSFET in Silvaco					X	X	X	X	X	X		X	X	X	X
Simulation of fabrication 18nm NMOS MOSFET					X	X	X	X	X	X		X	X	X	X
FYP I Report Preparation & Seminar FYP I					X	X	X	X	X	X					

ACTIVITIES	WEEK														
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Implementation of Taguchi orthogonal	X	X	X	X	X	X	X	X	X	X					
Comparison obtained values with ITRS 2013 standard			X	X	X	X	X	X	X	X		X	X	X	X
Design 18nm NMOS MOSFET in Silvaco					X	X	X	X	X	X		X	X	X	X
Data analysis									X	X	X				
Thesis writing	X	X	X	X	X	X	X	X	X	X	X	X			
Thesis Submission													X	X	X