WIRELESS POWER TRANSFER BASED ON CAPACITIVE APPROACH FOR LOW POWER APPLICATION

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This report is submitted in partial fulfilment of the requirements for the degree of Bachelor of Electronic Engineering with Honours

UNIVERSITI TEKNIKAL MALAYSIA MELAKA

Faculty of Electronic and Computer Engineering
Universiti Teknikal Malaysia Melaka

JUNE 2020

DECLARATION

I declare that this report entitled "**WIRELESS POWER TRANSFER BASED ON CAPACITIVE APPROACH FOR LOW POWER APPLICATION**" is the result of my own work except for quotes as cited in the references.

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Signature :

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Date: 26 JUNE 2020

APPROVAL

I hereby declare that I have read this thesis and in my opinion this thesis is sufficient in terms of scope and quality for the award of Bachelor of Electronic Engineering with Honours.

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Signature :

Supervisor Name : DR YUSMARNITA BINTI YUSOP

Date : 26 JUNE 2020

DEDICATION

This project is enthusiastically dedicated toward to my dearest family, friends and supervisor which had been help and support

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ABSTRACT

A CPT system is one of the near-field technologies of WPT system where it capable to transmit signal within short range and high efficiency. The CPT system was chosen due to the benefits such as simple topology, fewer components that could assist with better performance and robustness to EMI around metallic materials, and easy to build. A Class D inverter has been analysed towards ZVS condition, input power and output power based from two difference impedance approaches that are capable to perform the conversion from DC to AC efficiently. Next, by developing the simulation of this CPT system using MATLAB software, ranges of load and distance variation are used to analyse the performance of efficiency by observing the ZVS condition and power output based from obtained waveform. This project is expected to deliver a 10Watt output power with the frequency operating of 1MHz that suits with any electronic devices with low power rate consumption and efficiency rate 85% above. Eventually, the CLL impedance seems to be the compatible impedance network for Class D inverter while maintaining a better efficiency rate compared to LCCL impedance. In future, it is much recommended to study and develop the Class D inverter with various of impedance network to analyse the performances.

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ABSTRAK

Sistem CPT adalah salah satu teknologi jarak dekat sistem WPT di mana ia mampu menghantar isyarat dalam jarak pendek dan kecekapan tinggi. Sistem CPT dipilih kerana kelebihan seperti topologi sederhana, sedikit komponen yang dapat membantu dengan prestasi dan ketahanan yang lebih baik kepada EMI di sekitar bahan logam, dan mudah dibina. Penyongsang Kelas D telah dianalisis terhadap keadaan ZVS, daya input dan kuasa output berdasarkan dua pendekatan impedans perbezaan yang mampu melakukan penukaran dari DC ke AC dengan cekap. Selanjutnya, dengan mengembangkan simulasi sistem CPT ini menggunakan perisian MATLAB, rentang beban dan variasi jarak digunakan untuk menganalisis prestasi kecekapan dengan memerhatikan keadaan ZVS dan output daya berdasarkan bentuk gelombang yang diperoleh. Projek ini diharapkan dapat memberikan kuasa output 10Watt dengan frekuensi operasi 1MHz yang sesuai dengan mana-mana peranti elektronik dengan penggunaan kadar kuasa rendah dan kadar kecekapan 85% ke atas. Akhirnya, impedans CLL merupakan impedans yang serasi untuk penyongsang Kelas D sambil mengekalkan kadar kecekapan yang lebih baik berbanding dengan impedans LCCL. Di masa depan, sangat disarankan untuk mengkaji dan mencipta penyongsang Kelas D dengan impedans yang lain untuk menyelidik prestasi yang lebih baik.

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First and foremost, I would like to say Alhamdulillah praise to Allah, with his guidance and helps. I had completed my final year project for the given title “Wireless Power Transfer Based on Capacitive Approach for Low Power Application” successfully.

Besides, I would also like to express my sincere gratitude to my supervisor, Dr Yusmarnita Binti Yusop, who has a genius attitude and substance; she frequently and convincingly showed a spirit of adventure in terms of research and teaching enthusiasm. This thesis would not have been possible without her encouragement and constant support.

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LIST OF SYMBOLS AND ABBREVIATIONS

WPT	:	Wireless Power Transfer
CPT	:	Capacitive Power Transfer
AC	:	Alternating current
DC	:	Direct current
CLL	:	Capacitor Inductor - Inductor
EMI	:	Electromagnetic Interference
ZVS	:	Zero Voltage Switching
IPT	:	Inductive Power Transfer
V_{DC}	:	Volts Direct Current
PWM	:	Pulse Width Modulation
LED	:	Light Emitter Diode
RMS	:	Root Mean Square
ESR	:	Equivalent Series Resistance

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CHAPTER 1

INTRODUCTION

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The first chapter of this thesis discusses the context of the project, project objective, problem statement of the project, scope of the project, an overview of the methodology, and project outline.

1.1 Project Background

Nowadays, Wireless Power Transfer (WPT) has the potential to liberate us from power cord tyranny. This engineering is integrated into tools and systems of all kinds. This system could perform through an air gap, without needs from current-carrying wires. Instead of using physical connectors such as wires, the WPT may produce power from an alternating current (AC) source to any suitable batteries or devices. This

system also can be categorized into two part of technologies which are near-field and far field transmission. [1]

Capacitive Power Transfer (CPT) is one of the near-field transmission and advantageous systems in the WPT system. [2] The versatility of capacitive interfaces and their low cost had encouraged them to be very pleasing in the WPT system. The primary purpose of developing the CPT system is to prevent the disadvantages of WPT, where the issue of electromagnetic interference (EMI) possibly occurs, and the chances of the magnetic field to penetrate between the power source and load through a metal barrier is null. Hence, to increase the magnetic efficiency, obtaining a dependable coupling factor, and disallow EMI, the use of a magnetic shield and special shield are proposed.

A circuit topology where it consists of a Class D inverter along with a CLL matching circuit is proposed to operate the CPT system. This topology is capable of executing the direct current (DC) to AC conversion efficiently with corresponding to the switching losses by using MATLAB software and experimental approach. Next, to ensure the performance of the developed circuit, the input power, output power, switching losses, and dc-dc efficiency needs to be considered.

Eventually, the output power for the system expected to acquire 10W efficiently and able to suit any low power application. With the elimination of using physical wires, the appearance and sustainability of WPT on any low power application could be enhanced.

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1.2 Project Objective

In this study, several important goals were outstandingly set to be achieved after this task is completed.

1. Design a CPT system based on Class D inverter topology that can enhance the system efficiency.
2. To analyze the performance of the developed CPT system based on Zero Voltage Switching (ZVS) condition, input power, output power and efficiency.
3. Optimize the efficiency of CPT system using multistage impedance matching circuit that is capable of improving the ZVS condition that are less sensitive to the load and coupling variation.

1.3 Problem Statement

Currently, the most common application of the WPT system used is Inductive Power Transfer (IPT). Still, then, the limitation of penetrating metal and electromagnetic interference (EMI) make the CPT system more reliable.

It is suitable to use a CPT system for an application that produces low power consumption due to the limitation of exhibits output power and efficiency. Moreover, the effectiveness of the system depends on the gap distance between the coupling plate and load variation. Hence, the solution solved by using the Class D inverter with the CLL impedance matching network.

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1.4 Scope of Project

This project works in several parts. The initial stage begins with the simulation of Class D inverter by using MATLAB software to simulate the circuit and achieve the condition of Zero Voltage Switching (ZVS). Hence, power MOSFET was used as switches, and meanwhile, the performances were analyzed by applying ZVS condition, input power, output power, and efficiency. On the other hand, the Class D inverter

combines with the CLL matching network to produce resonance circuits and efficient power transfer. Regarding the capacitive coupling plate, this project proposed to replace the four plates of capacitive copper or known as Bipolar structure with using a couple of capacitor at the transmitter and receiver part. [3] Some of the values of the parameter in developing the CPT system has been set initially to obtain the desired output.

- Input voltage = 24Volt
- Output power = 10Watt
- Frequency, f = 1MHz
- Distance gap between plates ≤1mm
- Duty cycle = 0.5
- Efficiency, $\eta = \geq 85\%$

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1.5 Thesis Organization

Generally, there are five chapters to be written in this thesis. Each chapter had been organized structurally.

- Chapter 1 consist of the introduction of project, objective, problem statement, scope of work and thesis organization.
- Chapter 2 explains the literature review of CPT system based from the study on previous research.
- Chapter 3 will interprets the work flow and description towards completing this project.
- Chapter 4 is about explaining the progress result of project and discussion.

- Chapter 5 concludes the whole research and proposes the future enhancement of project.

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CHAPTER 2

BACKGROUND STUDY

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This chapter will discuss any literature discourse and review of the CPT system based on any sound sources such as journals, books, and relevant sources. In the process of developing this project, information and concept are essential to be considered as references to obtain the desired output and completed this project.

2.1 Introduction

In this technology era, WPT is the most significant system that people have been using nowadays. Due to the current trends, the awareness of the WPT through the use of the CPT method is essential for the understanding and will be reviewed in this

chapter. Throughout in developing this project, a number of researches and studies have been done for the topic of the WPT system, CPT system, capacitive coupling plate, Class D inverter/converter, and resonance circuit.

2.2 Wireless Power Transfer Technology

Due to the reduction of low power density, high cost, and heavyweight, unique technical challenges are faced with the design and deployment of the battery-powered system. Hence, the WPT system has been introduced where it provides a brand new way for an electrical-driven device to obtain energy, thus increasing overdependence on the battery. [4] WPT system is capable of delivering an overview of the concept as well as an excellent analysis of the development issues to be addressed to achieve optimal efficiency in high power transmission. [5] Besides, it also offers an excellent introduction to high-resonance WPT design theory, explaining fundamental system principles such as frequency splitting, ideal operating distance (capacitive coupling), and device behavior as it becomes over and under-coupling.

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Generally, the WPT system consists of two conventional techniques in delivering power, which are the far-field and the near-field transmissions. [6] By adopting the acoustic, optical, and microwave as the energy carrier, the far-field WPT can be realized. On the other hand, the near-field technique uses the inductive coupling effect of non-radiative electromagnetic fields, including capacitive and inductive mechanisms. According to the project title research, CPT has been chosen over inductive power transfer (IPT) due to the advantages of the capability of penetrating through metal-body, reduce energy loss, and good anti-interference ability of the magnetic field. [7]

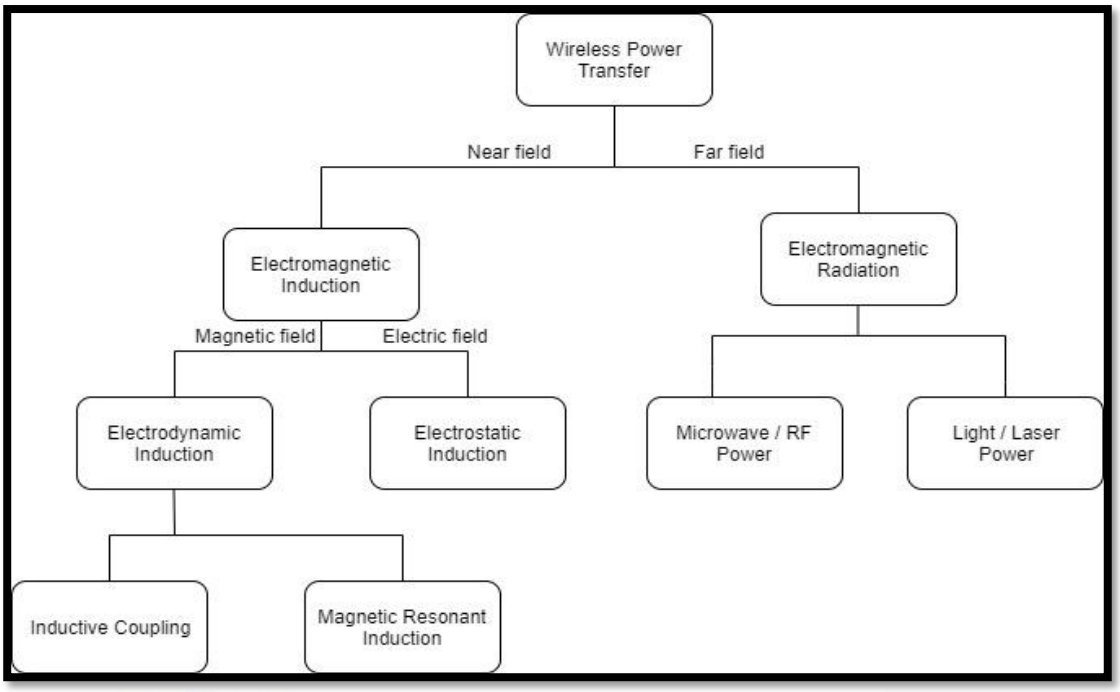

Figure 2.1 Wireless power transfer – Overview

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It usually is possible to compare the form of WPT with IPT and CPT method, where both of the systems are frequently used in a wide variety of applications nowadays. Firstly, the achievable power density for both systems makes them different from others, where the IPT is capable of high power density compared to CPT. In mutual methods, currently, the industry technology prefers contact-base electrical connection with the WPT method rather than the IPT. The concurrent concern in a variety of applications is the development of the IPT. Usually, this feature uses WPT stand for rotational devices that transfer power between stationary and rotating components using slip rings.

There is an inductive system of the immense dominance of inductive systems in the mechanical structure. Still, the capacitive methods have niche applications within the motor or generator community of Microelectromechanical System (MEMS). Thus, it

is effortless for the capacitive method to be designed at the MEMS scale. Moreover, it contains a power density equal to or higher than its magnetic equivalents.

The theoretical development of IPT technology has been very successful. It will provide power in the range of industrial applications such as powering consumer electronics devices, powering connections for implantable medical devices, [8] electric vehicle charging, [9] and wireless charging for robots. [10] Nevertheless, the main weakness of IPT has made the system hard to be implemented. [11] Last but not least, the CPT system completely overcomes the IPT limitation, where it is much better in penetrating a metal shielding environment.

2.3 Capacitive Power Transfer Topology

CPT system is a system that relies on the coupling capacitance that use to transmit power. [12] Due to the advantages of capability on penetrating through any metal shielding environment and achieving high power density, the CPT system has been dominance in the innovation technology nowadays based on electrical field coupling in WPT. [13]

By referring to Figure 2.2, the CPT system topology consists of two main parts where primary side reacts as the transmitter unit while the secondary side represents the receiver unit. The purpose of transmitter unit is to transform the signal from dc signal to high-frequency ac signal because the capacitive coupling requires only ac energy to transfer the power via the electrical fields. [14] Apart from that, an inverter is required to perform the conversion signal task. Meanwhile, in the receiver unit,

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high-frequency ac energy is safely converted back into dc with the used of rectifier to meet the requirements specified by the load parameters.

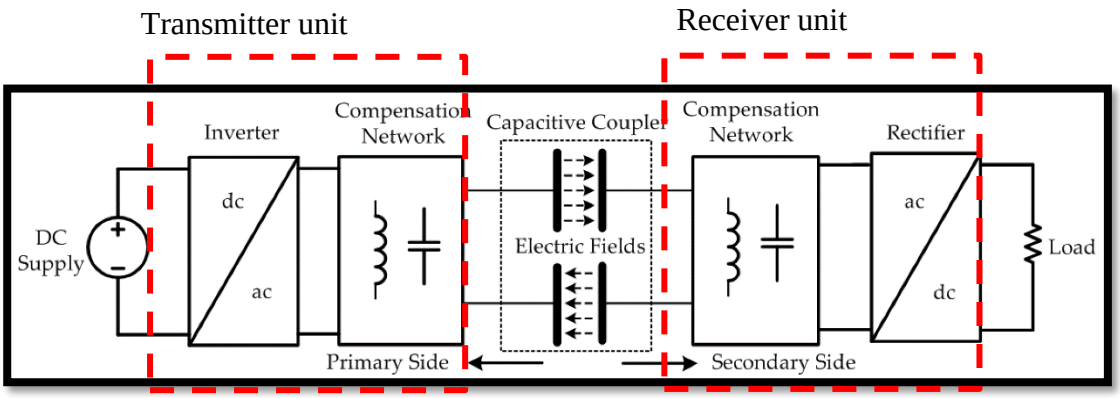

Figure 2.2: Block diagram of proposed CPT system [15]

2.3.1 Class D Inverter Topology

A Class D inverter that contain numbers of power MOSFET use to transmit the dc signal with peak amplitude same as the voltage input signal received with considering the total resistance in power MOSFET and voltage forward of diode. The power MOSFET are responsible to create a switching signal condition and react as the switches. The output signal produced by the Class D is supposed to be in a digital signal and continuous time depending on the instantaneous duty cycle. [16] In Figure 2.3 shows the schematic of Class D inverter with resistor load.

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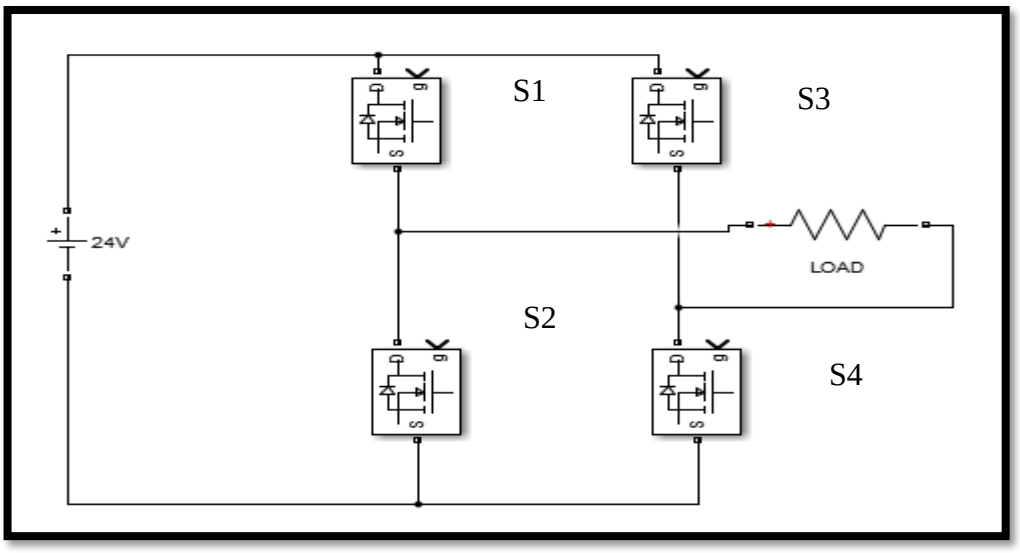

Figure 2.3: Schematic Class D inverter with R load

In this application, an AC output is synthesized from a DC input by closing and opening the switches in an appropriate sequence. [17] The output voltage V_o can be $+V_{DC}$, $-V_{DC}$, or zero, depending on which switches are closed. Note that S_1 and S_2 should not be closed at the same time, nor should S_3 and S_4. Otherwise, a short circuit would exist across the Dc source. Real switches do not turn ON or OFF instantaneously. Therefore, switching transition must be accommodated in the control of the switches by developing the PWM controller. [18] Overlap of switch "ON" times will result in a short circuit, sometimes called a *shoot-through fault*, across the DC voltage source. In practical, the dead time is required to avoid "shoot-through" faults.

The simplest switching scheme for the Class D inverter produces a square wave output voltage. The switches connect the load to $+V_{DC}$ when S_1 and S_4 are closed or to $-V_{DC}$ when S_2 and S_3 are closed. By referring to Figure 2.4, the periodic switching of

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the load voltage between $+V_{DC}$ and $-V_{DC}$ produces a square wave voltage across the load. Although this alternating output is non-sinusoidal, it may be an adequate AC waveform for some application.

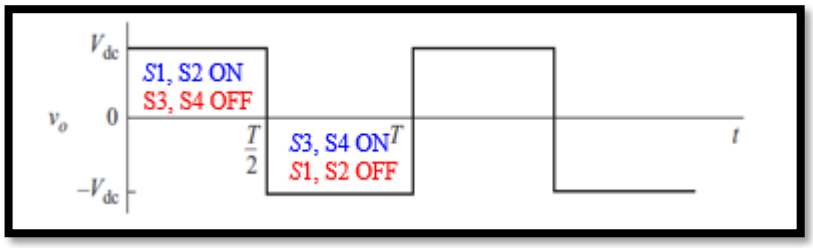

Figure 2.4: Square wave output voltage

2.3.2 CLL Impedance Matching

The DC-to-AC voltage transfer function of the inverter is almost independent of the load variations at a switching frequency higher than the resonant frequency. [19] An important advantage of the inverter is that the load presented by the resonant circuit to the switches is inductive at this frequency. [20] In addition, the circuit has high efficiency over a wide range of load resistance.

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The CLL resonant inverter shown in Figure 2.5 is composed of four bidirectional four-quadrant switches S_1, S_2, S_3 and S_4 and a resonant circuit CL_1L_2. The resonant capacitor C is connected in series with the inductor L_1 and L_2 while the load is connected in parallel with the inductor L_2. The switches consists of MOSFETs and their body diodes, and are driven by rectangular-wave voltage sources $_{vgs1}$ and $_{vgs2}$. Each switch can conduct a positive or a negative current. The transistors are driven by rectangular wave voltage sources $_{vgs1}$ and $_{vgs2.}$ Switches S_1 and S_4, S_2 and S_3 are

alternatively turned on and off at the switching frequency $f = \omega/2\pi$ with a duty cycle 50%.

The parallel R and L_2 can be converted into a series Rs-Ls circuit as shown in Figure 2.6 at a given frequency. The total series equivalent inductance is L*eq* = L_1 + L_s. In Figure 2.6 also, the DC voltage source and the switches S_1 and S_4, S_2 and S_3 are modeled by a square-wave voltage source, where the low level of the square wave is zero and the high level is V_{DC}. The equivalent on-resistance of the MOSFETs is $r_{DS} \approx (r_{DS1} + r_{DS2})/2$. The parasitic resistance *r* of the inverter is composed of the resistance of the switch r_{DS}, the equivalent series resistance (ESR) of the capacitor r_{Cr}, and the ESR_s of the inductors r_{L1} and r_{L2}.

Waveforms in the CLL inverter for $f > f_r = 1 / (2\pi\sqrt{LeqC}$ are the same as parallel-resonant inverter. The operation of the inverter above resonance is preferred because the reverse recovery of the MOSFET body diodes does not affect adversely the circuit operation. The input voltage $_{vds2}$ of the resonant circuit is a square wave. Assuming the loaded quality factor or at the resonant frequency f_r is high, the capacitor current *i* is nearly sinusoidal and flows alternately through switches S_1 and S_4, or S_2 and S_3.

If R $<<X_{L2}$ = ωL_2, most of the capacitor current flows through the load resistance, and therefore I_m is inversely proportional to the load resistance, resulting in high part-load efficiency. When the load resistance R becomes greater than X_{L2}, most of the capacitor current flows through the resonant inductor L_2, making I_m independent of R. Therefore, the efficiency is low at part loads.

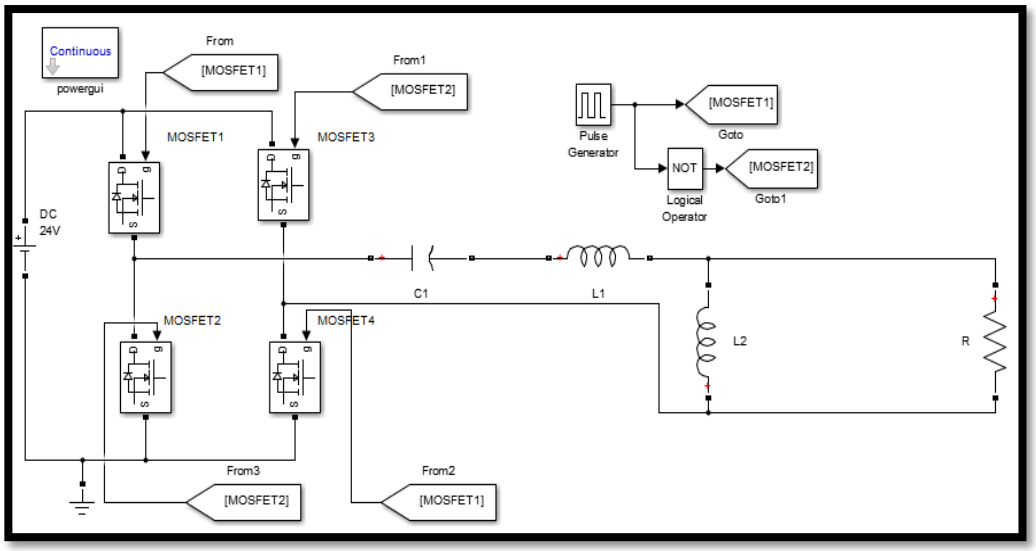

Figure 2.5: CLL Impedance matching schematic

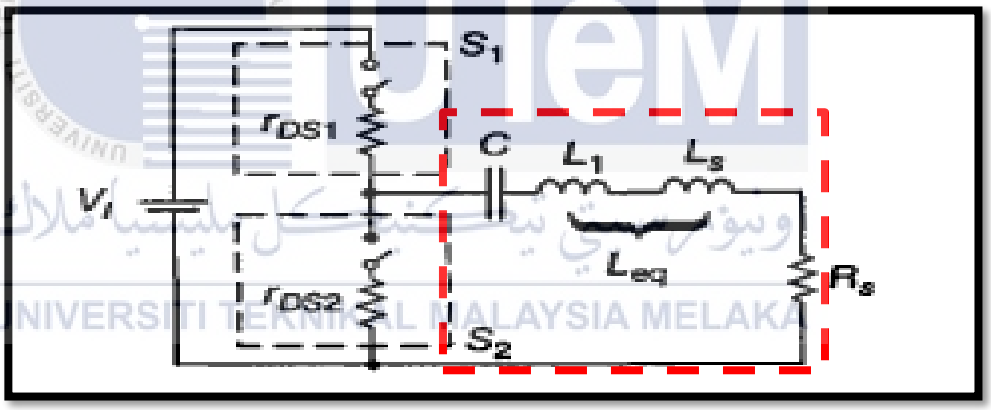

Figure 2.6: Series equivalent inductance

2.3.2.1 Zero Voltage Switching (ZVS)

Zero Voltage Switching (ZVS) is one solution which allows a return to faster switching frequency at higher input voltage and voltage drop. [21] Like virtually all contemporary switching voltage regulators, this technique uses pulse width modulation (PWM)-based operation, but with a different additional phase to the PWM

timing to permit for ZVS operation. ZVS allows for “soft switching” by the voltage regulator, preventing the switching losses typically accrued during conventional operation and timing of PWM.

While many contemporary non-isolated buck voltage regulators suffer high-switching losses due to the simultaneous presence of high-current and the voltage stress on the integrated MOSFET of the regulator during the transitions. With switching frequency and input voltage, these losses increase and limit the operation of maximum frequency, efficiency, and power density. Hard switching presences when the MOSFET switches performing transition on and off during the overlap between voltage and current. [22]

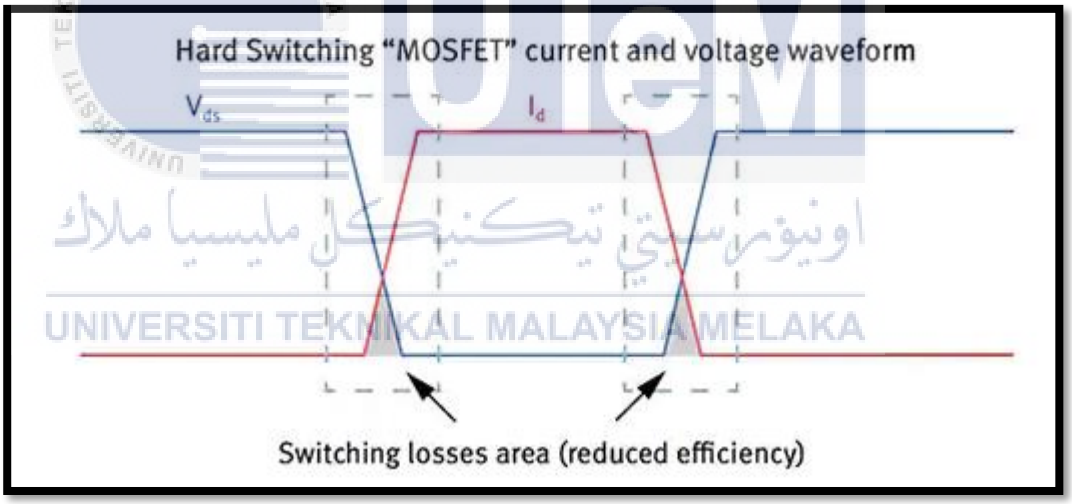

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Figure 2.7: Voltage regulator losses occur during voltage/current overlap when the MOSFET switches [23]

Increased electromagnetic interference (EMI) arising from the voltage regulator circuitry is the drawback of fast switching. In other hands, there is one method to reduce EMI effects by using a switching regulator that uses an improved

hard-switching technique called quasi-resonant switching or known as “valley” switching, while also making advantage of fast switching to increase performance. The MOSFET is turned on during quasi-resonant switching when the voltage across drain and source is at a minimum (in a valley) to reduce the switching losses. This enables the device to operate with a more modest voltage or current change rate, thereby reducing EMI. Another side benefit of quasi-resonant switching is that a degree of frequency latency is added, increasing the RF emission spectrum and further reducing the EMI, as switching is activated when a valley is detected, rather than at a constant frequency.

Quasi-resonant switching is a useful approach for assessing the productivity of voltage converters, but the execution of full soft switching can further improve the situation. [23] The voltage decreases to zero before turning on or off the MOSFET during soft switching, removing any variation between voltage and current and reducing losses.

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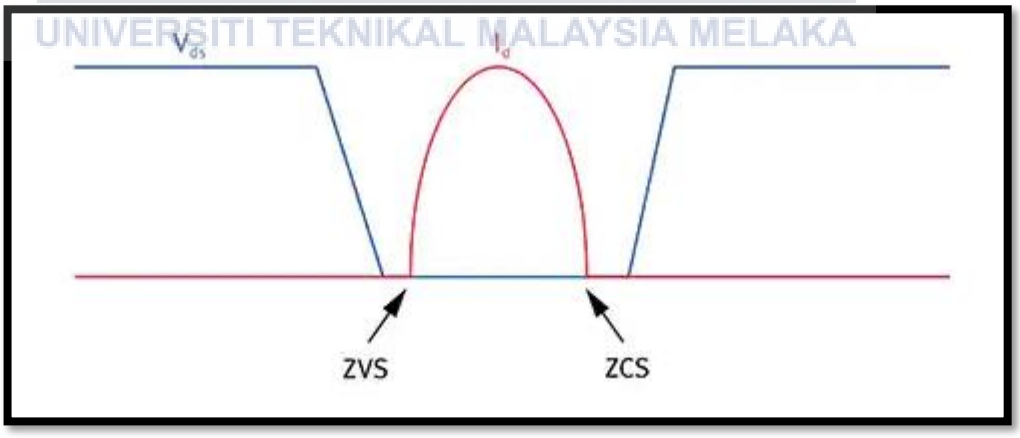

Figure 2.8: Soft-switching MOSFET current and voltage waveform [23]

A conventional PWM power conversion during the MOSFET's on time but with "resonant" switching transitions is the best term to be explained for soft switching. The method was considered as PWM power using a constant off-time control that changes the frequency of conversion, or on-time to maintain output voltage regulation. For a given unit of time, this approach is synonym to constant frequency conversion using an adjustable duty cycle.

The control of the output voltage is accomplished by changing the effective duty cycle (and therefore on-time), by varying the frequency of conversion. During the off-time ZVS switch, the resonant tank circuit of the regulator resonates through the voltage through the switch from zero to its peak and back to zero when the switch can be reactivated, facilitating lossless ZVS.

The advantages of ZVS are that it capable to reduces the harmonic spectrum of any EMI (centering it on the switching frequency) and permit higher frequency operation resulting in reduces, easier to filter noise and the use of minor filter components.

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2.3.3 Capacitance of Coupling Plate

By recognizing the relationship between distance and efficiency of the capacitive coupling sheet, the performance of the CPT device can be optimized. Next, by referring to Equation 2.1, the capacitance can be inferred, as defined by the plate area, is directly proportional to the dielectric constant and physical size of the surface. Capacitance is inversely proportional to the distance between plates. [24]

$$C = \frac{A\mathcal{E}_{\circ}\mathcal{E}r}{d} \qquad (2.1)$$

Generally speaking, several capacitive plate systems are consisting of a two-plate coupler structure, four-plate parallel structure, stacked structure, six-plate structure, and repetitive structure. Two-plated coupler arrangement, as shown in Figure 2.9, also known as the bipolar structure of the CPT system, has a more straightforward benefit than any other. The system uses only two plates for power transfer, where the first is for the transfer power, and other use to receive the energy. The relation between these two plates in the conductive path would influence the resulting of a quasi-wireless CPT device as a metal to the metal power receiver. Next, the mutual capacitance between two plates provides the way for the current to flow forward to the load and then needs a conductive path to allow the current to rush back to the primary side.

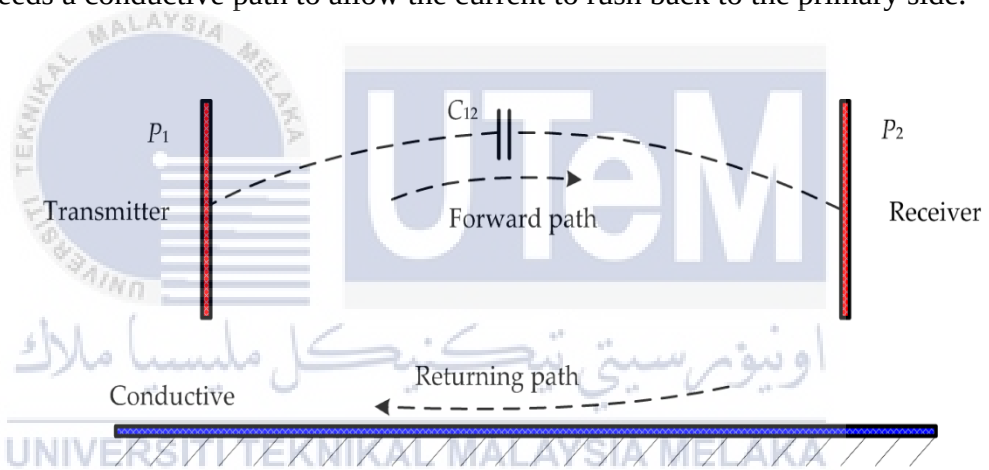

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Figure 2.9: Two-plate capacitive coupler structure

In the other hands, a four plate parallel structure is also known as a bipolar structure. Conversely, four plate structure is connecting each other in the parallel form as shown in Figure 2.10.

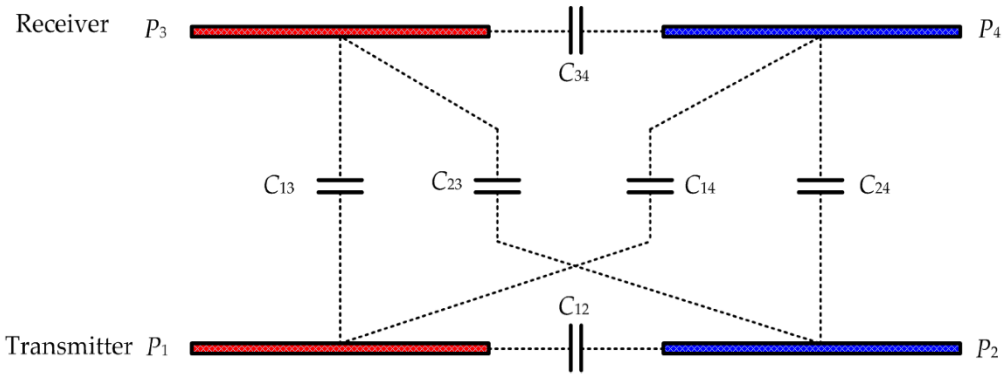

Figure 2.10: Four-plate capacitive coupler structure [25]

Each plate in Figure 2.10 is the coupling capacitance. This will result in six capacitances, where C_{13} and C_{24} are known as the vital coupling capacitances, then C_{14} and C_{23} are classified as cross-coupling capacitances. On the other hand, the C_{12} and C_{34} are defined as the self-coupling capacitance. The capacitive coupler works as a two-port network where the primary port is the input and secondary port react as the output. [26] It should be emphasized that this two-port network can be used as the equivalent of various coupler structures.

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The difference between the configurations, on the other hand, would affect the power transfer efficiency because the CPT system is a small volume and profile, particularly on the receiving side of power, which means it can be used for small scale applications. The flexibility in design and low cost makes it ideal when compared to the other WPT type for power delivery in the reconfigurable and moving system.

2.3.4 Rectifier circuit

In Figure 2.2 has already explained the purpose of rectifier circuit that contribute to this system. In addition, regarding the circumstances, the ac-to-dc

converter safely converts the high frequency ac power to suitable shape with the load parameter requirements and predominantly uses a diode rectifier with capacitive filter as the ac-to-dc converter.

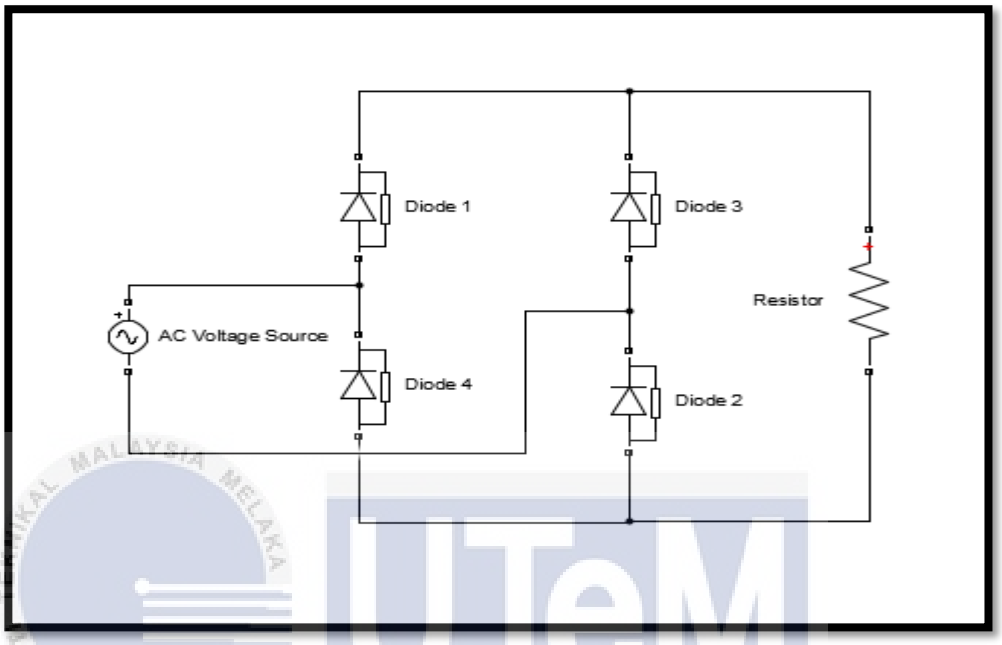

Figure 2.11: Single phase Full-wave Rectifiers – R load

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Diodes D_1 and D_2 conduct together and D_3 and D_4 conduct together. Kirchoff's voltage law around the loop containing the source, D_1 and D_3 cannot conduct simultaneously. The load current can be positive or zero but can never be negative. Besides, the voltage across the load is +Vs when D_1 and D_2 are ON. The voltage across the load is –Vs when D_3 and D_4 are ON. The maximum voltage across a reverse-biased diode is the peak value of the source. This can be shown by Kirchoff's voltage law around the loop containing the source D_1 and D_3. With D_1 ON, the voltage across D_3 is –Vs.

Next, the current entering the bridge from the source is $I_{D1} - I_{D4}$, which is symmetric about zero. Therefore, the average source current is zero. Moreover, the rms source current is the same as the rms load current. The source current is the same as the load current for one-half of the source period and is the negative of the load current for the other half. The squares of the load and source currents are the same, so the rms current are equal.

The fundamental frequency of the output voltage is 2ω, where ω is the frequency of the ac input since two periods of the output occur for every period of the input. The Fourier series of the output consists of a DC term and the even harmonics of the source frequency.

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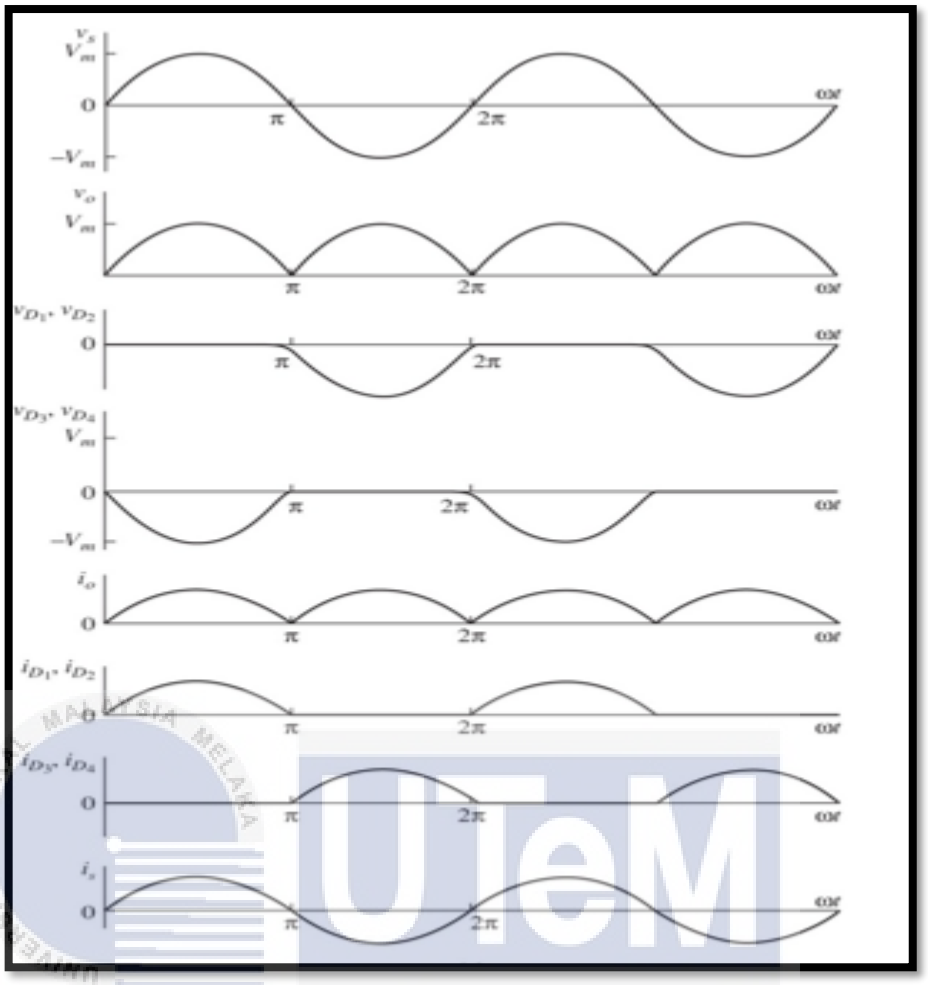

Figure 2.12: Voltage and currents waveform

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The voltage across a resistive load for the bridge rectifier is expressed as:

$$Vo(\omega t) = \begin{cases} Vm \sin \omega t & \text{for } 0 \le \omega t \le \pi \\ -Vm \sin \omega t & \text{for } \pi \le \omega t \le 2\pi \end{cases} \quad (2.2)$$

The DC component of the output voltage is the average value and load current is simply the resistor voltage divided by resistance:

$$\text{Vo} = \frac{1}{\pi}\int Vm \sin \omega t \; d(\omega t) = \frac{2Vm}{\pi} \qquad (2.3)$$

$$\text{Io} = \frac{Vo}{R} = \frac{2Vm}{\pi R}$$

The rms output current:

$$\text{Irms} = \frac{Im}{\sqrt{2}} \qquad (2.4)$$

Then, placing a large capacitor in parallel with a resistive load can produce an output voltage that is essentially DC. In the full-wave circuit, the time that the capacitor discharges is smaller than that for the half-wave circuit because of the rectified sine wave in the second half of each period. Figure 2.13 and Figure 2.14 shows the diagram of full-wave rectifier with capacitance filter and the output voltage.

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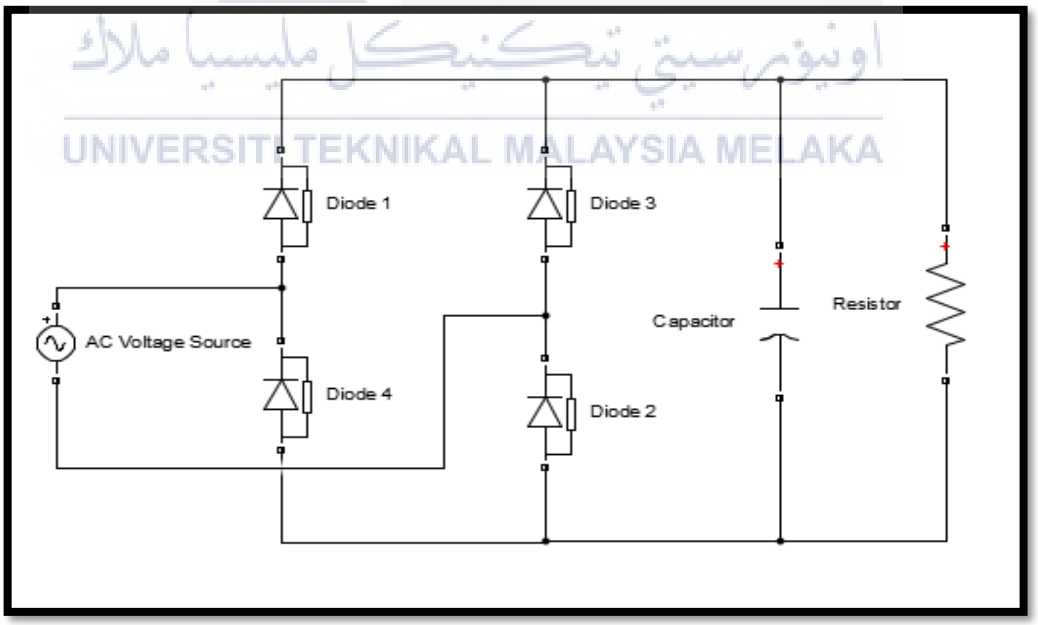

Figure 2.13: Full-wave rectifier with capacitance filter

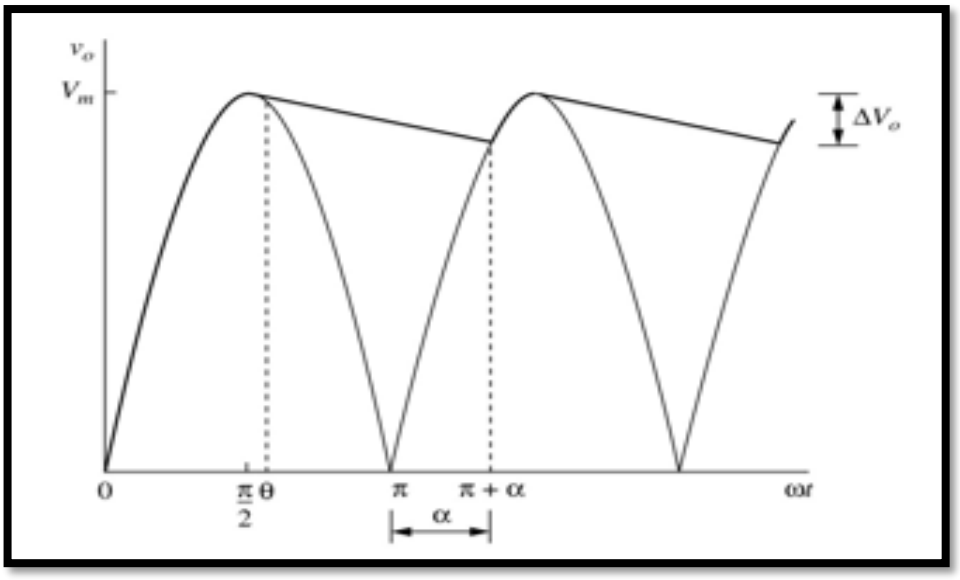

Figure 2.14: Output voltage

The output voltage can be defined from the equation as stated below by assuming ideal diodes.

$$V0\ (\omega t) = \begin{cases} |Vm \sin \omega t| \\ (Vm \sin\ \theta) e^{-\frac{\omega t - \theta}{\omega RC}} \end{cases} \begin{matrix} \text{one diode pair on} \\ \text{diodes off} \end{matrix} \qquad (2.5)$$

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Where θ is the angle where the diodes become reverse biased as stated in equation 2.6, which is the same as that for the half-wave rectifier.

$$\theta = \tan^{-1}(-\omega RC) = -\tan^{-1}(\omega RC) + \pi \qquad (2.6)$$

The peak-to-peak voltage variation, or ripple, is the difference between maximum and minimum voltages as stated in equation 2.7.

$$\Delta Vo = Vm - |Vm \sin(\pi+\alpha)| = Vm(1-\sin\alpha) \quad (2.7)$$

The approximation of peak-to-peak ripple can be defined in the equation 2.8.

$$\Delta Vo \approx \frac{Vm\pi}{\omega RC} = \frac{Vm}{2fRC} \quad (2.8)$$

2.4 Summary

This section discusses the concept of Class D inverter, impedance matching network and rectifier. This complete topology seems to be suitable for any electronic devices that consume with low power application. Therefore, the Class D inverter is used for the non-dissipative switching through the ZVS method to achieve higher efficiency and reduce stress in the semiconductor power rating. [27]

Besides, the CLL resonant inverter topology that used in this system is capable to achieve zero-voltage switching from zero load to a full load and zero current switching for output rectifiers and makes the implementation of a secondary rectifier easy. The power distribution depends on both load impedance and relative positions of receivers to the transmitter. [28] It is important to analyze the performance of Ids and Vds at MOSFET configuration (no overlapping occurred) in order to ensure the power losses at power input are avoided by applying a high operating frequency. [29] Next, an optimized design approach is suggested to achieve high performance over a wide load spectrum, understanding that dead time is a critical factor affecting the entire system design and using thorough investigation.

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CHAPTER 3

METHODOLOGY

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In chapter one, there are roughly explanation had been discuss through the concept and fundamental of this project. Then, in this chapter will elaborate more about the methods that implemented to accomplish this project. The overall methods explain based on the flowchart and introduction to the project construction.

3.1 Introduction

This approach offers detail and accurate data on the characteristic of the devices used in this CPT system. All the information used in this project based on the summarized review in chapter two.

Next, the initial process in developing this project is by considering the value of components used in the CPT system. A strong fundamental of electronic theories is required in order to well-performed this part. After that, it is possible to simulate the

circuit to obtain mutual results with the mathematical approach before proceed to the experimental parts. All the results then will be analyzed based on input power, output power and efficiency. At last, the ethical issues addressed in the process are also explored to ensure the completion of the project.

3.2 Flowchart Methodology

This section describes the methodology used during the development of this project. The process throughout the project will be discussed as below and referring to Figure 3.1.

1. Background study
   - Study the concept and fundamental of WPT and CPT system based from published journal and relevant sources.
   - Identify the limitation of CPT
2. Calculation and design of Class D inverter circuit
   - Develop calculation to obtain the value of components.
   - Compare the result with the theoretical of ZVS.
3. Components selection and simulation
   - Develop the Class D inverter simulation by using MATLAB software.
   - Combine the Class D inverter circuit with impedance matching network.
   - Identify the output, efficiency and ZVS with theoretical.
   - Combine the Class D inverter with CLL impedance with rectifier circuit.
4. Develop microcontroller to control the PWM for the inverter circuit
   - Microcontroller use to ensure the smoothness of switching among the switching devices without any overlapping.
   - To provide the duty cycle as stated in project scope

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5. Design Class D inverter with rectifier circuit.
    - Test the simulation for rectifier with the Class D inverter CLL topology.
    - Check the $P_{out,}$ $P_{in,}$ η and ZVS condition with theoretical.
6. Performance of the evaluation with theoretical part
    - Develop Class D inverter with LCCL impedance.
    - Compare the result between CLL and LCCL impedance matching network to analyze the ZVS condition, input power and output power towards load and distance variation.

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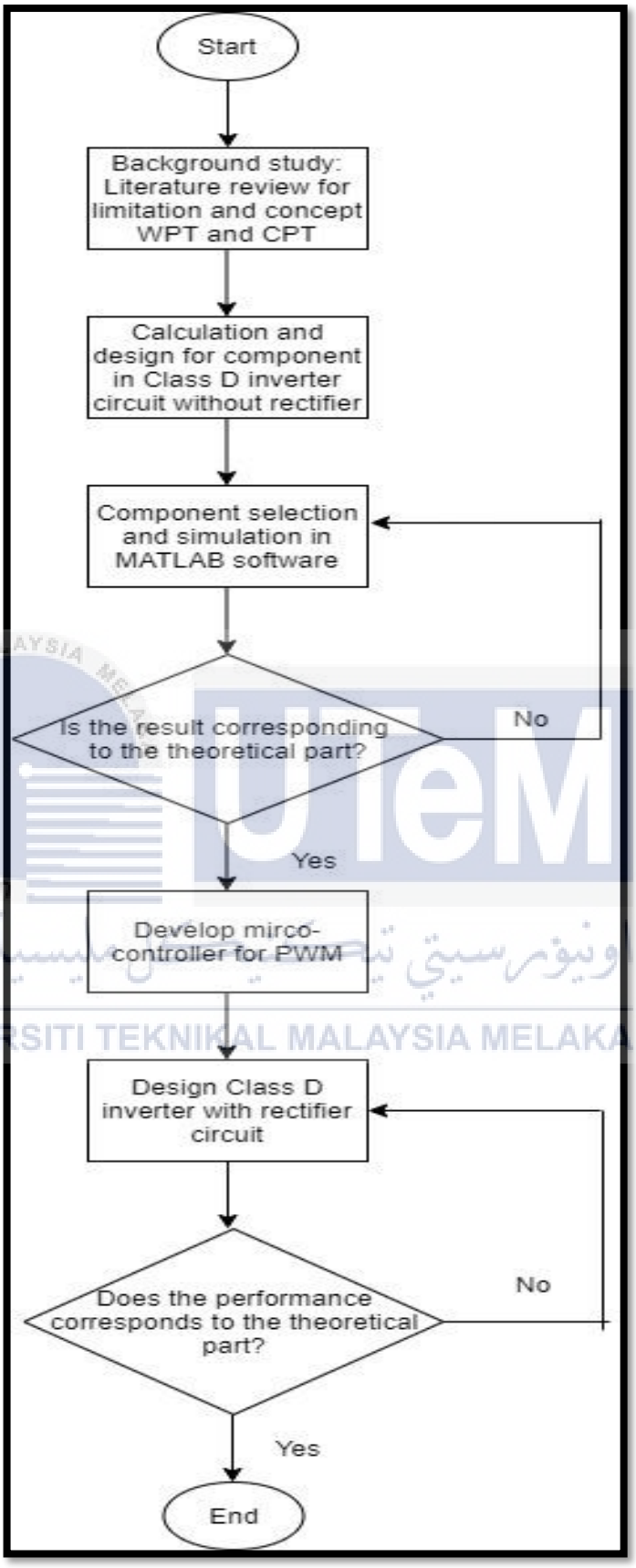

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Figure 3.1: Flowchart for methodology

3.3 CPT System Circuit Configuration

In this project, three main parts of the circuit operate the purpose of developing the CPT system. Those three circuits are Class D inverter, impedance matching network configuration and rectifier configuration. Besides, those configurations are meant to fulfil the objectives, as stated in chapter one.

3.3.1 Coding for controlling the PWM

PWM operates by pulsing DC and changing the amount of time each pulse stays 'on' to monitor the amount of current flowing through a system. PWM is physical, meaning it has two states; on and off (which corresponds to 1 and 0 in the binary sense, being precise to describe in microcontrollers.) In this project, Arduino UNO software has been chosen to be the medium in controlling the PWM. The main reason PWM circuits are so efficient is that they do not attempt to use resistance to partially restrict current flow. [30] They turn the current on and off. Then they only vary the amount of time it's going.

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Figure 3.2: Arduino UNO software

The squares in the PWM diagram below are the pulses representing ‘on’ time, and the depressed areas reflect the ‘off’ time of the control. The squares and the distressed areas are the same ‘width’, which means that the duty cycle is 50%. Typically, PWM signals are square waves, as in the picture below.

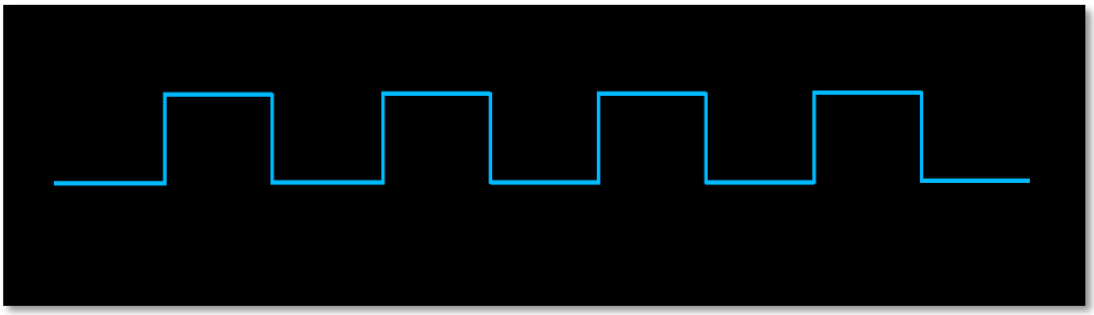

Figure 3.3: A PWM signal (square wave) with a 50% duty cycle

If the duty cycle were 0%, as seen below, the entire signal would be flat. A 0% PWM duty cycle means that the power is eliminated. An LED would not be operational in such a state and this always would be off.

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Figure 3.4: PWM signal (square wave) with a 0% duty cycle

PWM circuit usually require a very low, and a large, power source to break things down further. With the help of power transistors, the tiny power source controls the big one. The tiny one produces the signal, and the aforementioned transistors control the ‘heat’ which is the large current and voltage which heat on the LED. That tiny power source could be a GPIO microcontroller pin like an Arduino I/O pin, the output pin for a 555 timer, among others.

Establishing the duty cycle signal to 30% will also contribute in a duty cycle of 30% for the power, as the large current is only a modulated replica of the tiny current (which is the signal). This principle enables extremely developed microcontrollers (often called MCUs) and other computers to control, at a reasonable cost, very large currents. The signal is produced by the microcontroller/MCU, the signal then controls a power transistor.

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3.3.2 Class D inverter configuration

The flowchart of Class D inverter in Figure 3.5 is used to represent the analysis of achieving the following expectations:

i. The zero-voltage switching (ZVS) condition was to determine the on and off state of MOSFET sequentially.
ii. The output waveform of Class D inverter is obligatory in a square wave waveform.
iii. The peak amplitude should be the same as the input value of V_{dc}.
iv. Considering the ideal switches condition for this configuration.

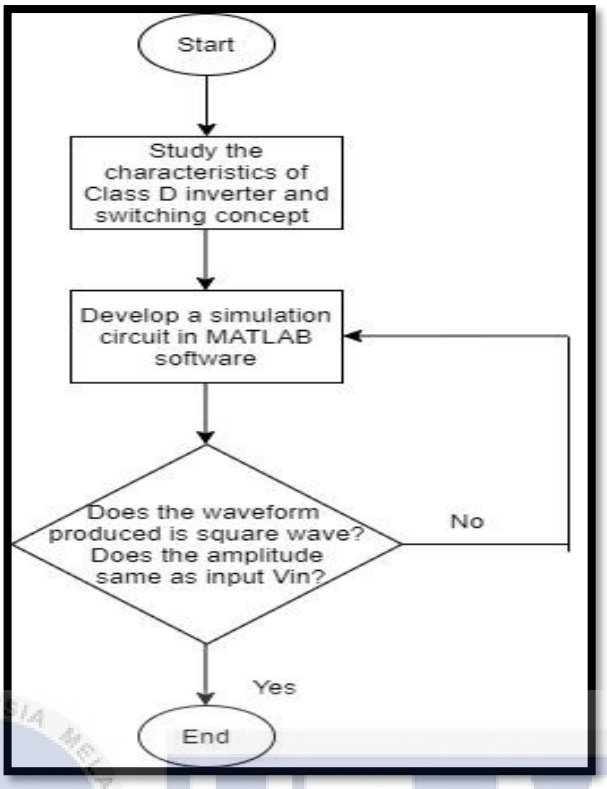

Figure 3.5: Flowchart for Class D inverter

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3.3.3 Impedance Matching Configuration

In the transmitter part where the dc signal needs to be converted to ac signal, the impedance matching of CLL topology is used as the resonance configuration. First, throughout the Class D circuit, the output is still in a digital form. Hence, the use of the impedance matching configuration is to develop the digital way to resonance form.

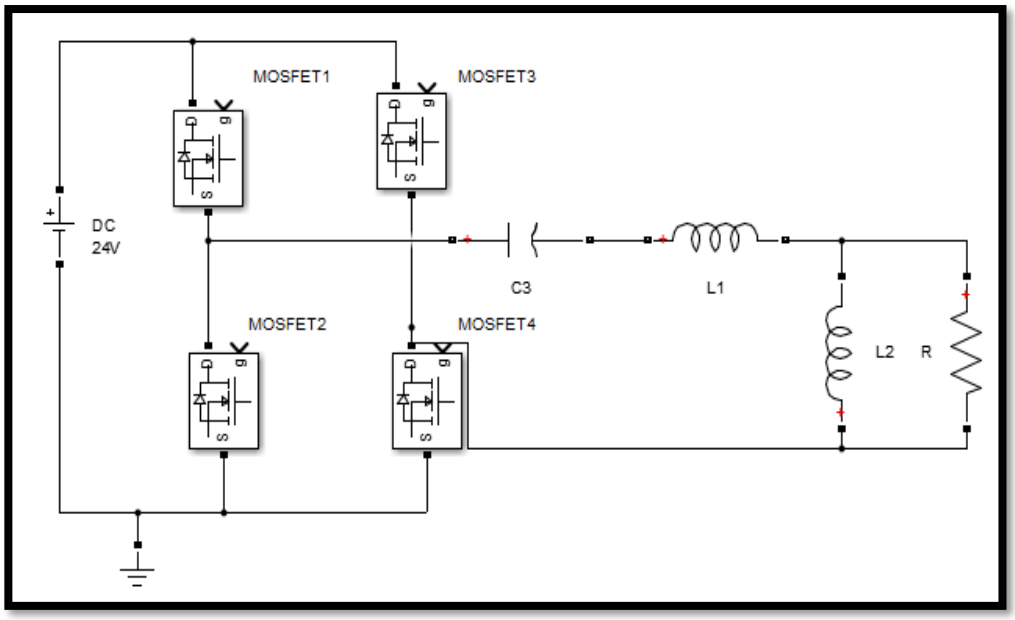

Figure 3.6: Class D inverter with CLL impedance matching schematic

In this part, it is required to perform the mathematical approach first to obtain the value for components, current and voltage, power and efficiency. All parameters are calculated based on the theory. [19]

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i. Maximum DC input power

$$P_{IMAX} = \frac{Primax}{\eta} \quad (3.1)$$

ii. Maximum value DC input current

$$I_{IMAX} = \frac{Pimax}{Vin} \quad (3.2)$$

iii. Value of components

$$C = \frac{Ql}{\omega_{\circ} Rimin} \quad (3.3)$$

$$L = \frac{Rimin}{\omega_{\circ} Ql} \quad (3.4)$$

$$L_1 = L_2 = \frac{L}{1+\frac{1}{A}} \quad (3.5)$$

In this part also, an analysis has been developed in order to fulfil objective 2 and objective 3. The comparison of impedance matching network has been performed by comparing two difference topology which are CLL impedance and LCCL impedance with the same Class D inverter. Those two topology has been analyzed towards the efficiency performance against the load variation and distance variation.

For (objective 2), the analysis towards the ZVS condition where the waveform of Vds and Ids for both topology had been observed in order to notice the overlapping existence between Vds and Ids. Thus, this condition will affected the power input and power output performance where the overlapping will causes the power losses.

Then, for (objective 3), a range of load variation and distance variation has been setup to analyze the performance of efficiency towards both parameter. Also, the analysis can be observed through the Vds and Ids waveform where it represent the input power of the CPT system and also the output power where the performance has been analyzed through the load resistor.

3.3.4 Rectifier Configuration

In the CPT method, the receiver circuit needed to monitor the phase of transferring the signal from ac to dc. Figure 3.7 shows the receiver circuit flowchart, which consists of the rectifier. Hence, the Class D implemented in this project will quickly attain voltage from ac to dc.

So that an ideal rectifier is used in this project, power can only be used in a particular voltage step. Due to this issue, the ideal diode has been used in this project

since the component selection in MATLAB software only provided ideal diode components.

Alternatively, after the result has been obtained by tuning the circuit, tabulate the table of comparative value between theoretical and simulation. Last but not least, to proceed with the next step, the outcome as a theoretical one must have perfect ZVS.

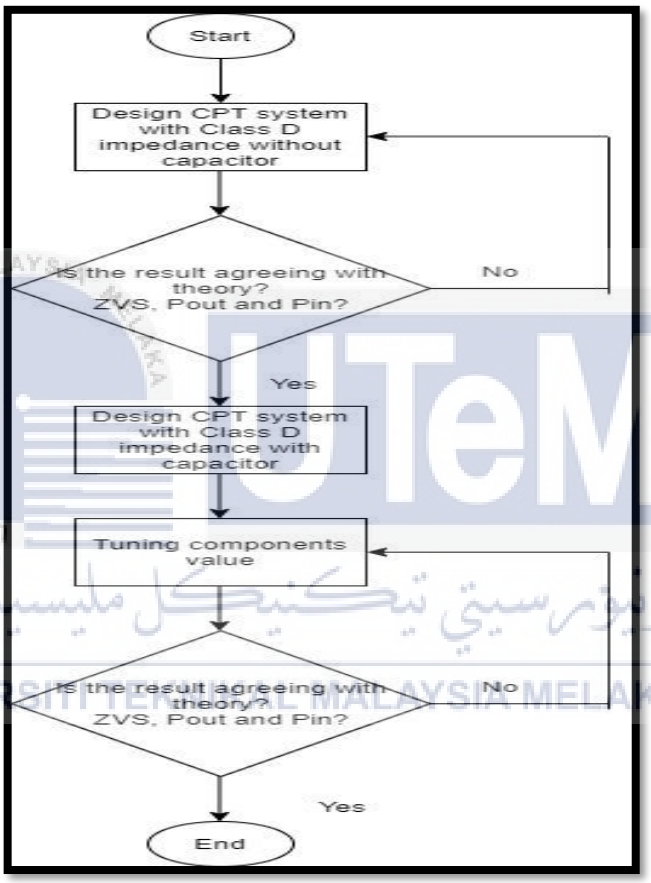

Figure 3.7: Flowchart of rectifier

By completing the full CPT system by using Class D inverter with CLL impedance and LCCL impedance, the comparison and analysis can be made in order to justify the capability of topology to enhance the system efficiency. (Objective 1)

3.4 Implementation

This section introduces the low power application to achieve high value for performance. The constant parameter in this project are the duty cycle which is 50%, V_{DC} = 24V and efficiency ≥ 85%.

The IRFZ44 MOSFET was chosen to be used in this project based from the criteria that fulfil the requirement of operating in fast switching mode and higher input value for V_{DS}. Besides, the advantage of this MOSFET is capable of producing without using a driver circuit. Next, the software used to develop the PWM is Arduino UNO. The pulse that generates by the PWM is essential to clarify the duty cycle was achieved.

Next, as stated in the previous chapter, the value for coupling capacitance must be precise to achieve the desired efficiency.

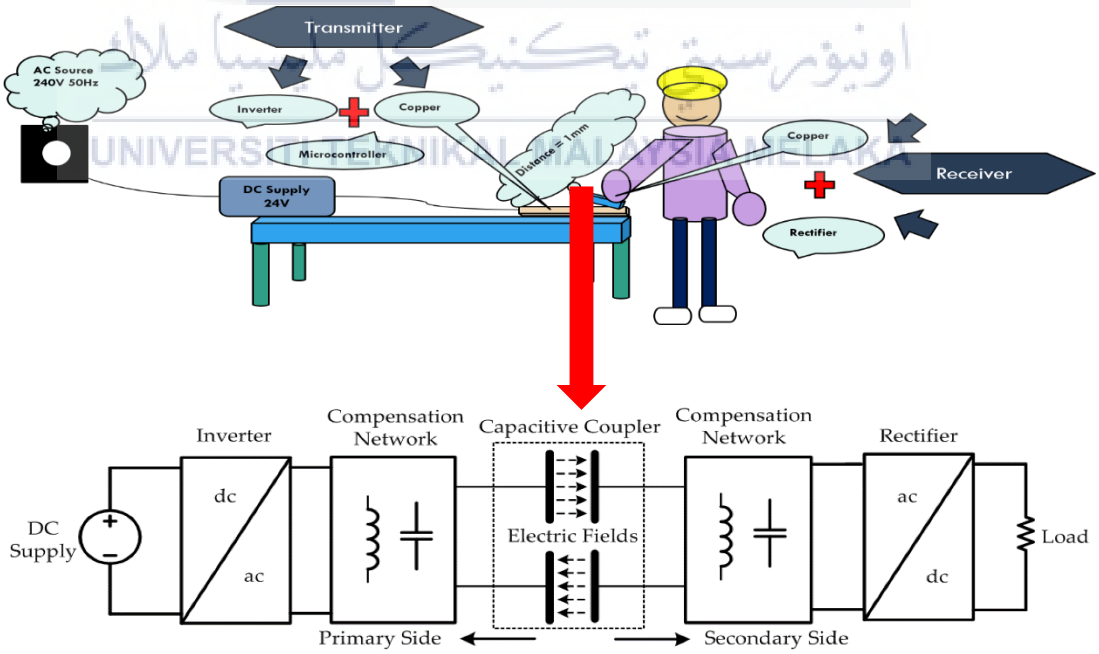

Figure 3.8: Picture of CPT system for purposes of low power application

CHAPTER 4

RESULTS AND DISCUSSION

This segment addressed and explained the research result at the initial stage of study based on the research questions highlighted. The research outcome describes the study results in terms of statistics and in written language. Graphical illustrations, table and diagram define the most crucial aspects of the result.

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4.1 Introduction

Based on researches and experimental that has been done during the PSM 1 and PSM 2, the results are about to be explained in this chapter. Referred to the objective that has been mentioned in the earlier section, this system is estimated to transfer power wirelessly with an amount of 10Watt and suits for any low power application devices.

This CPT system started with developing the simulation of configuration by using MATLAB software where all the results and waveform are included in this chapter. Besides, the comparison between theoretical and simulation are also has been tabulated precisely.

Table 4.1: Calculation for Class D inverter parameter

	Value
a) Maximum DC input power $P_{IMAX} = \frac{PRimax}{\eta}$	11.76W
b) Maximum value DC input current $I_{IMAX} = \frac{PImax}{Vin}$	0.49A
c) Quality Factor, Q_L $Q_L = \frac{1}{\sqrt{2}}$	0.707
d) Capacitance, C $C = \frac{QL}{\omega o\ RImin}$	750pF
e) Inductance, L $L = \frac{RImin}{\omega o\ QL}$	33.77uH
f) Inductance L_1 and L_2 $L_1 = \frac{L}{1+\frac{1}{A}}$ $L_2 = \frac{L}{1+A}$	17uH
g) Impedance , Z_o $Z_o = \frac{RImin}{QL}$	212.16Ω
h) Amplitude of the fundamental component of the voltage at the input resonant circuit. $V_M = \frac{4}{\pi}(vi)$	30.56V
i) RMS value of V_i $V_{rms} = \frac{Vm}{\sqrt{2}}$	21.61V
j) Voltage transfer function from V_i $M_{VS} \equiv \frac{Vrms}{Vi}$	0.9
k) Magnitude of the DC-to-AC voltage transfer function $M_{V1} \equiv \frac{VRi}{Vi} = \frac{2\sqrt{2}}{\pi\sqrt{(1+A)^2\left(1-\left(\frac{\omega o}{\omega}\right)^2\right)^2+\left(\frac{1}{QL}\left(\frac{\omega}{\omega o}\frac{A}{A+1}-\frac{\omega o}{\omega}\right)\right)^2}}$	1.27

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l) $\lvert M_{VR}\rvert = \frac{1}{\sqrt{(1+A)^2\left[1-\left(\frac{\omega o}{\omega}\right)^2\right]^2+\frac{1}{QL^2}\left(\frac{\omega}{\omega o}\right)\left(\frac{A}{A+1}\right)-\left(\frac{\omega o}{\omega}\right)^2}}$	1.414
m) Current through capacitor, I_m $I_M = \frac{4\,Vi}{\pi\, Zo\, QL}\sqrt{\frac{1+\left[QL\left(\frac{\omega o}{\omega}\right)(1+A)\right]^2}{(1+A)^2\left[1-\left(\frac{\omega o}{\omega}\right)^2\right]^2+\frac{1}{QL^2}\left(\frac{\omega}{\omega o}\frac{A}{A+1}-\frac{\omega o}{\omega}\right)^2}}$	498.85mA
n) Amplitude of output current of Class D inverter $I_{OM} = \frac{4\,Vi}{\pi\, Zo\, QL\sqrt{(1+A)^2\left[1-\left(\frac{\omega o}{\omega}\right)^2\right]^2+\left[\frac{1}{QL}\left(\frac{\omega}{\omega o}\frac{A}{A+1}-\frac{\omega}{\omega o}\right)\right]^2}}$	288.04mA
o) Voltage across capacitor, V_{CM} $V_{CM} = \left(\frac{\omega o}{\omega}\right)\left(\frac{4\,Vi\,\lvert Mvr\rvert}{\pi QL}\right)\sqrt{1+\left[QL\left(\frac{\omega o}{\omega}\right)(1+A)\right]^2}$	105.85V
p) Voltage across inductor L_1, V_{L1} $V_{L1} = \left(\frac{\omega}{\omega o}\right)\left(\frac{A}{1+A}\right)\left(\frac{4\,Vi\,\lvert Mvr\rvert}{\pi\, QL}\right)\sqrt{1+\left[QL\left(\frac{\omega o}{\omega}\right)(1+A)\right]^2}$	52.87V
q) Voltage across inductor L2, V_{L2} = Vo of the inverter $V_{L2} = (\sqrt{2})\,(M_{V1})\,(Vi)$	43.11V
r) Power output, P_{Ri} $P_{Ri} = \frac{8\,Vi^2}{\pi^2 Zo\, QL\left\{(1+A)^2\left[1-\left(\frac{\omega o}{\omega}\right)^2\right]^2+\frac{1}{QL^2}\left(\frac{\omega}{\omega o}\frac{A}{A+1}-\frac{\omega o}{\omega}\right)^2\right\}}$	10.73W
s) Total parasitic resistance of the inverter $r = 2\,r_{ds}+r_{cr}+r_{L1}+\frac{rL2}{1+\left(\frac{\omega L2}{Ri}\right)^2}$	Assume ideal
t) The conduction loss $Pr = \frac{rIm^2}{2}$	Assume ideal
u) Efficiency, η $\eta = \frac{Pri}{Pi}$	91.23%

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Based from the above equation in the table [19], it can be assume that the MOSFET used are in ideal condition since this project only require a simulation topology. Nevertheless, if the project is going to be implement for hardware part, the internal resistance need to be considered since each MOSFET has own characteristics.

4.2 Simulation Result

The results based from the simulation performs are highlighted in this chapter. The simulation part consists of three main parts which are Class D inverter, impedance matching network and rectifier.

4.2.1 PWM Controls Signal Using Arduino

In this project, as mentioned earlier in Chapter 1, a 50% duty cycle is used to control the signal from power to be in ‘on’ and ‘off’ state respectively. A 50% of duty cycle seems to be a perfect value for the signal to switching smoothly in an equally mode. The signal was tested by using Proteus software where the software is able to provide an oscilloscope with Arduino libraries included.

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It is necessary to concern the rise time and fall time of the significant MOSFET used to avoid overlap occurrence between rising and falling signal. All the fundamental features can be access through the datasheet provided by the manufacturer.

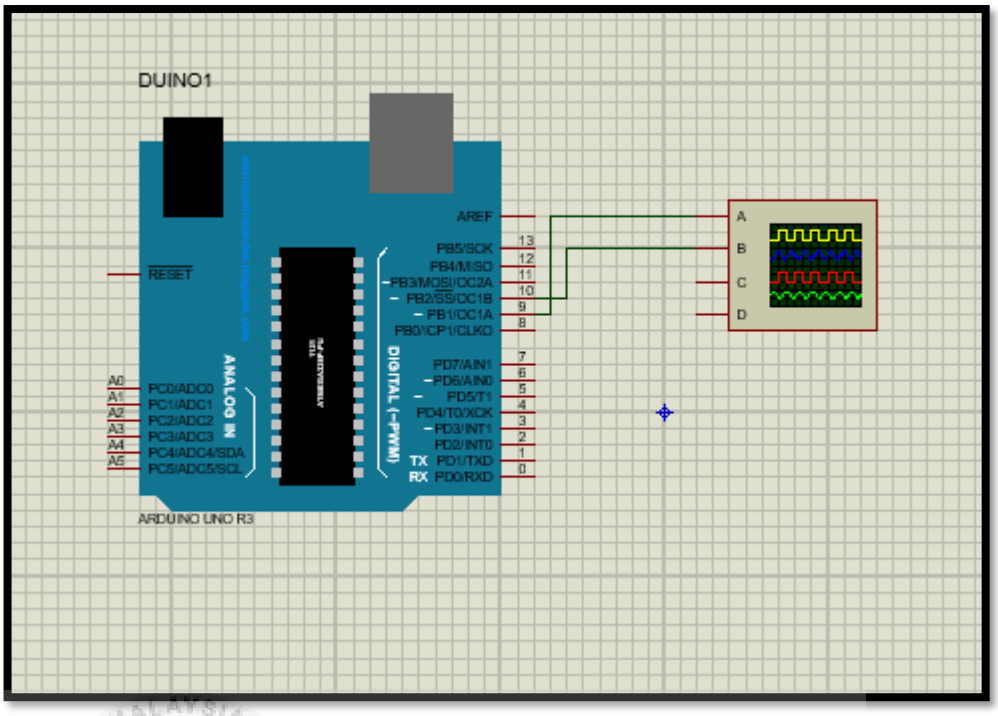

Figure 4.1: Simulation PWM connection (Proteus Software)

Referred to above diagram, Arduino UNO R3 was chose as the microcontroller based on the features and capability. Meanwhile, pin 9 and pin 10 had been chosen as the output pin from the Arduino. The output had been measured by the oscilloscope at Channel A and Channel B.

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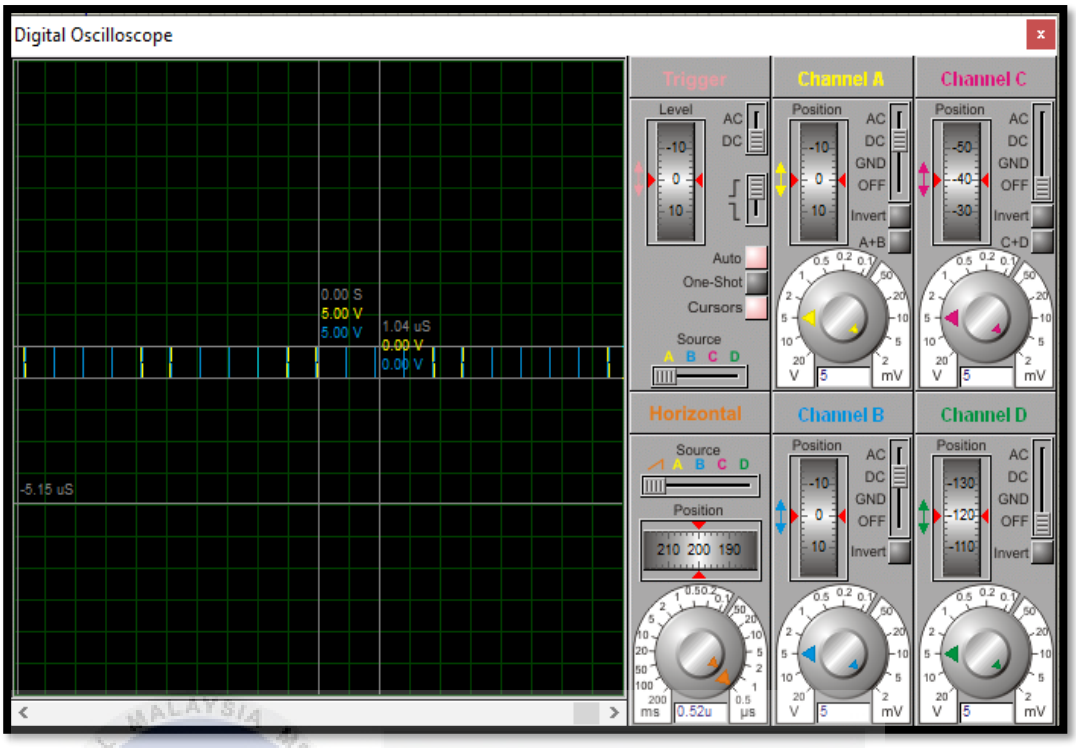

Figure 4.2: PWM waveform (inverted signal)

Based from the output waveform, it determine that the PWM is providing a 5V input to the gate terminal of MOSFET. The input voltage is switching repeatedly in 'on' and 'off' state based from the duty cycle set. In this project, for one complete cycle, it takes around 1 microseconds while there are positive and negative state in that period. During the positive cycle, the PWM will provide 5V and 0V during the negative cycle.

In this PWM system, there are two signals provided intervening each other. It is use to invert the signal for each pair of MOSFET contained in the Class D inverter. In other hands, it is compulsory to position both the output signal at ground level to ensure the amplitude are same and no overlapping occurrence between signal.

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4.2.3 PWM Control Signal Using MATLAB

In MATLAB software, the PWM can be controlled by using the pulse generator component. There are several ways to control the PWM in MATLAB, but this method seems to be the easier way to achieve that purpose. By connecting the pulse generator with a pair of MOSFET terminal block where the first block is connected to MOSFET 1 and MOSFET 4 while the one another connected to MOSFET 2 and MOSFET 3. A NOT gate is connected to a MOSFET terminal block where it used to invert the PWM signal. Then, the duty cycle can be adjusted at the pulse generator by entering the value desired and the frequency also can be insert by using the correlation of period.

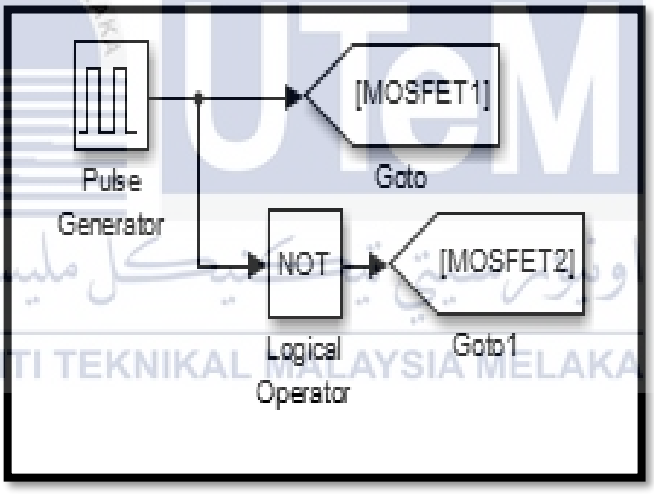

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Figure 4.3: Connection of pulse generator in MATLAB (Simulink)

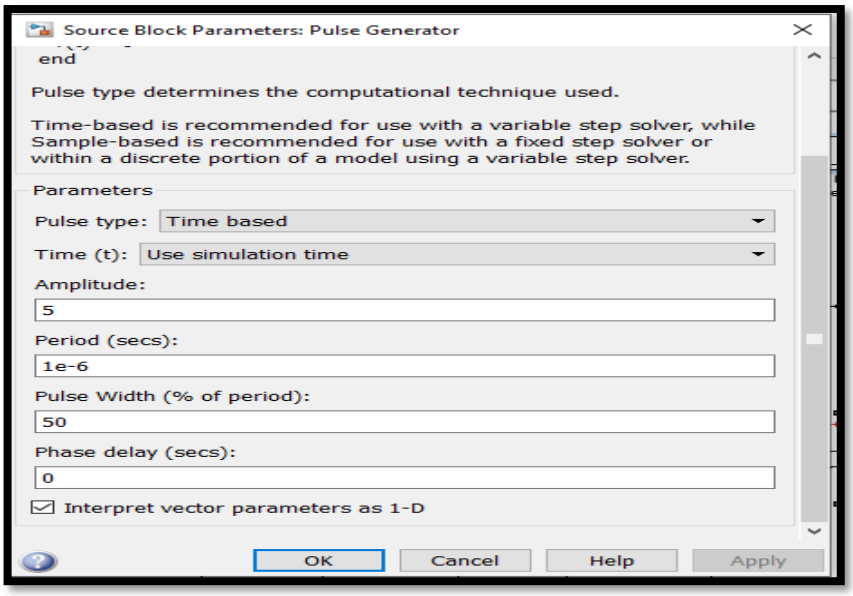

Figure 4.4: Setting of duty cycle and frequency

4.2.2 Class D Inverter

All the parameter that has been calculated were applied into each component accordingly and stated in Table 4.1. Second, the Class D circuit schematics were shown in Figure 4.5

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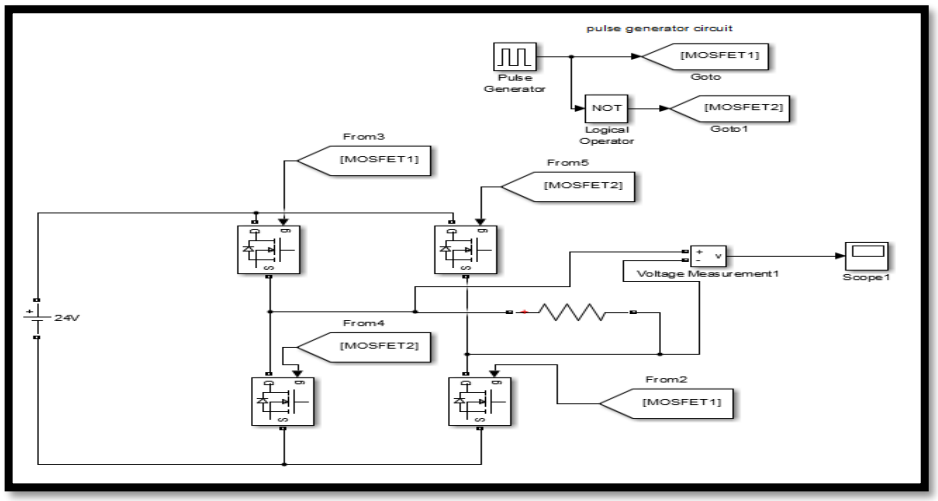

Figure 4.5: Class D inverter with R load schematic

Table 4.2: Parameter Class D inverter

Parameters	Value
V_{DC}	24V
R_L	220Ω
PWM Amplitude	5V

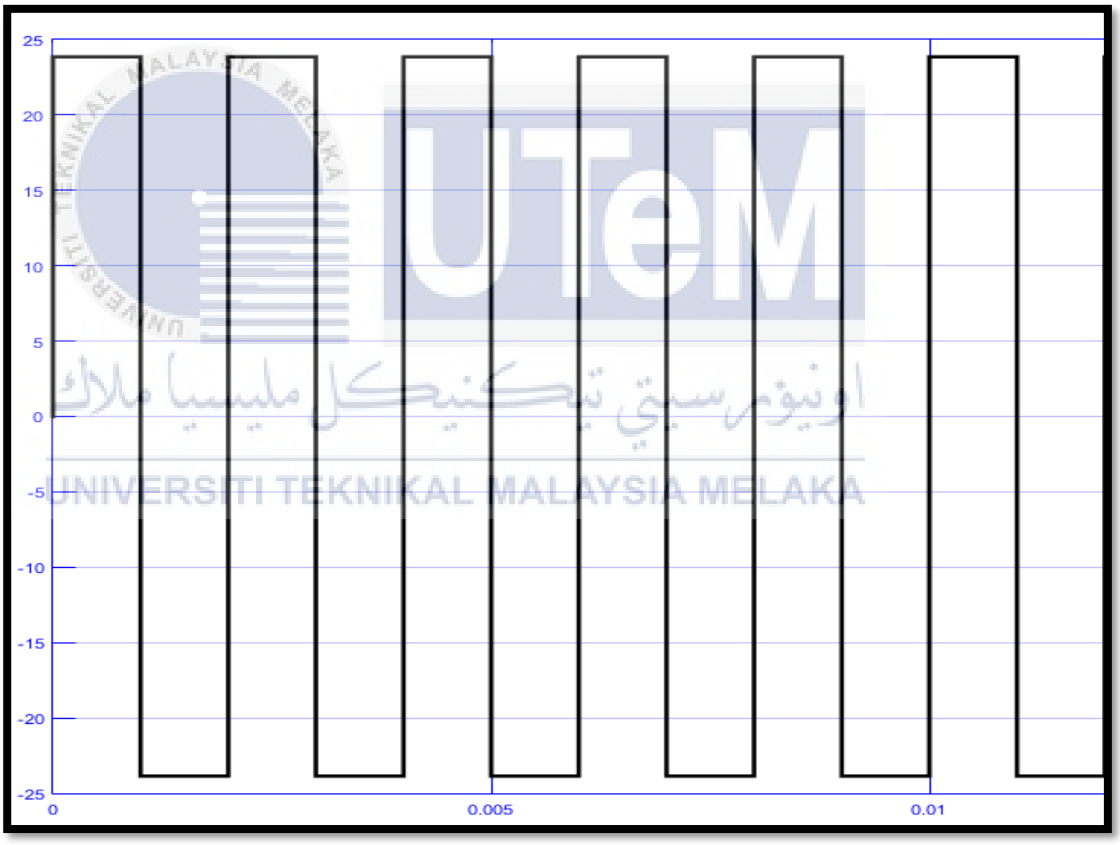

Figure 4.6: Class D inverter output waveform

Figure 4.6 shows that the output waveform is correlated with the theoretical part where the diode could be assumed as ideal, and the peak output waveform should exactly be the same value as V_{DC}. Then, the PWM contributes to the swing condition from positive cycle to the negative cycle.

4.2.3 CLL Impedance Matching

Figure 4.7 and Figure 4.8 shows both the schematic and output waveform from the simulation by MATLAB software. In this schematic, the value of capacitor and inductor are crucial to determine the smoothness of the sinusoidal waveform. Based on the formula of power, the simulation succeeds to achieve an output power of 10Watt.

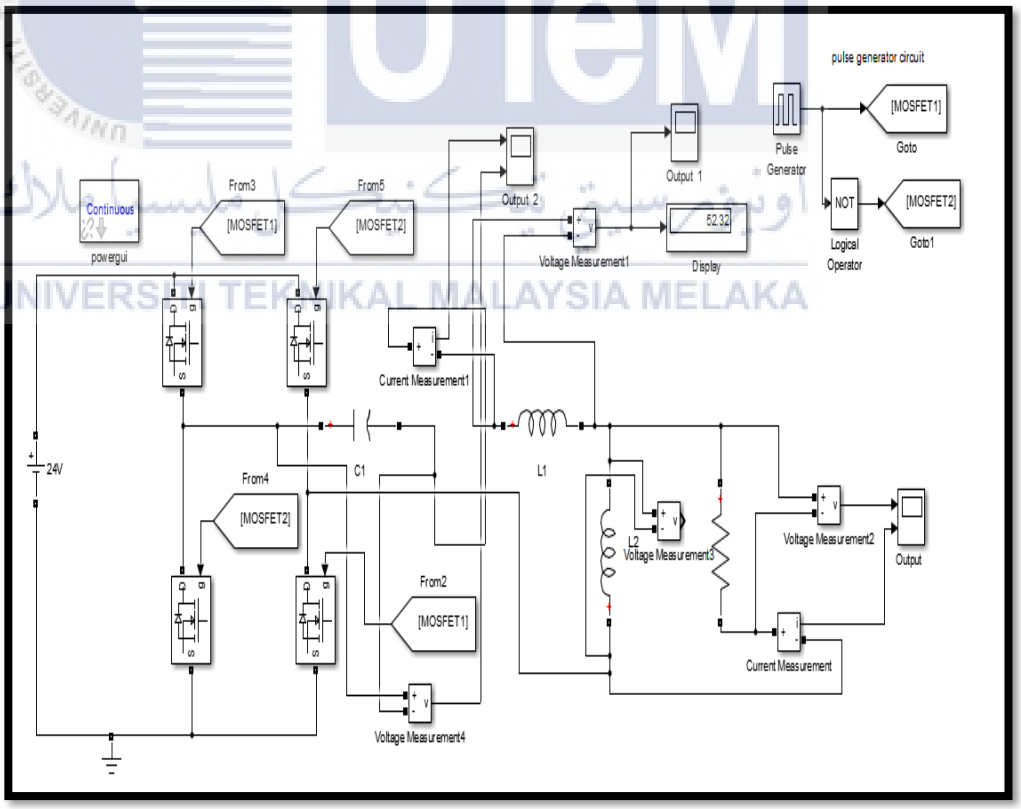

Figure 4.7: CLL impedance matching schematic

Table 4.3: Simulation results

Frequency = 1MHz	
	Simulation Results
V_c (rms)	84.85V
V_{L1} (rms)	36.99V
V_{L2} (rms)	49.5V
V_{DS}	24V
V_o (rms)	50V
I_o (rms)	0.203A
I_{dc}	0.44A
P_{in}	10.56W
P_O	10.16W
η	96.21%

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Table 4.4: Component values

Component	Value
Capacitor, C_1	0.97nF
Inductor, L_1 and L_2	17uH
Resistor	220Ω
Frequency operating	1MHz

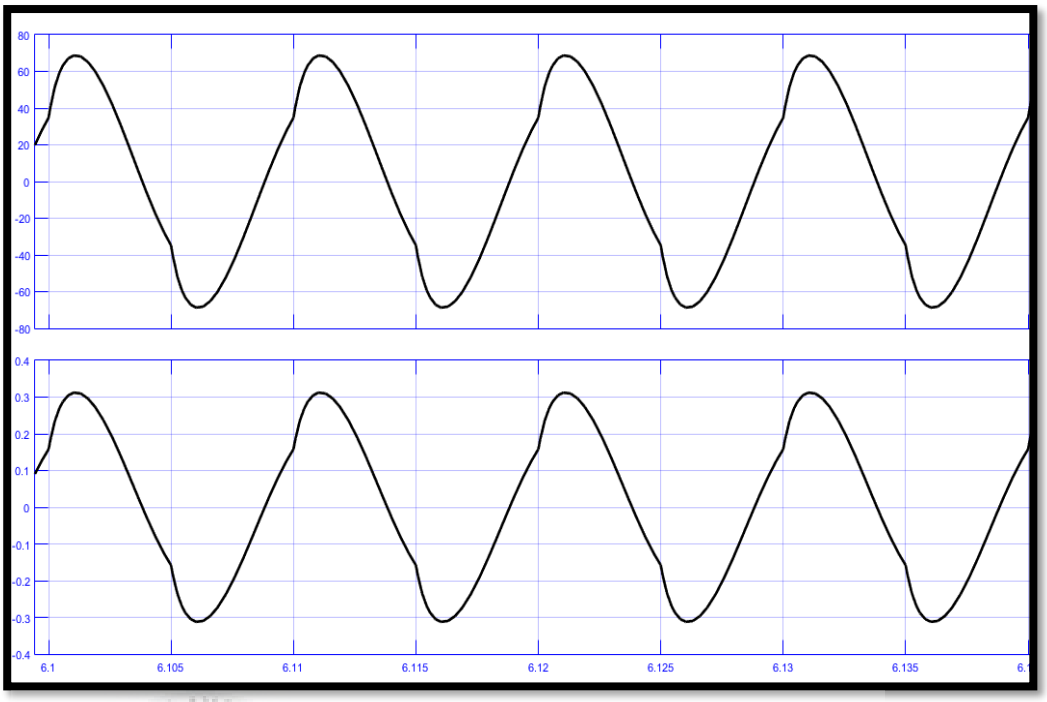

Figure 4.8: Voltage and current output waveform for CLL impedance

Table 4.5: Output results for CLL impedance matching schematic

Output	Value
Vo (rms)	50V
Io (rms)	0.203mA
Po	10.16W
Pin	10.56W
η	96.21%

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4.2.3.1 Analysis of ZVS by using comparison between CLL and LCCL impedance matching network (load variation) (Objective 2) (Objective 3)

There are some analysis approach has been developed in order to analyze the performance of impedance matching network between CLL and LCCL towards the Class D inverter topology.

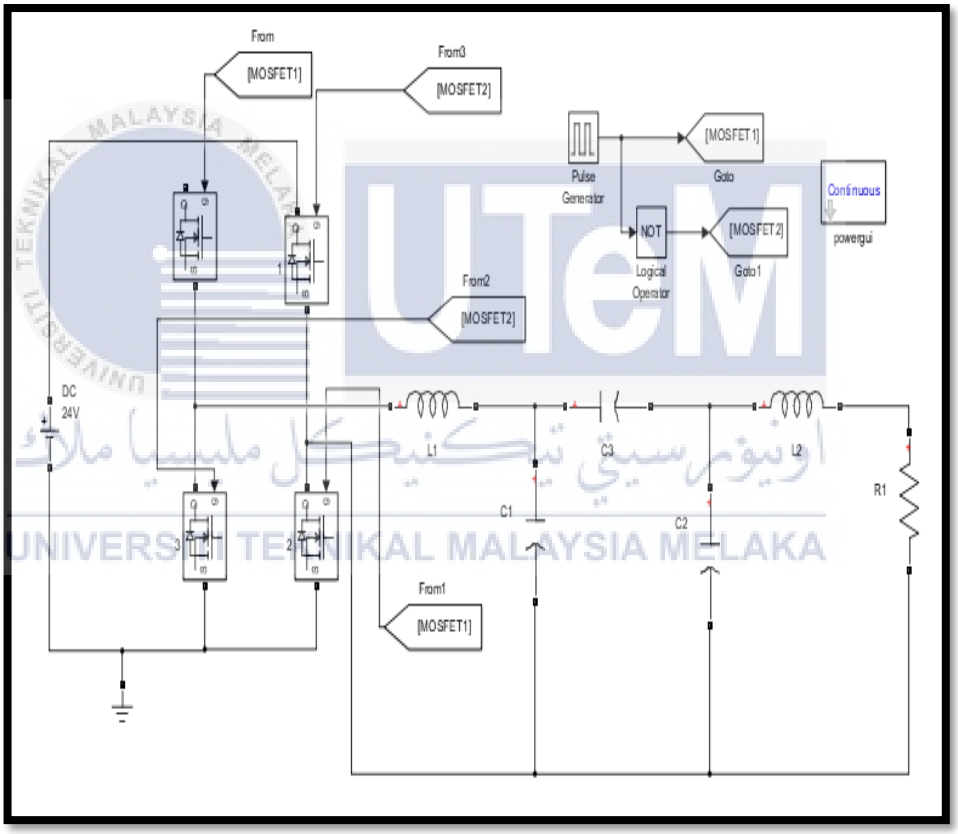

Figure 4.9: Class D inverter with LCCL impedance matching

Table 4.6: Component values for LCCL impedance

Parameter	Value
Series inductance, L_1	16.2uH
Series capacitance, C_1	9.82mF
Coupling capacitance, C3	0.97nF
C_2	9.82mF
L_2	16.2uH
R load	220Ω

Those values as stated in Table 4.6 has been developed by using the calculation part as same as in Table 4.1 since the class of inverter is same. In order to achieve the objective 2, two method of analysis has been developed based from the ZVS performance, power output and power input. Two parameter has been varies such as the load variation and coupling distance. This analysis are used to analyze the CLL and LCCL correspondent towards both parameter.

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4.2.3.2 Analysis ZVS condition comparison between efficiency and load variation (CLL and LCCL impedance)

In this part, a range value of resistance has been chosen (100Ω, 150Ω, 220Ω, 250Ω, 300Ω) to analyze the impact of variation load towards efficiency. Nevertheless, only the average result of resistance has been shown below in order

to display the comparison. The output waveform has been measured at Vds and Ids parameter where to observe the ZVS condition occurrence.

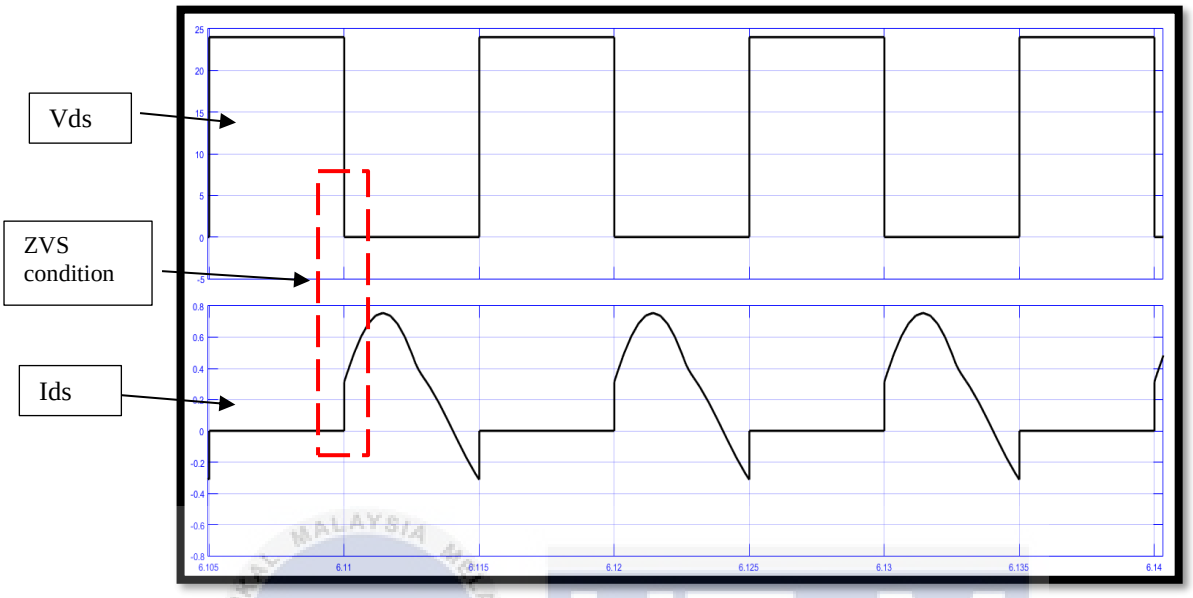

Figure 4.10: ZVS condition CLL impedance (100Ω)

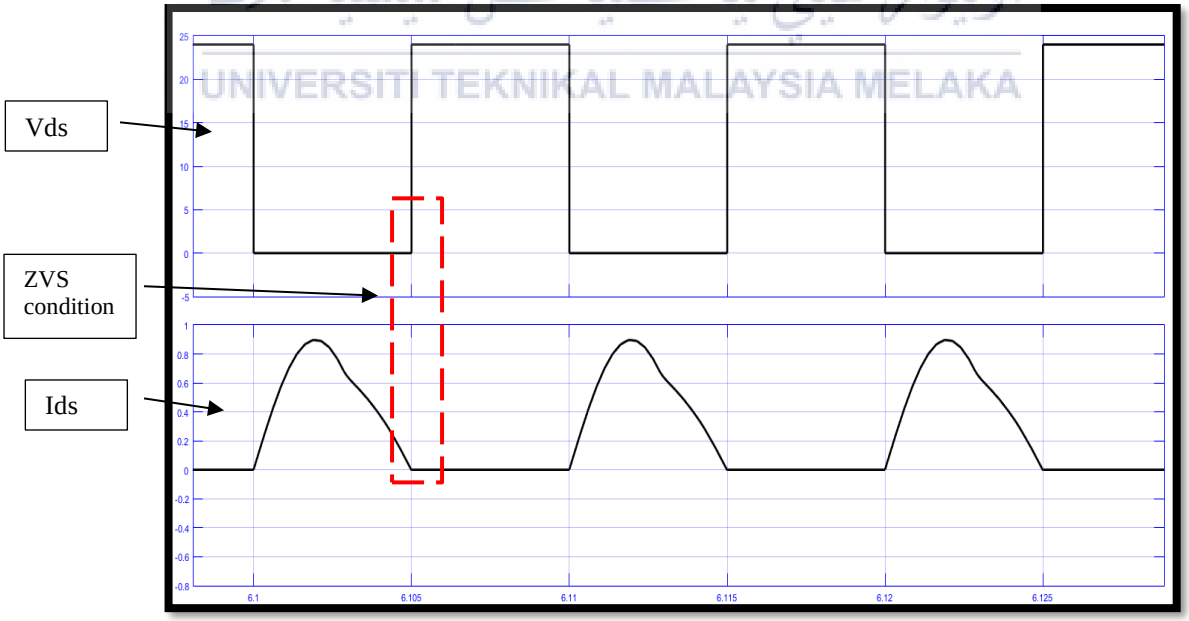

Figure 4.11: ZVS condition CLL impedance (220Ω)

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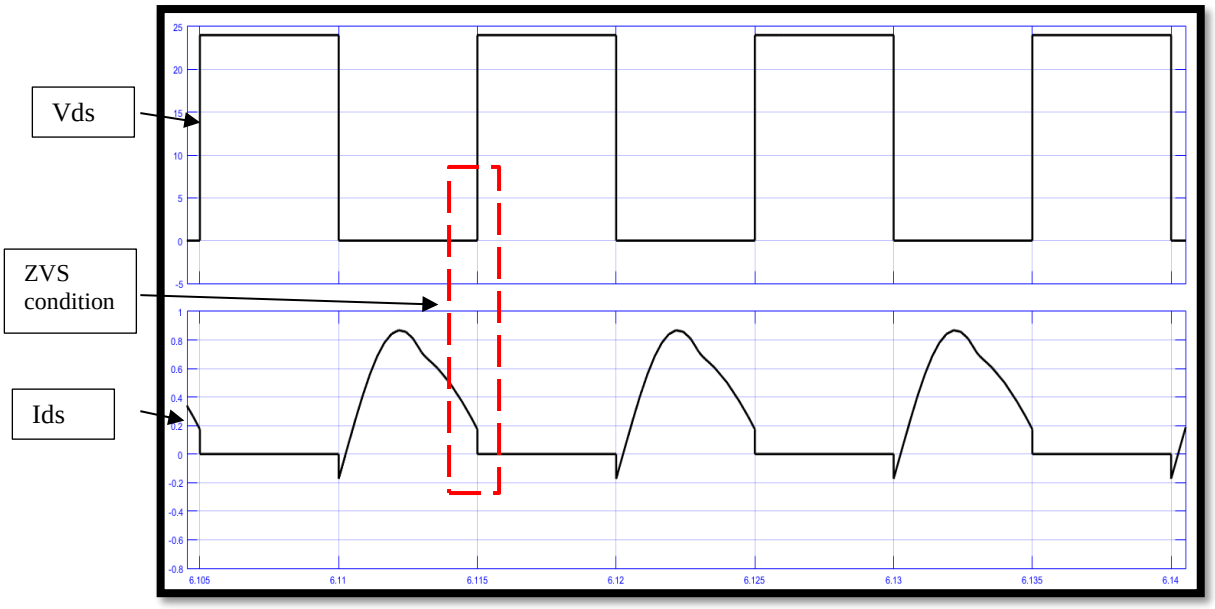

Figure 4.12: ZVS condition CLL impedance (300Ω)

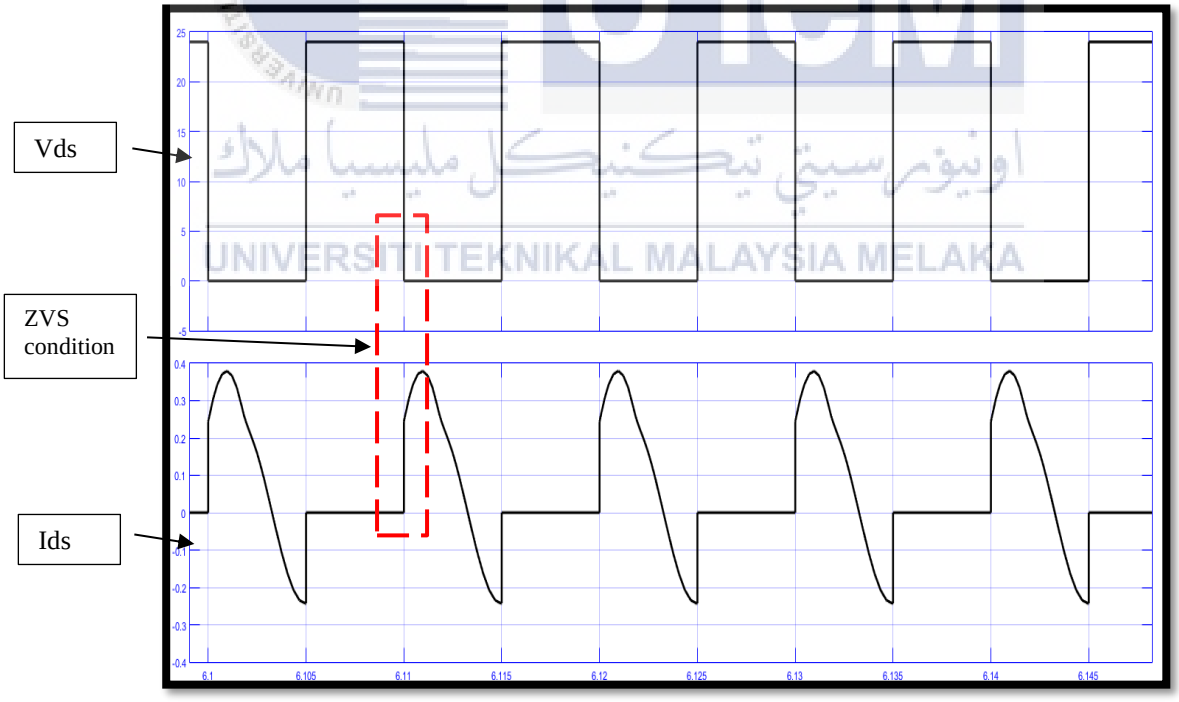

Figure 4.13: ZVS condition LCCL impedance (100Ω)

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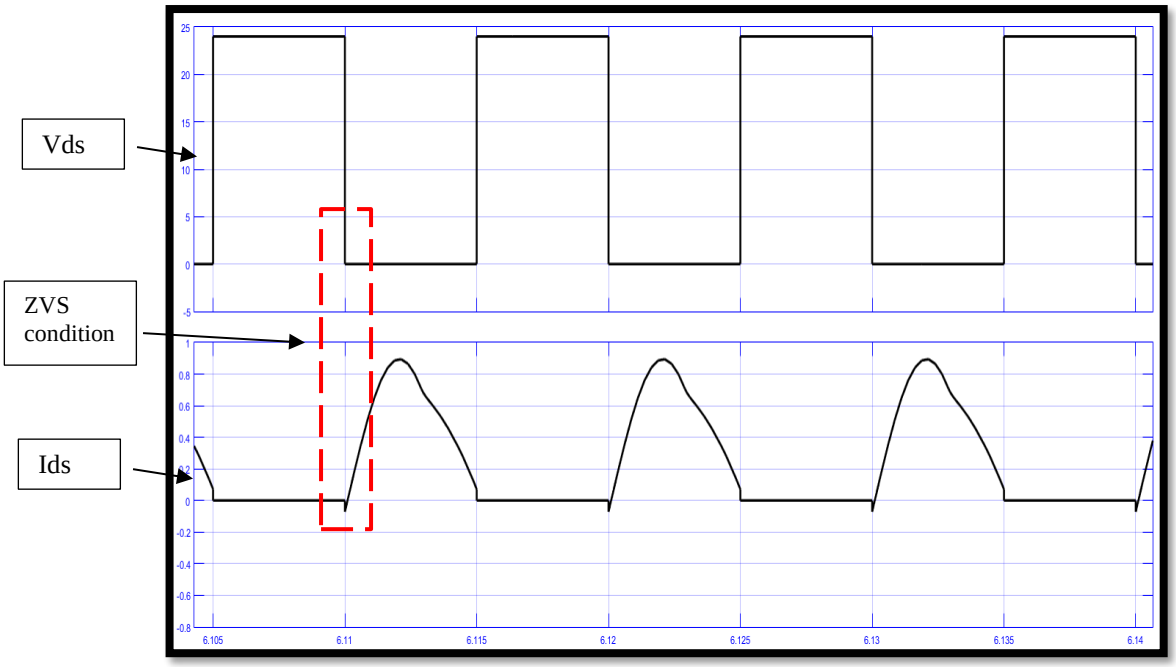

Figure 4.14: ZVS condition LCCL impedance (220Ω)

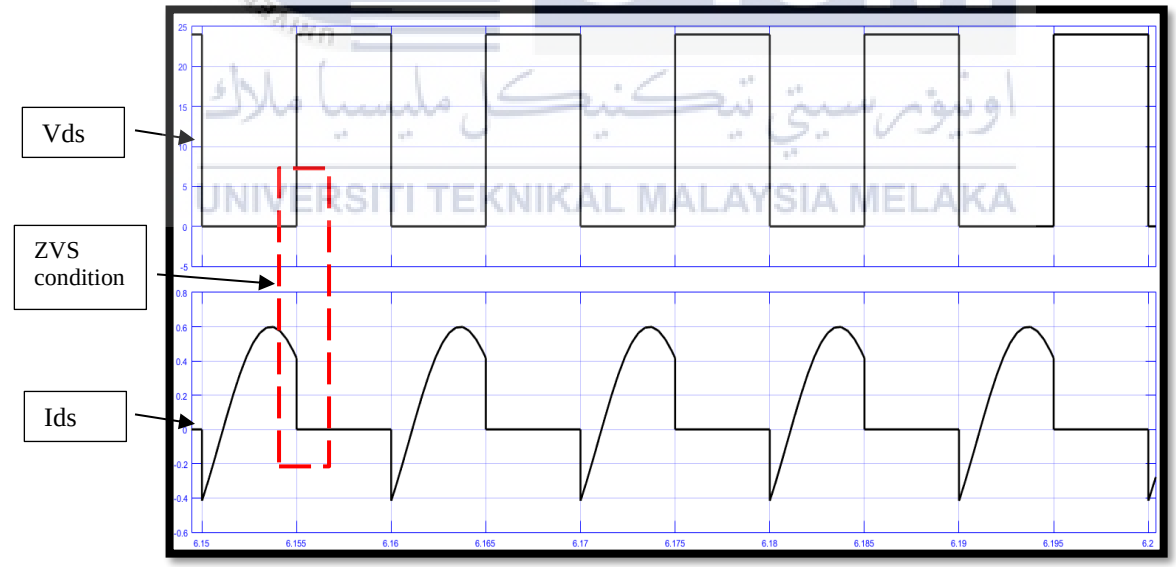

Figure 4.15: ZVS condition LCCL impedance (300Ω)

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Table 4.7: Parameter for CLL impedance load variation

Resistance (Ω)	Pin (W)	Pout (W)	Efficiency, η (%)
100	8.4	6.76	80.48
150	9.36	8.21	87.74
220	9.84	8.80	89.43
250	10.32	8.70	84.30
300	10.80	8.25	76.40

Table 4.8: Parameter for LCCL impedance load variation

Resistance (Ω)	Pin (W)	Pout (W)	Efficiency, η (%)
100	9.12	4.45	48.82
150	9.04	5.38	54.71
220	21.6	13.25	61.32
250	19.2	11.37	59.24
300	14.4	8.12	56.38

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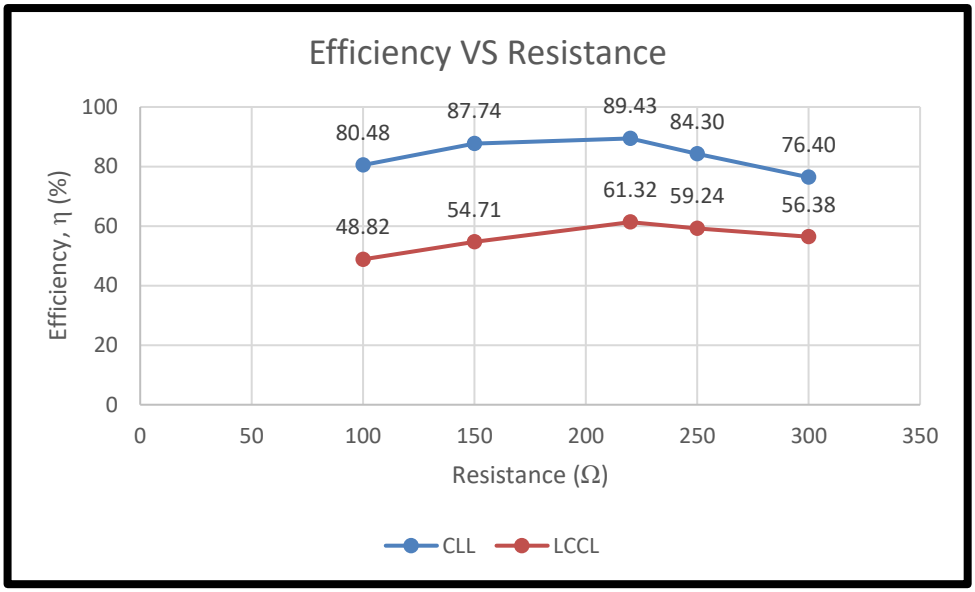

Figure 4.16: Efficiency VS Resistance graph

Based from the output ZVS condition waveform for both CLL impedance and LCCL impedance, when the value of resistance is at 220Ω, the ZVS condition shows no overlapping occurrence between Vds and Ids, where this is called as the resonant state. At this particular point, the value of efficiency has been optimized due to no power losses at the MOSFET configuration. Compared to resistance at 100Ω and 330Ω, the ZVS condition shows overlapping between both Vds and Ids and does occurred power losses. Next, by referring to Figure 4.16, technically has been proved that the CLL impedance has a better performance of efficiency compared to the LCCL impedance.

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4.2.3.3 Analysis comparison between efficiency and distance variation (CLL and LCCL impedance)

For this analysis, several values of distance coupling plate has been varied (1mm, 2mm, 3mm, 4mm, 5mm) in order to analyze the impact of distance coupling towards the efficiency of CPT. Also, only average of results has been shown below in order to observe the ZVS condition. Based from the formula (2.1), indeed the value of capacitance is inversely proportional to the distance coupling capacitance. For this part, the Class D inverter with CLL impedance and LCCL impedance has been analyzed by the performances towards variable distance. The value of area will determine the size of rectangular plate used. In this project, the permittivity of material can be assume as air.

$$A = \frac{(C)(d)}{(\varepsilon o)(\varepsilon r)}$$

$$A = \frac{(0.97nF)(1mm)}{(1)(8.85x10^{-12})} = 109.6\text{m}^2$$

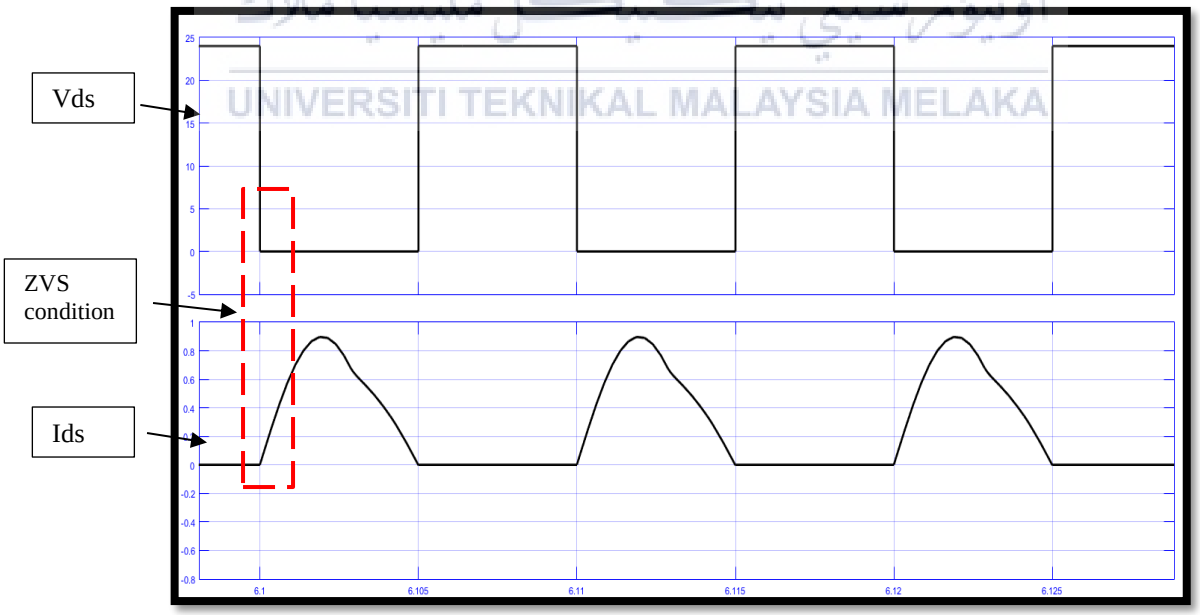

Figure 4.17: ZVS condition CLL impedance (1mm)

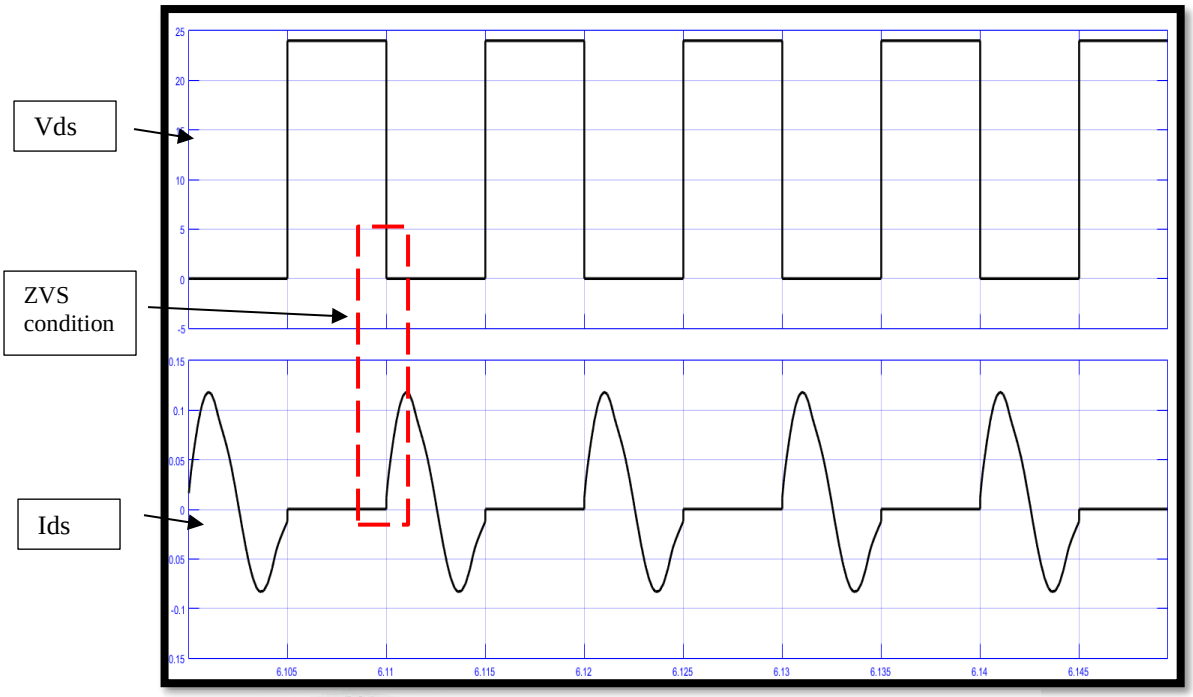

Figure 4.18: ZVS condition CLL impedance (3mm)

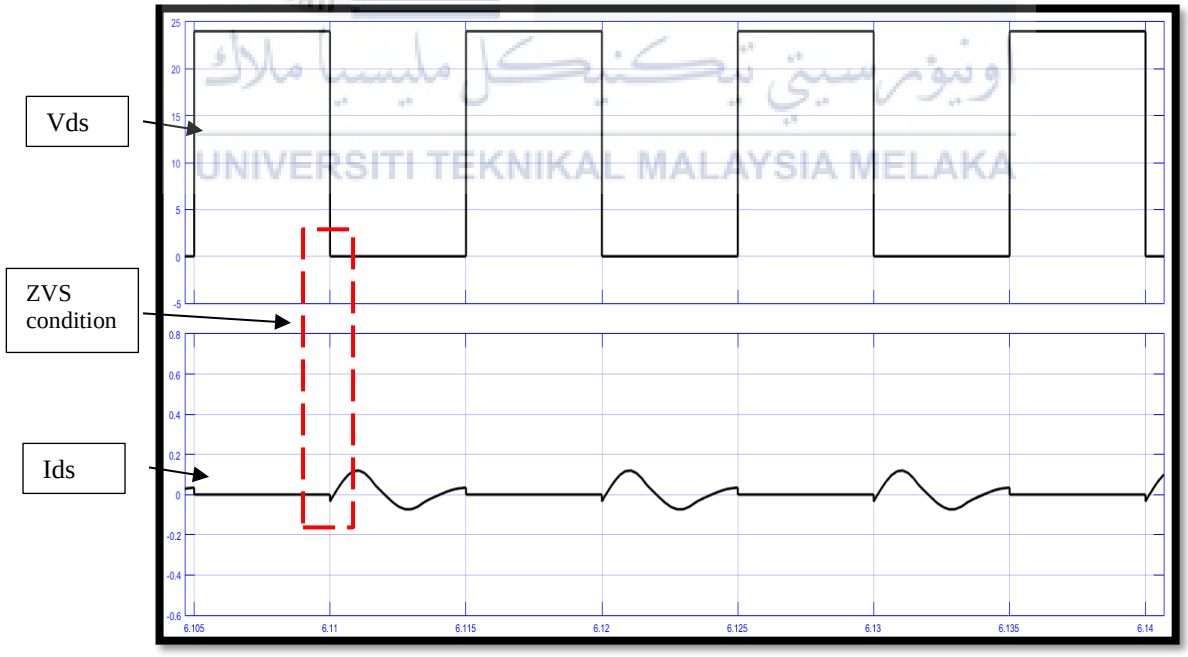

Figure 4.19: ZVS condition CLL impedance (5mm)

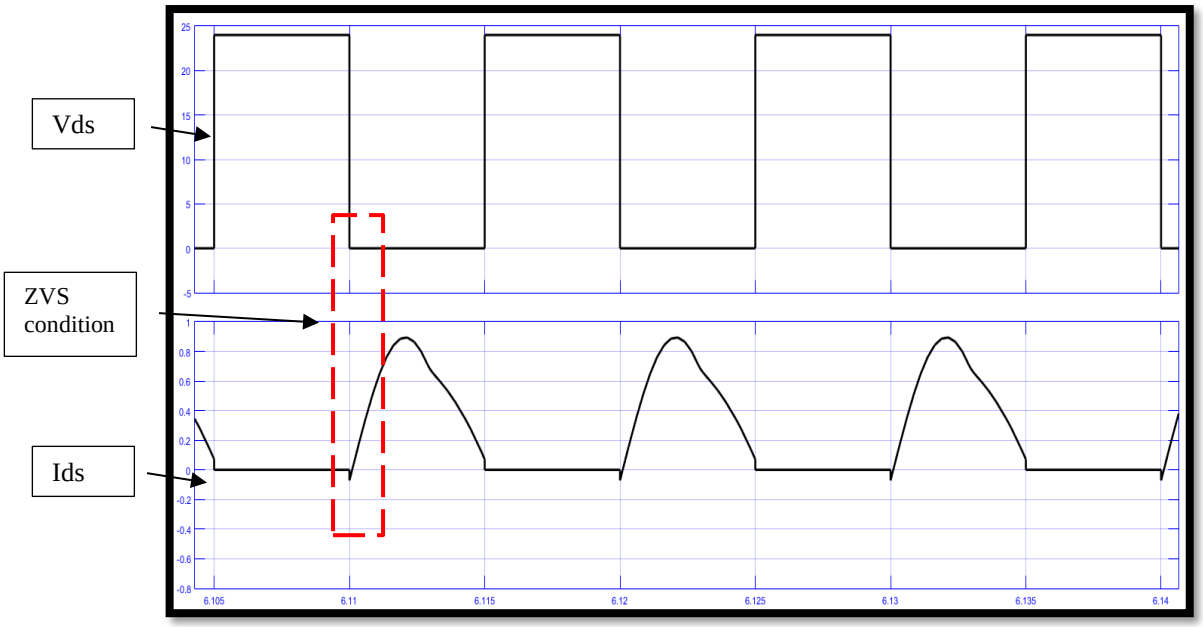

Figure 4.20: ZVS condition LCCL impedance (1mm)

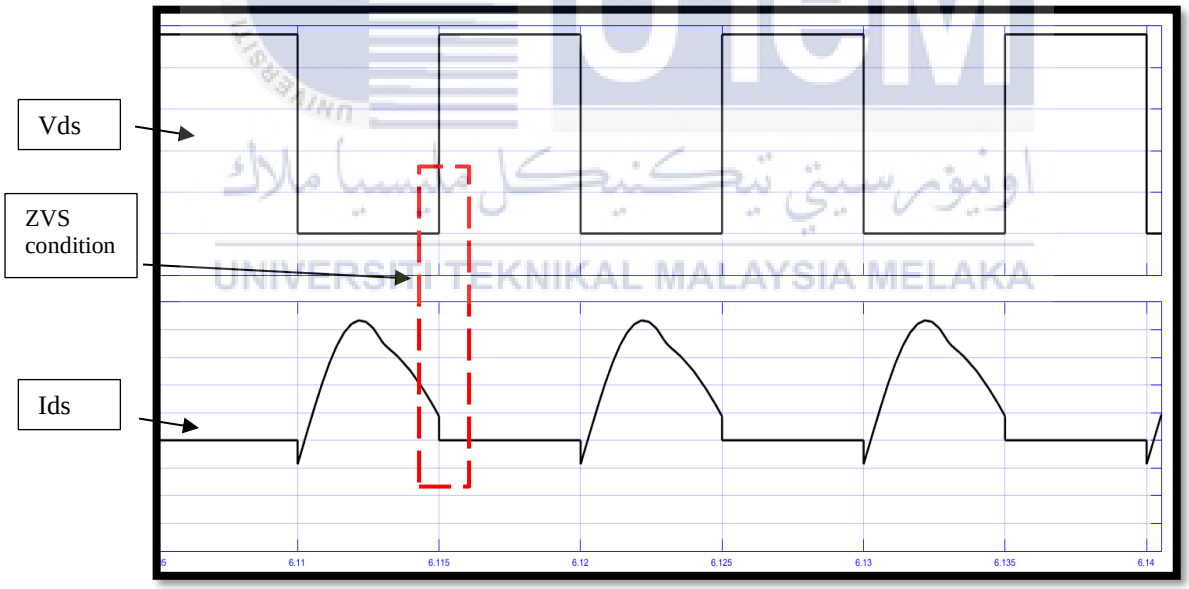

Figure 4.21: ZVS condition LCCL impedance (3mm)

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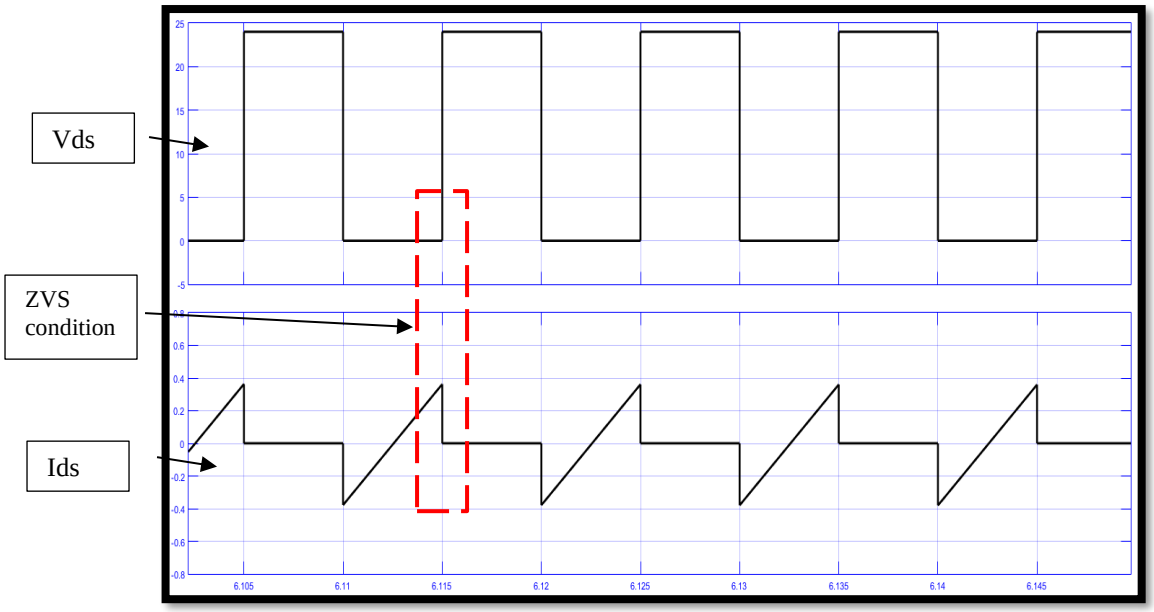

Figure 4.22: ZVS condition LCCL impedance (5mm)

Table 4.9: Parameter for CLL impedance distance variation

Distance (mm)	Capacitance (F)	Coupling capacitance (F)	Pin (W)	Pout (W)	Efficiency, η (%)
1	0.97nF	1.93nF	9.84	8.8	89.43
2	0.48nF	0.93nF	4.08	3.33	81.54
3	0.32nF	0.63nF	3.00	2.27	75.67
4	0.24nF	0.46nF	2.88	1.96	68.12
5	0.19nF	0.37nF	2.40	1.53	63.55

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Table 4.10: Parameter for LCCL impedance distance variation

Distance (mm)	Capacitance (F)	Coupling capacitance (F)	Pin (W)	Pout (W)	Efficiency, η (%)
1	0.97nF	1.93nF	21.60	13.98	64.71
2	0.48nF	0.93nF	20.40	12.03	58.97
3	0.32nF	0.63nF	19.44	11.08	57.02
4	0.24nF	0.46nF	18.72	10.23	54.63
5	0.19nF	0.37nF	9.36	4.35	46.50

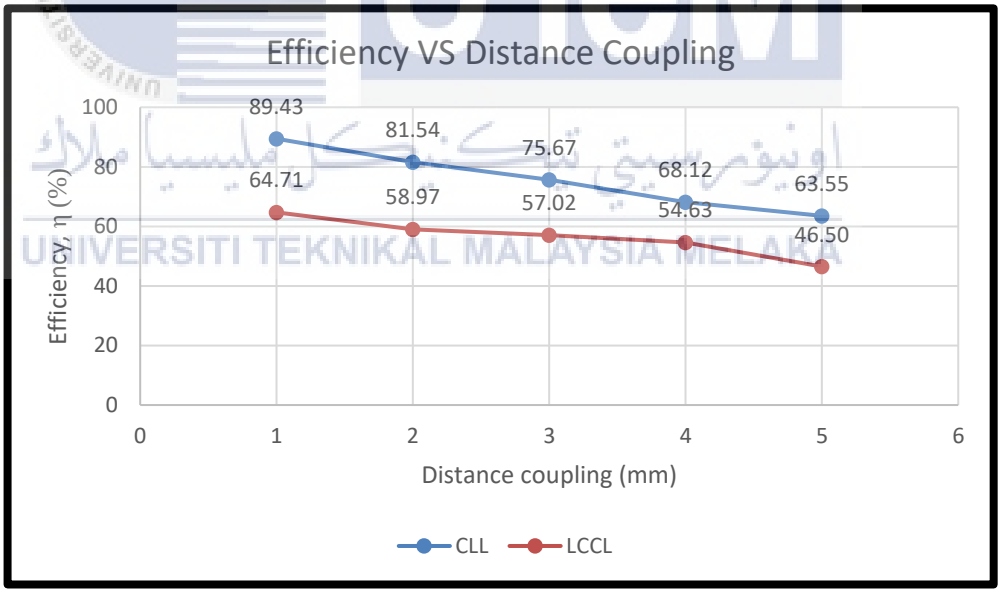

Figure 4.23: Efficiency VS Distance coupling graph

Based from the analysis results, it seems that both topology are experiencing decreasing of efficiency whenever the distance of coupling capacitance started to

increase. Hence, the results is proven to be corresponding towards equation 2.1. When the value of distance is at 1mm, the ZVS condition shows no overlapping occurrence between Vds and Ids for both impedance network, where this is called as the resonant state. At this particular point, the value of efficiency has been optimized due to no power losses. Compared to distance at 3mm and 5mm, the ZVS condition shows overlapping between both Vds and Ids and does occurred power losses. Then, the results also has shown at Figure 4.23, that the CLL impedance is having a better efficiency rate compared to LCCL impedance.

Ironic, the CLL impedance can be considered as the best solution to be used in Class D inverter topology based from the efficiency performance towards both parameter variation. Also, the objective 2 and objective 3 had been satisfied in this section.

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4.2.4 CPT System Schematic (Objective 1)

In this part, the Class D inverter, CLL impedance matching and rectifier circuit were combined to produce the desired output. It is expected to obtain dc signal output where the signal that produces from the impedance matching has been converted from ac to dc by the full bridge rectifier. Besides, it is essential to allocate a capacitor filter parallel with the load resistor to ensure the dc signal are in straight line.

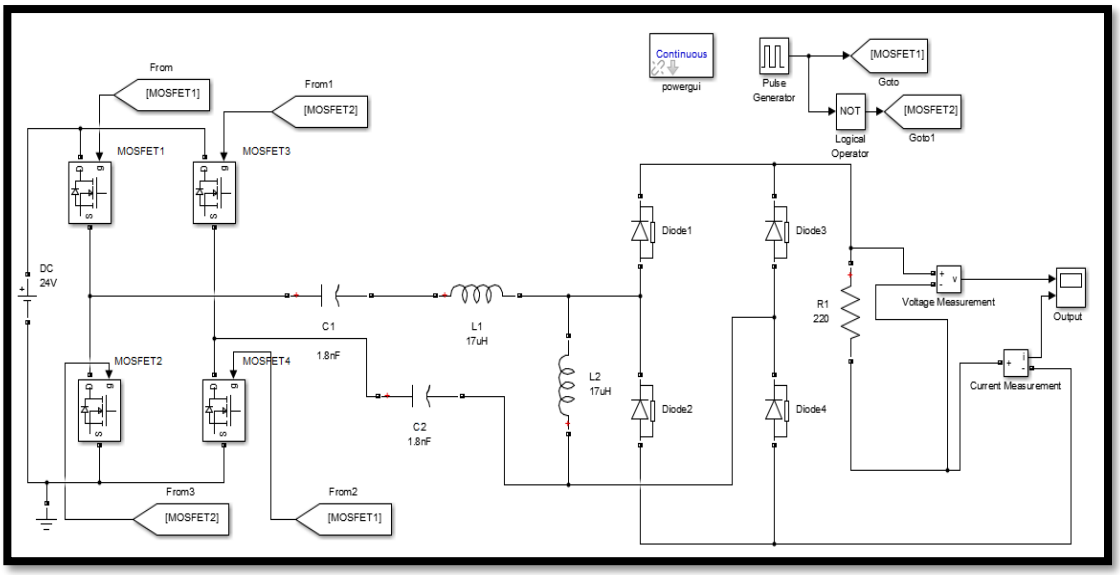

Figure 4.24: CPT system schematic with Full-wave rectifier

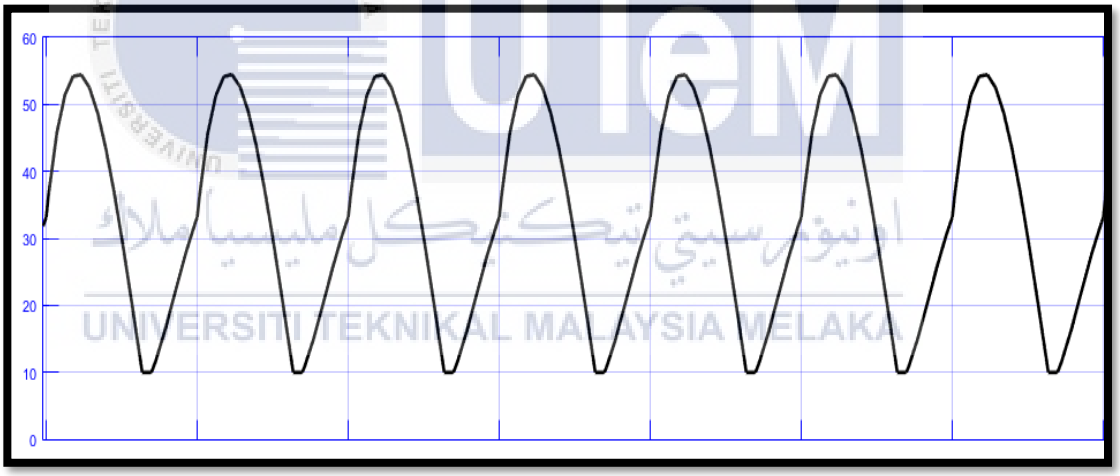

Figure 4.25 : Output voltage CPT system schematic with Full-wave rectifier

The value of filter capacitor can be obtained by the formula as stated below.

$$C = \frac{(Vm)(\pi)}{(\Delta Vo)(\omega)(R)} = 200\text{nF}$$

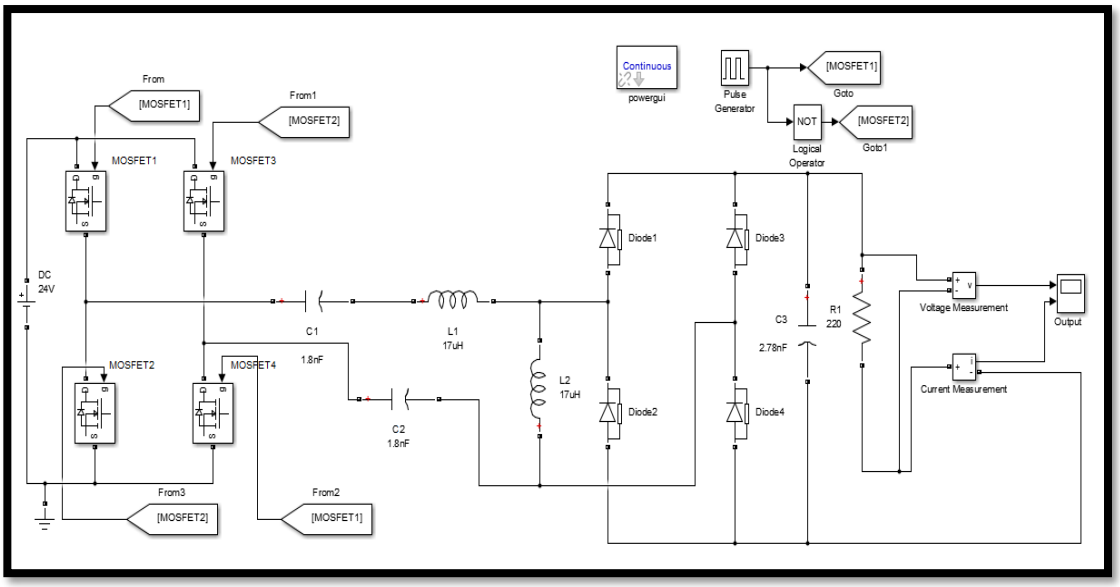

Figure 4.26: CPT system schematic with Full-wave rectifier (Capacitor filter)

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Figure 4.27: Voltage and current output

Table 4.11: Output results for CPT system with rectifier

Output	Value
Vo	42.5V
Io	0.19A
Po	8.1W
Pi	11.03
η	73.16%

4.3 Discussion

Based from the result achieved by performing the simulation on MATLAB software, it seems to be the results from calculation part need to be varies on some values to ensure the output desired could be obtained. Moreover, the parameter value for voltage and current in Table 4.1 need to be convert into rms values since this configuration is an AC configuration.

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In the initial stage of developing the calculation part, the initial minimum load resistor value was 150Ω but then the value has vary to 220Ω in the schematic of Class D inverter in order to get the desired output. Moreover, the value of capacitor, C_1 in Class D inverter also experienced a variation from the calculated value. Then, to replace the coupling capacitance part, the capacitor, C_1 is to partially connect in series and becoming C_1 and C_2.

Indeed, the resonance converter output will produce a smooth sinusoidal ac waveform where the MOSFETs play the role in switching the dc input into ac

sinusoidal waveform. In the obtained result as shown in Figure 4.8, the output waveform is experiencing a little contrast from the expected physical. This could be affected by the value of resonant components such as capacitor and inductor or the rise time that controlled by the PWM to the MOSFET.

The ZVS condition is the crucial part in this analysis. From the ZVS condition, it can be observed regarding of power losses at MOSFET configuration and also could lead to unsmooth of the resonance waveform. This ZVS condition can be one of the parts that can enhance the efficiency of the overall CPT system.

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CHAPTER 5

CONCLUSION AND FUTURE WORKS

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5.1 Conclusion

This chapter will outline and conclude all of the potential work that has been done. It will also address future works and suggestions that can be finished to improve this project further.

This project researches a radiate identity such as the output power, operating frequency, power loss and others. Research shows that Class D inverter topology is an ideal method to transform from dc to ac signal with lower efficiency. These characteristics will in future make the Class D inverter a predominance feature in the Capacitive Power Transfer system.

5.2 Completed Work

To conclude, the main aim of this project is to achieve low power for application and efficiency by using Class D inverter with corresponding CLL impedance. This project has resulted in the specification parameter with the 8.1W output power, 1MHz frequency and 73.16% efficiency. Besides, the performance of the components has been analyzed with the theoretical method and need some variation values that able to suit with the simulation schematic.

5.3 Future Works

In future, it is much recommended to pursue this project with implementing the hardware part where the consumption and working features will be much more accurate and understanding. Due to some limitation for this project to be completed, it only required to develop this wireless CPT system using capacitive approach by only using the simulation platform.

Next, it is much more possible to develop this project in future by considering the time taken to fully charge any electronic devices with low power rate. This is because time is the most crucial aspect to be evaluate nowadays since technologies are not making everything faster and efficient. Next, a future study regarding ZVS condition is much recommended in order to strongly understand and performing better overall efficiency for the CPT system.

Last but not least, the wireless CPT system is among the favorite methods in transmitting power wirelessly. This approach could be more advanced in future with much more exploration made by the engineer and researcher.

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LIST OF PUBLICATIONS AND PAPERS PRESENTED

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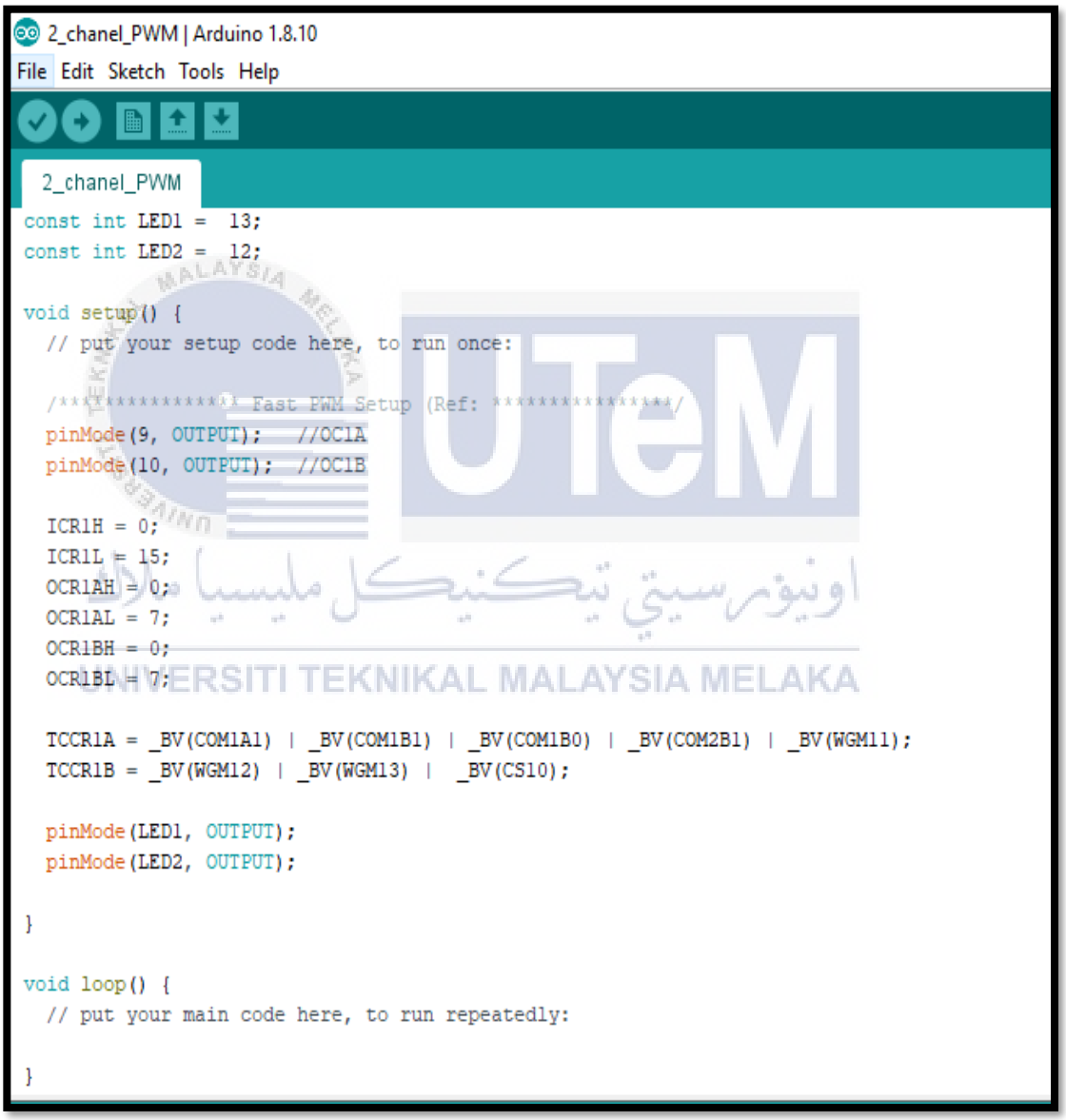
APPENDICES

Appendix A: PWM Coding Using



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Appendix B: IRFZ44 MOSFET Datasheet

VISHAY.

IRFZ44, SiHFZ44

Vishay Siliconix

Power MOSFET

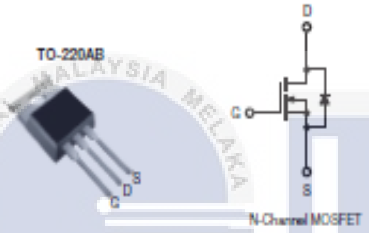
PRODUCT SUMMARY		
V_{DS} (V)	60	
$R_{DS(on)}$ (Ω)	V_{GS} = 10 V	0.028
Q_g (Max.) (nC)	67	
Q_{gs} (nC)	18	
Q_{gd} (nC)	25	
Configuration	Single	

FEATURES

- Dynamic dV/dt Rating
- 175 °C Operating Temperature
- Fast Switching
- Ease of Paralleling
- Simple Drive Requirements
- Compliant to RoHS Directive 2002/95/EC

RoHS* COMPLIANT

TO-220AB



DESCRIPTION

Third generation Power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220AB package is universally preferred for commercial-industrial applications at power dissipation levels to approximately 50 W. The low thermal resistance and low package cost of the TO-220AB contribute to its wide acceptance throughout the industry.

ORDERING INFORMATION	
Package	TO-220AB
Lead (Pb)-free	IRFZ44PbF
	SiHFZ44-E3
SnPb	IRFZ44
	SiHFZ44

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)

PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage			V_{DS}	60	V
Gate-Source Voltage			V_{GS}	± 20	
Continuous Drain Current[a]	V_{GS} at 10 V	T_C = 25 °C	I_D	50	A
Continuous Drain Current		T_C = 100 °C		36	
Pulsed Drain Current[a]			I_{DM}	200	
Linear Derating Factor				1.0	W/°C
Single Pulse Avalanche Energy[b]			E_{AS}	100	mJ
Maximum Power Dissipation	T_C = 25 °C		P_D	150	W
Peak Diode Recovery dV/dt[c]			dV/dt	4.5	V/ns
Operating Junction and Storage Temperature Range			T_J, T_{stg}	- 55 to + 175	°C
Soldering Recommendations (Peak Temperature)[d]	for 10 s			300	
Mounting Torque	6-32 or M3 screw			10	lbf · in
				1.1	N · m

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. V_{DD} = 25 V, starting T_J = 25 °C, L = 44 µH, R_g = 25 Ω, I_{AS} = 51 A (see fig. 12).
c. I_{SD} ≤ 51 A, dI/dt ≤ 250 A/µs, V_{DD} ≤ V_{DS}, T_J ≤ 175 °C.
d. 1.6 mm from case.
e. Current limited by the package, (die current = 51 A).

* Pb containing terminations are not RoHS compliant, exemptions may apply

This datasheet is subject to change without notice.
THE PRODUCT DESCRIBED HEREIN AND THIS DATASHEET ARE SUBJECT TO SPECIFIC DISCLAIMERS, SET FORTH AT www.vishay.com/doc?91000

IRFZ44, SiHFZ44

Vishay Siliconix

VISHAY.

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	62	°C/W
Case-to-Sink, Flat, Greased Surface	R_{thCS}	0.50	-	
Maximum Junction-to-Case (Drain)	R_{thJC}	-	1.0	

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 µA	60	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C, I_D = 1 mA	-	0.060	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	2.0	-	4.0	V
Gate-Source Leakage	I_{GSS}	V_{GS} = ± 20 V	-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 60 V, V_{GS} = 0 V	-	-	25	µA
		V_{DS} = 48 V, V_{GS} = 0 V, T_J = 125 °C	-	-	250	
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS} = 10 V; I_D = 31 A[b]	-	-	0.028	Ω
Forward Transconductance	g_{fs}	V_{DS} = 25 V, I_D = 31 A	15	-	-	S
Dynamic						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1.0 MHz, see fig. 5	-	1900	-	pF
Output Capacitance	C_{oss}		-	920	-	
Reverse Transfer Capacitance	C_{rss}		-	170	-	
Total Gate Charge	Q_g	V_{GS} = 10 V; I_D = 51 A, V_{DS} = 48 V, see fig. 6 and 13[b]	-	-	67	nC
Gate-Source Charge	Q_{gs}		-	-	18	
Gate-Drain Charge	Q_{gd}		-	-	25	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 30 V, I_D = 51 A, R_g = 9.1 Ω, R_D = 0.55 Ω, see fig. 10[b]	-	14	-	ns
Rise Time	t_r		-	110	-	
Turn-Off Delay Time	$t_{d(off)}$		-	45	-	
Fall Time	t_f		-	92	-	
Internal Drain Inductance	L_D	Between lead, 6 mm (0.25") from package and center of die contact 	-	4.5	-	nH
Internal Source Inductance	L_S		-	7.5	-	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	50	A
Pulsed Diode Forward Current[a]	I_{SM}		-	-	200	
Body Diode Voltage	V_{SD}	T_J = 25 °C, I_S = 51 A, V_{GS} = 0 V[b]	-	-	2.5	V
Body Diode Reverse Recovery Time	t_{rr}	T_J = 25 °C, I_F = 51 A, dI/dt = 100 A/µs	-	120	180	ns
Body Diode Reverse Recovery Charge	Q_{rr}		-	0.53	0.80	nC

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