ANALYSIS OF LOW NOISE AMPLIFIER DESIGN FOR MICROWAVE BREAST CANCER IMAGING APPLICATION

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This report is submitted in partial fulfilment of the requirements for the degree of Bachelor of Electronic Engineering with Honours

Faculty of Electronics and Computer Technology and Engineering
Universiti Teknikal Malaysia Melaka

2024

DECLARATION

I declare that this report entitled “Analysis of Low Noise Amplifier Design for Microwave breast Cancer Imaging Application” is the result of my own work except for quotes as cited in the references.

Signature : 

Author : Naili Khairina binti Khairul Zaman

Date : 17 Jun 2024

APPROVAL

I hereby declare that I have read this thesis and in my opinion, this thesis is sufficient in terms of scope and quality for the award of Bachelor of Electronic Engineering with Honours

Signature	:	……
Supervisor Name	:	Ts. Azahari bin Salleh
Date	:	17 Jun 2024

DEDICATION

This thesis is dedicated to all of my family members who have supported me in continuing this degree journey.

ABSTRACT

Radar-based microwave breast cancer imaging is a non-invasive, radiation-free method for early detection of breast cancer. It uses microwave signals to create images of breast tissue, identifying tumours and abnormalities. However, the existing system lacking on sensitivity, accuracy and high noise due to weak microwave signal from antenna which will create low-quality image of tumour. This project aims to design a low-noise amplifier with analysis & verify the simulation performance of designed LNA using Advanced Design System (ADS) software with expected result are in frequency of 1.5GHz. The analysis is based on single stage and two-stage(cascade) design with different transistor technology and matching network comparison which is stub and L-matching. The pHEMT MGA-684P8 and Silicon (Si) AT-42086 were used to design and simulate the LNA by connecting two-port network transistor with input/output matching network and DC biasing network. The cascaded design of transistor AT-42086 perform a better result in noise figure which is 0.082 dB(L-matching) and 0.061 dB(stub) meanwhile the gain achieved 45.165 dB in both matching techniques. This project has a potential application in the field of medical imaging to provide a non-invasive method for breast cancer detection.

ABSTRAK

Pengimejan kanser payudara gelombang mikro radar ialah kaedah bebas radiasi dan tidak invasif untuk pengesanan awal. Ia menggunakan isyarat gelombang mikro untuk mengesan tisu dan tumor serta keabnormalan payudara. Namun, sistem sedia ada kurang tepat dan sensitif, serta menghasilkan imej tumor berkualiti rendah kerana isyarat gelombang mikro yang lemah dari antenna. Projek ini bertujuan mereka bentuk LNA dan mengesahkan prestasi pada frekuensi 1.5 GHz menggunakan perisian ADS. Analisis ini mereka bentuk dan membandingkan peringkat satu dan dua (lata) menggunakan teknologi transistor serta padanan rangkaian, iaitu padanan punting dan L. Transistor pHEMT MGA-684P8 dan silikon AT-42086 digunakan untuk merekabentuk dan mensimulasikan LNA dengan menyambungkan transistor dua alur dengan rangkaian padanan input/output bersama rangkaian pincangan DC. Rekabentuk lata dari transistor AT-42086 menunjukkan hasil lebih baik dengan angka hingar iaitu 0.082 dB (padanan L) dan 0.061 dB (punting) manakala gandaan mencapai 45.165 db dalam kedua-dua teknik padanan. Projek ini berpotensi tinggi untuk pengimejan perubatan tidak invasif dalam pengesanan kanser payudara.

ACKNOWLEDGEMENTS

Alhamdulillah all praises to Allah SWT for giving me the opportunity, strength, determination, and patience in completing my bachelor's degree research and thesis.

I would like to express my deepest gratitude to my supervisor, Ts. Azahari bin Salleh for giving me a chance to do this project for the last two semesters. His invaluable guidance and patience were a constant source of motivation to complete this whole project. May Allah ease everything and give good health to Ts. Azahari bin Salleh. I am also grateful for the opportunity to pursue studying at Faculty of Electronics and Computer Technology and Engineering (FTKEK) in University Technical Malaysia Melaka.

Finally, my thanks go to all people who have supported me in completing this work directly or indirectly.

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LIST OF SYMBOLS AND ABBREVIATIONS

For examples:

LNA	:	Low Noise Amplifier
ADS	:	Advanced Design System
GaAs	:	Gallium Arsenide
HEMT		High Electron Mobility Transistor
pHEMT	:	Pseudomorphic High-Electron Mobility Transistor
BJT		Bipolar junction transistors
FET		Field-effect transistors
RF	:	Radio Frequency
NF		Noise Figure
G_T		Transducer Gain
Hz		Hertz
K		Rollet's Stability Factory
dB		Decibel
Z		Impedance
f		frequency

C	Capacitor
L	Inductance
R	Resistor
I	Current
V	Voltage
G	Giga
n	Nano
p	Pico
Ω	Ohm
π	pi

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CHAPTER 1

INTRODUCTION

This chapter includes the background of the project which includes the project overview, problem statement, objectives, and scope of the project.

1.1 Research Background

Breast cancer remains a formidable global health challenge, affecting millions of lives and underscoring the critical importance of advanced diagnostic technologies. Breast cancer is a malignant condition characterized by the uncontrolled growth of cells in the breast tissue. It is one of the most prevalent cancers globally, affecting both men and women, although it is much more common in women. Early detection is crucial for successful treatment, emphasizing the significance of advanced diagnostic technologies in identifying abnormalities within breast tissue. Common

methods for breast cancer screening include mammography, ultrasound, and magnetic resonance imaging (MRI [1]).

In the pursuit of early detection and effective treatment, the field of medical imaging has seen remarkable advancements, with microwave breast cancer imaging emerging as a promising modality. Microwave imaging techniques have found application in the nondestructive testing of constructions and the search for concealed items, among other areas. Microwave imaging is less expensive and non-ionizing than traditional techniques including computed tomography (CT) scans, mammograms, and X-rays. The use of microwave imaging technology to human diagnosis has been the subject of several investigations in recent times due to advancements in hardware, algorithms, and processing approaches. This is predicated on the difference in electric characteristics in the microwave spectrum between the tumor and healthy breast tissue. Microwave tomography and radar-based imaging are the two primary types of microwave imaging. By reconstructing the dielectric constant of the imaging object from the dispersed electromagnetic field of one or more frequencies, microwave tomography operates. The radar-based technique measures the dispersed field of a target by sending a brief pulse in its direction. When compared to tomography, radar-based microwave imaging requires fewer processing resources, which allows for faster detection [1].

This innovative approach utilizes microwave signals to create detailed images of breast tissue, offering potential advantages in sensitivity and safety compared to traditional methods. However, like any evolving technology, microwave breast cancer imaging faces its own set of challenges, including issues related to reduced sensitivity, increased noise, and compromised accuracy. In this context, the

integration of a Low Noise Amplifier (LNA) becomes pivotal, promising to address these challenges and elevate the capabilities of microwave breast cancer imaging. A LNA is a device that amplifies very low-power signals without significantly degrading their signal-to-noise ratio. The LNA is typically located immediately after the antenna in a receiver circuit, although a duplexer or filter may precede it. An LNA is a crucial component of the front end of any receiver module found in a transceiver module. Without lowering the signal to noise ratio (SNR), the LNA increases the signal (SNR). A few of the factors that need to be optimized in the design of an LNA include gain, noise figure, stability factor, and non-linearity. The three stages that make up a simple LNA are the input impedance matching circuit, the amplifier stage and the output impedance matching circuit [2]. Figure 1.1 is an illustration of the functional components of a communication system.

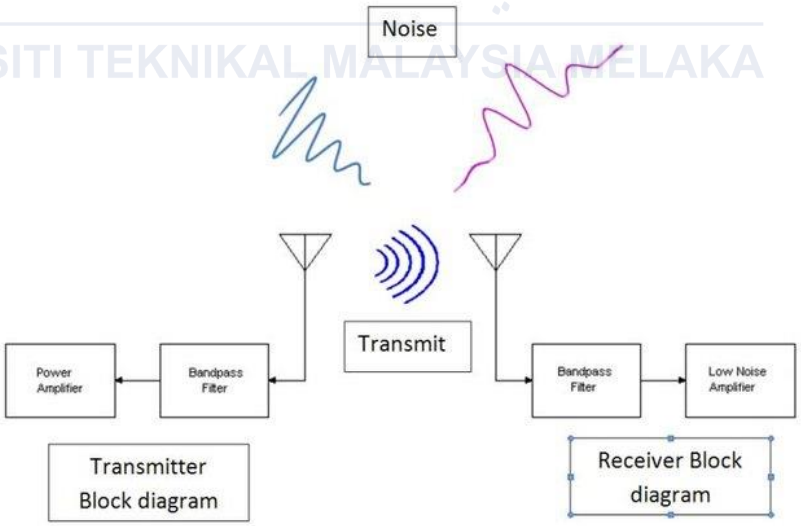


Figure 1.1: Transmitter and Receiver Block Diagram

1.2 Problem Statement

The evolution of technology in the field of microwave breast cancer imaging has been marked by significant advancements, transitioning from initial implementations to present-day systems. The problem statement revolves around identifying and addressing issues within an existing radar-based microwave breast cancer imaging system. The system is currently experiencing the ability to detect tumors due to sensitivity that impact the signal and would make increase the noise levels. This is particularly challenging in breast cancer imaging, where the weak signals and the noise levels can be significant. If LNA is not amplified weak signals efficiently, the accuracy in detect the small tumor will leading to decrease, ultimately cannot enhance the potential as a valuable tool in early-stage breast [3].

The integration of an LNA into the radar-based microwave breast cancer imaging system is proposed as a comprehensive solution to address the existing issues, ultimately aiming to produce higher quality images and significantly enhance the system's ability to detect smaller tumors. The anticipated benefits of adding an LNA are enhance the strength of weak signals received by the antenna. Besides that is expected to reduce overall system noise by mitigating noise levels, the signal-to-noise ratio will improve, hence resulting in clearer and more accurate images. This contributes to better distinguishing between normal and abnormal breast tissue. Thus, the combined effect of improved sensitivity and reduced noise leads to an overall enhancement in system accuracy.

1.3 Objectives

The objectives of the project are as follows:

a) To design the Low Noise Amplifier for Microwave Breast Cancer Imaging Application.

b) To analysis & verify the simulation performance of designed LNA using Advanced Design System (ADS) software.

1.4 Scope of Project

The scope of this project revolves around the design and simulation of an LNA tailored for radar-based microwave breast cancer imaging, using Advanced Design System (ADS) software. The LNA operational frequency is set between 1.5 GHz, aligning with the specific requirements of breast cancer imaging. The project encompasses a thorough parameter analysis, including stability, gain, and noise figure. Stability analysis ensures reliable operation, while gain analysis focuses on amplification within the desired frequency band, crucial for enhancing system sensitivity. Additionally, noise figure analysis aims to minimize noise introduced during signal amplification, maintaining a high signal-to-noise ratio. This project aims to contribute to the advancement of breast cancer imaging technology by developing a specialized LNA that optimizes the performance of radar-based systems within the specified operational parameters. Therefore, the analysis is based on single stage design and two-stage(cascade) design with different transistor technology which is GaAs pHEMT MGA-684P8 and silicon (Si) BJT AT-42086. The comparison of matching network has been used L-matching and stub matching type.

1.5 Thesis Outline

Based on the thesis outline for this project, there are five chapters to follow accordingly to completing the thesis. The content of chapter 1 is basically a research

background to the title of the project which is a general overview about low noise amplifier and application in microwave imaging for breast cancer. Then, for the rest of the outline of chapter 1 is indicated to problem statement, objectives and scope of work.

Chapter 2 describes the specific overview of the design of low noise amplifier. The characteristics and design of other projects are also discussed in literature review. Additionally, there is also a summary of comparisons between transistor technology to design low noise amplifier.

Chapter 3 provides a methodology of the project. The flow process of the project step by step until the end is constructed to designing the low noise amplifier. The specification of the LNA is involved in this chapter to fulfill the requirements of the best LNA.

Chapter 4 primarily discusses the low noise amplifier's analysis and results following its design using the Advanced Design System. It also compares the two transistor types that were chosen MGA-684P8 and AT-42068.

The study's accomplishments are concluded in Chapter 5. The chapter's conclusion contains a number of recommendations aimed at enhancing the caliber of this research going forward.

CHAPTER 2

LITERATURE REVIEW

2.1 Overview of Microwave Breast Cancer Imaging

Low Noise Amplifier also known as LNA is one of the most important parts of a microwave system. It is a crucial part of an RF receiver as it may reduce noise figure produced by the amplifier when the noise is directly received. To address this challenges in the design of a low noise amplifier, different transistor technology and topology approaches have been included in the literature to solve this difficulties in the construction of 1-2 GHz frequency range for low noise amplifier.

This project will briefly discuss the advantages and disadvantages of each transistor technologies. Furthermore, the analysis of various behavior transistor

technologies and topologies will reveal the LNA system's overall performance for microwave breast cancer imaging application.

2.2 Overview of Transistor Technologies

The choice of transistor technology for LNA is crucial to achieving the desired performance characteristics, such as low noise figure, high gain, and reliable signal amplification. Transistor also known as Semiconductor devices, have three or more terminals. The third terminal allows a comparatively modest and low-power input signal to control the output current. Transistors are employed in amplifiers to provide power, voltage, or current gain. In most cases, the goal of RF and microwave design is power gain. Silicon (Si) or compound semiconductors like gallium arsenide (GaAs), indium phosphide (InP), or gallium-nitride (GaN) are used to produce the majority of transistors. Due to the far higher integration density that silicon technology allows, this technology is currently dominating the market. Compound semiconductor technology is only utilized when it offers a special benefit, such as high power, enhanced noise performance, or high efficiency. Germanium is employed as a dopant in silicon, which is therefore called silicon germanium. However, silicon and germanium are typically found in very minute amounts, so silicon with a dopant is what is meant to be understood as SiGe. SiGe is a compound semiconductor that is occasionally used. It has equivalent concentrations of silicon and germanium [4].

GaAs is a compound material that been used in semiconductor devices technology. It based circuits and devices are used in many different systems and products, indicating that they have a well-defined role in both commercial and defense applications. Applications cover the millimeter wave to several hundred

MHz low-frequency spectrum. The selection of a device is determined by various factors that pertain to its basic functioning mechanisms and performance, in addition to its manufacturing maturity.

Based on the [5] research, in applications requiring low-noise amplifiers, the PHEMT is widely acknowledged as the preferred choice, closely followed by the CMOS. The primary source of noise in FETs stems from thermal-diffusion effects caused by random variations in carrier speed within the device channel. This variability leads to fluctuations in current and subsequently introduces noise. A critical factor is the capacitive coupling between the gate and the channel, influencing noise by subtracting a portion of the gate noise from the drain noise. This unique characteristic of FETs contributes to their remarkably low-noise performance.

Optimal noise performance is achieved by minimizing source access resistance and maximizing the current gain cutoff frequency f_t . This necessitates designing the device for maximum transconductance g_m and minimum gate capacitance C_{gs}, conditions that can be controlled to some extent by careful bias selection. As a general guideline, the minimum noise (F_{min}) is obtained under conditions of approximately ~Idss/10. However, there is a distinction in the required bias range for achieving this condition. HEMT exhibits a broader range of Ids values over which F_{min} is attained, providing a more extensive margin in LNA circuit design. Given the usual preference for high gain in amplifiers, a trade-off between gain and noise is often necessary as the bias for F_{min} does not always align with the bias for maximum gain. This trade-off is less pronounced in HEMTs due to their broader range of bias for F_{min}. On the other hand, CMOS transistors are voltage-controlled devices that

operate at low power and low voltage, and their bias range is typically in the range of 1-5 volts.

The pursuit of high gain also demands specific device designs featuring a heterojunction or another type of buffer beneath the channel to minimize carrier injection and reduce the output conductance. The potential for high base doping opens new possibilities for HBTs, making them intrigued for wide bandwidth and low-noise operation. An analysis of noise characteristics reveals that PHEMTs exhibit less bias sensitivity in noise performance compared to CMOS devices that generally have higher bias sensitivity. For the ultimate solution in achieving low-noise operation, InP-based HEMTs are considered. Typically, HBTs exhibit lower levels of low-frequency noise. By implementing effective circuit designs that minimize the impact of nonlinearities and consequently reduce noise up conversion, HBT oscillators can be crafted to deliver exceptionally low phase-noise performance. Table 2.1 shows comparison of each technology.

Table 2.1: Comparison of Tansistor technology

Technology	Advantages	Disadvantages
Heterostructure Bipolar Transistor (HBT)	• Offers higher cut-off frequency • Lower cost and delivers higher efficiency • Wideband impedance matching	• Higher power consumption • Larger in size • More complex biasing requirements
Complementary MOSFET (CMOS)	• Lower power consumption and smaller size compared to BJTs. • Widely used in digital applications	• Higher noise figure and lower gain compared to BJTs
High Electron Mobility	• Offers a	• HEMTs can be

Transistor (HEMT)	combination of low noise figure and very high frequency performance. • Low noise performance is better than other devices, including HBTs, MESFETs, CMOS, and BJT • Suitable for applications where high gain and low noise at high frequencies are required.	sensitive to temperature and bias conditions. • may not handle high power levels as efficiently as some other technologies.
Pseudomorphic HEMT (pHEMT)	• PHEMTs are a type of HEMT that improves the performance of the device by using an extremely thin layer of one of the materials, so thin that the crystal. • Allows the construction of transistors with larger bandgap differences than otherwise, giving them better performance.	• may involve more complex fabrication processes. • Sensitivity to temperature and bias conditions may be a consideration.

2.3 Review of LNA Previous Research

In literature review this is an overview of previous research on a topic. It can be used to help make a comprehensive survey of scholarly sources on a specific topic to get the knowledge to allow identify relevant theories, methods and gaps in existing research.

Based on this paper [6], the title was mainly discussed about analyzing and designing with implementation of T-matching at the input and output port and uses of negative feedback technique to highlight the trade-off among the parameters which is gain, noise figure, sensitivity and stability. Besides known using the cascode topology, this proposed project also using PHEMT technology FHX76LP manufactured by Eudyna Devices Inc to design and simulate by using ADS software. This project was achieved their parameter with frequency range is 5.8GHz, forward gain 20.19dB, noise figure 0.360dB and stability 1.048 respectively.

The paper [7] was focusing to design of two stage cascaded ultra-wideband by using negative image amplifier technique. This technique succeeds in the desired specification with the average gain 23dB and low noise figure less than 2dB with return loss less than 8dB. But, to make the specification ideal the negative lumped elements for input and output matching of LNA was used. The AWR microwave tool design was used to design the low noise amplifier. This study uses the parasitic effects of the microstrip line to suggest a novel approach for acknowledging the negative valued lumped elements. whose effects are amply demonstrated by simulation data and quantitative study.

In this paper [8], it describes the crucial role plays in low noise amplifier was a technology of transistor itself. With assistance from pHEMT 0.15μm the ability to handle with specific requirements make it the best technology to design, simulate and fabricate a C-band (5.4-5.9GHz) two stage common-source wideband. The analysis from this paper shows the perfect comparison from simulated and measured with just slight difference from the specification of proposed designed LNA. Simulated results of minimum noise figure 0.9dB and for forward gain 18.6dB

meanwhile for measured results proved for minimum noise figure is 1dB and for forward gain is 18dB. This paper also proposed great fabrication techniques and circuitry designed that have capability to high survival up to 37dBm principally for highly survival radar receiver component. Thus, it concludes that the proposed technology is to show the results of comparable low noise figure, gain, high dynamic range and top survivability.

This work [9] describes the design, simulation, and prototype of a 1.5GHz LNA with a 100MHz bandwidth. ADS software was utilized to model the circuit. Surface mount devices (SMD) are used, with the transistor "Infineon BFP420" serving as a key component. Other parts are microstrip lines, which are replacing resistors, capacitors, and inductors. The FR4 board was used to create the circuit. Using a spectrum analyzer, noise figure meter, and VNA, numerous LNA characteristics were measured. The LNA's maximum noise figure is 1.33 dB, while its minimum gain is 15.4 dB. It is completely stable between 50 MHz and 10 GHz. There is a 5V DC supply and a 10mA current consumption. With this lNA, OIP3 is around 14dBm.

The goal of the research [10] is to use double feedback approach architecture to design a novel cascode low noise amplifier (LNA) for wireless communication, specifically for long term evolution (LTE). The aim of this paper is to illustrate how novel strategies for the execution of Long-Term Evolution (LTE) might increase gain performance by lowering noise figures. By implementing the twofold feedback technique architecture, the innovation technique offers the potential to enhance performance in multiple areas, including power consumption, noise figure, gain, bandwidth, stability, and complexity. The features needed to gather data for a Smith

chart and s-parameter produced by simulation are obtained using the Advance Design System (ADS) program.

Table 2.2: Existing LNA Design

No.	References	Specification	Transistor Technology	Limitations
1	[6]	Frequency range: 2300-2400bMHz Gain: 14 dB Noise Figure: 1.2dB	pHEMT FHX76LP	• Sensitivity and Third Order Intercept Point (IIP3) analysis missing.
2	[11]	Gain: 22dB Noise Figure: 3.5dB	SMIC 130nm CMOS	• Simulation only.
3	[12]	Frequency: 3.1-10.6Ghz Noise figure: 3.9dB Gain: 12.5dB	CMOS 130nm	• Lower gain.
4	[7]	Frequency: 3-10Ghz Gain: 23dB Noise Figure: <2dB	pHEMT ATF 36163	• Lacks measured results to validate proposed concepts. • Stability analysis is incomplete.
5	[8]	Frequency range: 5.4-5.9Ghz Noise figure: <1 dB Gain:18 dB	pHEMT 0.15µm	• lack of stability analysis.
6	[9]	Frequency Range: 1.5GHz Gain: 15.4 dB Noise Figure: 1.33 dB Bandwidth: 100MHz	BJT BFP420	• lack of stability analysis.

7	[10]	Frequency Range: 3-5GHz Gain: >20 dB Noise Figure: <1.5 dB Bandwidth: 100MHz	pHEMT ATF-34143	• Simulation only.
8	[13]	Frequency Range: 5.8 GHz Gain: 20 dB Noise Figure: <3 dB	HEMT FHX76LP	• Simulation only
9	[14]	Frequency Range: 400-800MHz Gain: 30-50 dB Noise Figure: ~0.34 dB	GaAs pHEMT	• lack of stability analysis.
10	[15]	Frequency Range: 13-16 GHz Gain: >20 dB Noise Figure: <1.2 dB	InGaAs HEMT MGF4937AM	• Lack of stability analysis.
11	[16]	Frequency Range: 1.57 GHz Gain: 21 dB Noise Figure: 1.98 dB	pHEMT ATF-34143	• Stability analysis is incomplete.
12	[17]	Frequency range: 2.11-2.33 GHz Gain: 21 dB Noise Figure: 0.78 dB	SOI CMOS 65nm	• Lacks measured results to validate proposed concepts.
13	[18]	Frequency range: 102-155 GHz Gain: 16.2-21.2 dB Noise Figure: 3.6-5.6 dB	70nm GaN HEMT	• Lack of stability analysis.
14	[19]	Frequency Range: 1.5-15.7GHz Gain: 20.5 dB Noise Figure: <2dB	RFCMOS 45nm	• lack of stability analysis
15	[20]	Noise Figure > 6.3dB Gain varies between 10 to 16.9dB	CMOS 180nm	• Simulation only

CHAPTER 3

METHODOLOGY

This chapter discusses a proposed LNA design based on the findings of a study of common LNA design specification, topologies, transistor technology and fundamental of noise figure, gain, stability and linearity. The LNA is recognized as the essential block because it increases the received signal from the antenna to a desired frequency range. The primary objective of this project is to use the electrical circuit modeling program ADS to create the ideal and compact circuit.

3.1 Flow Chart Project

The LNA design method is shown by the design flow in Figure 3.2. This flowchart defines the specific procedures needed to accomplish the project's primary objective. First, investigations analyzing transistor selection and topology have been made. Thus, the GaAs pHEMT and silicon (Si) technology meanwhile the single

stage and cascade topology have been selected as the suitable approach for designing the low-noise amplifier.

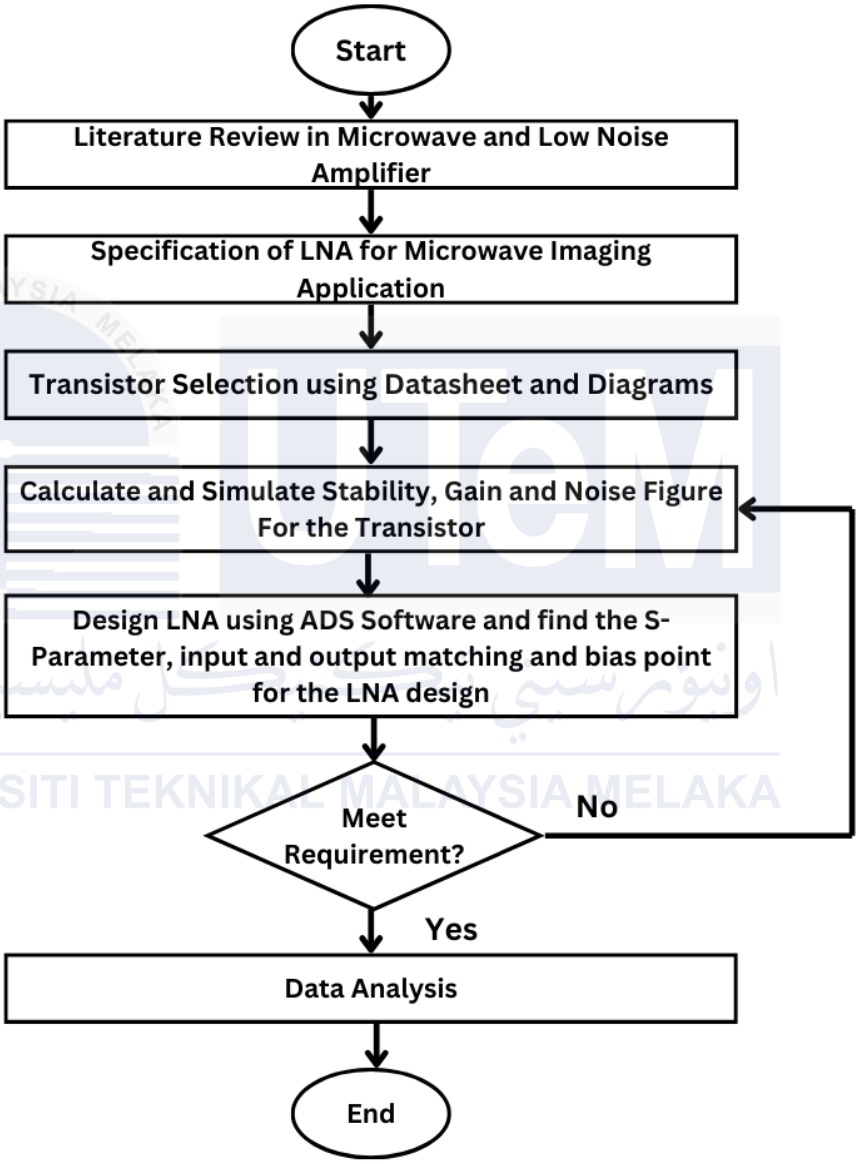


Figure 3.1 : Flow Chart of Project

3.2 Low Noise Amplifier Design Methodology

This section will provide a quick explanation of the stages involved in designing the LNA. Examining the LNA architecture comes first, then specifications, transistor

selection, stability, transistor biasing, matching network, optimization, and simulation analysis.

3.2.1 Specification of Low Noise Amplifier

It is essential to find out the specifications of an LNA before beginning its design. The LNA frequency range will align with the application frequency band in accordance with the specifications required to build the LNA system. The LNA will use a transistor that is suitable for LNAs, generate the most gain, and have the lowest level of noise figure.

A literature review should be conducted in order to identify appropriate specifications for the LNA based on its intended usage. The specifications listed in Table 3.1 below must be followed to design the LNA.

Table 3.1: Specifications of LNA

Parameter	Value
Noise figure	<2 dB
Gain	>20 dB
Frequency	1-2 GHz
Input/output impedance	50Ω
Circuit topology	Cascade

3.2.2 Matching Network

A matching network is a set of circuits designed to match the impedance of a given source to impedance of a given load at specified frequency. This is achieved by using lossless elements such as lumped components and transmission lines to

minimize reflections and maximize power transfer between source and load. Initially, for input matching network the reflection coefficient for source is justified from the centre with $Z_0 = 50\ \Omega$ and it is also similar for output matching network.

L-shaped matching is a simple method to adjust components of the load and source impedances. The network uses capacitor and inductor elements either one series reactance or shunt reactance either. The basic step design for an L-matching network is:

a) Normalize ($z_L = Z_L/50$) and locate the point of z_L on the smith chart
b) Based on the location of z_L select the appropriate type of LC L-section topoplogy
c) For type 1 L-section:

   i) Move along the constant conductance circle until it intersects with the unit resistance circle. Record the susceptance change and thus determine the value of shunt L or C.

   ii) Move along the unit resistance circle to the origin, record the reactance change and thus determine the value of series L or C.

d) For type 2 L-section:

   i) Move along the constant resistance circle until it intersects with the unit conductance circle. Record the reactance change and thus determine the value of series L or C.

   ii) Move along the unit conductance circle to the origin, record the susceptance change and thus determine the value of shunt L or C.

Stub matching is a technique used to match the impedance of a source to a load by using transmission line segments called stubs. The stubs are connected in parallel or series to the main transmission line and can be open-circuited or short-circuited. The key steps in designing a stub matching network are:

a) Find the normalized load impedance and construct an appropriate SWR circle.
b) Note that the SWR circle intersects the 1 + jx circle or 1 + jb at two points, all values read on the chart are normalized admittances.
c) Read the line normalized admittance in correspondence of the stub insertion locations determined in (d). These values will always be of the form

$$y(d_{stub}) = 1 + jb \text{ top half of chart}$$

$$y(d_{stub}) = 1 - jb \text{ bottom half of chart}$$

d) Select the input normalized admittance of the stubs, by taking the opposite of the corresponding imaginary part of the line admittance.
e) Use the chart to determine the length of the stub. The imaginary normalized admittance values are found on the circleof zero conductance on the chart.

3.2.3 Selection of Circuit Topology

There are a number of different methods and topologies that can be used to design low-noise amplifiers (LNA) for microwave imaging applications. Some of the most common methods and topology. This project is chosen to use a cascade topology to design a low noise amplifier. The configuration of transistors is connected in series by combining different stages with different gain and noise characterisrics. The key

components of cascade design are common source stage and common gate stage. The common source stage is typically a first stage a common source amplifier which operates the noise figure performance and the initial gain. For the common gate stage basically provides for improvement of noise performance as well as additional gain. The stages are designed to match the matching network in both port in order for the power transfer signal loss to be efficient. The cascade architecture is a common topology for LNA because it offers high gain amplification and minimizes noise figure performance due to having the combination of different stages. Figure 3.2 shows the cascaded stages design.

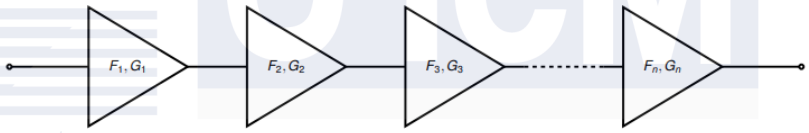


Figure 3.2 Cascade Stages

3.2.4 Selection of Transistor

An essential part of designing an LNA is choosing the right transistor. Every transistor has a minimum noise figure (NFmin) and maximum available gain (MAG) at a specific frequency. Therefore, it is not possible to construct an LNA that provides a gain more than the maximum available gain and a noise figure lower than the lowest NF. Common types of transistors used for LNA include Bipolar Junction Transistors (BJTs) and Field-effect Transistors (FETs). Among BJTs, the most commonly used are the Silicon Bipolar Junction Transistor (Si BJT) and the Pseudomorphic High Electron Mobility Transistor (pHEMT). FETs can be further divided into Junction Field-effect Transistors (JFETs) and Metal-Oxide-

Semiconductor Field-effect Transistors (MOSFETs). GaAs MESFETs and GaAs pHEMTs are commonly used FETs for high frequency and high performance LNA.

The choice of transistor for a particular LNA design will depend on the specific requirements of the application. The Pseudomorphic High Electron Mobility Transistor (pHEMT) technology is one well-known and extremely useful technology utilized in LNA. The pHEMT are semiconductor devices with outstanding low noise amplification performance characteristics because of its distinctive heterojunction structure, which allows for great carrier mobility. pHEMTs are a good choice for applications that demand high frequency performance and low noise figures and also are the recommended option for LNA because of their capacity to function at high frequencies and low noise levels. The GaAs pHEMT MGA-684P8 has featues in low noise figure, high linearity performance, low-cost small package size and excellent uniformity in product specifications. The application of this transistor can be used in various low noise amplifier applications such as for GSM, TDS-CDMA and CDMA.

The Silicon Bipolar Junction Transistor (Si BJT) has the ability to achieve low noise figures due to inherent properties of low noise, as well as can provide a high gain. The AT-42086 also from Avago Technologies is an example of Silicon Bipolar Junction Transistor (Si BJT) that been used for LNA due to have an optimum match. The applications of this transistor include use in LNA, gain stage, buffer, oscillator and mixer.

3.3 Transistor Amplifier Design

Stability, gain, noise, bandwidth, and dc needs are the most crucial design factors in a microwave transistor amplifier. The selection of the appropriate transistor and a

set of specifications typically precede a design. Acquiring the desired ac performance requires careful selection of the appropriate dc operating point and dc network structure.

3.3.1 Stability

A single power transistor can be used in LNA design to provide amplification at the required frequency and linearity. An unstable amplifier will cause the signal to oscillate instead of continuing, hence it is imperative that the amplifier remain steady with any passive termination. The amplifier's stability can be indices by using Rollet's Condition (K test) geometric stability factors (Mu or Mu Prime). In formula form, the set of unconditional stability is given below.

$$\boldsymbol{Stability\ factor, K = \frac{1-|S_{11}|^2-|S_{22}|^2+|\Delta|^2}{2|S_{12}S_{21}|} > 1} \quad (3.1)$$

$$|\Delta| = |\boldsymbol{S_{11}S_{22} - S_{12}S_{21}| < 1} \quad (3.2)$$

The stability factor (K) in an amplifier or called unconditional stability must be ensures greater than 1 and the delta factor (|Δ|) must be less than 1 because the matching network determines the load (Γ_L) and source (Γ_S), meaning the amplifier will be always be stable regardless of load and source impedances. This can be achieved in simulation by utilizing Advance Design System (ADS) technologies to meet the designation result.

3.3.2 Noise Figure

The important design considerations for a microwave amplifier are its noise figure. Noise can be passed into a microwave system from external sources or generated within the system itself. In receiver applications especially it is often

required to have a preamplifier with as low a noise figure as possible, the first stage of a receiver front end has the dominant effect on the noise performance of the overall system.

An alternative characterization is the noise figure of the component, which is a measure of the degradation in the signal-to-noise ratio between the input and output of the component. The signal-to-noise ratio is the ratio of desired signal power to undesired noise power, and so is dependent on the signal power. The noise figure, F, is a measure of this reduction in signal-to-noise ratio, and is defined as

$$\boldsymbol{F = \frac{S_i/N_i}{S_o/N_o} \geq 1} \qquad (3.3)$$

where the noise figure is defined as the ratio of the output noise power of the network to the input noise power of the network, expressed in decibels (dB) 1. The noise factor can be calculated using the following formula

$$\boldsymbol{NF = 10 \log F} \qquad (3.4)$$

The RF amplifier's noise performance is generally displayed by the noise figure, which also helps to identify signal change. The larger the noise figure, the more the signal is degraded. To select a suitable trade-off between noise figure and gain, which is used to check the input (Γ_{in}= Γ_{opt}) and output reflection coefficient (Γ_{out}) of the circuit, this can be accomplished by employing circles with constant gain and circles with constant noise figure. The transistor's noise figure can be computed using a number of characteristics provided by the manufacturer, including F_{min}, R_N, and Y_{opt} at the appropriate frequency, using the formula below.

$$\boldsymbol{F = F_{min} + \frac{R_N}{G_S}|Y_S - Y_{opt}|^2} \quad (3.5)$$

$$\boldsymbol{F = F_{min} + \frac{4R_n}{50}\frac{|\Gamma_S - \Gamma_{opt}|^2}{(1-|\Gamma_S|^2)|1+\Gamma_{opt}|^2}} \quad (3.6)$$

3.3.3 Gain

The power gain is represented by equation 3.7, which is the ratio of power delivered to the two-port network and power dissipated to the load. In addition, Equation 3.8 shows the power that is accessible when the network's ratio to the two-port network's power available indicates that the input and output match. Equation 3.9 also expresses the transducer gain, which is the power provided to the load divided by the power available from the source, as illustrated below:

(Power Gain) $\boldsymbol{G_P = \frac{P_L}{P_{in}} = \frac{1}{1-|\Gamma_{in}|^2}|S_{21}|^2\frac{1-|\Gamma_L|^2}{|1-S_{22}\Gamma_L{}^2}}$ (3.7)

(Available Power Gain) $\boldsymbol{G_A = \frac{P_{AVN}}{P_{AVS}} = \frac{1-|\Gamma_S|^2}{|1-S_{11}\Gamma_S{}^2}|S_{21}|^2\frac{1}{|1-\Gamma_{OUT}|^2}}$ (3.8)

(Transducer Gain) $\boldsymbol{G_T = \frac{P_L}{P_{AVS}} = \frac{1-|\Gamma_S|^2}{|1-S_{11}\Gamma_S{}^2}|S_{21}|^2\frac{1-|\Gamma_L|^2}{|1-\Gamma_{OUT}\Gamma_L|^2}}$ (3.9)

For the AC analysis for LNA design is derived after transient analysis. The primary design criterion for the LNA was the input value of the DC biasing voltage in order to obtain the required parameters gain. The gain of the amplifier that is picked up by the antenna can be used to minimize noise once a high gain has been reached. The expression to get the LNA design's benefit can be used as below:

$$\boldsymbol{Gain: 20\log\frac{V_{out}}{V_{in}}} \quad (3.10)$$

3.4 Low Noise Amplifier Block diagram

The LNA structure usually consists of two stages: an input stage and an output stage. The input stage is designed to have a low noise figure, which is the ratio of the signal-to-noise level of the amplifier, and a high gain, which is the ratio of the output to the input. The output stage is designed to have a low output impedance matching. Figure 3.3 shows block diagram of LNA.

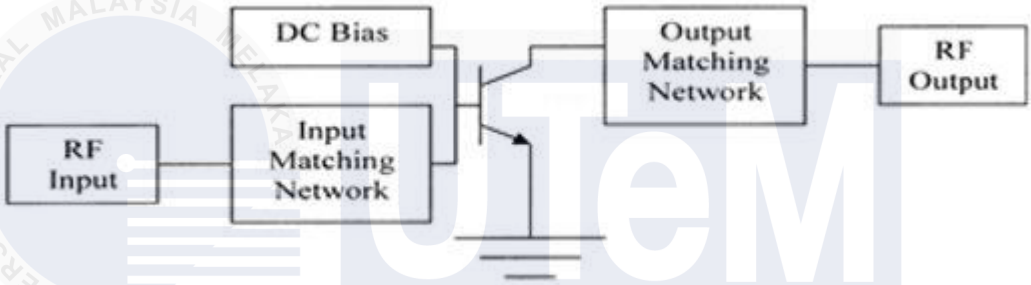


Figure 3.3: Block Diagram of Low Noise Amplifier

The key components of a Low-Noise Amplifier (LNA) are shown in the block diagram below:

a. Input Matching Network: The input matching network is responsible for impedance matching between the LNA and the signal source, such as an antenna. It ensures maximum power transfer and minimizes signal reflections.
b. Active Device: The active device, usually a transistor such as a BJT, FET, HEMT, or CMOS device, forms the core of the LNA. It provides amplification and low-noise performance.
c. Biasing Circuit: The biasing circuit establishes the appropriate operating conditions for the active device, ensuring it remains within its linear

operating range. It sets the DC voltages and currents needed for optimal performance.

d. Gain Control: In some LNAs, a gain control block may be included to adjust the gain of the amplifier. This can be achieved through variable biasing or gain control circuitry.

e. Output Matching Network: The output matching network matches the impedance between the LNA and the load, such as a downstream amplifier or receiver. It optimizes power transfer and minimizes signal reflections.

f. DC Blocking Capacitors: DC blocking capacitors are often included at the input and output of the LNA to prevent any DC bias from affecting the input source and load, respectively.

g. Power Supply: The LNA requires a power supply to provide the necessary DC voltage and current for operation.

3.5 Reflection Coefficient of Source and Load

For the LNA, a lumped and stub element matching is performed in both of input and output matching network to make an analysis between two different matching technique. The design applied to transistor MGA-684P8 and AT-42086. The calculation will be done by focusing at only 1.5 GHz.

$$B_1 = 1 + |S_{11}|^2 - |S_{22}|^2 - |\Delta|^2 \quad (3.11)$$

$$B_2 = 1 + |S_{22}|^2 - |S_{11}|^2 - |\Delta|^2 \quad (3.12)$$

$$C_1 = S_{11} - \Delta S_{22}^{*} \quad (3.13)$$

$$C_2 = S_{22} - \Delta S_{11}^{*} \quad (3.14)$$

Based on the above equation, the reflection coefficient of source and load can be substitute into those equations,

$$\Gamma_{MS} = \frac{B_1 \pm \sqrt{B_1{}^2 - 4|C_1|^2}}{2C_1} \quad (3.15)$$

$$\Gamma_{ML} = \frac{B_2 \pm \sqrt{B_2{}^2 - 4|C_2|^2}}{2C_2} \quad (3.16)$$

3.6 S-parameter Simulation

The simulation result is performed to find the noise figure, gain and stability in ADS software to compared to the results of calculation that has been done. The first process to design is by adding S-parameter in ASCII text files to create a S2P file.

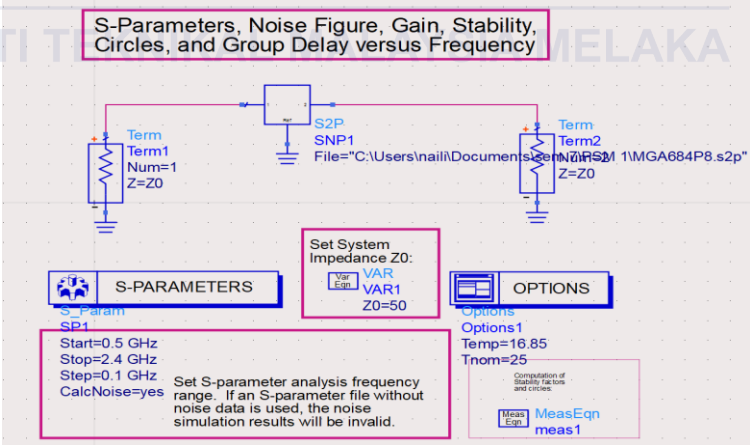


Figure 3.4: S-Parameter simulation circuit

3.7 Circuit Topologies

Circuit topologies is basically referred to various configurations and arrangements of elements such as resistors, capacitors dan inductors. Understanding circuit topologies is crucial for analyzing and designing the circuit. In the case of this project, the single stage and cascade circuit is designed to simulate LNA.

3.7.1 Single Stage

Below a figures of single stage circuit in different matching techniques (L-matching and stub matching) using different transistors (MGA-684P8) and (AT-42086).

For the L-matching network both input and output matching network are made of capacitors and inductors respectively, the value calculated analytically using the smith chart in ADS software. By inserting the value of reflection coefficient at source and load that calculate analytically, the L-matching can be generate automatically using auto element that provide in ADS software. The design of single stage LNA also include an input and output matching with DC biasing. Figure 3.4(a) shows the first stage of MGA-684P8 using L-matching.

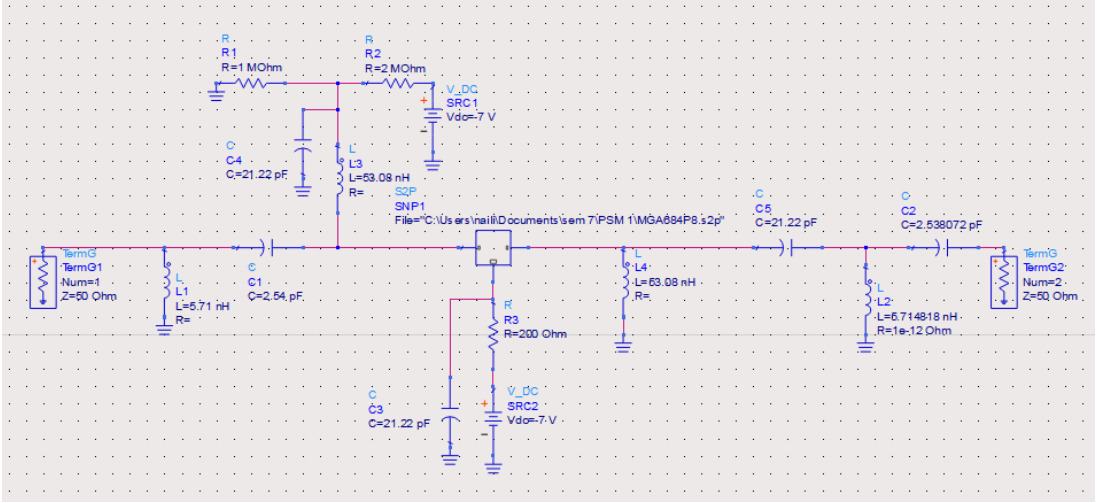


Figure 3.5 (a): Single Stage Circuit of MGA-684P8 using L-Matching

The figure 3.5(a) and (b) will do a comparison after design is completing done connecting respectively. The comparison is made between different transistor but same in matching technique and topology. Figure 3.5 (b) single stage circuit of AT-42068 using L-Matching.

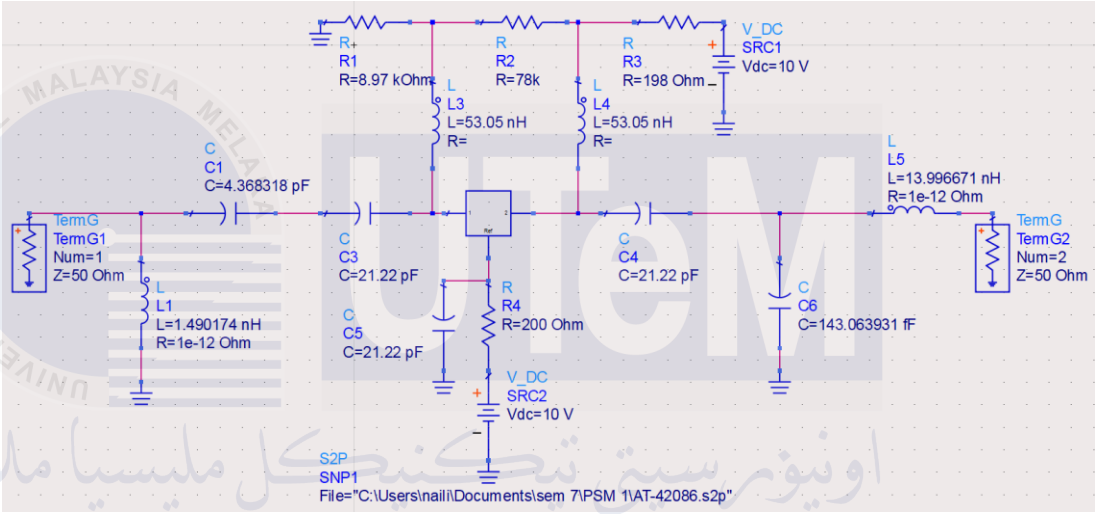


Figure 3.5 (b): Single Stage Circuit of AT-42068 using L-Matching

Stub matching is another technique that using a same process using smith chart in ADS software. By inserting the value of reflection coefficient that calculate analytically, the components like transmission line and open stub are used to design the smith chart in ADS. Figure 3.5 (d) and (e) shows single stage circuit of MGA-684P8 and AT-42086 using Stub Matching respectively.

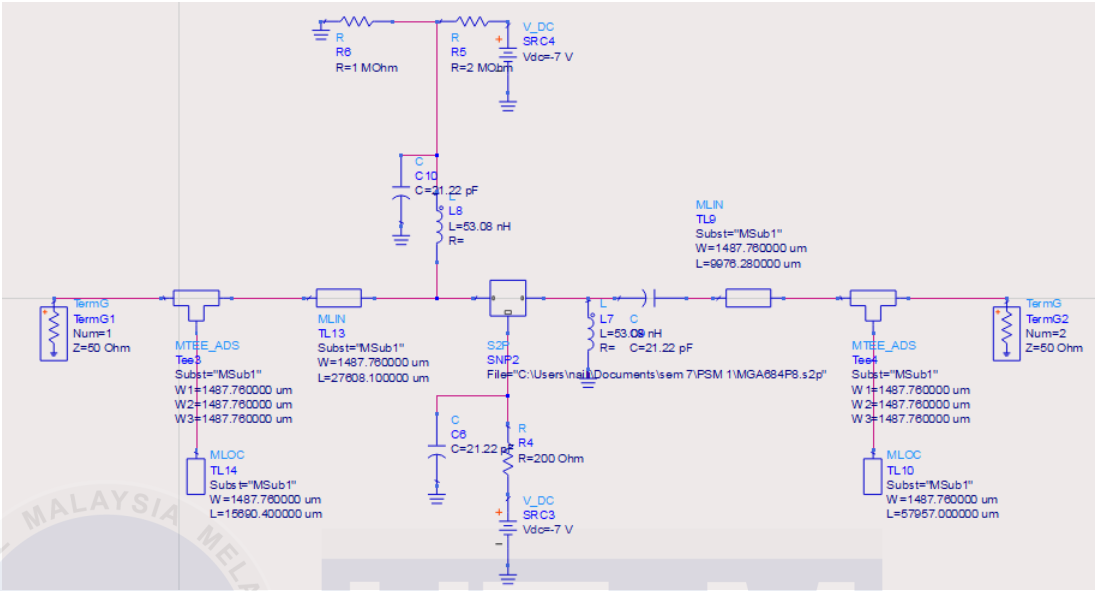


Figure 3.5 (d): Single Stage Circuit of MGA-684P8 using Stub Matching

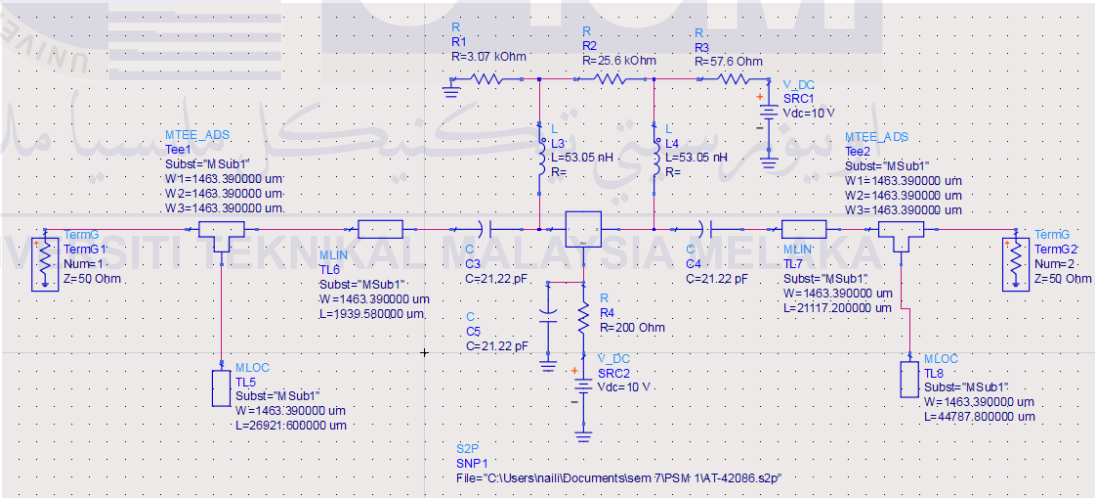


Figure 3.5 (e): Single Stage Circuit of AT-42068 using Stub Matching

3.7.2 Cascaded Circuit

The cascaded circuit is designed to optimize a better gain. Noise figure is less important in this stage. Both the input and output of this stage are conjugate matched to the active device. The second stage input and output match are same and all the values of the components are also the same with single stage. In this design, the

cascade in two stage of LNA is designed. The cascaded circuit shows a different design of circuit in different matching and transistors.

As seen in figure below, the two-stage of L-matching are connecting serially with 2-port transistor. The single stage of transistor is connected serially with second transistor without ignoring the single component of input and output matching network or DC biasing. Figure 3.5 (a) and (b) shows cascaded circuit of different transistor (MGA-684P8) and (AT-42086) with same L-matching technique.

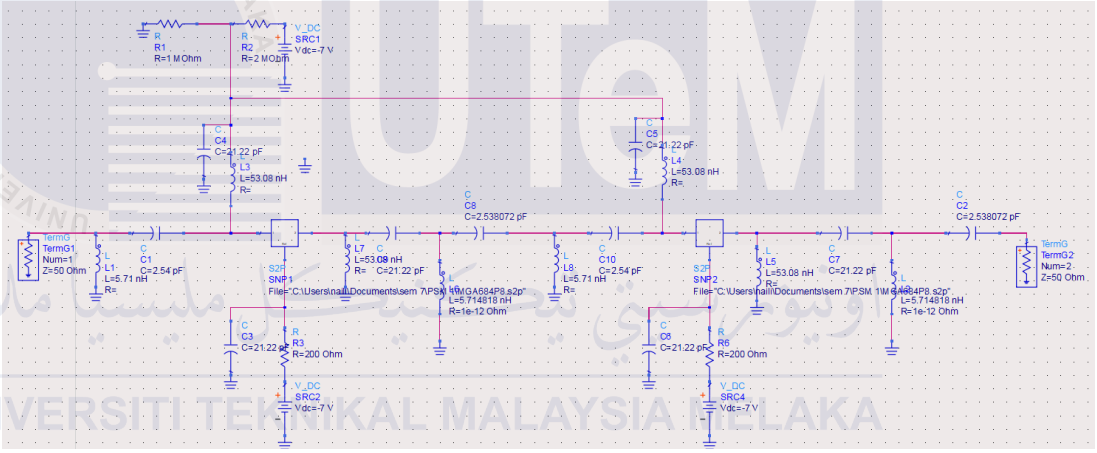


Figure 3.6 (a): Cascaded Circuit of MGA-684P8 using L-Matching

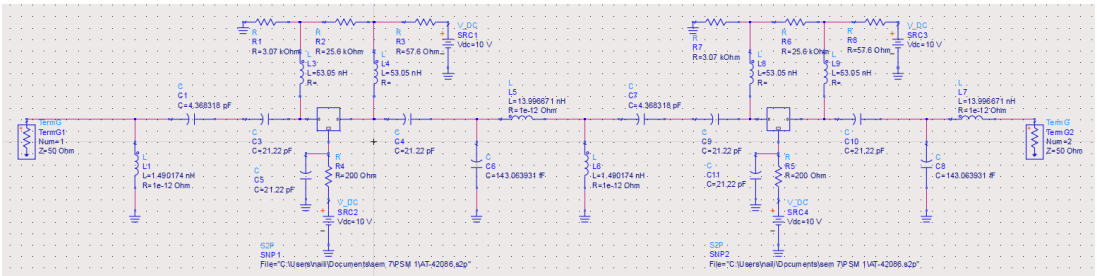


Figure 3.6 (b): Cascaded Circuit of AT-42068 using L-Matching

As same as L-Matching technique, the stub matching is connecting serially to each single stage to single stage without neglect input and output matching in each

stage and DC biasing. Figure 3.5 (c) and (d) shows cascaded circuit of different transistor (MGA-684P8) and (AT-42086) using stub matching.

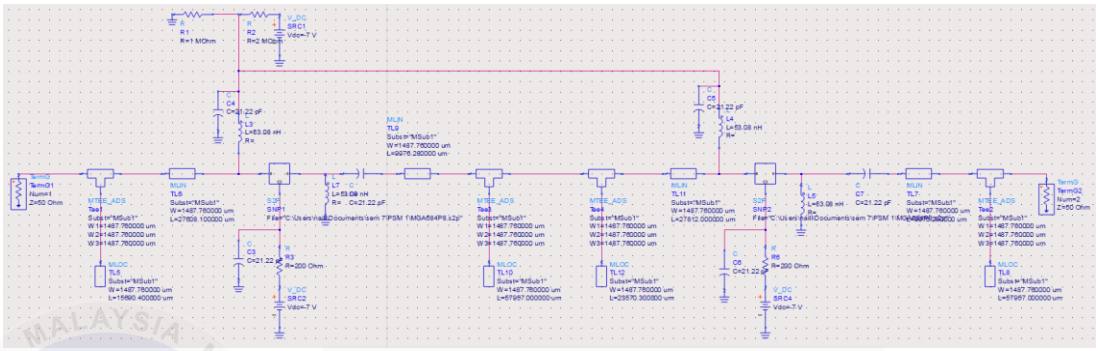


Figure 3.6 (c): Cascaded Circuit of MGA-684P8 using Stub Matching

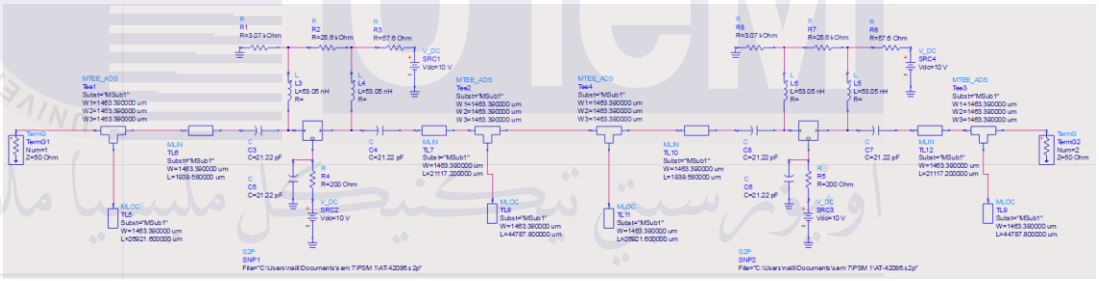


Figure 3.6 (d): Cascaded Circuit of AT-42068 using Stub Matching

CHAPTER 4

RESULTS AND DISCUSSION

In this chapter, Advance Design System (ADS) was used as a main work process to design a LNA simulation. The ADS software will show all the simulation results that get from the S-parameter of transistor such as stability, noise figure and gain.

The main component in order to simulate design LNA for Microwave Breast Cancer Imaging application is to about noise figure and gain. The result that shown in simulation and optimization of LNA design was compared to find the best results.

4.1 Transistor Selection

In designing the LNA, the first step to consider in process to design was by finding the stability of transistor. Stability is an important part of the transistor selection to get the analysis in unconditionally stable. If the transistor stability is too

low when choosing specific DC bias point and frequency, another transistor testing needs to be considered and seen. The calculation for noise figure and gain can be done after transistor device testing is passed in stability condition. Thus, the S-parameter in transistor's datasheet can be helping to calculate the next calculation part in LNA.

For initial testing, the MGA-684P8 and AT-42086 have been selected to design an LNA. This transistors have lot of features, for instance in low noise figure, high linearity performance and using GaAs E-pHEMT technology (MGA-684P8) and NPN bipolar transistor that utilizes Silicon (Si) technology (AT-42086).

Table 4.1: S-parameter in 1.5 GHz frequency

Transistor	MGA-684P8	AT-42086
S_{11}	0.33∠ -101.54	0.61∠ 154
S_{12}	0.02∠57.72	0.057∠64
S_{21}	8.67∠70.27	4.48∠62
S_{22}	0.33∠ -51.61	0.31∠ -31

4.1.1 Unilateral Figure of Merit

Unilateral figure of merit is performed to assuming S_{12} equal to zero when S_{12} is in bilateral case, if $S_{12} = 0$ the procedure to design is much simpler.

The equation of unilateral figure of merit (U) is known as

$$U = \frac{|S_{12}||S_{21}||S_{11}||S_{22}|}{(1-|S_{11}|^2)(1-|S_{22}|^2)} \quad (4.1.1)$$

The lower and upper ranges is introduced when using G_{TU} is bounded by

$$\frac{1}{(1+U)^2} < \frac{G_T}{G_{TU}} < \frac{1}{(1-U)^2} \quad (4.1.2)$$

From the above equation, the S-Parameter of MGA-684P4 and AT-42086 can be substituted into (4.1.1). Thus, can determine error ranges using (4.1.2).

For MGA-684P4,

$$U = \frac{|0.02||8.67||0.33||0.33|}{(1-|0.33|^2)(1-|0.33|^2)}$$

$$= 0.0238$$

$$\frac{1}{(1+0.0238)^2} < \frac{G_T}{G_{TU}} < \frac{1}{(1-0.0238)^2}$$

or in decibels,

$$-0.2045 < \frac{G_T}{G_{TU}} < 0.2078$$

For AT-42086,

$$U = \frac{|0.057||4.48||0.61||0.31|}{(1-|0.61|^2)(1-|0.31|^2)}$$

$$= 0.085$$

$$\frac{1}{(1+0.085)^2} < \frac{G_T}{G_{TU}} < \frac{1}{(1-0.085)^2}$$

or in decibels,

$$-0.7086 < \frac{G_T}{G_{TU}} < 0.7716$$

The error of both transistor is small enough to justify the unilateral assumption. A value can be considered high if the unilateral figure of merit (U) is greater than 0.1. Therefore, the error in this method can be more than 1dB.

4.1.2 Calculation of Parameter

This calculation shows the initial results for gain, noise figure and stability on 1.5 GHz with reference in S-parameter datasheet between MGA-684P8 and AT-42086.

For MGA-684P8,

a) Gain

$$G_{TU,max} = \frac{1}{1-|S_{11}|^2}|S_{21}|^2\frac{1}{1-|S_{22}|^2}$$

= 18.89 dB

b) Noise Figure

$$NF = F_{min} + \frac{4R_n}{Z_0}\frac{|\Gamma_s - \Gamma_{opt}|^2}{(|1+\Gamma_{opt}|^2)(|1-\Gamma_s|^2)}$$

= 0.39 dB

c) Stability

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|}$$

= 2.36>1

For AT-42086,

a) Gain

$$G_{TU,max} = \frac{1}{1-|S_{11}|^2}|S_{21}|^2\frac{1}{1-|S_{22}|^2}$$

= 13.57 dB

b) Noise Figure

$$NF = F_{min} + \frac{4R_n}{Z_0}\frac{|\Gamma_s - \Gamma_{opt}|^2}{(|1+\Gamma_{opt}|^2)(|1-\Gamma_s|^2)}$$

= 0 dB

c) Stability

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|}$$

=1.05>1

Table 4.2: Comparison of Calculation Results of 1.5 GHz from different transistors

Parameter	MGA-684P8	AT-42086
Transducer Power Gain, G_T	18.89 dB	13.57 dB

Noise Figure, NF	0.39 dB	0 dB
Stability, K	2.36	1.05

Based on the above results, the performance of the MGA-684P8 and AT-42086 transistor at 1.5 GHz are compared for the analysis of different technology. The MGA-684P8 transistor has a better performance than AT-42086 in terms of gain (18.89 dB vs. 13.57 dB). Meanwhile in noise figure's parameter AT-42086 transistor has overcome MGA-684P8 transistor (0 dB vs. 0.39 dB). In terms of stability, both of transistor exhibits unconditional stability at 1.5 GHz with K>1.

4.1.3 Simulation of Transistor

Using ADS software, the value of stability is described in figure 4.1(a) and (b) shows the simulation result for two different transistors based on 1.5 GHz. The result's simulation of stability for MGA-684P8 and AT-42086 is shown below.

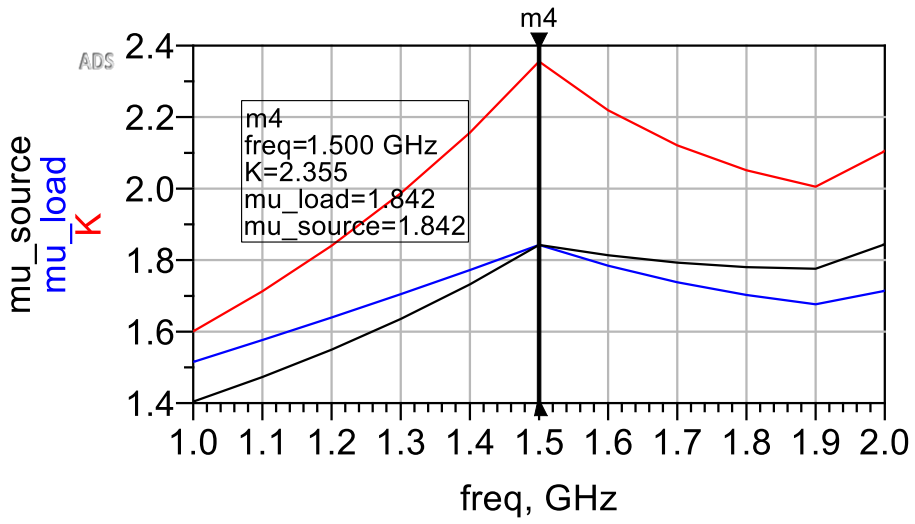


Figure 4.1 (a): Stability of MGA-684P8

MGA-684P8 has a stability of 2.355 which means unconditionally stable over a wider range of input and output impedances and operating frequencies. Hence, the design and matching of amplifier is easier to perform without risk oscillations.

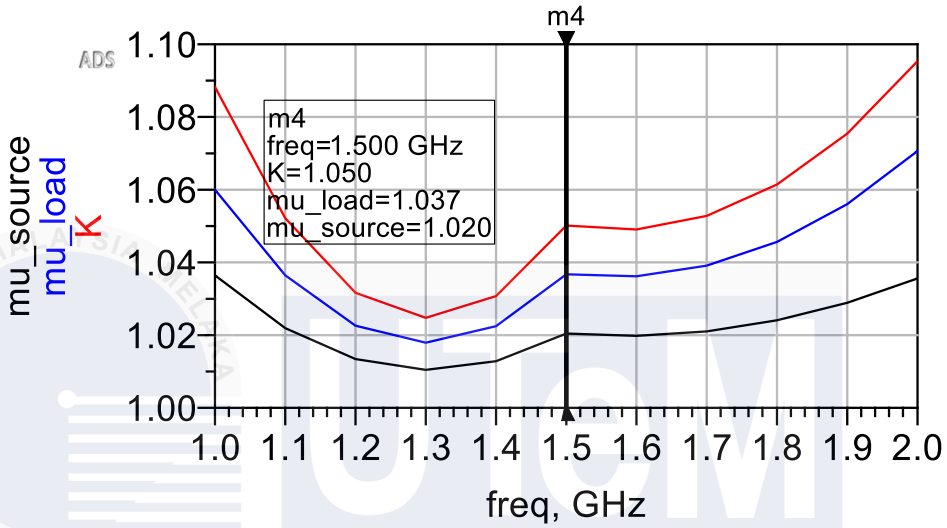


Figure 4.1 (b): Stability of AT-42086

The stability of AT-42086 has a stability of only 1.05 which shows lower than MGA-684P8 transistor (2.355). It is potentially prone to oscillate if impedances are not carefully matched. Even though the value is nearly to 1 in stability factor, the stability of AT-42086 still indicates unconditionally stable condition.

4.2 DC Bias

Biasing is a first step in the design of amplifier to ensure the transistor meets specification design requirements in order for the transistor operates in active or linear region. The stability of Q-Point is crucial for transistor to DC biased at a suitable middle point.

4.2.1 Graphical Analysis

The value can be calculated from the graph below by using bias point provided in datasheet. The DC biasing design for different type of transistor has been analysis respectively. In the case of Field Emitter Transistor (FET), Q-point is chosen on ID-VDS curve, while in a case of the bipolar junction transistor (BJT), Q-point is chosen on IC-VCE curve. Figure 4.2 shows an I-V curves's graph.

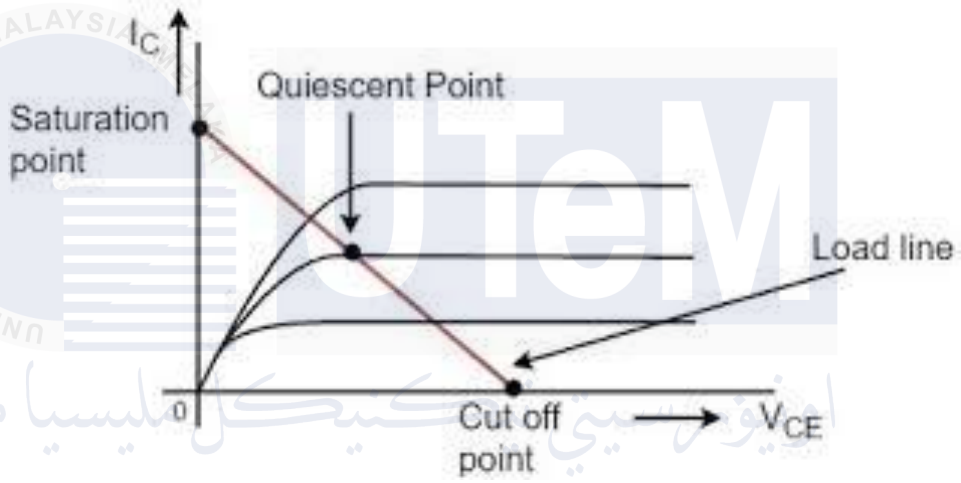


Figure 4.2: I-V curves

For MGA-684P8, the given I_{DS} is 35 mA meanwhile V_{DS} is 5 V, using the given Q-point we can see that the value of V_{GS} is determined to be -0.89 V graphically. From this graph the value of I_{DSS} is 150mA when I_{DSS} = 0 and V_T is = -0.5 V when V_T = 0. Figure 4.3 shows a graph of V_{GS}.

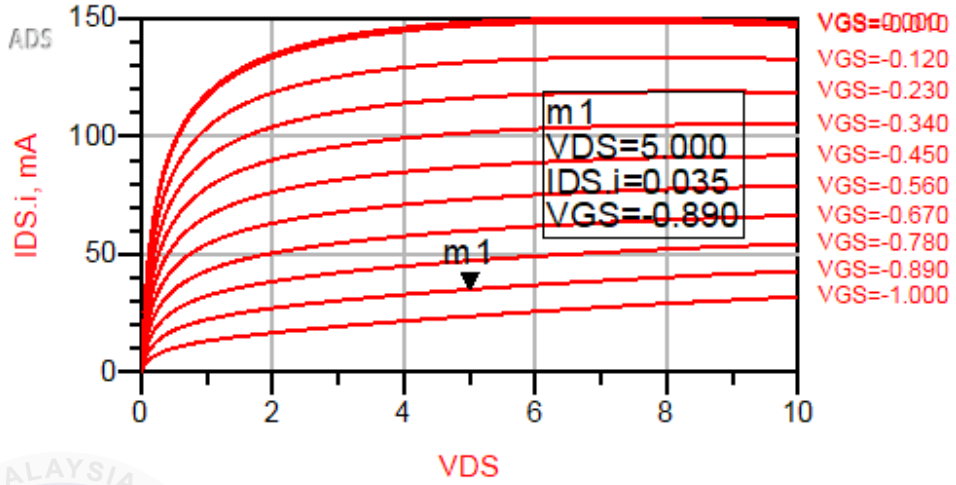


Figure 4.3: V_{GS} graph

The AT-42086 is applied passive bias in order to construct a single stage and cascaded LNA. The components that passive bias use is resistors, conductors and inductors which is connected to the gate (G) drain (D) and source (S). The given I_c is 35 mA and V_{CE} is 8 V. By using the Q-point, V_{BE} is determined to be 0.857 V meanwhile for I_{BB}. The beta of BJT transistor is decided to state 160. Figure 4.4 (a) and (b) shows V_{BE} graph and I_{BB} graph respectively.

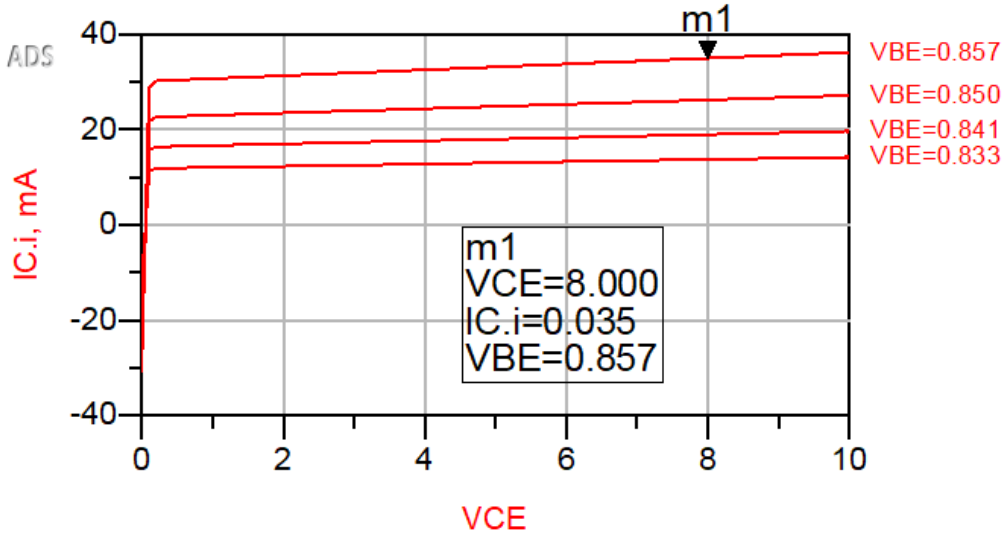


Figure 4.4 (a): V_{BE} graph

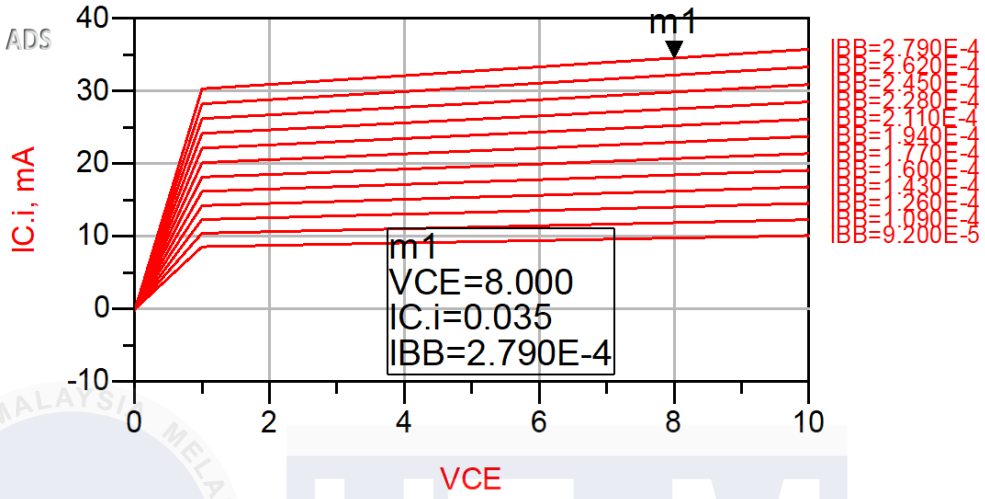


Figure 4.4 (b): I_{BB} graph

4.2.2 Analytical Analysis

The given value from the datasheet of MGA-684P8 is I_{DS} = 35 mA and V_{DS} = 5 V meanwhile V_{GS} is -0.89 V from figure 4.5.

Assuming V_{GG} = -7V

The resistance R_1 and R_2 are calculated as $\left(\frac{R_2}{R_1+R_2}\right)$.

Solving above equations, $R_1 = 2R_2$

Assume $R_1 = 1\ M\Omega, R_2 = \ 2M\Omega$, R_S = 200 Ω

For calculating the RFC choke, assuming Z_L should be ten times greater than the value of Z_0.

$$Z_L = j\omega L$$

Therefore, L = 53.08 nH

Meanwhile the DC-Block capacitor value can be justified when Z_C is 1/10 times of Z_0.

$$Z_C = \frac{1}{j\omega C}$$

Thus, C = 21.22 pF

The biasing circuit of FET is shown below in figure 4.5(a)

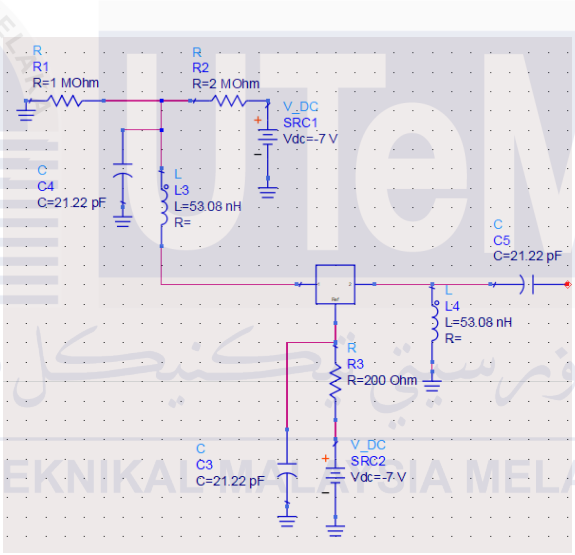


Figure 4.5 (a): DC biasing of MGA-628P8

For the transistor AT-42086,

$$R_1 = \frac{V_{BE}}{I_{BB}} = 3.07\ k\Omega$$

$$R_2 = \frac{V_{CE} - V_{BE}}{I_{BB}} = 25.6\ k\Omega$$

$$R_3 = \frac{V_{CC} - V_{CE}}{I_C - I_{BB}} = 57.6\ \Omega$$

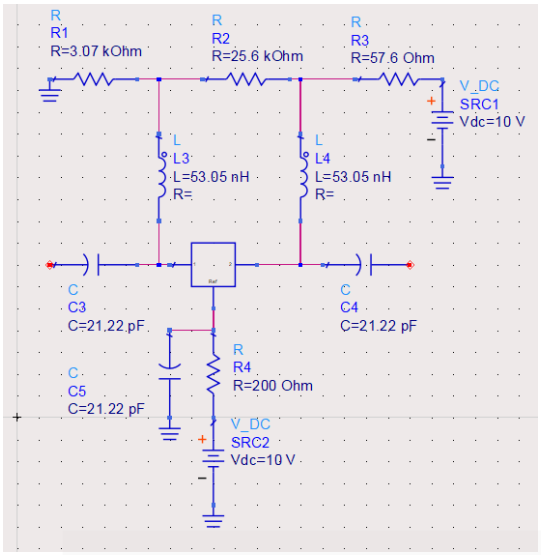


Figure 4.5 (b): DC biasing of AT-42086

4.3 Input and Output Matching Network

For the LNA, a lumped and stub element matching is performed in both of input and output matching network to make an analysis between two different matching technique. The design applied to transistor MGA-684P8 and AT-42086. The calculation will be done by focusing at only 1.5 GHz.

4.3.1 L-matching

The smith chart for L-matching is performed by using ADS simulation. The smith chart of MGA-684P4 is obtained by inserting the value of reflection coefficient at source and load.

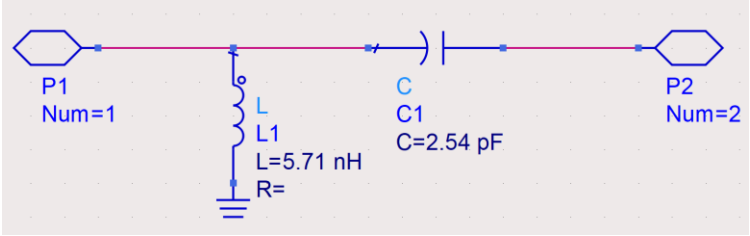


Figure 4.6 (a) : Input matching of L-matching for MGA-684P8

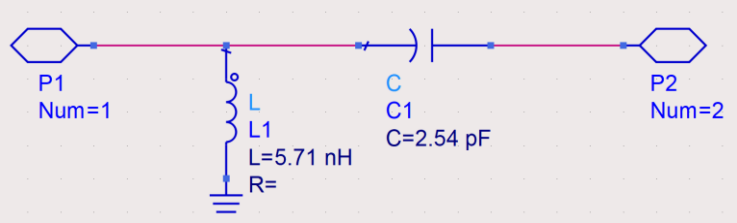


Figure 4.6 (b) : Output matching of L-matching for MGA-684P8

Meanwhile for AT-42086,

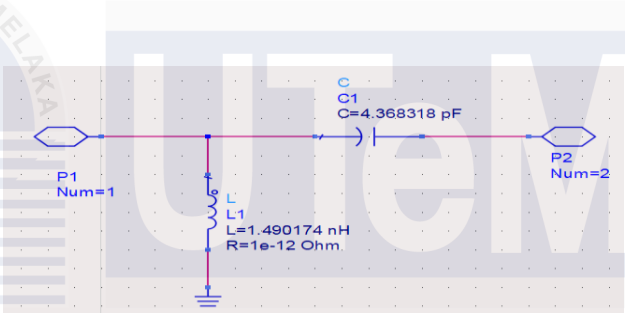


Figure 4.7 (a): Input matching of L-matching for AT-42086

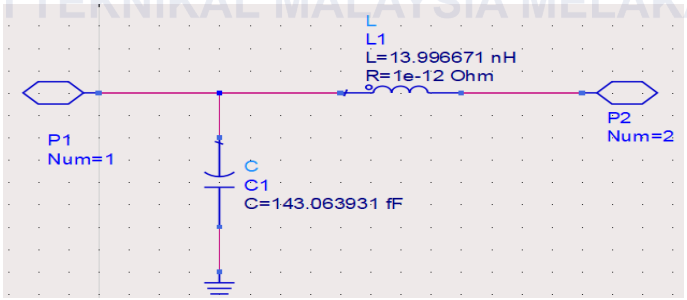


Figure 4.7 (b): Output matching of L-matching for AT-42086

4.3.2 Stub matching

For MGA-684P8

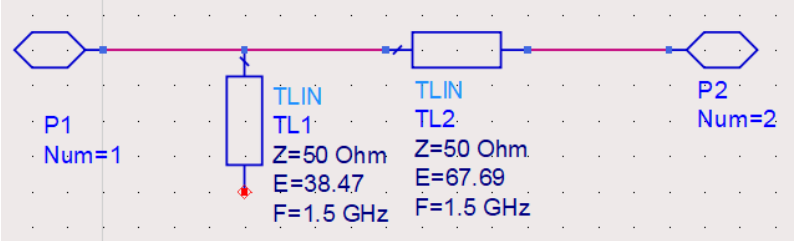


Figure 4.8 (a) : Input Matching of Stub matching for MGA-684P8

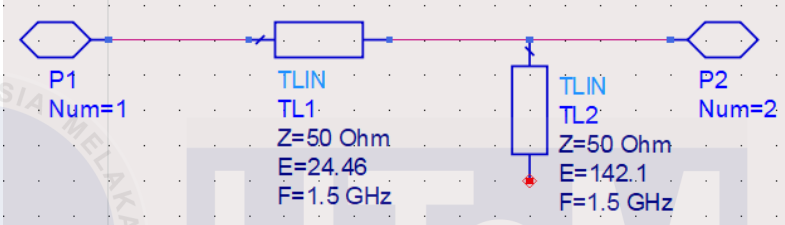


Figure 4.8 (b): Output Matching of Stub matching for MGA-684P8

For AT-42086

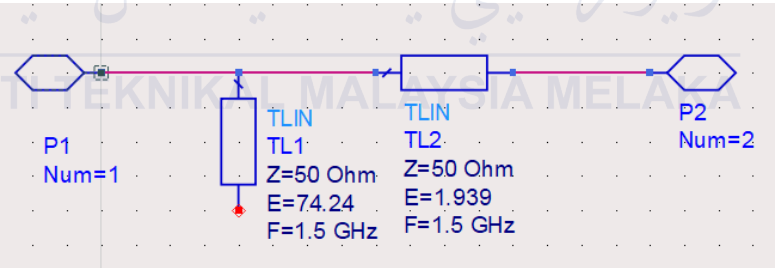


Figure 4.9 (a): Input Matching of Stub Matching for AT-42086

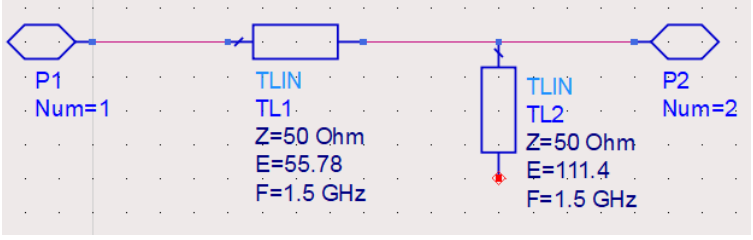


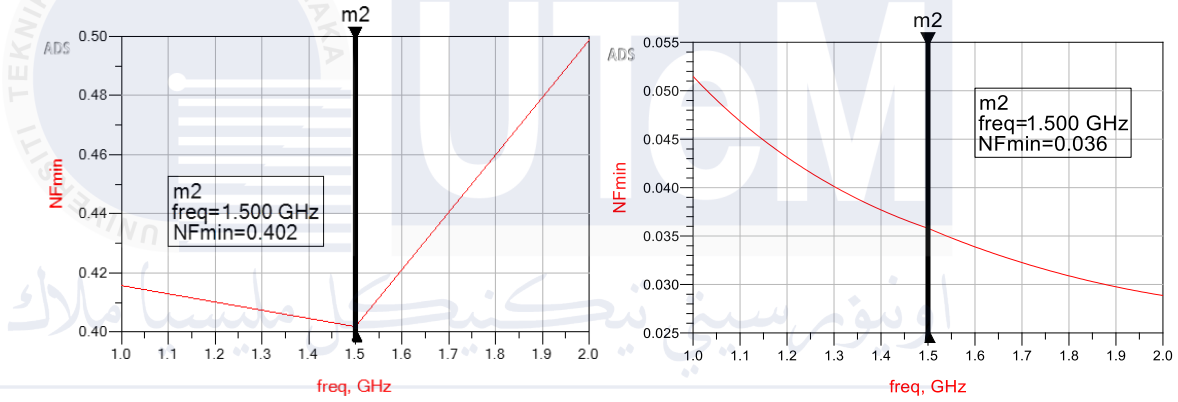
Figure 4.9 (b): Output Matching of Stub Matching for AT-42086

4.4 Simulation of Circuit Topologies

The simulation of circuit topologies has been investigate using comparison between single stage and cascaded circuit. Each of the design circuit have different matching techniques that been applied to make an analysis.

4.4.1 Single Stage Simulation

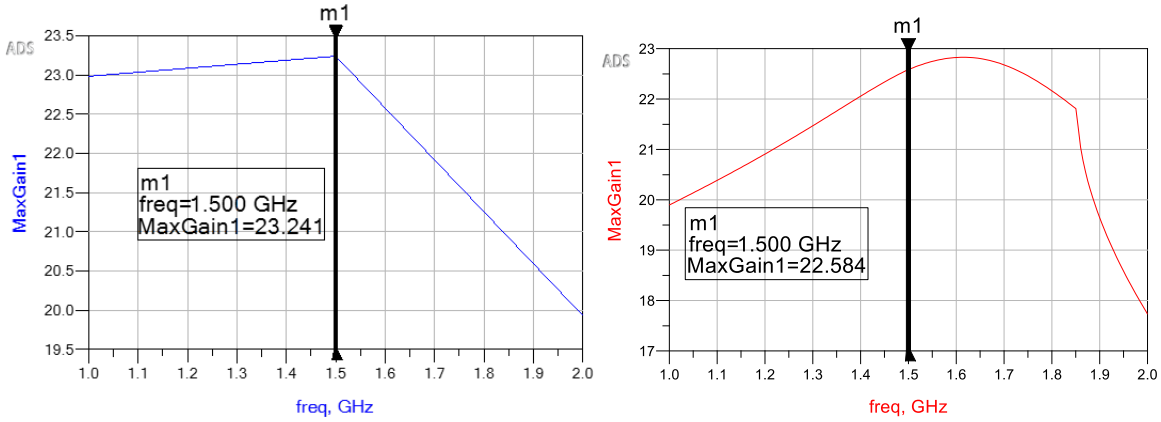
Comparison graph of different transistor between MGA-684P8 and AT-42086 using different matching techniques.



MGA-684P8 AT-42086

Figure 4.10 (a): Noise Figure in L-Matching

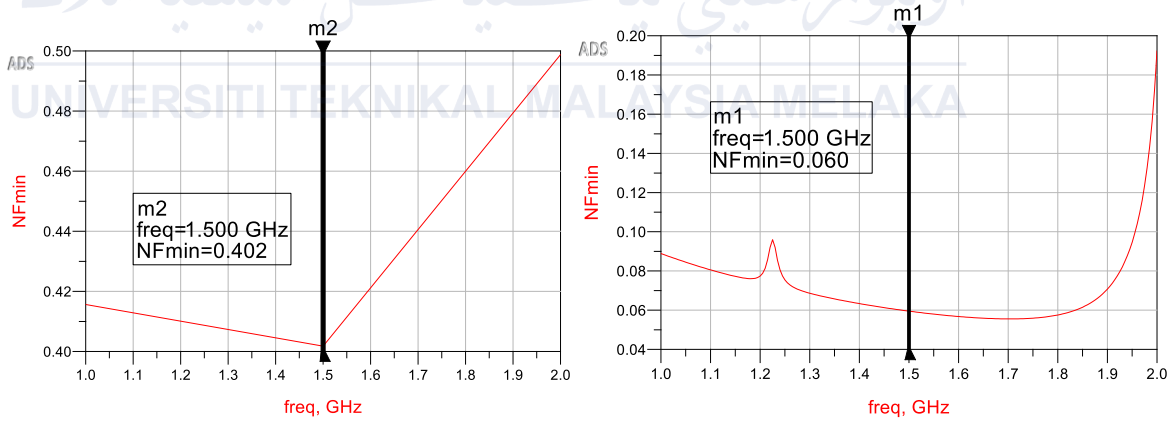
The simulation results in figure 4.12 have shown that noise figure of AT-42086 is lower than MGA-684P8 transistor. The noise figure at single stage using L-matching of AT-42086 is shows 0.036 dB meanwhile for MGA-684P8 is 0.402 dB.



MGA-684P8 AT-42086

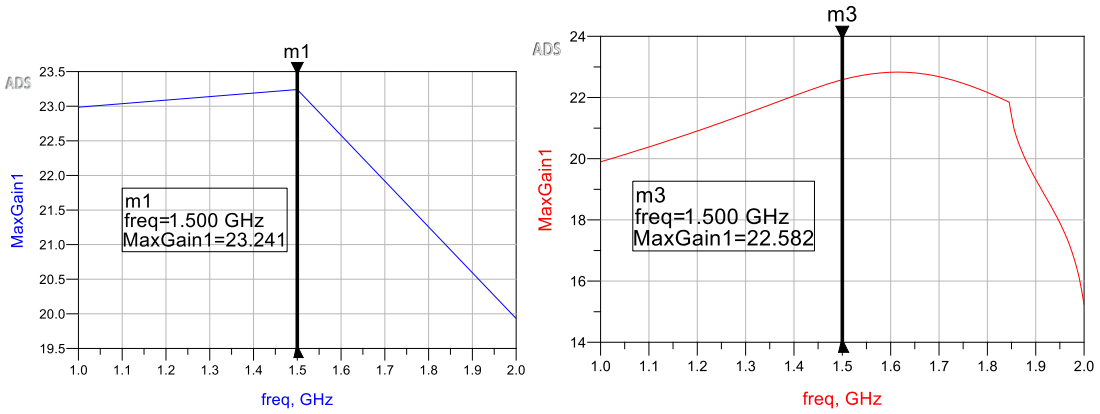
Figure 4.10(b): Gain in L-Matching

Value of gain shows the MGA-684P8 is 23.24 dB slightly more than AT-42086 transistor which 22.58 dB so that both of transistor achieved the specification in single stage using L-Matching.



MGA-684P8 AT-42086

Figure 4.10(c): Noise Figure in Stub Matching



MGA-468P8 AT-42086

Figure 4.10(d): Gain of in Stub Matching

The figure 4.10(d) AT-42086 based on 1.5 GHz made a value of noise figure at 0.06 dB compared to MGA-684P8 that have slightly bigger noise figure. Besides, the gain of both transistors has a little different in value. As in the graph, the MGA-684P8 made a 23.23 dB while AT-42086 is 22.58 dB.

Table 4.3: Simulation Result of MGA-468P8 and AT-42086 in Single Stage using Different Matching Technique

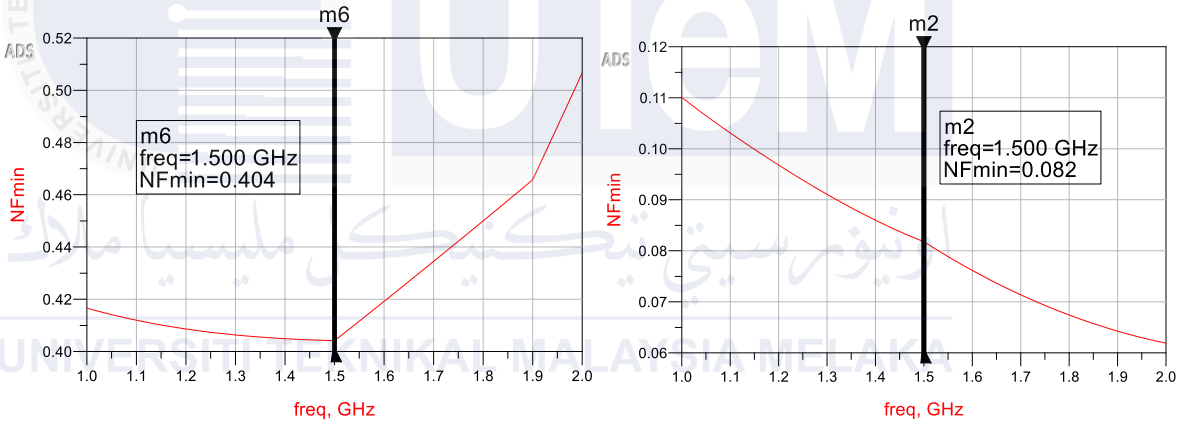
TRANSISTOR	MGA-684P8		AT-42086	
Matching Network	L-matching	Stub	L-matching	Stub
Noise Figure	0.402 dB	0.405 dB	0.036 dB	0.06 dB
Gain	23.56 dB	23.24 dB	22.584 dB	22.582 dB

From the different transistors, the calculation and simulation are already shown that the comparison with gain and noise figure. The result of MGA-684P8 and AT-42086 transistor have a meet the requirments for specification LNA design.

Transistor AT-42086 achieved lower noise figure 0.036 dB (L-matching) and 0.06 dB (stub) compared to MGA-684P8 get the value 0.402 dB (L-matching) and 0.405 dB (stub). However, the results for the gain show both transistor meet specifications above 20 dB by using different matching technique.

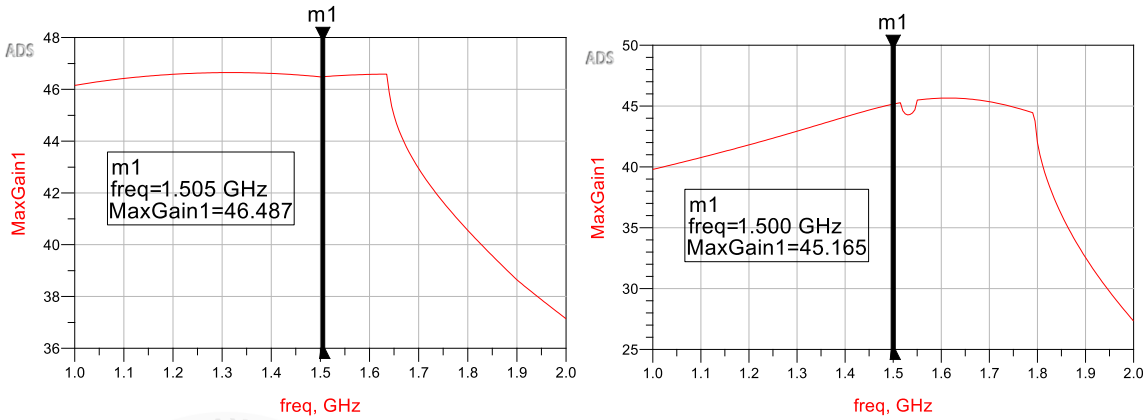
4.4.2 Cascade Simulation

The overall simulation result of cascading the two-stage amplifier using transistor MGA-684P8 and AT-42086 and using different matching (L and stub). Figure 4.? Shows noise figure in cascade using L-matching.



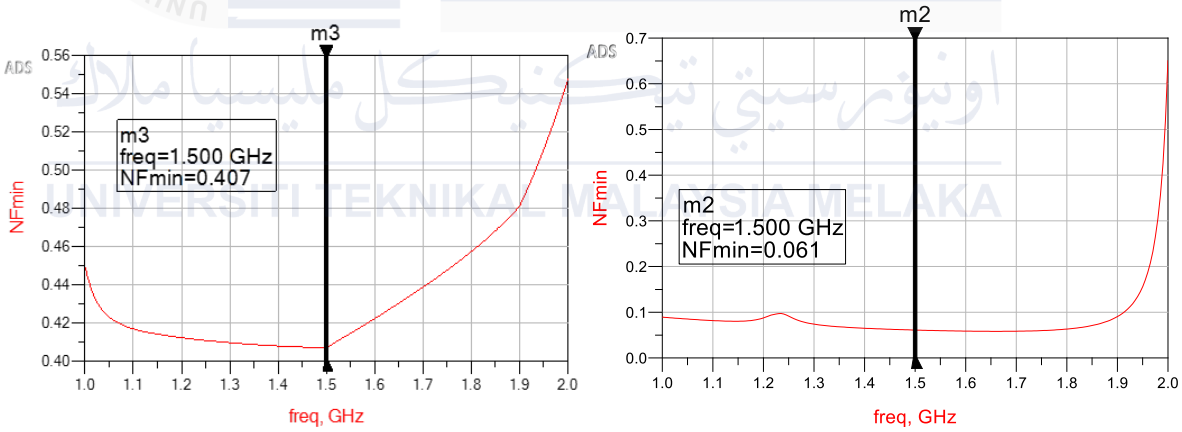
MGA-468P8 AT-42086

Figure 4.11(a): Noise Figure in Cascade using L-Matching



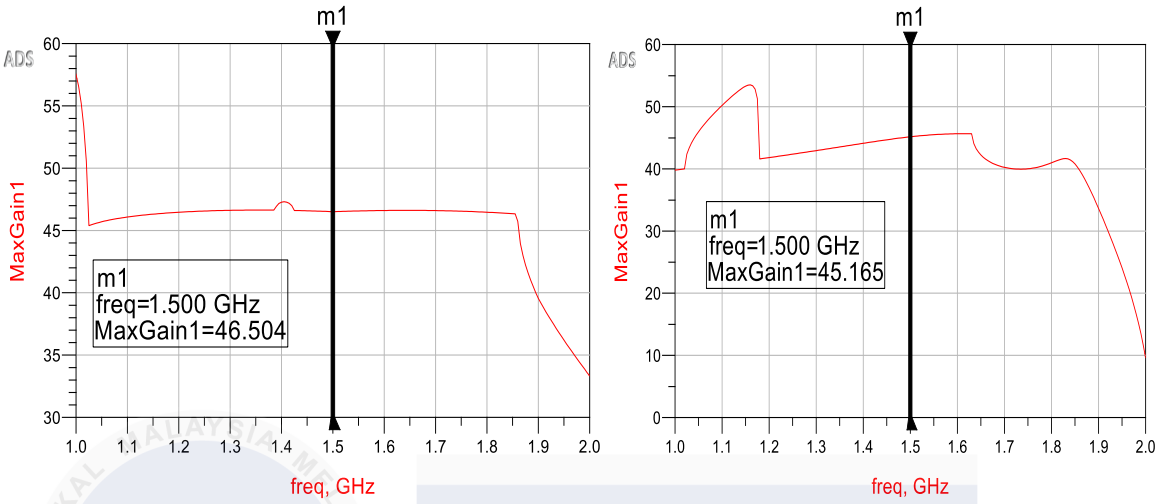
MGA-468P8 AT-42086

Figure 4.11(b): Gain in Cascade using L-Matching



MGA-468P8 AT-42086

Figure 4.11(c): Noise Figure in Cascade using Stub Matching



MGA-468P8 AT-42086

Figure 4.11(d): Gain of AT-42086 in Cascade using Stub Matching

Table 4.4: Simulation Result of MGA-468P8 and AT-42086 in Cascaded using Different Matching Technique

Transistor	MGA-684P8		AT-42086	
Matching Network	L-Matching	Stub	L-Matching	Stub
Noise Figure	0.614 dB	0.407 dB	0.082 dB	0.061 dB
Gain	46.481 dB	46.504 dB	45.165 dB	45.165 dB

The design of cascade circuit is connected in two stages. As shown in table 4.5, the result for parameter of noise figure is achieved to target specification because we focused for minimum noise figure which is less than 2dB. So, noise figure for MGA-684P8 is 0.614 dB (L-matching) and 0.407 dB (stub) but for AT-42086 is 0.082 dB (L-matching) and 0.061 dB (stub). Besides that, the gain has proven additional gain value. It shows the gain increase two times of dB (above 40 dB) compared to single stage which is above than 20 dB.

4.5 Project Significant

This project is simulation-based work and does not involve hardware and chemical elements thus the impact on sustainability and environmental aspects is minimal. The sustainability design goals that involved in this project are listed below.

a) SDG 3: Good Health and Well-being

Microwave breast cancer imaging aims to contribute to early and accurate detection of breast cancer, promoting good health by enabling early intervention and treatment for all at all ages.

b) SDG 5: Gender Equality

Breast cancer predominantly affects women, and early detection through technologies like microwave imaging contributes to gender equality by improving healthcare outcomes for women.

c) SDG 9: Industry, Innovation and Infrastructure

The development and use of low noise amplifiers in microwave breast cancer imaging contribute to technological innovation in the healthcare sector, supporting the goal of sustainable infrastructure for healthcare.

d) SDG 10: Reduced Inequality

Access to advanced medical technologies, such as microwave breast cancer imaging, can contribute to reducing health inequalities by providing more accurate

and accessible diagnostic tools, benefiting all individuals, regardless of their socio-economic status.

e) SDG 11: Sustainable Cities and Communities

The application of medical technologies like microwave breast cancer imaging can improve healthcare services in urban areas, contributing to the development of sustainable and resilient healthcare systems.

f) SDG 12: Responsible Consumption and Production

The development and use of low noise amplifiers in medical imaging should align with responsible consumption and production practices, considering the environmental impact and sustainability of the technologies.

g) SDG 17: Partnerships for the Goals

Collaboration between governments, private sectors, and research institutions is crucial for advancing technologies like microwave breast cancer imaging. Partnerships can facilitate the sharing of knowledge, resources, and expertise, accelerating progress toward the SDGs.

CHAPTER 5

CONCLUSION AND FUTURE WORKS

5.1 Conclusion

The LNA is design for Microwave Breast Cancer Imaging application. The goals of this project are to design a LNA with frequency range 1-2 GHz and to analysis and verify the simulation performance of the designed LNA using ADS software. The reason this frequency is used is because it plays a crucial role in various imaging applications, offering advantages related to penetration depth, SNR, scattering reduction, and specific imaging techniques.

The transistor that has been used to get initial result in stability, noise figure and gain is pHEMT MGA-684P8 and AT-42086. The transistor is chosen because it meets requirement to satisfy stability condition k>1. Thus, the next calculation can

be proceeded to get gain and noise figure to satisfy specifications of LNA in this project. The specifications of noise figure and gain is satisfied to meet with the requirements below 2 db in noise figure and above 20 dB for gain.

For input and output matching of the component, L-matching and single stub matching is used. The all value of L-matching, length and distance of the stub matching are found by calculation and smith chart. The calculation is done by using the frequency at 1.5 GHz.

When all the simulation work for both transistors was completed using the ADS, the results obtained by both transistors demonstrate that in terms of gain and noise figure. Hence, the most suitable transistor for 1.5 GHz LNA design in cascade is silicon bipolar junction transistor (Si BJT) AT-42086 since it represents a low noise figure which is 0.082 dB (L-matching) and 0.061 dB (stub) in two different matching technique compared to MGA-684P8 when the value is 0.614 dB (L-matching) and 0.407 dB (stub). Noise figure is the important parameter for the LNA to reduce the sensitivity of the signals. Moreover, the gain for the AT-42086 is 45.165 dB (L-matching) and 45.165 dB (stub) meanwhile for MGA-684P8 represents 46.481 dB (L-matching) and 46.504 dB (stub).

5.2 Future Work

From this project, the two-stage design of LNA for the future will have a practical test and fabrication with have satisfied specifications. Its result will be compared to the simulation results for the analysis. Thus, the fabrication of LNA also can be apply to the real system of microwave breast cancer imaging. The experiences in fabricating of LNA will make a good experience and better understanding in RF

designs. The fabrication results are important for this project commercialized value for future used.

The most important when designing a LNA is a proposed transistor, the transistor is the component that will produce the gain and affect the noise figure of the LNA need to be selected which can be satisfied into specification. In finding the best transistor, increasing research and selection of the transistor or make acomparison using another transistor technology is important to get the performance of the overall operation of LNA.

For the parameter in LNA, the linearity and PAE can be considered to analysis to have more output in LNA. By adding the parameter, we can see the different result and performance using different matching techniques and circuit designs.

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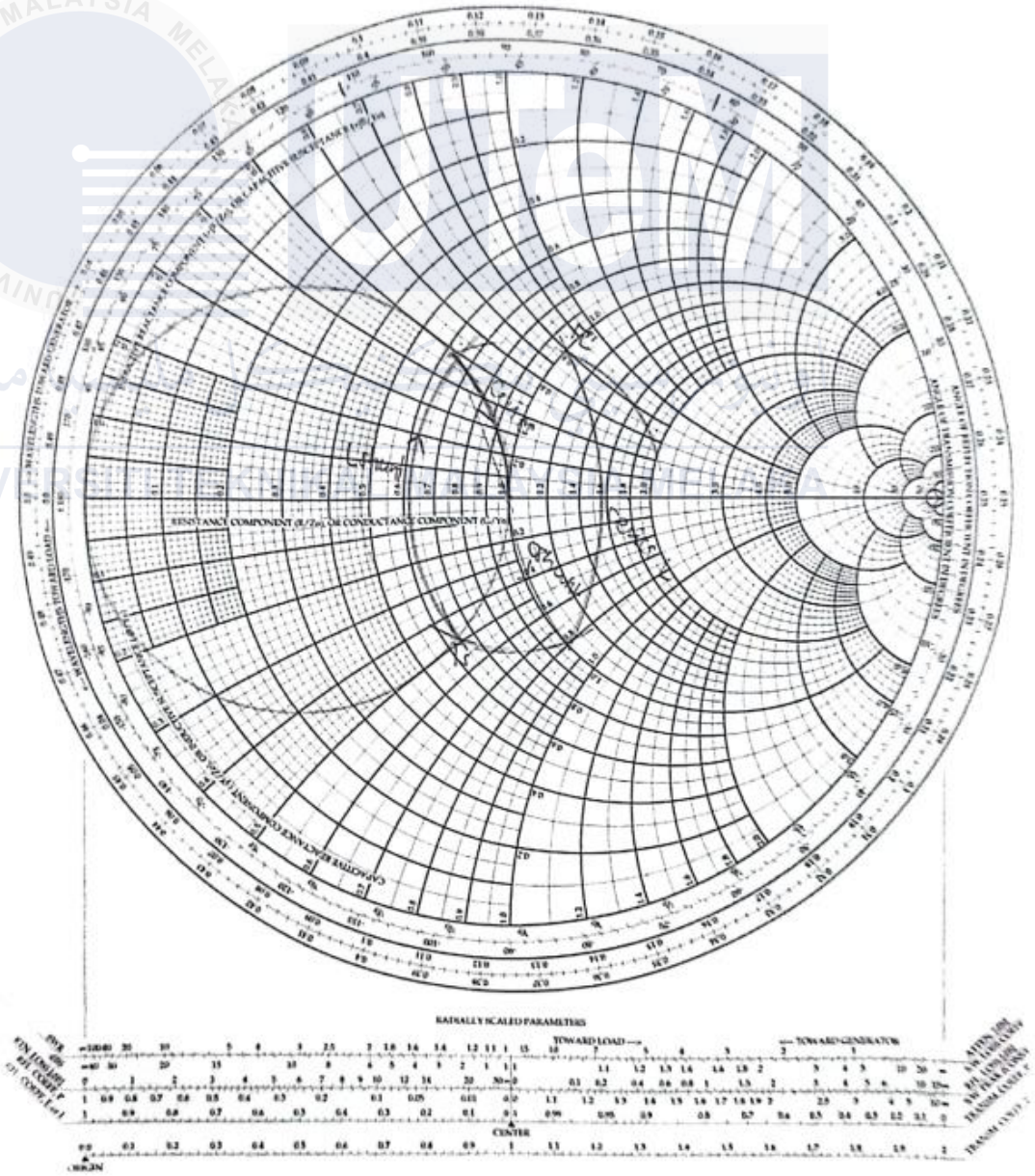
APPENDICES A

MGA-684P8 L-MATCHING

$\Gamma_T = 0.36 \angle$ **Smith Chart**

$\Gamma_L = 0.36 \angle 62$

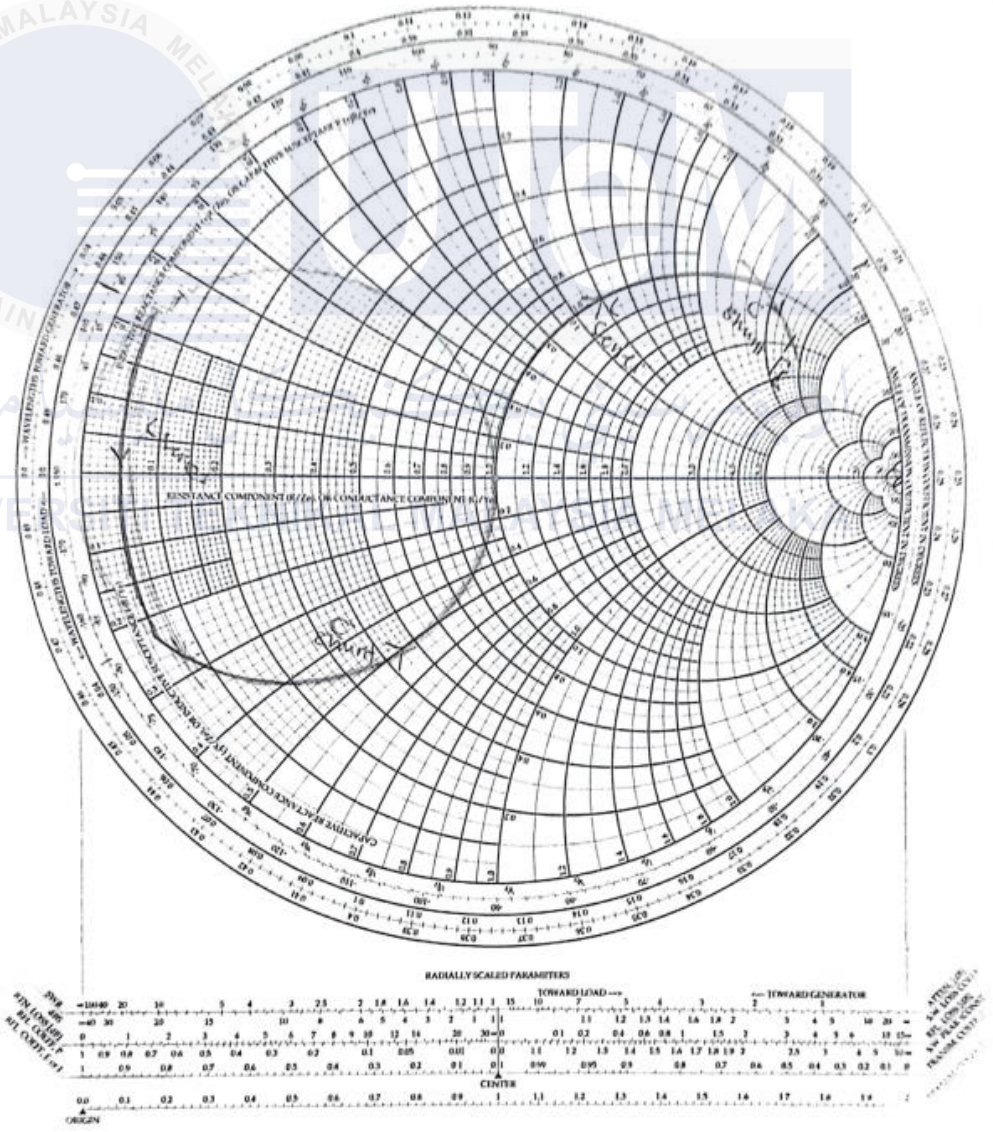


APPENDICES B

AT 4308c L-Matching

$\Gamma_s = 0.88 \angle 154$

$\Gamma_L = 0.79 \angle 30$

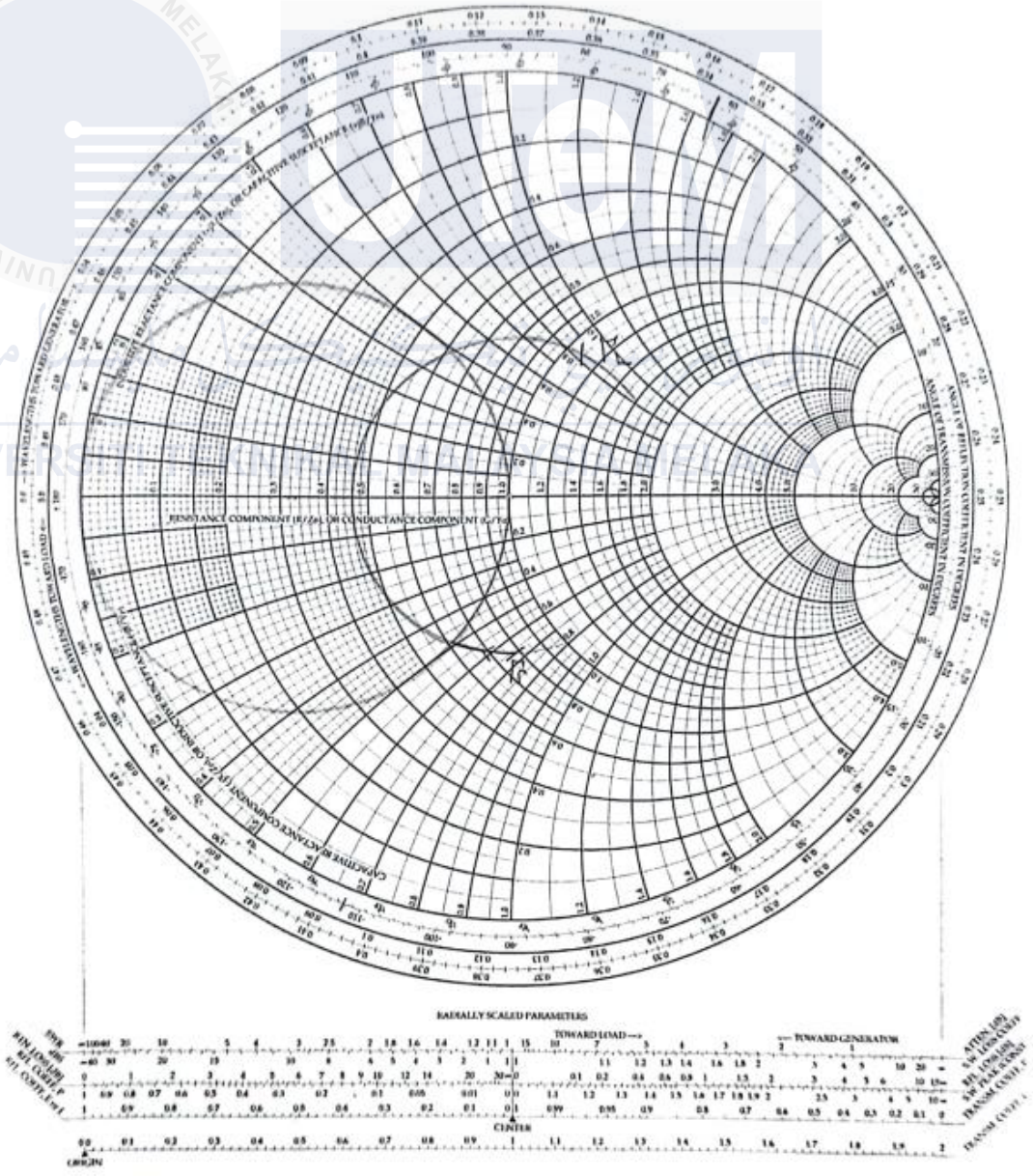


APPENDICES C

MAH - Stub Matching

$\Gamma_S = 0.36 \angle -117$

$\Gamma_L = 0.36 \angle 63$ **Smith Chart**



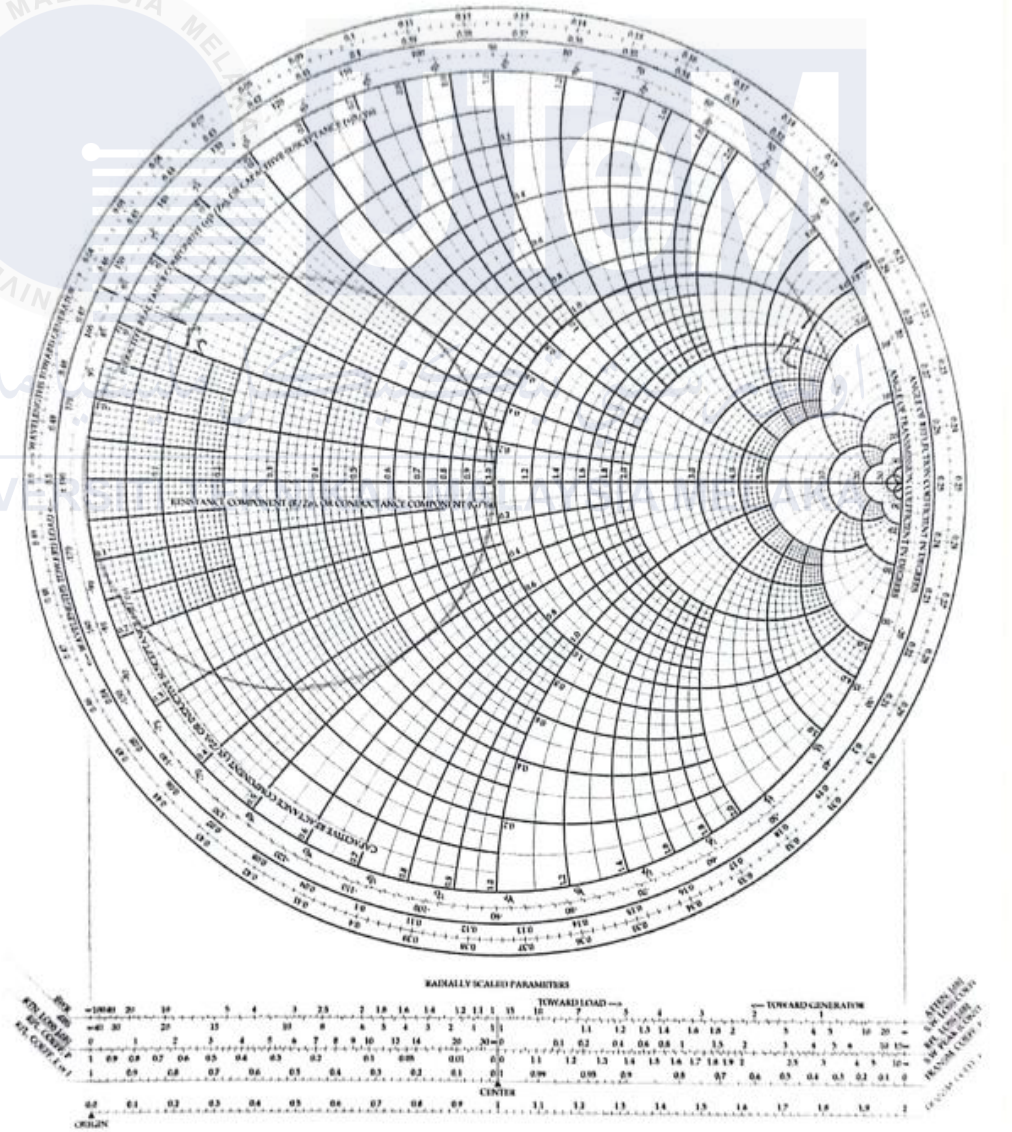
APPENDICES D

AT-42086 Stub-matching

$\Gamma_S = 0.88 \angle 154$

$\Gamma_L = 0.79 \angle 30$

Smith Chart



APPENDICES E

MGA-684P8

Low Noise Active Bias Low Noise Amplifier

Avago TECHNOLOGIES

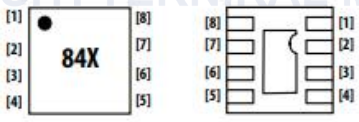
Data Sheet

Description

Avago Technologies' MGA-684P8 is an economical, easy-to-use GaAs MMIC Low Noise Amplifier (LNA). The LNA has low noise and high linearity achieved through the use of Avago Technologies' proprietary 0.25 µm GaAs Enhancement-mode pHEMT process. It is housed in a miniature 2.0 x 2.0 x 0.75 mm^3 8-pin Quad-Flat-Non-Lead (QFN) package. It is designed for optimum use from 1.5 GHz up to 4 GHz. The compact footprint and low profile coupled with low noise, high gain and high linearity make the MGA-684P8 an ideal choice as a low noise amplifier for cellular infrastructure for GSM and CDMA. For optimum performance at lower frequency from 450 MHz up to 1.5 GHz, MGA-683P8 is recommended. Both MGA-683P8 and MGA-684P8 share the same package and pinout configuration.

Pin Configuration and Package Marking

2.0 x 2.0 x 0.75 mm^3 8-lead QFN



Top View

Pin 1 – Vbias
Pin 2 – RFinput
Pin 3 – Not Used
Pin 4 – Not Used

Bottom View

Pin 5 – Not Used
Pin 6 – Not Used
Pin 7 – RFoutput/Vdd
Pin 8 – Not Used
Centre tab - Ground

Note:
Package marking provides orientation and identification
"84" = Device Code, where X is the month code.

Attention: Observe precautions for handling electrostatic sensitive devices.
ESD Machine Model = 70 V (Class A)
ESD Human Body Model = 500 V (Class 1B)
Refer to Avago Application Note A004R: Electrostatic Discharge, Damage and Control.

Features

- Low noise Figure
- High linearity performance
- GaAs E-pHEMT Technology[1]
- Low cost small package size: 2.0 x 2.0 x 0.75 mm^3
- Excellent uniformity in product specifications
- Tape-and-Reel packaging option available

Specifications

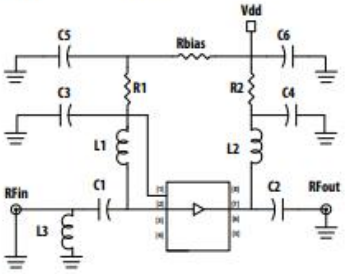
1.9 GHz; 5 V, 35 mA

- 17.6 dB Gain
- 0.56 dB Noise Figure
- 21 dB Input Return Loss
- 32.4 dBm Output IP3
- 22 dBm Output Power at 1dB gain compression

Applications

- Low noise amplifier for cellular infrastructure for GSM TDS-CDMA, and CDMA.
- Other low noise application.
- Repeater, Metrocell/Picocell application.

Simplified Schematic



Note:

- The schematic is shown with the assumption that similar PCB is used for both MGA-683P8 and MGA-684P8.
- Detail of the components needed for this product is shown in Table 1.
- Enhancement mode technology employs positive gate voltage, thereby eliminating the need of negative gate voltage associated with conventional depletion mode devices.
- Good RF practice requires all unused pins to be earthed.

Absolute Maximum Rating [1] T_A=25° C

Symbol	Parameter	Units	Absolute Maximum
V_{dd}	Device Voltage, RF output to ground	V	5.5
V_{bias}	Gate Voltage	V	0.7
Idd	Drain Current	mA	90
$P_{in,max}$	CW RF Input Power (V_{dd} = 5.0 V, I_d = 50 mA)	dBm	+20
P_{diss}	Total Power Dissipation [2]	W	0.5
T_j	Junction Temperature	°C	150
T_{stg}	Storage Temperature	°C	-65 to 150

Thermal Resistance

Thermal Resistance [3]
(V_{dd} = 5.0 V, I_{dd} = 35 mA per channel), θ_{jc} = 62°C/W per channel

Notes:
1. Operation of this device in excess of any of these limits may cause permanent damage.
2. Thermal resistance measured using Infra-Red Measurement Technique.
3. Power dissipation with unit turned on. Board temperature T_B is 25° C. Derate at 16 mW/°C for T_B > 119° C.

Electrical Specifications [1], [4]

RF performance at T_A = 25° C, V_{dd} = 5 V, R_{bias} = 6.8 kOhm, 1.9 GHz, measured on demo board in Figure 5 with component list in Table 1 for 1.9 GHz matching.

Symbol	Parameter and Test Condition	Units	Min.	Typ.	Max.
I_{dd}	Drain Current	mA	23	35.2	47
Gain	Gain	dB	16.1	17.6	19.1
OIP3 [2]	Output Third Order Intercept Point	dBm	29	32.4	
NF [3]	Noise Figure	dB		0.56	0.8
OP1dB	Output Power at 1dB Gain Compression	dBm		22	
IRL	Input Return Loss, 50 Ω source	dB		21	
ORL	Output Return Loss, 50 Ω load	dB		12	
REV ISOL	Reverse Isolation	dB		30	

Notes:
1. Measurements at 1.9 GHz obtained using demo board described in Figure 1.
2. OIP3 test condition: F_{RF1} = 1.9 GHz, F_{RF2} = 1.901 GHz with input power of -10 dBm per tone.
3. For NF data, board losses of the input have not been de-embedded.
4. Use proper bias, heatsink and derating to ensure maximum channel temperature is not exceeded. See absolute maximum ratings and application note for more details.

Product Consistency Distribution Charts [1, 2]

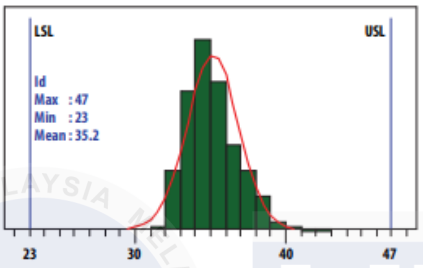


Figure 1. Idd @ 1.9 GHz Mean = 35.2 mA

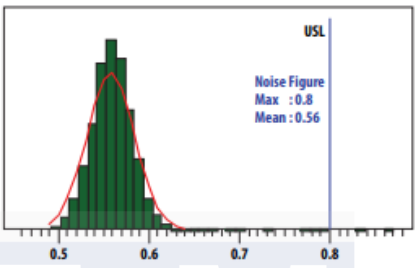


Figure 2. Noise Figure @1.9 GHz, Mean = 0.56

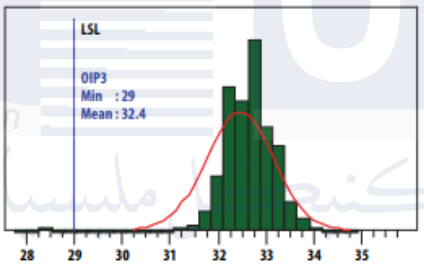


Figure 3. OIP3 @ 1.9 GHz, Mean = 32.4

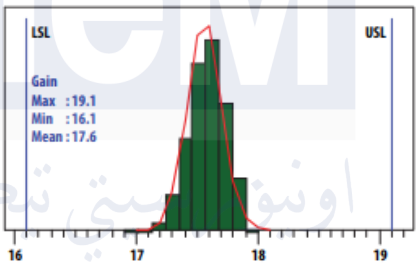


Figure 4. Gain @ 1.9 GHz, Mean = 17.6

Notes:
1. Distribution data samples are 500 samples taken from 3 different wafers. Future wafers allocated to this product may have nominal values anywhere between the upper and lower limits.
2. Circuit Losses have not been de-embedded from the actual measurements.

Demo Board Layout

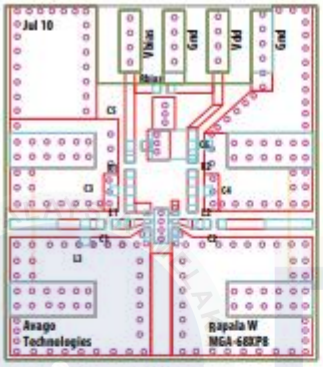


Figure 5. Demo Board Layout Diagram

- Recommended PCB material is 10 mils Rogers RO4350.
- Suggested component values may vary according to layout and PCB material.

Demo Board Schematic

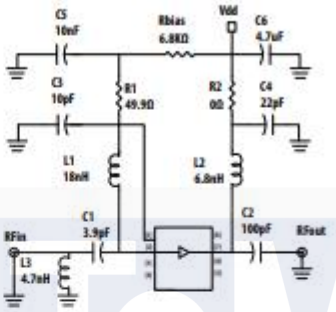


Figure 6. Demo Board Schematic Diagram

Notes:
- The schematic is shown with the assumption that similar PCB is used for both MGA-683P8 and MGA-68P8.
- Detail of the components needed for this product is shown in Table 1.

Table 1. Component list for 1.9 GHz matching

Part	Size	Value	Detail Part Number
C1	0402	3.9 pF	Murata GRM15
C2	0402	100 pF	Murata GRM15
C3	0402	10 pF	Murata GRM15
C4	0402	22 pF	Murata GRM15
C5	0402	10 nF	Murata GRM15
C6	0805	4.7 µF	Murata GRM15
L1	0402	18 nH	Coilcraft CS0402
L2	0402	6.8 nH	Toko FHL1005
L3	0402	4.7 nH	Coilcraft CS0402
Rbias	0402	6.8 KOhm	KOA RK73
R1	0402	49.9 Ohm	KOA RK73
R2	0402	0 Ohm	KOA RK73

Notes:
C2 is a blocking capacitor
L2 output match for OIP3
L1, C1 and L3 are used for IRL matching.
C3, C4, C5, C6 are bypass capacitors
R1 is stabilizing resistor
Rbias is the biasing resistor

MGA-684P8 Typical Performance in Demoboard

RF performance at T_A = 25° C, Vdd = 5 V, Rbias = 6.8 kOhm, measured on demo board in Figure 5 with component list in Table1 for 1.9 GHz matching, unless otherwise stated.

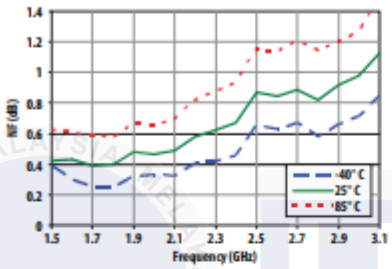


Figure 7. NF vs Frequency vs Temperature

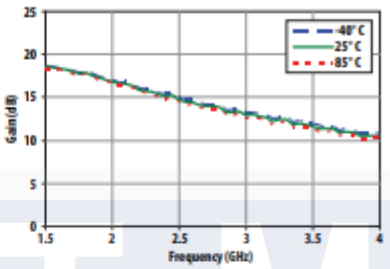


Figure 8. Gain vs Frequency vs Temperature

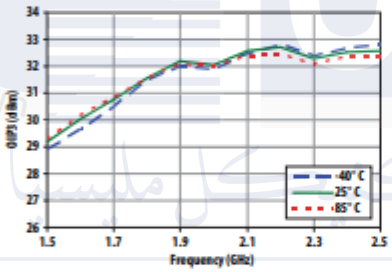


Figure 9. OIP3 vs Frequency vs Temperature

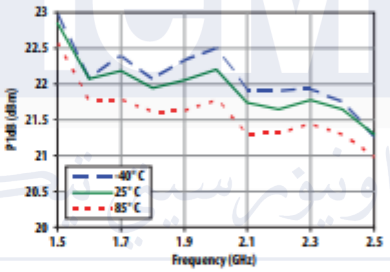


Figure 10. OP1dB vs Frequency vs Temperature

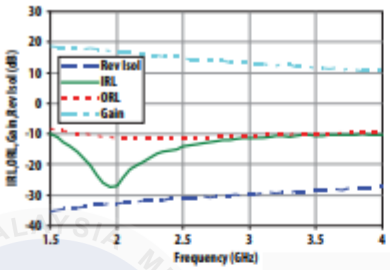


Figure 11. S-Parameter performance with DUT on demoboard shown in Figure 1.

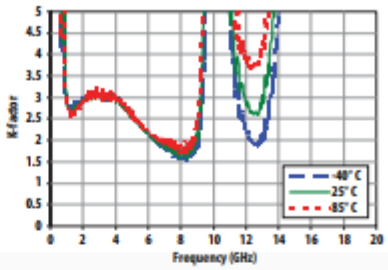


Figure 12. K-factor vs Frequency vs Temperature

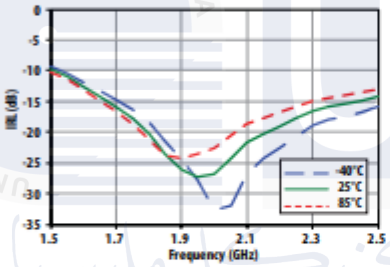


Figure 13. Input Return Loss vs Frequency vs Temperature

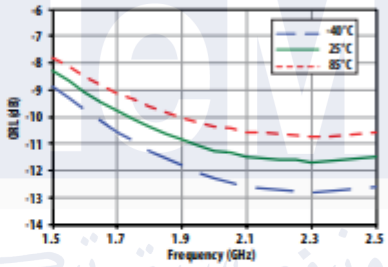


Figure 14. Output Return Loss vs Frequency vs Temperature

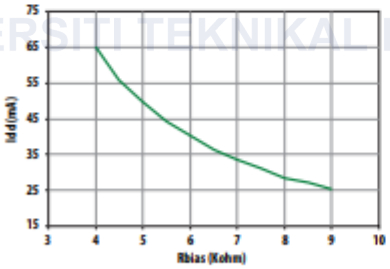


Figure 15. Idd vs Rbias

MGA-684P8 Typical Scattering Parameters, Vdd = 5 V

Freq	S11		S21			S12		S22	
GHz	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.	Mag.	Ang.
0.10	0.91	-16.78	30.68	34.18	158.93	0.00	45.07	0.54	-17.76
0.50	0.62	-58.89	26.12	20.22	116.50	0.01	54.53	0.35	-30.30
0.90	0.45	-81.40	22.58	13.46	93.41	0.01	56.93	0.33	-39.58
1.00	0.42	-85.56	21.83	12.35	88.97	0.02	57.63	0.33	-41.24
1.50	0.33	-101.54	18.76	8.67	70.27	0.02	57.76	0.33	-51.61
1.90	0.29	-113.04	16.88	6.98	57.33	0.03	56.51	0.34	-63.11
2.00	0.28	-115.99	16.47	6.66	54.26	0.03	55.16	0.34	-66.07
2.50	0.27	-131.72	14.62	5.38	39.44	0.03	51.70	0.34	-81.79
3.00	0.28	-146.73	13.02	4.48	25.29	0.04	47.69	0.36	-97.97
4.00	0.35	-164.20	10.29	3.27	-1.28	0.05	38.99	0.41	-128.02
5.00	0.37	-168.83	8.27	2.59	-24.54	0.06	32.11	0.50	-145.67
6.00	0.36	-176.50	7.00	2.24	-46.71	0.08	25.46	0.55	-158.74
7.00	0.36	158.90	5.73	1.93	-72.15	0.10	14.33	0.57	179.26
8.00	0.47	132.96	3.89	1.57	-99.05	0.12	0.48	0.62	148.79
9.00	0.58	123.68	1.47	1.18	-122.64	0.13	-11.23	0.71	126.95
10.00	0.59	115.01	-0.34	0.96	-143.22	0.14	-21.09	0.77	117.70
11.00	0.52	93.03	-1.08	0.88	-166.72	0.19	-35.04	0.77	106.08
12.00	0.49	54.25	-2.56	0.75	161.15	0.22	-58.42	0.76	76.15
13.00	0.58	37.37	-6.12	0.49	132.57	0.21	-78.94	0.82	47.95
14.00	0.65	45.34	-9.98	0.32	115.94	0.20	-87.61	0.87	36.90
15.00	0.65	48.42	-12.83	0.23	100.46	0.22	-94.49	0.86	33.52
16.00	0.57	29.23	-15.49	0.17	72.55	0.26	-111.55	0.80	22.79
17.00	0.55	-6.38	-20.42	0.10	29.92	0.26	-135.35	0.78	2.52
18.00	0.63	-24.55	-26.61	0.05	-29.09	0.23	-152.31	0.83	-10.20
19.00	0.69	-20.93	-26.44	0.05	-92.58	0.21	-162.51	0.85	-19.78
20.00	0.69	-14.10	-23.23	0.07	-128.03	0.21	-173.20	0.83	-32.83

Typical Noise Parameters, Vdd=5V

Freq	Fmin	Γopt	Γopt	
GHz	dB	Mag.	Ang.	Rn/50
1.5	0.39	0.135	76.1	0.05
1.9	0.45	0.191	118.2	0.04
2	0.49	0.174	125.9	0.05
2.2	0.61	0.181	139.4	0.04
2.5	0.69	0.204	151.3	0.05

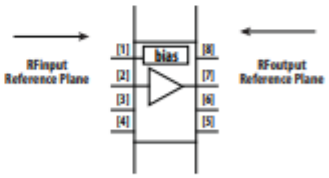
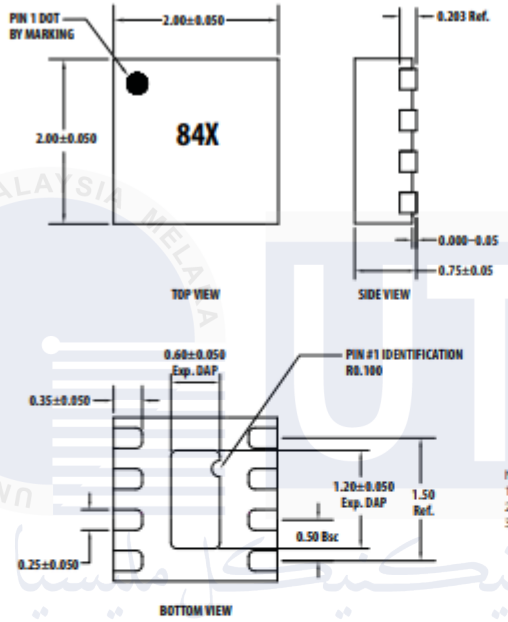


Figure 16.

Notes:
1. The Fmin values are based on noise figure measurements at 100 different impedances using Focus source pull test system. From these measurements a true Fmin is calculated.
2. Scattering and noise parameters are measured on coplanar waveguide made on 0.010 inch thick ROGER 4350. The input reference plane is at the end of the RFinput pin and the output reference plane is at the end of the RFoutput pin as shown in Figure 16.

SLP4X4 Package

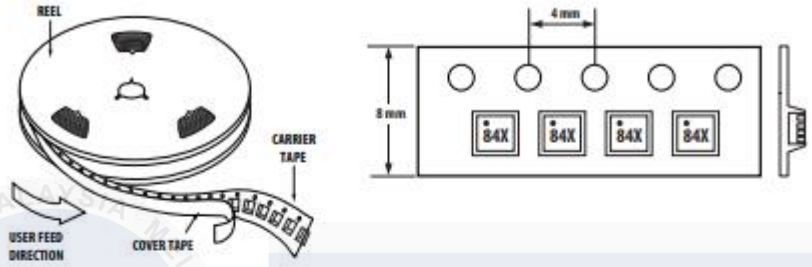


Notes:
1. All dimensions are in millimeters.
2. Dimensions are inclusive of plating.
3. Dimensions are exclusive of mold ash and metal burr.

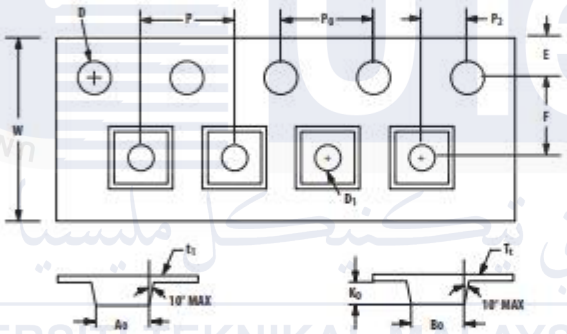
Part Number Ordering Information

Part Number	No. of Devices	Container
MGA-684P8-BLKG	100	Antistatic Bag
MGA-684P8-TR1G	3000	7 inch Reel

Device Orientation

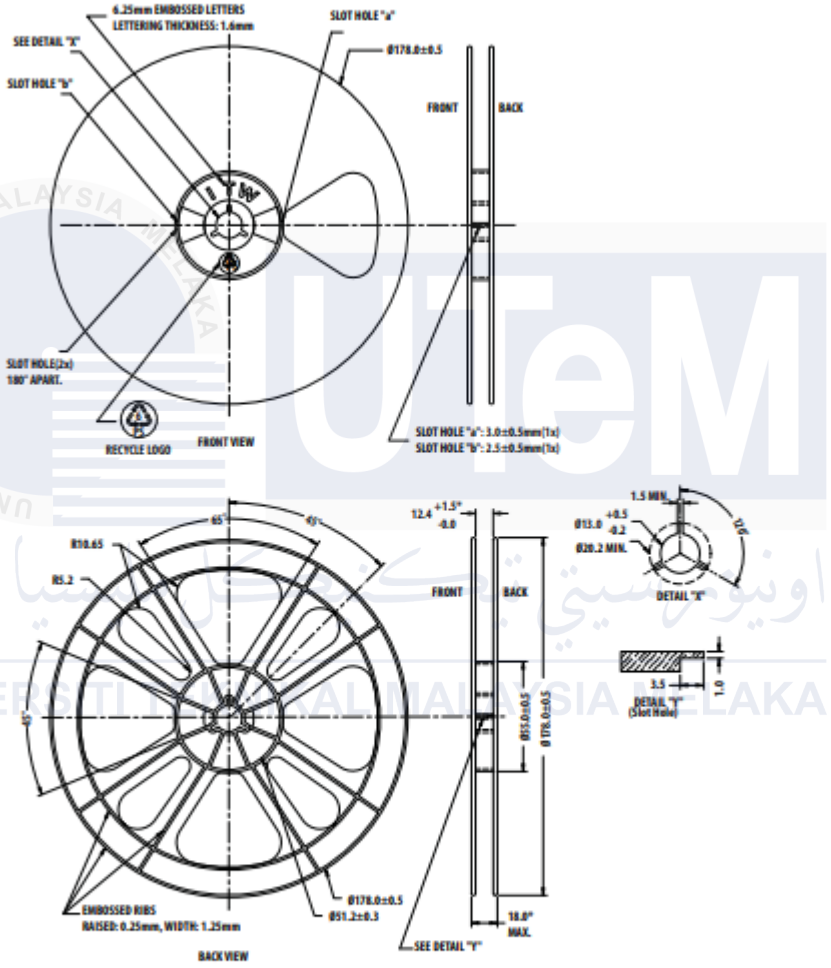


Tape Dimensions



DESCRIPTION		SYMBOL	SIZE (mm)	SIZE (INCHES)
CAVITY	LENGTH	A_0	2.30 ± 0.05	0.091 ± 0.004
	WIDTH	B_0	2.30 ± 0.05	0.091 ± 0.004
	DEPTH	K_0	1.00 ± 0.05	0.039 ± 0.002
	PITCH	P	4.00 ± 0.10	0.157 ± 0.004
	BOTTOM HOLE DIAMETER	D_1	1.00 + 0.25	0.039 + 0.002
PERFORATION	DIAMETER	D	1.50 ± 0.10	0.060 ± 0.004
	PITCH	P_0	4.00 ± 0.10	0.157 ± 0.004
	POSITION	E	1.75 ± 0.10	0.069 ± 0.004
CARRIER TAPE	WIDTH	W	8.00 ± 0.30	0.315 ± 0.012
			8.00 ± 0.10	0.315 ± 0.004
	THICKNESS	t_1	0.254 ± 0.02	0.010 ± 0.0008
COVER TAPE	WIDTH	C	5.4 ± 0.10	0.205 ± 0.004
	TAPE THICKNESS	T_t	0.062 ± 0.001	0.0025 ± 0.0004
DISTANCE	CAVITY TO PERFORATION (WIDTH DIRECTION)	F	3.50 ± 0.05	0.138 ± 0.002
	CAVITY TO PERFORATION (LENGTH DIRECTION)	P_2	2.00 ± 0.05	0.079 ± 0.002

Reel Dimensions – 7 inch



For product information and a complete list of distributors, please go to our web site: **www.avagotech.com**

AV02-2951EN - May 23, 2012

AVAGO TECHNOLOGIES

APPENDICES F

AT-42086
Up to 6 GHz Medium Power
Silicon Bipolar Transistor

AVAGO TECHNOLOGIES

Data Sheet

Description

Avago's AT-42086 is a general purpose NPN bipolar transistor that offers excellent high frequency performance. The AT-42086 is housed in a low cost surface mount .085" diameter plastic package. The 4 micron emitter-to-emitter pitch enables this transistor to be used in many different functions. The 20 emitter finger interdigitated geometry yields a medium sized transistor with impedances that are easy to match for low noise and medium power applications. Applications include use in wireless systems as an LNA, gain stage, buffer, oscillator, and mixer. An optimum noise match near 50Ω up to 1 GHz, makes this device easy to use as a low noise amplifier.

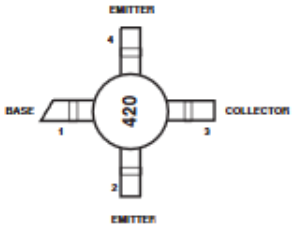
The AT-42086 bipolar transistor is fabricated using Avago's 10 GHz f_T Self-Aligned-Transistor (SAT) process. The die is nitride passivated for surface protection. Excellent device uniformity, performance and reliability are produced by the use of ion-implantation, self-alignment techniques, and gold metalization in the fabrication of this device.

Features

- High Output Power:
  20.5 dBm Typical $P_{1\ dB}$ at 2.0 GHz
- High Gain at 1 dB Compression:
  13.5 dB Typical $G_{1\ dB}$ at 2.0 GHz
- Low Noise Figure:
  1.9 dB Typical NF_O at 2.0 GHz
- High Gain-Bandwidth Product: 8.0 GHz Typical f_T
- Surface Mount Plastic Package
- Tape-and-Reel Packaging Option Available
- Lead-free Option Available

86 Plastic Package

Pin Connections



AT-42086 Absolute Maximum Ratings

Symbol	Parameter	Units	Absolute Maximum[1]
V_{EBO}	Emitter-Base Voltage	V	1.5
V_{CBO}	Collector-Base Voltage	V	20
V_{CEO}	Collector-Emitter Voltage	V	12
I_C	Collector Current	mA	80
P_T	Power Dissipation [2,3]	mW	500
T_J	Junction Temperature	°C	150
T_{STG}	Storage Temperature	°C	-65 to 150

Thermal Resistance[2]:
$\theta_{jc} = 140°C/W$

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. $T_{CASE} = 25°C$.
3. Derate at 7.1 mW/°C for $T_C > 80°C$.

Electrical Specifications, $T_A = 25°C$

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.
$\|S_{21E}\|^2$	Insertion Power Gain; $V_{CE} = 8\,V$, $I_C = 35\,mA$	f = 1.0 GHz	dB	15.0	16.5	
		f = 2.0 GHz			10.5	
		f = 4.0 GHz			4.5	
$P_{1\,dB}$	Power Output @ 1 dB Gain Compression	f = 2.0 GHz	dBm		20.5	
	$V_{CE} = 8\,V$, $I_C = 35\,mA$	f= 4.0 GHz			20.0	
$G_{1\,dB}$	1 dB Compressed Gain; $V_{CE} = 8\,V$, $I_C = 35\,mA$	f = 2.0 GHz	dB		13.5	
		f = 4.0 GHz			9.0	
NF_O	Optimum Noise Figure: $V_{CE} = 8\,V$, $I_C = 10\,mA$	f = 2.0 GHz	dB		1.9	
		f = 4.0 GHz			3.5	
G_A	Gain @ NF_O; $V_{CE} = 8\,V$, $I_C = 10\,mA$	f = 2.0 GHz	dB		13.0	
		f = 4.0 GHz			9.0	
f_T	Gain Bandwidth Product: $V_{CE} = 8\,V$, $I_C = 35\,mA$		GHz		8.0	
h_{FE}	Forward Current Transfer Ratio; $V_{CE} = 8\,V$, $I_C = 35\,mA$		—	30	150	270
I_{CBO}	Collector Cutoff Current; $V_{CB} = 8\,V$		μA			0.2
I_{EBO}	Emitter Cutoff Current; $V_{EB} = 1\,V$		μA			2.0
C_{CB}	Collector Base Capacitance[1]: $V_{CB} = 8\,V$, f = 1 MHz		pF		0.32	

Note:
1. For this test, the emitter is grounded.

AT-42086 Typical Performance, $T_A = 25°C$

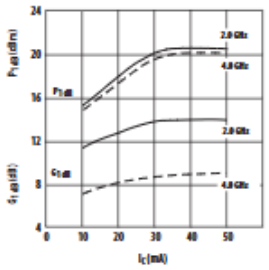


Figure 1. Output Power and 1 dB Compressed Gain vs. Collector Current and Frequency. $V_{CE} = 8$ V.

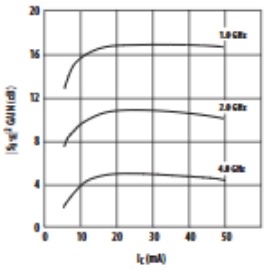


Figure 2. Insertion Power Gain vs. Collector Current and Frequency. $V_{CE} = 8$ V.

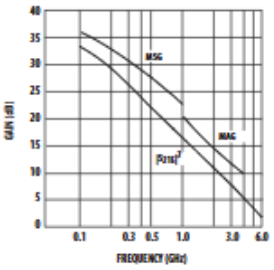


Figure 3. Insertion Power Gain, Maximum Available Gain and Maximum Stable Gain vs. Frequency. $V_{CE} = 8$ V, $I_C = 35$ mA.

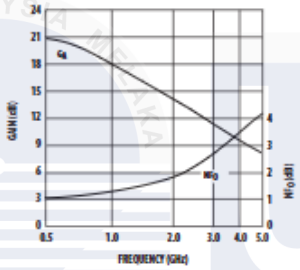


Figure 4. Noise Figure and Associated Gain vs. Frequency. $V_{CE} = 8$ V, $I_C = 10$ mA.

AT-42086 Typical Scattering Parameters,
Common Emitter, $Z_O = 50\ \Omega$, $T_A = 25°C$, $V_{CE} = 8\ V$, $I_C = 10\ mA$

Freq.	S_{11}			S_{21}			S_{12}		S_{22}	
GHz	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.
0.1	.68	-48	28.0	25.12	153	-36.0	.016	65	.91	-15
0.5	.63	-141	20.9	11.07	102	-29.9	.032	42	.54	-30
1.0	.63	-176	15.4	5.87	80	-27.4	.043	43	.43	-30
1.5	.65	164	12.0	3.98	65	-26.0	.050	46	.40	-34
2.0	.66	151	9.5	2.99	53	-23.9	.064	52	.38	-40
2.5	.69	142	7.8	2.44	45	-23.1	.070	53	.36	-46
3.0	.71	132	6.2	2.04	34	-21.6	.084	54	.34	-54
3.5	.73	123	4.8	1.74	24	-19.7	.104	53	.33	-67
4.0	.75	115	3.6	1.51	14	-18.3	.122	51	.30	-80
4.5	.78	108	2.6	1.34	5	-17.2	.138	50	.31	-94
5.0	.80	101	1.6	1.20	-4	-16.0	.159	46	.31	-110
5.5	.82	95	0.6	1.08	-12	-14.8	.182	40	.32	-129
6.0	.85	89	-0.2	0.97	-21	-14.0	.200	35	.34	-148

AT-42086 Typical Scattering Parameters,
Common Emitter, $Z_O = 50\ \Omega$, $T_A = 25°C$, $V_{CE} = 8\ V$, $I_C = 35\ mA$

Freq.	S_{11}			S_{21}			S_{12}		S_{22}	
GHz	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.
0.1	.48	-94	32.8	43.62	137	-37.7	.013	65	.77	-25
0.5	.57	-168	22.4	13.21	92	-32.6	.023	57	.39	-28
1.0	.59	168	16.5	6.69	75	-28.7	.037	62	.33	-27
1.5	.61	154	13.0	4.48	62	-24.8	.057	64	.31	-31
2.0	.63	143	10.5	3.36	51	-23.0	.071	61	.29	-37
2.5	.68	137	8.7	2.72	43	-21.0	.089	56	.26	-45
3.0	.68	127	7.0	2.25	33	-19.7	.104	58	.25	-53
3.5	.71	118	5.7	1.92	24	-18.4	.121	55	.24	-65
4.0	.73	111	4.5	1.69	14	-17.3	.136	49	.20	-80
4.5	.76	104	3.5	1.49	5	-15.9	.161	46	.21	-95
5.0	.78	98	2.4	1.32	-3	-15.2	.174	43	.21	-115
5.5	.81	91	1.6	1.20	-12	-14.3	.193	36	.22	-136
6.0	.84	85	0.7	1.08	-20	-13.4	.213	31	.25	-156

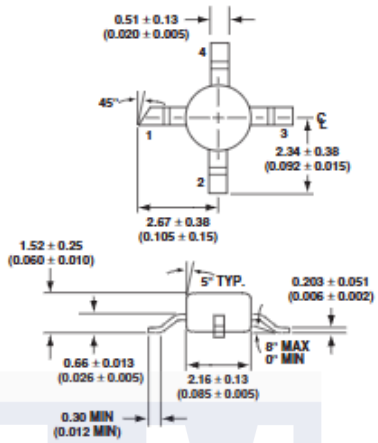
AT-42086 Noise Parameters: $V_{CE} = 8\ V$, $I_C = 10\ mA$

Freq.	NF_0	Γ_{opt}		$R_N/50$
GHz	dB	Mag	Ang	
0.1	1.0	.04	8	0.13
0.5	1.1	.03	62	0.12
1.0	1.5	.06	168	0.12
2.0	1.9	.25	-146	0.12
4.0	3.5	.58	-100	0.52

Ordering Information

Part Numbers	No. of Devices	Comments
AT-42086-BLKG	100	Bulk
AT-42086-TR1G	1000	7" Reel
AT-42086-TR2G	4000	13" Reel

86 Plastic Package Dimensions



DIMENSIONS ARE IN MILLIMETERS (INCHES)

For product information and a complete list of distributors, please go to our web site: **www.avagotech.com**

AV02-1460EN - August 8, 2008

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