N-TYPE DOUBLE GATE MOSFET – BASED FOR EFFICIENT DIGITAL CIRCUITS

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This report is submitted in partial fulfilment of the requirements for the degree of Bachelor of Computer Engineering with Honours

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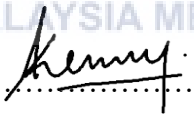
Signature : 

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DEDICATION

I would like to dedicate this thesis to my parents, who always support me and ensure I would have the oppurtunity in education.

ABSTRACT

Over the past few years, there has been a growing need for digital circuits offering high performance and energy efficiency. This has led to the investigation of new transistor designs. The Double Gate Metal-Oxide-Semiconductor Field-Effect Transistor (DGMOSFET) has emerged as an up-and-coming option for enhancing device performance and minimising power usage. The main objective of this research is to concentrate on creating and improving digital circuits utilising n-type double-gate MOSFET. This project presents a thorough examination of the N-type double-gate MOSFET in the creation of efficient digital circuits. The suggested transistor configuration takes advantage of the distinctive qualities of double-gate MOSFET to augment the performance parameters of digital circuits, including speed, power consumption and area. By utilising n-type double-gate MOSFET, offer enhanced electrostatic control, eliminate short-channel effects and improved subthreshold slope compared to single-gate MOSFET. The research found that double-gate MOSFET has a 39% of power reduction and 50% faster switching activity compared to single-gate MOSFET in this project. The results and discoveries outlined in this project offer valuable knowledge to designers and researchers involved in advanced transistor technologies and the optimisation of digital circuits.

ABSTRAK

Keperluan yang semakin meningkat untuk litar digital yang menawarkan prestasi tinggi dan kecekapan tenaga membawa kepada kajian akan reka bentuk transistor baru. Double Gate MOSFET (DGMOSFET) merupakan pilihan yang akan untuk meningkatkan prestasi peranti dan meminimumkan penggunaan kuasa. Objektif utama penyelidikan ini adalah untuk mencipta dan menambah baik litar digital menggunakan n-type double-gate MOSFET. Projek ini mempamerkan penyelidikan double-gate MOSFET dalam penciptaan litar digital yang cekap. Konfigurasi transistor yang dicadangkan memanfaatkan ciri double-gate MOSFET untuk meningkatkan prestasi litar digital, termasuk kelajuan, penggunaan kuasa dan saiz. Dengan menggunakan double-gate MOSFET, kawalan elektrostatik dapat dipertingkatkan, menghapuskan 'short channel effects' dan 'subthreshold slope' yang lebih baik berbanding MOSFET. Di akhir penyelidikan ini, mendapati double-gate MOSFET mempunyai pengurangan kuasa sebanyak 39% dan masa peralihan lebih pantas sebanyak 50% berbanding MOSFET dalam projek ini. Keputusan dan penemuan yang digariskan dalam projek ini menawarkan pengetahuan berharga kepada design engineer dan penyelidik dalam teknologi transistor dan pengoptimuman litar digital.

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LIST OF SYMBOLS AND ABBREVIATIONS

%	:	per cent
°	:	degree
µ	:	micro
A	:	Ampere
CAD	:	Computer-Aided Design
CMOS	:	Complementary Metal-Oxide-Semiconductor
DGMOSFET	:	Double Gate Metal-Oxide-Semiconductor Field-Effect Transistor
DIBL	:	Drain Inducer Barrier Leakage
DTCO	:	Design Technology Co-Optimization
FET	:	Field Effect Transistor
FinFET	:	Fin Field-Effect Transistor
$Hf O_2$	:	Hafnium Dioxide
I_{OFF}	:	Current OFF
I_{ON}	:	Current ON
I_{ON}/I_{OFF}	:	Current ON/Current OFF
IRDS	:	International Roadmap for Devices and Systems
I-V	:	Current-Voltage

keV	:	kilo energy volt
L	:	Length
m	:	meter
MOS	:	Metal Oxide Silicon
MOSFET	:	Metal-Oxide-Semiconductor Field-Effect Transistor
n	:	nano
p	:	pico
s	:	seconds
S/D	:	Source/drain
SCE	:	Short Channel Effect
SDG	:	Sustainable Development Goal
SOI	:	Silicon On Insulator
SPICE	:	Simulation Program with Integrated Circuit Emphasis
SiO_2	:	Silicon Dioxide
SS	:	Subthreshold Slope
TCAD	:	Technology Computer-Aided Design
TiSix	:	Titanium Silicide
V	:	Volt
V_{TH}	:	Threshold Voltage
W	:	Watt
XOR	:	Exclusive OR

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CHAPTER 1

INTRODUCTION

1.1 Introduction

Moore's law projected that the number of transistors on a chip would double every two years. This motivated the semiconductor industry for decades to advance transistor technology. The advancement of transistors technology led to the size of transistors reducing every two years. However, this has caused issues such as leakage current and behavioral variability. Double-Gate MOSFET technology uses two gates instead of one to improve and reduce leakage current, is an alternative to solve the problems. Double-gate MOSFET technology can enhance the performance of a circuit by increasing switching rates, decrease power consumption and enhance noise immunity. In this project, a double-gate MOSFET with 14nm technology design in Silvaco TCAD to analyze digital circuit performance. At the end of this project, a comparison between conventional MOSFET and designed DOUBLE-GATE

MOSFET for an efficient digital circuit obtain by analyses area, power and delay. The designed double-gate MOSFET has low power consumption and high-performance frequency for an efficient digital circuit. As technology evolves, it is crucial to identify innovative solutions that meet industry requirements to enhance performance and decrease energy use. Using double-gate MOSFET in constructing logic gates is one of the good strategies for achieving these objectives and continuing the trend of advancing transistor technology.

1.2 Semiconductor Technology Scaling: A Historical Overview

The integrated circuit (IC) is the primary constituent of semiconductor electronics, encompassing the fundamental components of electronic circuits, including transistors, diodes, capacitors, resistors and inductors, all integrated into a single semiconductor substrate. Transistors and memory devices are the two critical components of silicon electronics. MOSFET, which stands for Metal Oxide Semiconductor Field Effect Transistors, are also employed in logic applications. The ongoing research in semiconductor devices and their use in technological advancement mutually strengthen one another, leading to the scaling of semiconductor devices being the most formidable undertaking[1].

1.2.1 Reasons for MOSFET Scaling

Smaller MOSFET are advantageous for several reasons. The primary motivation for reducing the size of transistors is to increase the density of devices within a particular chip area, achieving either a compact chip with equivalent capability or greater functionality within the same space. Reducing the size of integrated circuits (ICs) enables more chips to be produced on a single wafer, decreasing the cost per chip. Indeed, throughout the last four decades, the number of transistors per chip has

increased twice every two years after introducing a new technological node. As an illustration, the quantity of MOSFET in a microprocessor produced using a 45 nm technology is double that found in a 65 nm chip[2].

1.2.2 Moore's law

Moore's law proposes that the quantity of transistors on integrated circuits undergoes a twofold increase every two years, as seen in Figure 1.1. It has been noted that the sustainability of Moore's Law is limited. Nevertheless, the ability to forecast the limitations of size reduction caused by material or design restrictions and the rate at which size reduction occurs has been shown to be elusive even to the most perceptive scientists.

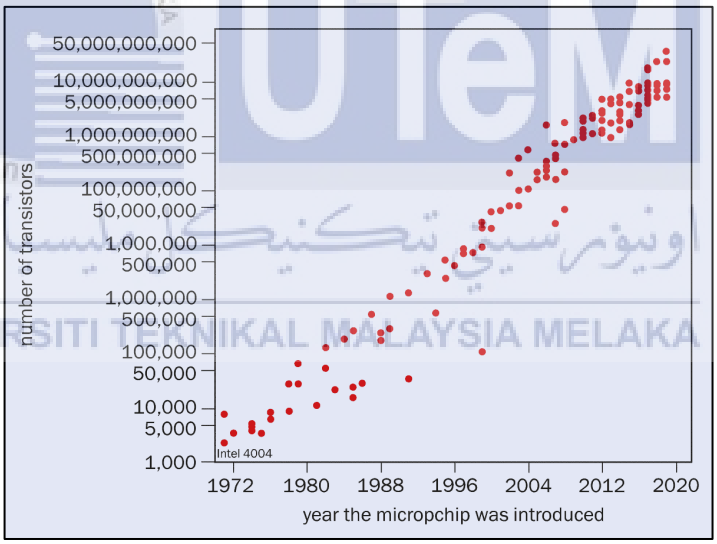


Figure 1.1: Moore's Law on the number of transistors[3]

1.3 Problem Statement

Efficient digital circuits are in high demand, so novel transistor designs like the double-gate MOSFET are being investigated. The design of MOSFET presents several difficulties because of the reduction in transistor size. The short-channel effects due to the decreasing of transistor size is one of the main problems with MOSFET. These effects make the device behave and perform abnormal way and cause the threshold

voltage roll-off and drain-induced barrier lowering (DIBL). As a result, it causes unwanted differences in transistor properties, affecting digital circuits' dependability and efficiency. Furthermore, the inability to regulate the channel correctly, MOSFET results in longer switching delays and inefficiencies when turning transistors on or off. The overall performance of digital circuits has a slower switching speed and decreased operational efficiency and slower data processing capabilities.

Therefore, double-gate MOSFET addresses the challenges presented by short-channel effects and switching delays in MOSFET-based digital circuits. In order to overcome the problems, increase transistor performance and improve digital circuit efficiency, research was conducted to develop an innovative technique and design ideas. By tackling these issues, double-gate MOSFET proved to be a good solution in an effective digital circuit and drive computer systems forward and improve the performance in various fields.

1.3.1 Short Channel Effects (SCE)

The short channel effect is a phenomenon observed in Metal Oxide Silicon Field Effect Transistors (MOSFET) when the length of the channel is comparable to the widths of the depletion layers formed at the source and drain junctions[4][5]. In order to prevent edge effects, the channel length in MOSFET should be larger than the combined widths of the source and drain depletion layers. As the technologies advance, reduction in channel length caused, a short-channel length happened. Some of the short-channel effects in MOSFET are Drain-induced barrier lowering (DIBL), threshold voltage roll-off and velocity saturation.

1.3.2 Threshold Voltage Roll-Off

Threshold voltage roll-off is observed in MOSFET, where the threshold voltage decreases as the channel length decreases[6]. This reduction in threshold voltage happened due to variations in the manufacturing process that impact the channel length of transistors. As the channel length reaches short dimensions, physical effects such as quantum confinement and hot carrier degradation will take place. Threshold voltage roll-off can impact the performance of MOSFET by reducing the threshold voltage as the channel length is decreased. This will set-off the device at an exceedingly low voltage, leading to higher power consumption and decreased reliability. However, overcoming the threshold voltage roll-off can enhance the performance of the device.

Double-gate MOSFET potentially addresses the problem of threshold voltage roll-off in traditional MOSFET. Double-gate MOSFET improved the control over the channel by utilising two gate electrodes and making sure that no portion of the channel is obscure from a gate electrode. This emerging technology of double-gate MOSFET device allows for further downsizing in MOSFET technology due to its practical management of short channels.

1.3.3 Switching Delays

This delay results from the time required for the gate voltage to charge or discharge the MOSFET gate capacitance. The turn-on delay is the time needed to charge the input capacitance of the device before the drain current is supplied. Meanwhile, the turn-off delay is the time taken to discharge the input capacitance of the device before the drain current break-off. Various factors influence the delay, including the loop inductance, excessive current densities and the timing of switching between devices. In high-frequency applications, slow off-time between switching becomes crucial as

the delay will cause the timing of the switching process between devices to slow. A research paper has presented an analytical expression for the intrinsic MOSFET delay based on physical models considering the MOSFET effective current and total capacitance.

Double-gate MOSFET have emerged as a potential solution to address several challenges associated with scaling down MOSFET, including switching delay. These double-gate MOSFET can be scaled down to dimensions ranging from 20 to 30 nm without experiencing the adverse effects of short channel effect (SCE), which indicates their superior ability to mitigate SCE compared to single-gate MOSFET. By independently controlling the top gate and bottom gate, double-gate MOSFET offers advantages that allow for balancing between switching capacitance or leakage and circuit delay. However, when the channel length goes below 100 nm, modifications to the double-gate MOSFET structure are required to minimize the impact of drain control on device characteristics. Double-gate MOSFET have demonstrated enhanced performance in threshold voltage roll-up, reduced drain conductance and improved transconductance compared to single-gate MOSFET. Consequently, double-gate MOSFET promises as a potential solution for addressing the challenges associated with scaling down MOSFET, including overcoming switching delays.

1.4 Objectives

1. To design n-type Double-Gate MOSFET at 14nm technology.
2. To analyze the performance of 14nm double-gate MOSFET and conventional MOSFET from a digital circuit perspective.

1.5 Scope of Project

Silvaco TCAD software is used to design and simulate a double-gate MOSFET at the 14nm scale. The potential of double-gate MOSFET as a viable alternative to conventional MOSFET by considering its performance and efficiency will be analyzed.

Secondly, a full-adder digital circuit was developed to compare the efficiency of double-gate MOSFET and single-gate MOSFET in terms of area, power and delays. This involves design and simulation of the full-adder circuit using double-gate MOSFET and single-gate MOSFET. The efficiency of digital circuits compares and analyses in terms of area, power and delays.

Cadence PSPICE and LTSPICE are used to simulate the full adder circuit. The simulations of the full-adder circuit using SPICE tools included to analyse the performance and identify potential issues or improvement in the circuits. The results obtained from simulations were used to refine the design of the full-adder circuit and optimize the performance.

In summary, this project focuses on design and simulation of a double-gate MOSFET at the 14nm scale. The performance of single-gate MOSFET and double-gate MOSFET is analyzed to evaluate its efficiency of digital circuit.

1.6 Thesis Outline

The remaining part of the work is divided into four chapters, each with multiple sub-sections. Each chapter can be summarized as follows. CHAPTER 2 is a background study in which a literature review was done to study the performance of single-gate and double-gate MOSFET. Also, this chapter explains the effect of the

short channel effect, threshold voltage roll-off and switching delays in single-gate and double-gate MOSFET. CHAPTER 3 begins with the TCAD Software and its various features. It also briefly describes the different tools of the TCAD Software used in the current simulation work. CHAPTER 4 summarizes the analysis of the design of double-gate MOSFET and digital circuit analysis in terms of power consumption and switching delays. CHAPTER 5 concludes the thesis and mentions the scope for future work.

1.7 Summary

MOSFET devices experience a decline in performance due to continuous scaling, leading to significant complications, including short-channel effects (SCEs) and leakage currents. In order to address these challenges, a device known as the double-gate MOSFET has been devised. In order to optimize the performance and density of CMOS technology, a novel MOSFET model has been designed to counter the problem in single-gate MOSFET. Double-gate MOSFET scaling is a conventional method to achieve quicker and smaller circuits with increased current drive. Reducing channel lengths at each succeeding technological node results in enhanced performance and cost savings.

CHAPTER 2

BACKGROUND STUDY

2.1 Literature Review

Single-gate and double-gate MOSFET are three-terminal, four-layer devices comprising gates, sources and drains. The fundamental distinction pertains to the number of gates: the double-gate MOSFET possesses two electrically isolated gates, whereas the single-gate MOSFET possesses only one gate. An electric field is generated when a voltage is supplied to the gates, which induces carrier attraction in the channel region bounded by the source and drain. The gate voltages regulate the current flow between the source and drain by influencing the number of carriers present in the channel.

When both gates are initiated, the operation of a double-gate MOSFET is identical to that of a single-gate device. A mode of operation known as “substrate biassing” is

employed when only one gate is active. Double-gate MOSFET are characterized by reduced source/drain (S/D) capacitance, increased drive for saturated current, diminished short channel effects, scalability to L = 10 nm, subthreshold slopes (SS) that are close to optimal and the ability to alter threshold voltages electrically. The transconductance-to-drain current ratio of the double-gate MOSFET is approximately 1.2% higher than that of the single-gate MOSFET[7][8].

2.1.1 Single Gate and Double Gate MOSFET

The ultimate scalability of MOSFET technology appears to be quite promising when it comes to double-gate MOSFET employing lightly doped ultrathin layers. Numerous theoretical and practical research on this device has demonstrated excellent short-channel effect (SCE) immunity, high transconductance and optimum sub-threshold factor. Figure 2.1 shows the structure of single-gate MOSFET.

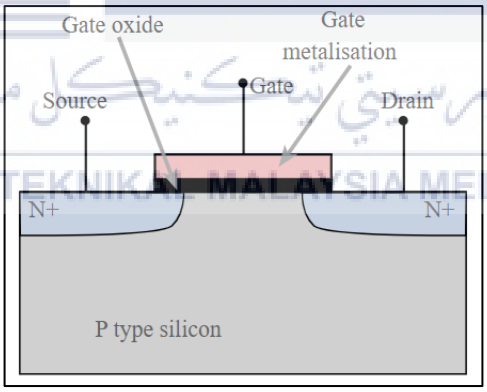


Figure 2.1: Single-gate MOSFET structure[9]

In addition to providing excellent immunity against dopant fluctuation effects that lead to threshold-voltage variation, this structure uses a very thin body to eliminate sub-surface leakage paths between the source and drain. It also benefits from reduced drain-to-body capacitance and higher carrier mobility, which enhances circuit performance. Adjusting the gate material's work function may modify the threshold

voltage of a lightly doped double-gate MOSFET. Figure 2.2 shows the structure of a double-gate MOSFET consisting of top and bottom gates.

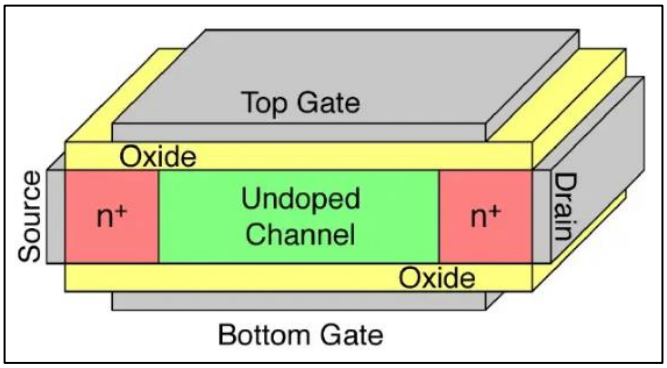


Figure 2.2: Double-gate MOSFET structure[10]

Hisamoto unveiled a self-aligned double-gate MOSFET scalable to 20nm. This type of MOSFET successfully suppresses SCEs, even with a gate length of just 17nm. An appropriate threshold voltage for an ultrathin body MOSFET was provided by the Silicon Oxide and Germanium gate[11]. The gate self-aligns with the elevated source and drain in order to lower the resistance of parasites. Research published by Ali A. Rouji and M. Jagdish Kumar said that the suppression of charge sharing by the inversion layer underneath the side gates caused by the double gate structure substantially reduces the SCEs. According to the suggestions, when the side gate length and main gate length are equivalent, the optimized side gate length condition in terms of SCEs and the hot carrier effect is reached[12]. Besides that, double-gate MOSFET are a viable option for the nanoscale regime. They are appropriate architectures for reducing short-channel effects, according to Pedram Razavil[13]. The gate tunnelling current is a problem in the sub-100 nm range since shrinking the device's dimensions necessitates reducing the oxide thickness. The current leakage from gates grows exponentially as gate oxide (SiO_2) thickness decreases. Using high-k compounds in oxide might be helpful to get over the gate oxide thickness constraint.

A gate oxide stack is preferred because a thicker gate dielectric produces a greater fringing field. Double-gate MOSFET can be configured in two ways, either with a four-terminal (4T) configuration, where the front gate functions as the control electrode independent of the back gate bias and the back-gate bias is fixed, as proposed by Ramesh Vaddi[14]. Double-gate MOSFET come in different varieties: separated gate symmetric double gate, tied gate asymmetric double gate and tied gate symmetric double gate. Different gate voltages, oxide thicknesses for the front and back gates, gate material work functions, or a combination may all be used to create an asymmetrical double-gate MOSFET.

2.1.2 Short Channel Effect in MOSFET

Short-channel effects (SCE) are notable occurrences in MOSFET devices, especially in light of the reduction in channel lengths in contemporary semiconductor technologies. Single-gate MOSFET exhibit multiple manifestations of SCE. Drain-induced barrier lowering (DIBL) is a phenomenon that transpires when the length of a channel decreases, resulting in a diminished effective barrier at the source end[15][16]. Consequently, the threshold voltage is diminished, the subthreshold leakage current increases and the transistor's control is compromised. Another concern is threshold voltage roll-off, which occurs when the transistor is activated at a lower gate-source voltage than intended, resulting in inadvertent leakage current and diminished noise margins. As SCE worsens, the on-current decreases, impacting switching velocities and introducing performance variability to the device[17].

Double-gate MOSFET are engineered to reduce SCE. The gate material is bounded by a three-dimensional channel structure to enhances electrostatic control over the channel and decreases DIBL[15][18]. This improvement decreases leakage current

and increases energy efficiency. Moreover, in a physical gate length, the three-dimensional structure of double-gate MOSFET reduced the effective channel length and minimize the impact of short-channel effects. This lead further scaling of semiconductor technology[15][18]. Consequently, the advancement in scalability of double-gate MOSFET compared to single-gate MOSFET has made huge progress in integrated circuit technology. Figure 2.3 shows the difference between the long and short channels of MOSFET.

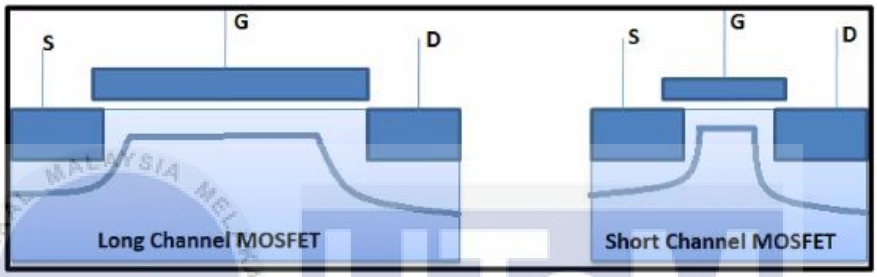


Figure 2.3: Long channel and short channel MOSFET[19]

2.1.3 Threshold Voltage Roll-Off Impact

The threshold voltage is an essential parameter that controls the transition of MOSFET from off to on state. The threshold voltage influences the operational characteristics of single-gate and double-gate MOSFET directly. It affects leakage current, power consumption and switching speed in device performance.

Single-gate MOSFET requires higher gate-source voltage to transition from the off to the on state as threshold voltage increases. It causes the increases in power consumption[20]. On the other hand, a lower threshold voltage will operate transistors at a lower gate-source voltage, which may lead to a decrease in power consumption. The lower threshold voltage potentially increases the leakage current during the device not operating. The adjustment within threshold voltage, power consumption and

switching speed is essential when developing integrated circuits that meet good performance criteria.

Double-gate MOSFET illustrates how it has surfaced as a solution for the drawbacks of single-gate MOSFET. Double-gate MOSFET enhanced the modelling of the transistor's behavior by precisely manipulating threshold voltage[21]. By decreasing threshold voltage in double-gate MOSFET, an enhanced switching speed and decreased power consumption can be achieved. These are an important benefit for cutting-edge semiconductor technologies. The semiconductor industry has been transformed by the precise electrostatic regulation assisted by the adjustable threshold voltage of double-gate MOSFET. This innovation has allowed a good energy-efficient and high-performing devices designed.

A thorough understanding of the threshold voltage is critical when it comes to the design of semiconductor devices. A comprehensive analysis of semiconductor devices, including MOSFET and properties, provides engineers and researchers with valuable information on how to manipulate threshold voltage to achieve performance objectives[22]. Engineers frequently use the comprehension in semiconductor devices to optimize and trade-off among leakage current, speed and power. The threshold voltage being an important engineering parameter in compromising the parameters. In order to fulfil the specifications of integrated circuits, engineers and researchers play with threshold voltage and take into account variables including power consumption, switching speed and leakage current.

2.1.4 Switching Delays Effects Performance

The principal cause of switching delays in MOSFET is the reciprocating current through the parasitic capacitors[23]. This remains true for MOSFET with single and

double gates. When the efficiency of a single gate MOSFET is maintained at the nanometer scale, the following issues occur interface coupling, channel orientation, channel mobility, leakage current, switching latency and latch-up. Further parameters, including but not limited to short channel effects such as drain-induced barrier leakage, gate-induced barrier leakage, body effect, hot electron effect, punch-through effect, surface scattering, impact ionization, subthreshold swing and volume inversion, influence the drive current to decrease leakage current to increase[24].

Conversely, it has been observed that double-gate MOSFET exhibit superior performance in these parameters when compared to that of presently available single-gate MOSFET. Double-gate MOSFET depend on the investigation of innovative materials with enhanced mobility channels. Before attempting to gain a foundational comprehension of the switching behavior of a MOSFET, it is most beneficial to examine the device in a state of isolation, devoid of any external influences. Two input capacitors (C_{gs} and C_{gd}) and an internal gate resistance (R_g) constitute the equivalent circuit of the MOSFET gate. It is possible to evaluate the switching behaviour of the MOSFET in a practical application circuit, proving that double-gate MOSFET have higher switching speeds than single-gate[25].

2.2 Past Work

Patnaik's research compared the electrical properties of three varieties of MOSFET: bulk, silicon-on-insulator and double-gate[26]. Compared to the other two categories of MOSFET, the double-gate MOSFET demonstrated superior drain current, transconductance and subthreshold slope performance. The double-gate MOSFET demonstrated low leakage current and capacitance. The study showed that

double-gate MOSFET is a promising technology for developing future electronic devices.

Faysal Al Mahmud research on the “Comparative study on single-gate MOSFET and double-gate MOSFET” compared the efficiency between single-gate MOSFET and double-gate MOSFET[27]. The research result proved the superior performance and energy efficiency of double-gate MOSFET over single-gate MOSFET. Double-gate MOSFET has low subthreshold slope, higher on-and-off ratio and low leakage current compared to single-gate MOSFET. These benefits allow to increase operating rates, decrease power consumption and enhance digital circuit performance.

The electrical properties of two varieties of MOSFET, bulk and Silicon-on-Insulator (SOI) by Aziz found that the SOI MOSFET had superior electrical properties to the Bulk MOSFET[28]. It was proven the SOI MOSFET has low threshold voltage, high drain current and higher transconductance.

Patel study on the performance of double-gate and silicon-on-insulator MOSFET by varying device parameters found that the double-gate MOSFET has better electrical performance than the SOI MOSFET[29]. It shows a higher drain current, lower threshold voltage and improved subthreshold slope in double-gate MOSFET. Additionally, the double-gate MOSFET is less sensitive to changes in device parameters such as gate oxide thickness and channel length. Meanwhile, Ishraqul Huq, 6-transistor Full Adder Circuit constructed with low-power MOSFET and double-gate FinFETs, which employ PTM 32 nm technology analyzed the efficiency of circuit [30][31]. It proved that the double-gate FinFET-based Full Adder Circuit performed better in terms of power and delay.

Aakansha's study on a novel double-gate MOSFET architecture as an inverter compared to conventional MOSFET-based inverters[31]. The study proposed by double-gate MOSFET shows an enhanced performance in terms of reduction in propagation delay, low power consumption and increased noise immunity.

Aditya on first study examined the design and performance of advanced MOSFET structures, such as nanowire MOSFET, FinFETs and Tunnel FETs discovered that these advanced MOSFET structures had superior electrical performance compared to conventional MOSFET[32]. The advanced device reduced leakage current and enhanced on-state current. The second study show that the FinFET demonstrated good drain current and transconductance efficiency compared to other advanced MOSFET structures[33]. Both studies show that advanced MOSFET structures can enhance circuit performance.

Rajesh Kumar suggested a power-efficient full adder circuit using double gate MOSFET in 45nm technology redesigned transmission gate and XOR gate to decrease power consumption and latency[34]. The author suggested an architecture that offers significant power consumption and delay reductions over conventional solutions.

Ankita Wagadre's paper "Design & Performance Analysis of DG-MOSFET for Reduction of Short Channel Effect over Bulk MOSFET at 20nm" presented a study on the use of double-gate MOSFET to reduce Short Channel Effects(SCE) in bulk MOSFET[4]. The research showed the design and analysis of various parameters, including gate capacitance, sub-threshold slope, leakage current and threshold voltage. The results demonstrated that double-gate MOSFET outperforms bulk MOSFET in decreasing SCE and enhancing device characteristics.

Surya's investigation involved the design and performance evaluation of a 20nm Double-Gate Silicon-based MOSFET[35] showed the proposed double-gate MOSFET demonstrated enhanced performance. Furthermore, the double-gate MOSFET has higher drain current and transconductance with reduced subthreshold slope and lower threshold voltage.

2.3 Summary

Since its establishment nearly fifty years ago, the semiconductor industry has been guided by Moore's Law. FinFETs, Nanowire FETs and double-gate MOSFET are just a few of the new transistor topologies that have improved performance and energy efficiency. Because of double-gate MOSFET, a condensed model accounting for critical physical phenomena may now be used in IC design. Double-gate MOSFET devices provide increased noise immunity, more precise regulation of threshold voltages and lower power consumption when designing logic circuits. A full-adder circuit using double-gate MOSFET has been presented to reduce power consumption. At the 20nm technological node, double-gate MOSFET can also mitigate Short Channel Effects in bulk MOSFET, making them ideal for low- and high-performance uses. Thus, this project aims to design and simulate a 14nm double-gate MOSFET and study its efficiency in a digital circuit.

CHAPTER 3

METHODOLOGY

3.1 Silvaco TCAD

Silvaco TCAD is a collection of simulation tools employed to develop and enhance new semiconductor processes and devices before manufacturing. It forms a crucial part of the Design Technology Co-Optimization (DTCO) process, which aims to enhance designs across various areas such as layout, process, device, SPICE and RC extraction. Integrating TCAD with SPICE in a comprehensive DTCO environment provides actionable insights for optimizing circuit designs. Using Silvaco makes conveying device and process modifications easier, enabling clear communication of potential performance enhancements while reducing manufacturing time.

Additionally, Silvaco offers a comprehensive environment for schematic-driven analogue, mixed-signal and RF circuit design, layout and analysis.

Two kinds of input files are utilized in Silvaco: a text file containing commands for Atlas and a structure file containing the definition of the simulated structure. Atlas output files are of three distinct varieties. First, the runtime output, which displays error and warning messages during the simulation, becomes available once the input has been imported. Second, a file containing voltage and current logs. Lastly, the structure file in which two-dimensional and three-dimensional data on the values of solution variables is stored.

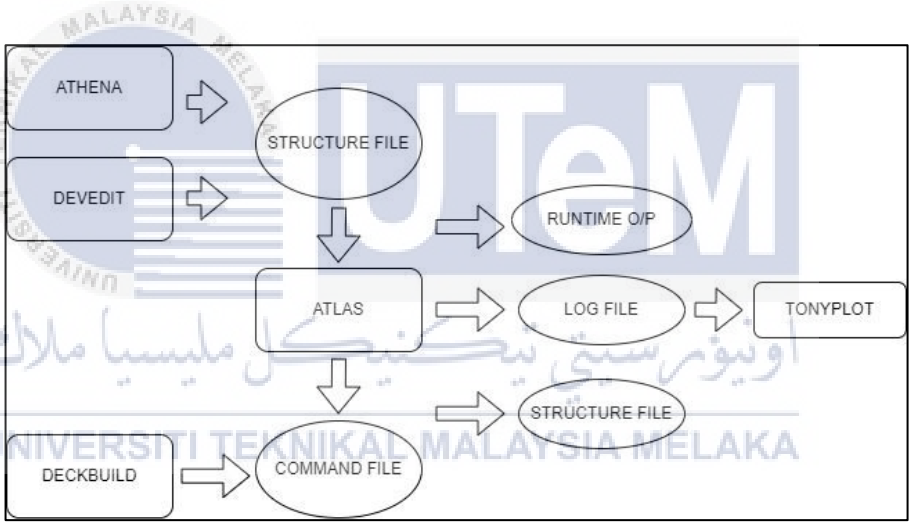


Figure 3.1: Atlas data flow

The data progress throughout the simulation is depicted in Figure 3.1. The output of Deckbuild, Devedit and Athena is sequentially appended to the structure file and command file before being appended to the log file, which also contains the output. It displays the O/P at runtime. The structure's specifics are captured in the Tonyplot.

3.2 Double-Gate MOSFET Design

In the context of a double-gate MOSFET, both gates are positioned symmetrically to span the channel at the opposite end of the pair. The formation of the channel occurs close to the gate. Symmetric double-gate MOSFET refers to a device in which both gates are connected to identical potential and possess the same dimensions. Figure 3.2 shows the simple structure of double-gate MOSFET, whether n-type or p-type.

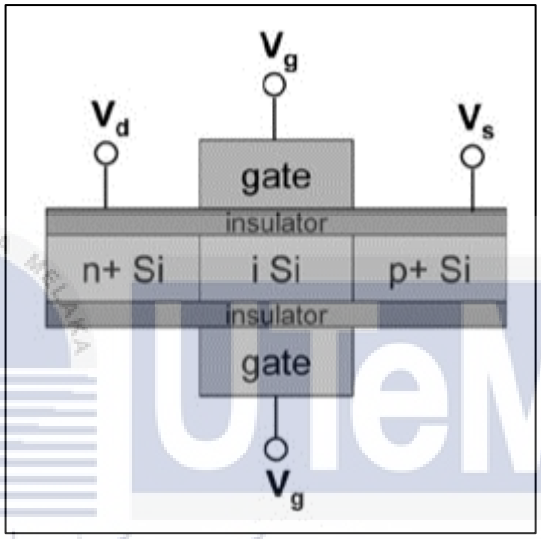


Figure 3.2: Simple double-gate MOSFET structure[36]

3.2.1 Flowchart

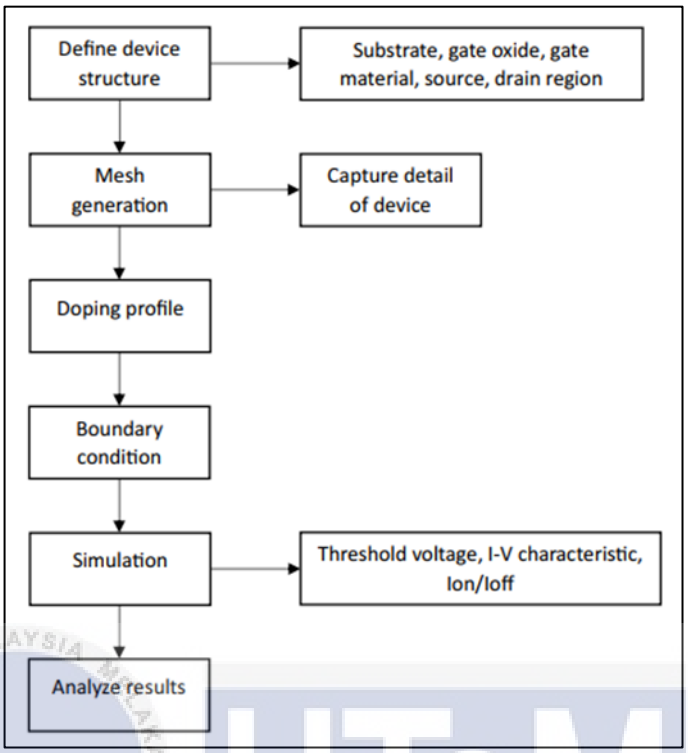


Figure 3.3: Double-gate MOSFET design flow

Figure 3.3 above shows the flow of the design process in Silvaco. Before designing double-gate MOSFET, the device structure needs to be identified, such as device substrate, gate oxide, gate material, source and drain region, which need to be specified. Then, the details of double-gate MOSFET are captured by using mesh generation. Mesh generation plays a crucial role in device simulation when utilizing Silvaco's TCAD software suite to represent complex physical phenomena occurring in semiconductor devices accurately, including but not limited to electrical fields, current flow and heat dissipation. Mesh generation ensures accurate simulations by partitioning the device structure into small sections.

Additionally, a well-constructed mesh improves computational efficiency, especially in regions where physical phenomena are most complex. In semiconductor

devices, it is critical to utilize an accurately calibrated mesh that can comprehensively depict these structures and encapsulate every facet of the device's operation.

Doping profiles are important in the design of double-gate MOSFE. These parameters adjust the electrical characteristics of the semiconductor material, which are needed to establish the p-type and n-type regions of the device. The highly doped source and drain regions needed for efficient carrier injection and collection are produced during the doping process. Additionally, it is important to establish the threshold voltage of the double-gate MOSFET. This allows engineers to design devices such as high-speed or low-power operation devices. The reduction in device dimensions necessitates the implementation of a carefully planned doping profile to reduce short-channel effects. This will improve the performance and scalability of miniaturized circuits.

Moreover, a correct doping profile will reduce leakage currents, an essential consideration for low-power applications. It also enhances the device's dependability by affecting voltages and hot carrier injection. This underscores the indispensable function of doping profiles in semiconductor devices efficient design and operation.

Then, the device was simulated to obtain threshold voltage, I-V characteristic and I_{ON}/I_{OFF}. This parameter is observed to analyze the device's parameters to enhance performance.

3.2.2 Material

3.2.2.1 Silicon

Silicon, the most commonly utilized semiconductor material in the electronics industry, is the second most abundant element in the Earth's crust. Its durability and

distinctive electrical properties, including a comparatively small bandgap, render it highly suitable for semiconductor integration. Doping is introducing additional elements into silicon to modify its electrical characteristics. Additionally, silicon is suitable for high-temperature applications due to its high melting point. Deposition of numerous layers of material, including silicon, is required in the fabrication of semiconductors in order to produce essential components such as resistors, diodes and transistors. On the contrary, silicon is frequently favored owing to its economical nature and ability to withstand high temperatures. Figure 3.4 shows the initial deposition of silicon into a substrate with boron doping to create an n-type double-gate MOSFET.

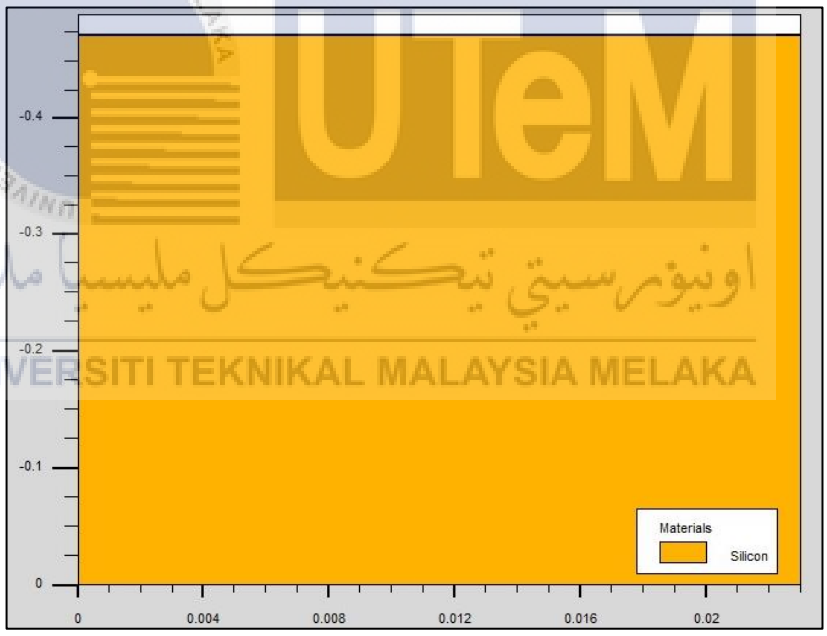


Figure 3.4: Initial silicon substrate

3.2.2.2 Silicon Dioxide

Silicon dioxide growth is a critical step in producing MOS transistors. The semiconductor industry finds SiO_2 attractive due to its facile deposition on various materials and thermal growth on silicon substrates. While exhibiting resistance to

numerous chemicals commonly employed in the etching process of other materials, it can still undergo selective etching with specific chemicals or dry etching using plasmas. It can obstruct the implantation of ions or the diffusion of numerous undesirable impurities. It is an exceptional insulator with a wide band gap and a high dielectric strength. Its high-temperature stability of 1600 degrees Celsius makes it a material suitable for device and process integration. Figure 3.5 shows the process of silicon dioxide growth in the process flow to stack the oxide.

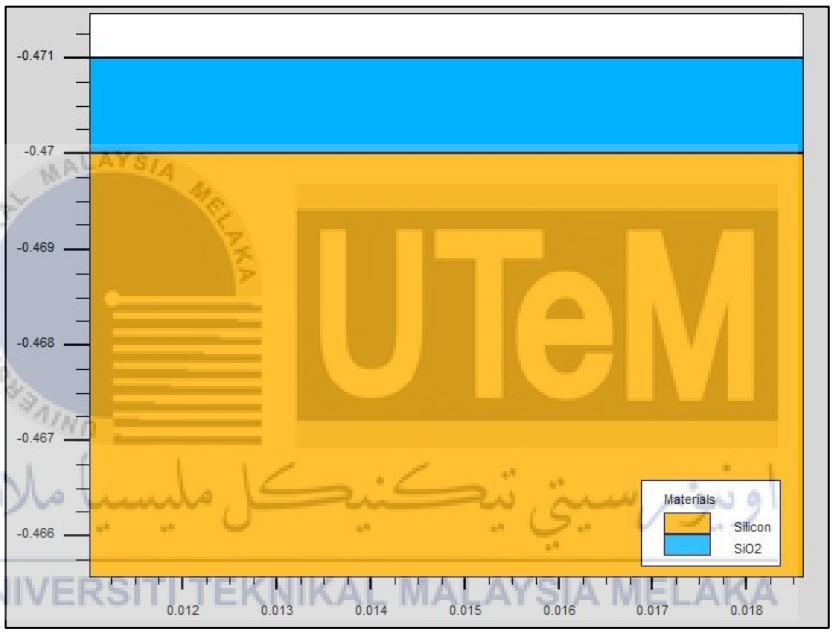


Figure 3.5: Silicon dioxide growth in the process flow

3.2.2.3 Hafnium Dioxide

The charge impurity scattering can be diminished due to the greater screening effect exhibited by high-k materials. Furthermore, the charge control of the channel can be enhanced by leveraging the larger gate capacitance of high-k materials by using Hafnium Dioxide (HfO_2) as a high-k material, which possesses excellent thermal and electrical properties. High-K dielectrics are highly electrically advantageous due to their exceptionally high permittivity, including those composed of hafnium-based

substances. There is an assumption that HfO_2 exhibits greater efficacy in mitigating short-channel effects, including but not limited to leakage current and I_{ON}/I_{OFF}ratio. This contributes to the achievement of a minimal leakage current. The permittivity of high-K dielectric materials is directly proportional to the I_{ON} of those materials. The I_{ON} value increases when high-K dielectrics with a greater permittivity are utilised as gate insulators. The decrease in depletion can be attributed to the reduced boron absorption when high-K dielectrics with higher permittivity are employed as gate insulators. Increasing the gate oxide's physical thickness while maintaining a constant equivalent oxide thickness (EOT), high-K dielectrics effectively inhibit gate tunnelling. Figure 3.6 shows the deposit of HfO_2 into the design of double-gate MOSFET.

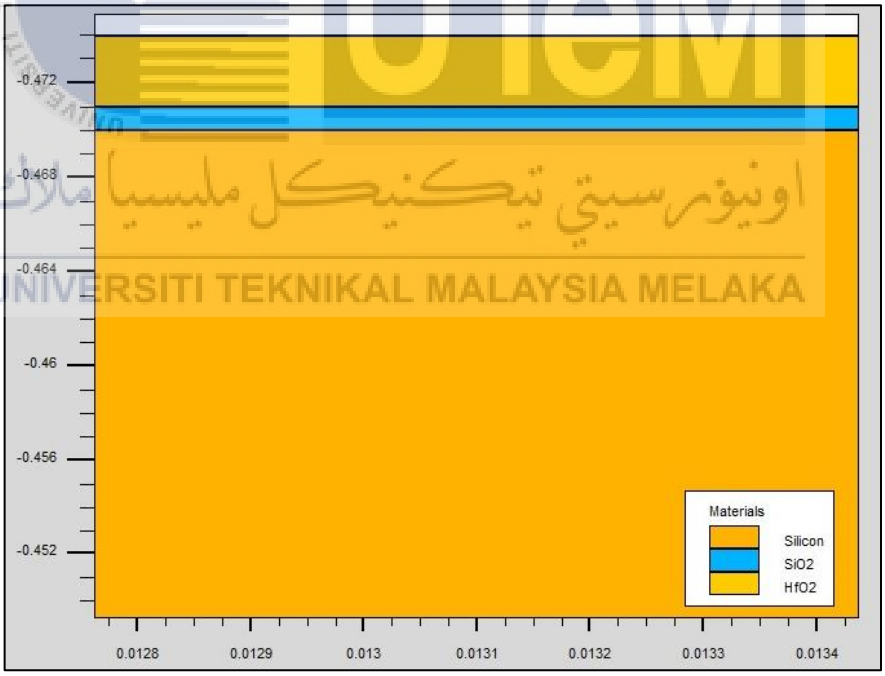


Figure 3.6: Deposit of $\boldsymbol{HfO_2}$

3.2.2.4 Titanium Silicide

Titanium silicide (TiSix) is a feasible substance to be utilised as the gate electrode in n-type MOSFET because of its beneficial characteristics. The low resistivity is crucial

to enables a faster switching and efficient current flow. This will reduce latencies and increase the transistor's speed. The material effectively injects electrons into the n-type channel due to its well-aligned work function with n-type MOSFET. The good thermal stability of TiSix is important, as it guarantees consistent performance with high temperatures frequently encountered during semiconductor process. The compatibility of TiSix with silicon technology, establishes a sturdy interface with the silicon substrate. This is a critical factor to ensure the overall performance and dependability of the device. Significantly, with the ongoing trend towards miniaturisation in semiconductor devices, the scalability of TiSix display it well-suited for contemporary, compact n-type MOSFET.

The practicality and appeal for large-scale production, let the integration of TiSix into established manufacturing processes easier and it is cost-effective. Titanium silicide is a highly promising material for the gate electrodes of n-type MOSFET due to its work function, low resistivity, silicon compatibility, scalability and cost-effectiveness. These attributes significantly contribute to the double-gate MOSFET enhanced performance, efficiency and reliability. Figure 3.7 shows the deposition of titanium silicide as top gate and bottom gate material.

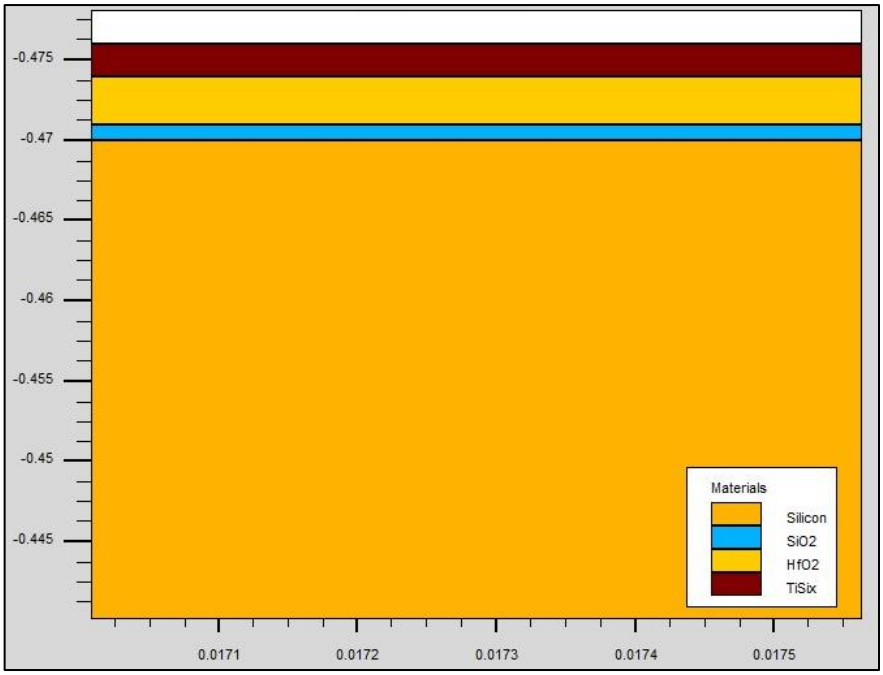


Figure 3.7: Titanium silicide deposition

3.2.3 Device Process

The modelling approach relies on utilising the Silvaco ATHENA module, a simulation tool designed to teach fundamental skills in two-dimensional simulation of semiconductor processing. All fabrication procedures were based on prior research related to high-K/Metal gate technology[37]. By using Silvaco, a double-gate MOSFET featuring a 14nm gate length was designed. With a similar workflow involving transistor complementary processes, the fabrication steps were fine-tuned to achieve the desired outcome by adjusting certain process parameters in doping density range referring to the International Roadmap for Devices and Systems (IRDS).

A silicon wafers with orientation of 100 and a p-type boron-doped orientation employed as the primary substrates. A boron doping level of 1x10^{14} atoms/cm^3 was introduced into the silicon substrate. This implantation was conducted with 20 keV energy and a 10° tilt, resulting in a threshold voltage implant of 1.13x10^{13} atoms/cm^3. A 1nm silicon dioxide was deposited onto the substrate with 3nm of HfO_2 was

deposited as the high-K dielectric material to attain the desired threshold voltage. The size of TiSix adjusted to 14nm aligned with gate length functions as the metal gate. The source/drain (S/D) implantation involved injecting $1x10^{17}$ atoms/cm3 of arsenic into the p-type substrate. This creates a highly n-type doped region within the substrate. Finally, the 14 nm NMOS structure was etched to aluminium metal to complete the device. Figure 3.8 shows the design of a 14nm gate length double-gate MOSFET.

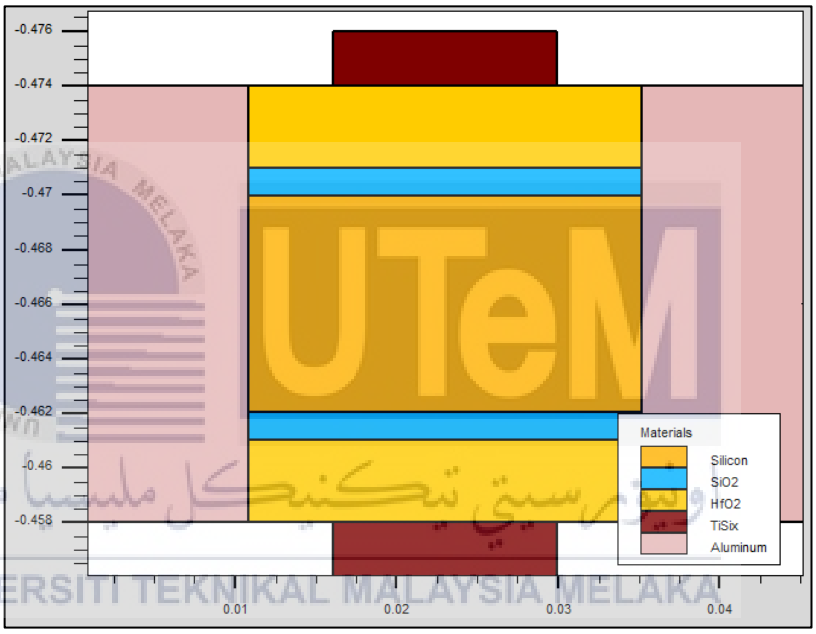


Figure 3.8: 14nm gate length double-gate MOSFET

The expected performance of the 14nm n-type MOSFET should align with the 2022 International Roadmap for Devices and Systems (IRDS) predictions regarding the device's behaviour. Adherence to a specific international standard is mandatory for a particular design. Altering the dosage, energy levels and implantation angles of these processes could lead to a decline in the electrical properties of the FET device, including parameters like V_{TH}, I_{ON}, I_{OFF} and SS.

Statistical methodologies are frequently employed to enhance the overall performance of electronic devices, necessitating careful consideration of all device characteristics. Keeping the channel thickness narrow and thin is advisable to minimise leakage current, facilitating the device's operation in depletion modes[38]. Consequently, controlling process parameters like doping concentration becomes crucial, significantly influencing device performance. Table 3.1 summarises the input parameters used in this process.

Table 3.1: Device input parameters

Parameters	Value
V_{TH} implant dose	1.13x10^{13} atom/cm3
V_{TH} implant energy	20 keV
V_{TH} tilt angle	10°
S/D implant dose	1x10^{17} atom/cm3
S/D implant energy	2 keV
S/D implant tilt angle	77°

3.3 LTSpice

LTSpice is a free circuit simulation application developed by Analogue Devices. Before committing to manufacturing, it assists electronic engineers in gaining a thorough comprehension of the behavior of a circuit, which is an invaluable ability. The subsequent are several prevalent analyses that are accessible in LTspice.

1. Transient analysis - The time domain behavior of a circuit is more significant than its stable state. When a circuit transitions between two states, such as power-up, the designer can determine whether the start-up behavior conforms to expectations and falls within the design margins and implement and validate any necessary modifications.
2. DC sweep - This function permits the incremental increase of a source or parameter over a specified range. Determining a circuit's secure operating range is a frequent application of this.
3. Monte Carlo Analysis – This function permits the investigation of the impact of component tolerances. It denotes a collection of concurrent simulations, frequently yielding worst-case data. It empowers a designer to ascertain whether the current component tolerances are adequate to maintain the circuit's functionality within specifications or whether they are accumulating and generating conditions that deviate from the intended range.

The functions listed above are among the most frequently utilized ones in LTspice.

3.4 Cadence (PSPICE)

PSpice SPICE simulation technology, renowned for its native analogue and mixed-signal engines, provides a comprehensive circuit simulation and verification solution. It adapts to the evolving simulation requirements of designers throughout different stages of the design process, from initial exploration to detailed development and verification. When used alongside PSpice A/D, the PSpice Advanced Analysis feature enhances designers' ability to boost product yield and reliability. PSpice offers a virtual simulation platform with the most extensive model library, enabling designers to prototype using top-tier analogue, mixed-signal and advanced analysis engines.

This platform supports analyzing and refining straightforward and complex systems, including their components and parameters, before progressing to layout and fabrication. Cadence PSpice A/D merges leading analogue and mixed-signal engines, offering a total solution for circuit simulation and verification tailored to the dynamic needs of circuit designers.

3.5 Double-Gate MOSFET Model

Silvaco Utmost IV was used to extract the device parameter using Atlas and Athena. The extracted device parameter was used to model double-gate MOSFET in Pspice by associating the device SPICE model with the model. Figure 3.9 shows that the spice model has been extracted from Silvaco to model the double-gate MOSFET at Level 3.


```
*---------- DGMOSFET Spice Model ----------
* TERMINALS : D G S
* Editor : Kenny
.SUBCKT DGMOSFET 1 2 3
.MODEL MOS N MOS
+ LEVEL=3
+ L=14n
+ W=20n
+ KP=2.00E-06
+ RS=10.000E-3
+ RD=0
+ VTO=0.23
+ RDS=60.000E6
+ TOX=4n
+ CGSO=124p
+ CGDO=8p
+ CBD=0
+ RG=0
+ N=2
+ RB=0
+ GAMMA=0.8
+ ETA=0.0015
+ KAPPA=0
+ NFS=0
.ENDS
```

Figure 3.9: Double-gate MOSFET Spice model

SPICE simulators employ different types of device models, which can be categorized into three groups:

1. First Generation Models (Level 1, Level 2 and Level 3 models)

2. Second Generation Models (BISM, BSIM2 and HSPICE Level 28)

3. Third Generation Models (Level 7, Level 48, BSIM3 and more)

Level 3 modelling used in double-gate MOSFET is relatively simple compared to 2nd and 3rd generation SPICE model. The simplicity is advantageous in specific scenarios, especially for academics purposes and simple. Level 3 models actually maintain the compatibility with the existing simulators that have already been employed, simplifying the process and ensuring data consistency. These models provide quicker simulation results compared to 2nd and 3rd-generation models and it is preferred choice for critical speed computational.

Figure 3.10 shows the double-gate MOSFET part associated with the spice model in Pspice for digital circuit simulation.

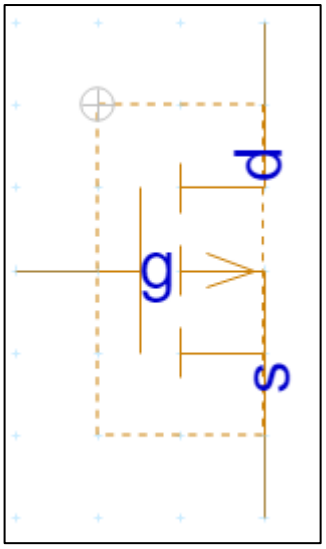
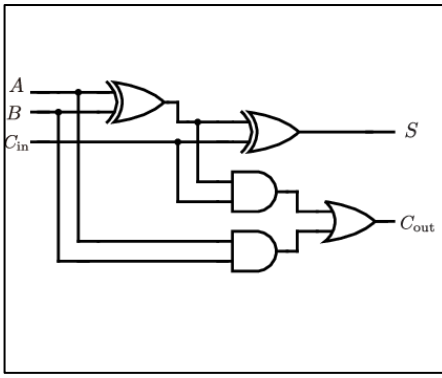


Figure 3.10: Double-gate MOSFET model part

3.6 Full Adder

In computers, a full adder is a digital logic circuit used to compute the sum of three binary inputs and generate two outputs. Typically, these three inputs consist of two integers to be added and a carry from the preceding bit. The carry to the subsequent bit and the aggregate of the three inputs comprise the two outputs. Implementing a full adder with NAND or NOR gates, two half-adders and an OR gate is also possible. They are utilized in circuits where multi-bit addition is required. Full adders have benefits such as adaptability, the capability to process and convey information and rapid operation.

Full adders hold significant importance within computer engineering and digital logic. Incorporating three pieces of information into their design renders them more versatile than half-adders. Their exceptionally rapid operation qualifies them for implementation in high-speed digital circuits. The full adder consumes comparatively less power than the half adder. Figure 3.11 shows the sample circuit of a full adder using logic gates and the truth table of a full adder.



Inputs			Outputs	
A	B	C_{in}	S	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Figure 3.11: Full adder and truth table[39]

3.6.1 Single-Gate MOSFET Full Adder Design

Full adder circuits for single-gate MOSFET have been constructed in LTspice using 11 MOSFET (11T). A 16nm technology node MOSFET was used to design the circuit with a width of 40nm for NMOS and 80nm for PMOS with a supply voltage of 0.85V. A 16nm technology node MOSFET was chosen in this project because as the gate length scales down to 22nm, the semiconductor industries venture into 14nm technology. By the year 2014, all 14nm technology nodes were used to mass produce FinFET, a type of multi-gate transistor. Then, the semiconductor industries introduced a 16nm technology node for MOSFET as the next technology node after 22nm and continued with a 12nm technology node. By comparing the 12nm and 16nm technology nodes, a 16nm technology node was chosen as it has the lower threshold voltage compared to 12nm, which is 0.85V and 1.8V, respectively. Thus, a 16nm technology node was chosen for single-gate MOSFET to run the full-adder circuit.

CMOS circuit design has a notable design choice where PMOS transistors are about 2.5 times larger than NMOS transistors. This is not a random decision, as it is deeply rooted in the physics of how these components work. The crux of the matter lies in the difference in mobility between electrons and holes. Electrons, the charge carriers in NMOS, move faster than holes, the charge carriers in PMOS. This ensures that both

transistors can conduct the same amount of current, which is crucial for the circuit's efficiency and power consumption. Figure 3.12 shows the full adder design constructed in LTspice.

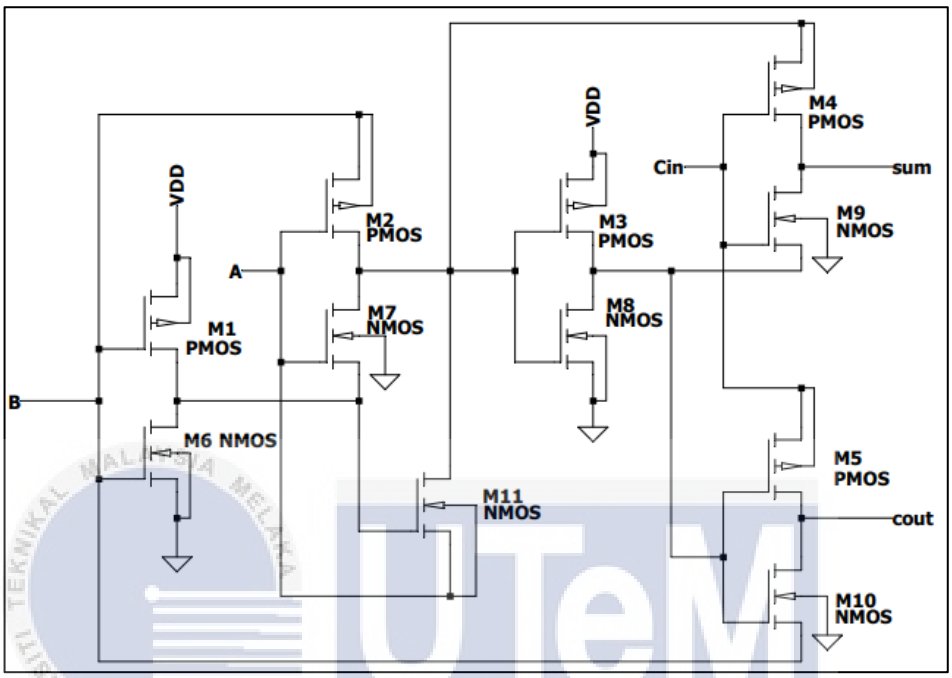


Figure 3.12: Single-gate MOSFET full adder design

3.6.2 Double-Gate MOSFET Full Adder Design

Full adder circuits for double-gate MOSFET have been constructed in Pspice using 8 MOSFET (8T). The design double-gate MOSFET was used to design the circuit and virtual PMOS at the 14nm technology node to synchronize with the design n-type double-gate MOSFET. Figure 3.13 shows the full adder design constructed in Pspice.

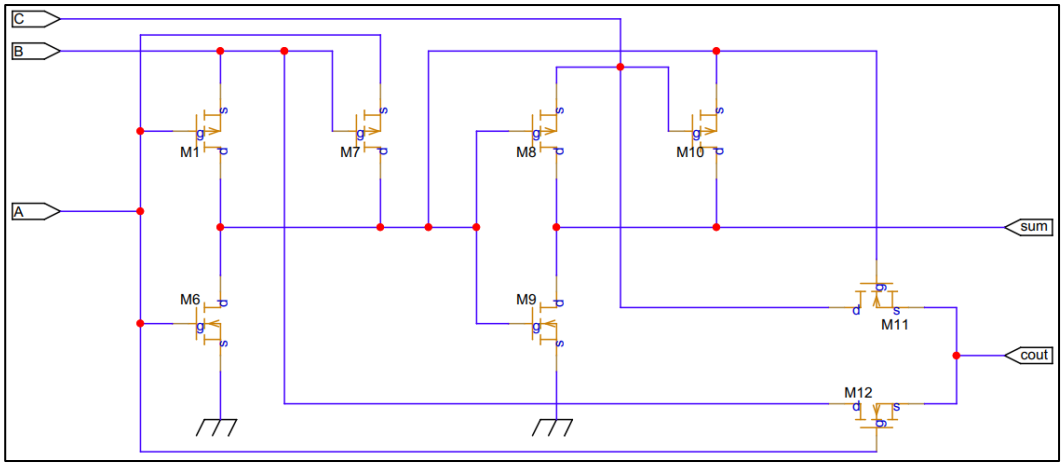


Figure 3.13: Double-gate MOSFET full adder design

3.7 Summary

Silvaco TCAD used to design and simulate a double-gate MOSFET at the 14nm scale. The device structure had identified, such as device substrate, gate oxide, gate material, source and drain region, which need to be specified before the simulation. Doping profiles adjusted for the electrical characteristics of the semiconductor material, which are needed to establish the p-type and n-type regions of the device. Materials such as silicon, hafnium dioxide and titanium silicide deposited into the device during the virtual fabrication process. The extracted device parameters are then used to generate SPICE model for double-gate MOSFET to simulate digital circuit . Finally, analysis in term of power, delays and area has been carried out to evaluate the performance of digital circuit.

CHAPTER 4

RESULTS AND DISCUSSION

4.1 Design Double-Gate MOSFET

Silvaco ATHENA module and Atlas module used to model double-gate MOSFET. Both gates were positioned symmetrically to span the channel at the opposite end of the pair and the formation of the channel occurred close to the gate. The double-gate MOSFET featuring a 14nm gate length was designed by depositing silicon as substrate, hafnium dioxide and silicon dioxide as stacked oxide with titanium silicide as metal gate.

Figure 4.1 shows the completed device for 14 nm n-type double-gate MOSFET. Meanwhile, Figure 4.2 shows the measurement of the material. Figure 4.3 shows the doping profile of the completed device and Figure 4.4 shows the cutline of the device. Lastly, Table 4.1 summarizes the data for the n-type double-gate MOSFET design.

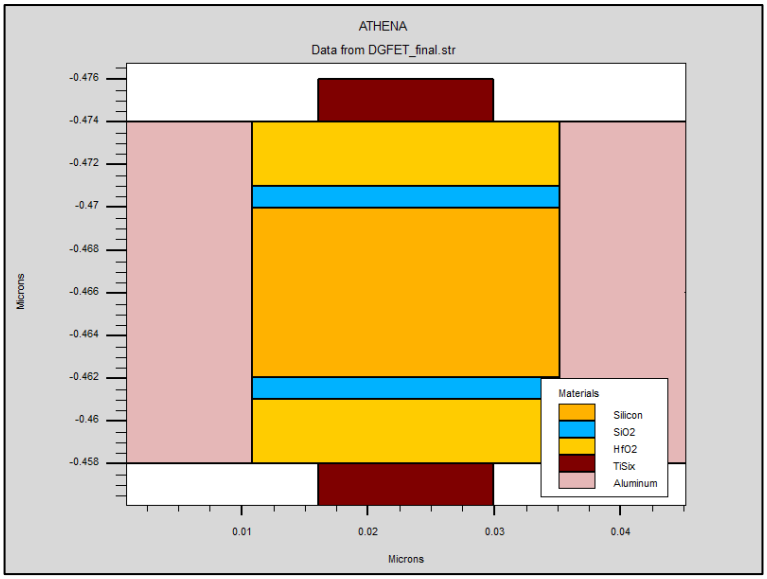


Figure 4.1: 14 nm n-type double-gate MOSFET

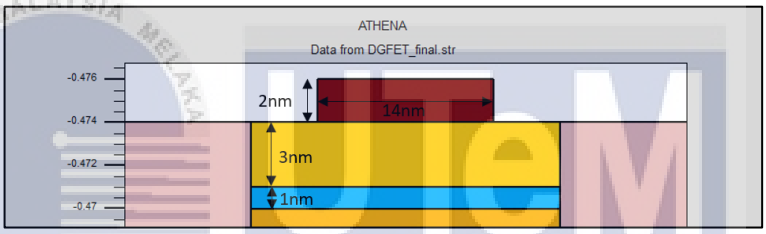


Figure 4.2: Double-gate MOSFET measurement

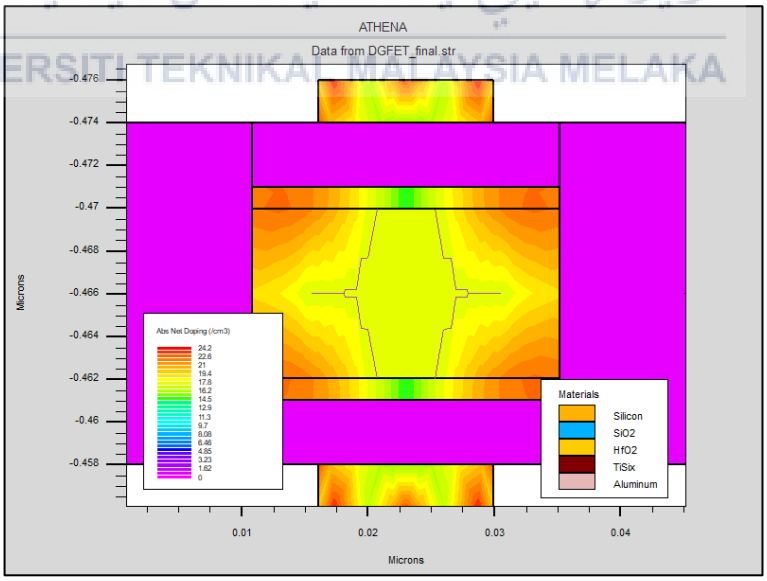


Figure 4.3: Doping profile

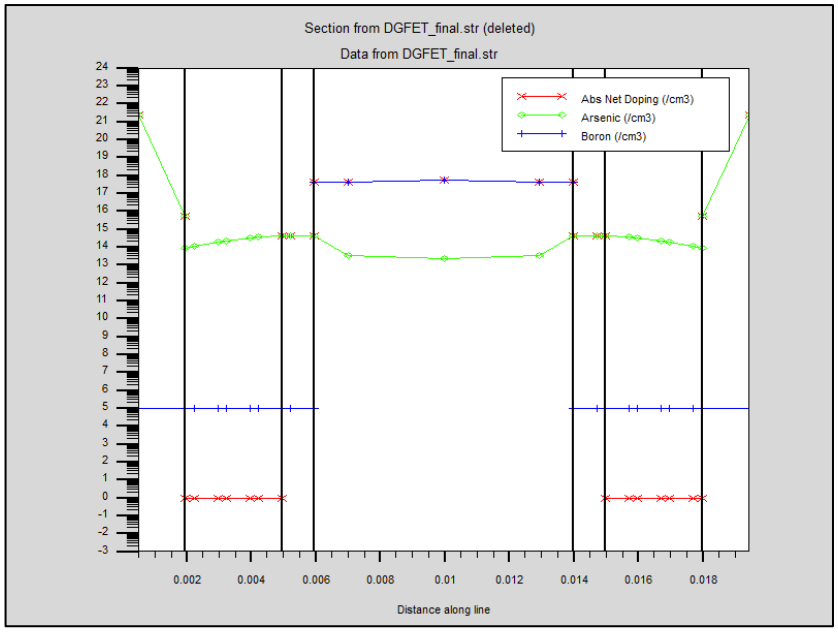


Figure 4.4: Device Cutline

Table 4.1: Fabrication Recipe Summary

Process Step	n-type MOSFET parameters
Silicon Substrate	<100> orientation
Threshold Voltage adjusts implant.	• 1.13×10^{13} Boron • 20keV implant energy • 10° tilt • 30 rotations
Stacked Oxide Deposition	• 1nm SiO_2 • 3nm HfO_2
Metal Gate Deposition	• 2nm TiSix
Source/drain implantation	• 1.17×10^{17} Arsenic • 2keV implant energy • 77° tilt • 60 rotations
Aluminums deposition	10nm

4.2 Device Simulation

The ATLAS module is employed to predict the electrical characteristics of specific device configurations and offers a comprehensive understanding of the device's internal physical structure relevant to its functionality. In the case of transistor simulation, the ATLAS module is utilized to simulate the electrical behavior of the transistor. Figure 4.5 displays the relationship between drain current (I_{DS}) and gate voltage (V_{GS}) for the device.

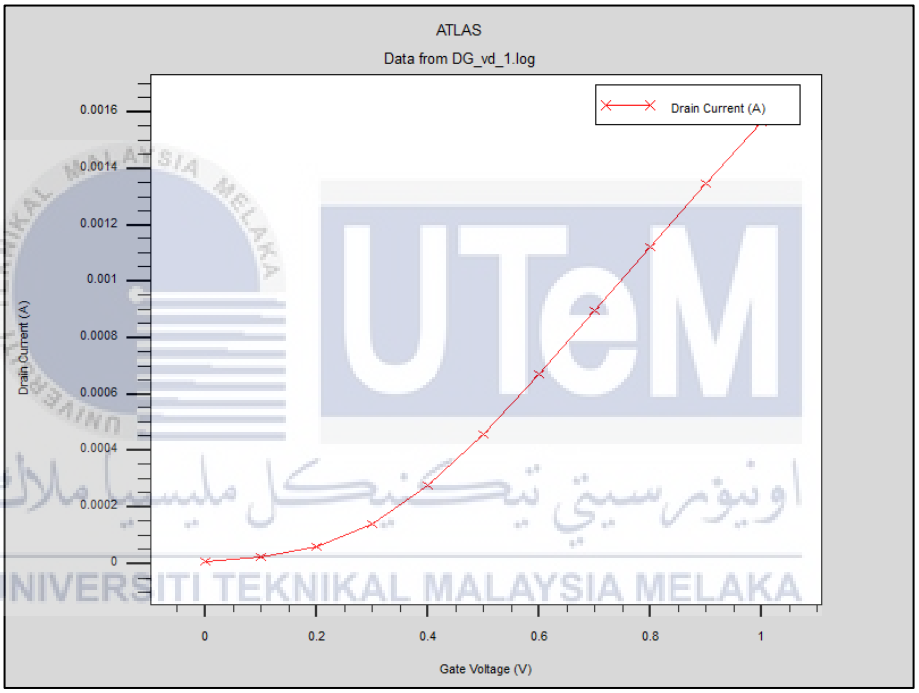


Figure 4.5: $\boldsymbol{I_D}$ *vs* $\boldsymbol{V_G}$

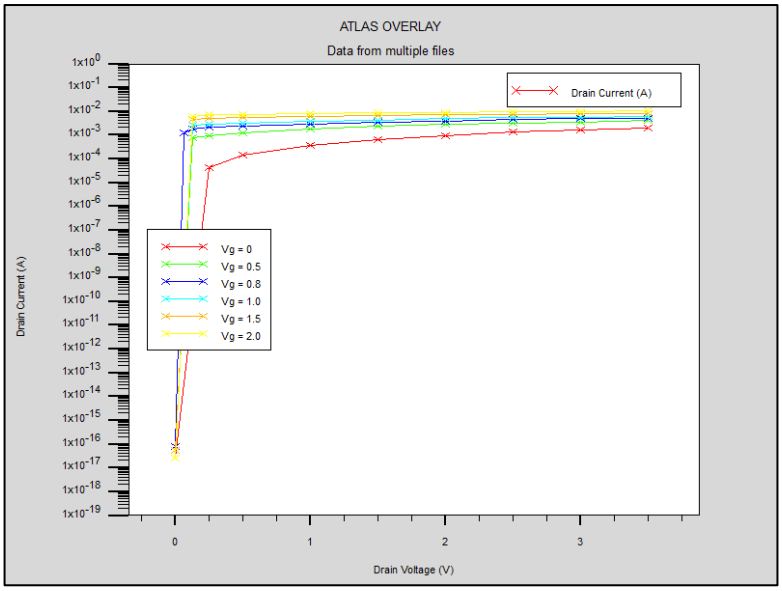


Figure 4.6: $\boldsymbol{I_D}$ *vs* $\boldsymbol{V_D}$

Figure 4.6 shows the double-gate MOSFET characteristics, the drain current ($\boldsymbol{I_D}$) versus the drain voltage ($\boldsymbol{V_D}$) for different gate voltages ($\boldsymbol{V_G}$). The device behaves like a resistor as the drain current increases linearly with the drain voltage, showing that the double-gate MOSFET is in the linear region. However, at higher drain voltages, the curves flatten out and the double-gate MOSFET enter the saturation region. In this region, the drain current becomes relatively constant and the MOSFET operation is similar to an amplifier.

A small subthreshold leakage can be observed as there is a small amount of current flowing with low drain voltage in the curve near the origin. This subthreshold leakage is more common in modern MOSFET, especially as device length shrinks and it can only be minimized and cannot be removed completely.

Meanwhile, Figure 4.7 contains data for each drain current loaded, along with the incremental changes in gate voltage applied. During the simulation, the drain voltage (V_D) is fixed at 0.05V and the gate voltage (V_{GS}) is systematically increased in 0.05V

increments from 0V to 1V. A small drain voltage is given to analyze the subthreshold behavior and leakage current. This will accurately model and analyze the subthreshold slope and leakage current that are crucial for low power and digital applications. The graph reveals that V_{TH} (threshold voltage) is measured at 0.225V, which aligns well with the IRDS 2022 predictions. This is particularly satisfying as the V_{TH} value remains within 16% of the expected 0.271V threshold voltage. This indicates that factors such as the physical dimensions of the doping channel, surface profile and oxide gate thickness could influence I_{ON} (on-state current), are well within acceptable limits.

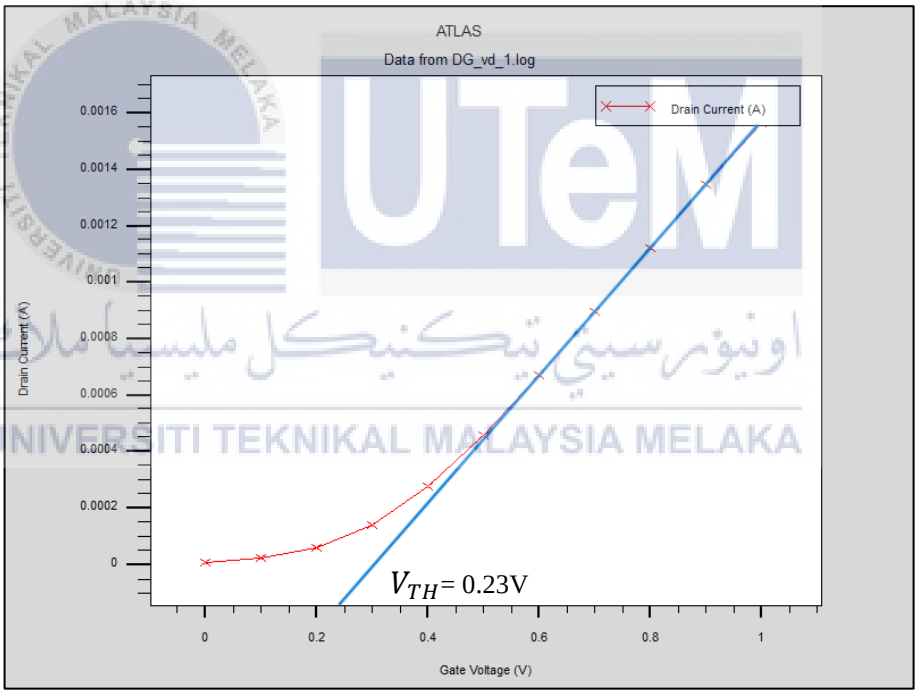


Figure 4.7: Threshold voltage extraction

Figure 4.8 shows the device parameters that have been extracted from the Silvaco. It can be seen that the double-gate MOSFET has a drain current of about 0.0016A, which shows that a lower drain current in transistors makes it ideal for various low-power applications. These transistors are particularly well-suited for tasks such as signal processing, small-scale digital logic circuits and battery-powered devices. One

significant benefit of lower drain current is the reduced heat generation, simplifying thermal management and proving advantageous in compact or sensitive electronic designs. Additionally, they are more power-efficient, making them efficient options for applications that do not demand high current handling.

Figure 4.8 also shows the on and off currents of the device. I_{ON} which is 0.00156A, represents the current flowing through the MOSFET when it is in the on state, conducting electricity. This value signifies the current passing through the device when a sufficient voltage is applied to the gate, turning it on. On the other hand, I_{OFF} measures at 0.698 μA, representing the state's leakage current when the MOSFET is not conducting. Even in its off state, a small amount of current can still leak through the MOSFET and in this case, it amounts to 0.698 μA, which is low for applications not sensitive to power.

Another critical parameter is the I_{ON}/I_{OFF} ratio, which stands at 2242. This ratio holds particular importance in digital electronics, especially for transistors used in logic gates and integrated circuits. It indicates the device's efficiency in switching between on and off states. A higher I_{ON}/I_{OFF} ratio is generally preferred because it implies that the transistor can deliver a robust current while minimising leakage when off. With a ratio of 2242, the double-gate MOSFET demonstrates effective switching capability and power efficiency. A high I_{ON} combined with a low I_{OFF}, leads to a high I_{ON}/I_{OFF} ratio is typically desirable for reducing power consumption and enhancing the efficiency of digital circuits that rely on the MOSFET.

leak1	0.001565379355	(# 136)
nvt1	0.22510619747232	(# 137)
subvt	0.203213777135389	(# 143)
Ion	0.001565379355	(# 145)
Ioff	6.979003836e-07	(# 146)
Ion/Ioff ratio	2242.98394410569	(# 147)

Figure 4.8: Extracted device parameters

Table 4.2: Simulation results as compared to IRDS 2022 prediction

Performance Parameter	IRDS 2022 Prediction[40]	Designed Transistor
V_{TH} (V)	$\pm$0.271	0.225
I_{ON} (µA/µm)	>787	1565
I_{OFF} (nA/µm)	<100	697.9

Table 4.2 shows the performance metrics for V_{TH}, I_{ON} and I_{OFF}. The simulation outcomes for the 14nm double-gate n-type MOSFET align with the IRDS 2022 predictions for V_{TH} and I_{ON}. However, it is worth noting that the I_{OFF} value observed in the simulations falls significantly higher than the anticipated value.

Table 4.3: Comparison between single-gate and double-gate MOSFET device parameter

Performance Parameter	Single-gate MOSFET[41]	Designed Transistor
V_{TH} (V)	0.85	0.225
I_{ON} (µA/µm)	697.25	1565
I_{OFF} (nA/µm)	79.4	697.9

Table 4.3 shows the comparison between single-gate MOSFET and double-gate MOSFET and it can be observed that double-gate MOSFET have higher I_{ON}/I_{OFF} compared to single-gate MOSFET, which is 2242 and 8781, respectively. In a digital

circuit, the higher the ratio, the switching speed between one transition will be faster. Although single-gate MOSFET have lower leakage current but, in digital circuit I_{ON} should be higher to obtain a low-power consumption device with faster switching activity.

4.3 Full Adder

The performance of the single-gate MOSFET full adder and double-gate MOSFET have been analyzed in terms of power, delay and area to obtain an efficient digital circuit.

4.3.1 Single-Gate MOSFET Full Adder

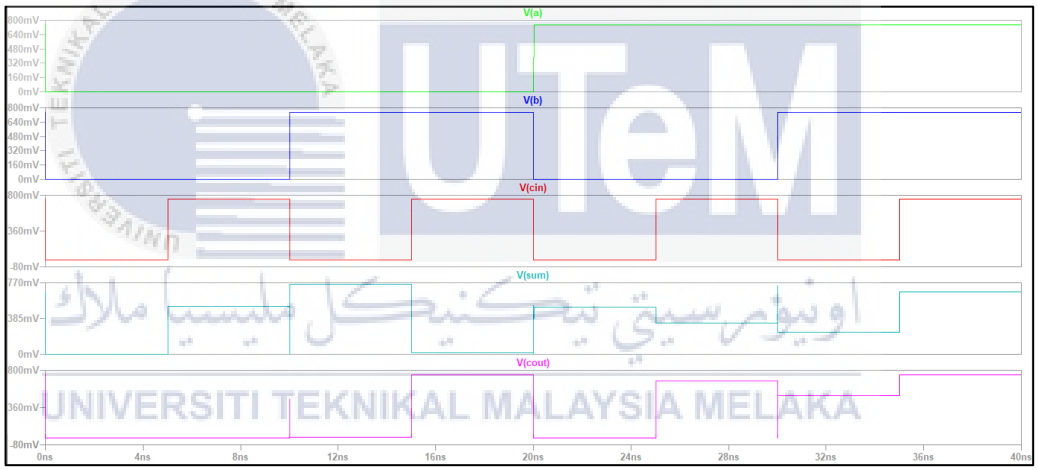


Figure 4.9: Input and output of single-gate MOSFET full adder

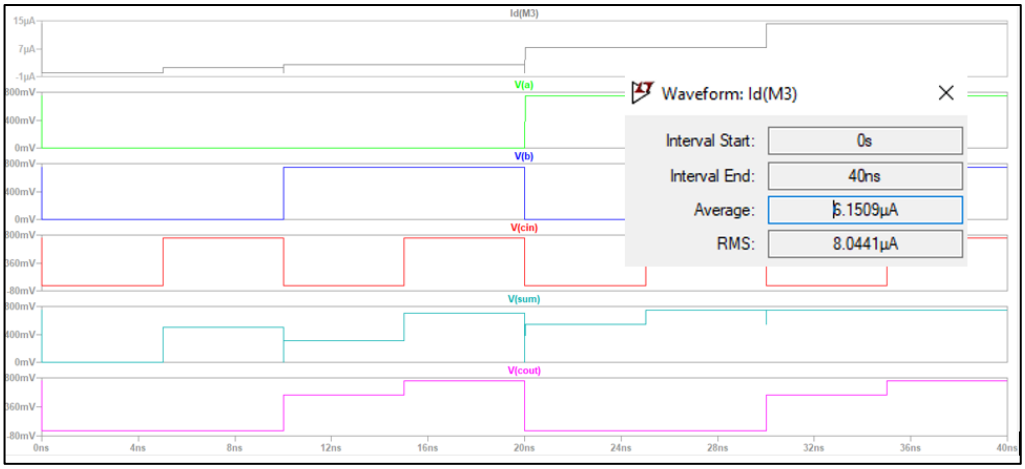


Figure 4.10: Average drain current of full adder

4.3.2 Double-Gate MOSFET Full Adder

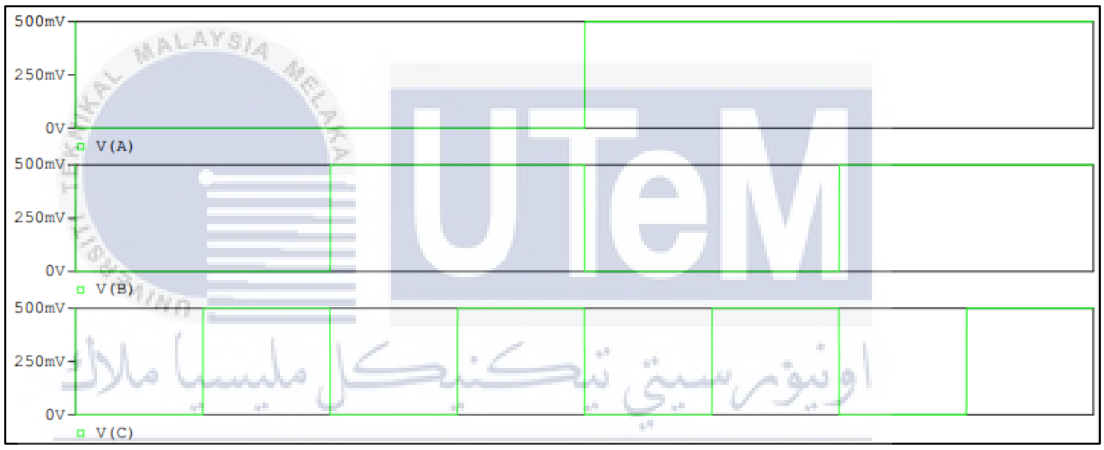


Figure 4.11: Input of double-gate MOSFET full adder

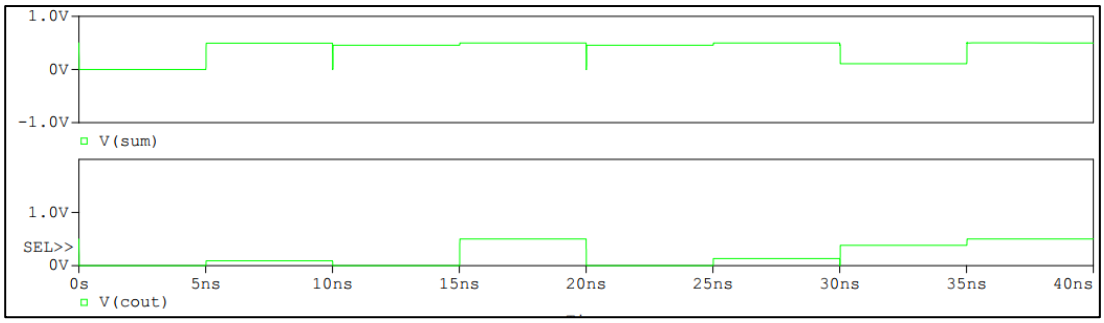


Figure 4.12: Output of double-gate MOSFET full adder

4.4 Performance Analysis

The primary criteria for evaluating the excellence of a digital circuit encompass three key factors: size or area, power and delay in operation[38]. Given the trend of MOSFET scaling, there is a natural inclination to decrease the dimensions of circuits. Therefore, the digital circuit performance analysis between single-gate MOSFET and double-gate MOSFET will be discussed.

4.4.1 Power

In this section, the primary issues related to how power is lost in metal-oxide-semiconductor field-effect transistor (MOSFET) static logic circuits will be discussed. It is important to differentiate between two key concepts in electronic circuits, which are energy consumption and energy dissipation. Energy consumption refers to the total amount of energy that originates from the power source and flows into the circuit. In contrast, energy dissipation represents the energy leaving the circuit and being released into the environment, typically as heat. It is worth noting that these two values are equal and interchangeable due to the principle of energy conservation.

Considering an ideal transistor, it is important to understand that the electrical charge from the power source is not simply discharged into the ground. This is because one of the transistors remains partially closed at all times. In this scenario, energy consumption occurs when charging the circuit's capacitance while transitioning from 0 to 1. Conversely, energy dissipation, which manifests as heat generation, takes place when the transistor discharges into the ground as it switches from 1 back to 0. This specific type of power consumption is referred to as "switching power."

However, in the real world, transistors are not flawless. Transistors do not switch instantaneously. During the switching process, there is a brief moment when the

transistor is in an intermediate state. During this time, its resistance rapidly changes and the transistor remains partially open, allowing some current to pass through. This situation can temporarily create a pathway between the voltage supply and the ground, known as short circuit power.

In this project, the primary focus is on reducing the number of switches performed by gates, a measure known as switching activity. This reduction directly affects both switching power and short-circuit power, collectively referred to as dynamic power. Mainly concentrate on clocked or synchronous circuits, where operations occur periodically at a fixed frequency determined by a clock signal.

Theoretically, it is assumed that the gate's capacitance is charged only when the logical value at the gate's output changes. In practice, due to signal propagation delays within the circuit, changes in different gate inputs can become unsynchronized. This can result in the gate being partially charged or discharged for a very brief period, followed by immediate discharge or recharge.

In full adder circuits, a gate consumes the highest dynamic power when it switches during every clock cycle. However, in reality, gates typically do not switch with every clock cycle. Therefore, the actual average dynamic power consumption (P_{avg}) of a gate while performing certain computations is lower than the maximum power consumption (P_{max}).

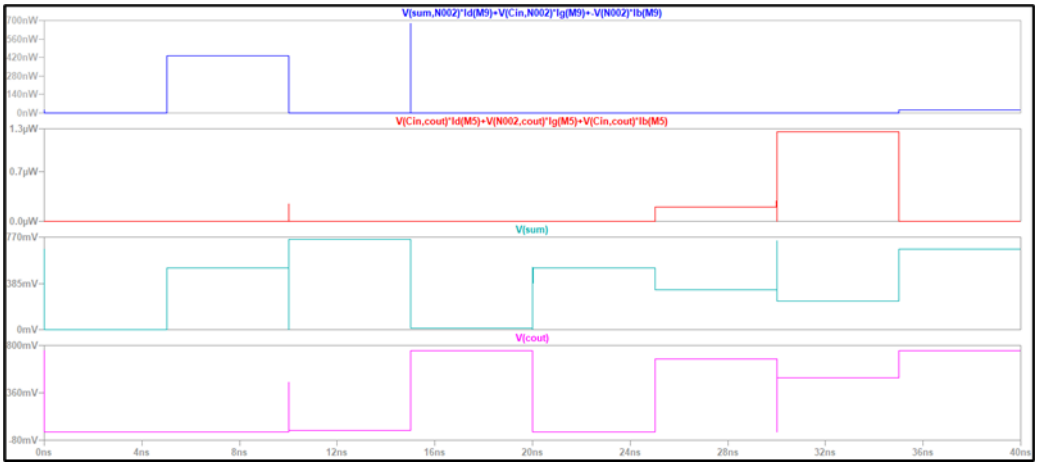


Figure 4.13: Power dissipation of single-gate MOSFET

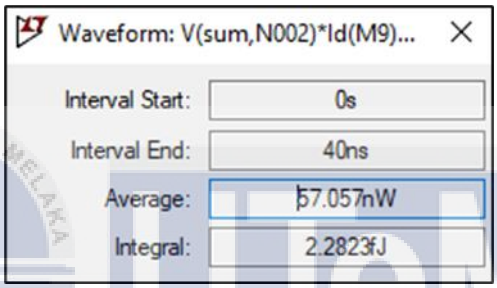


Figure 4.14: Average power dissipation of the single-gate MOSFET full adder

Figure 4.13 shows the power dissipation of the single-gate full adder when transitioning from one period to another. It can be noticed that the sudden spike of power that occurs shows the current leakage when switching did not happen. In Figure 4.14, an average of 57.057nW of power dissipated while the circuit was operating.

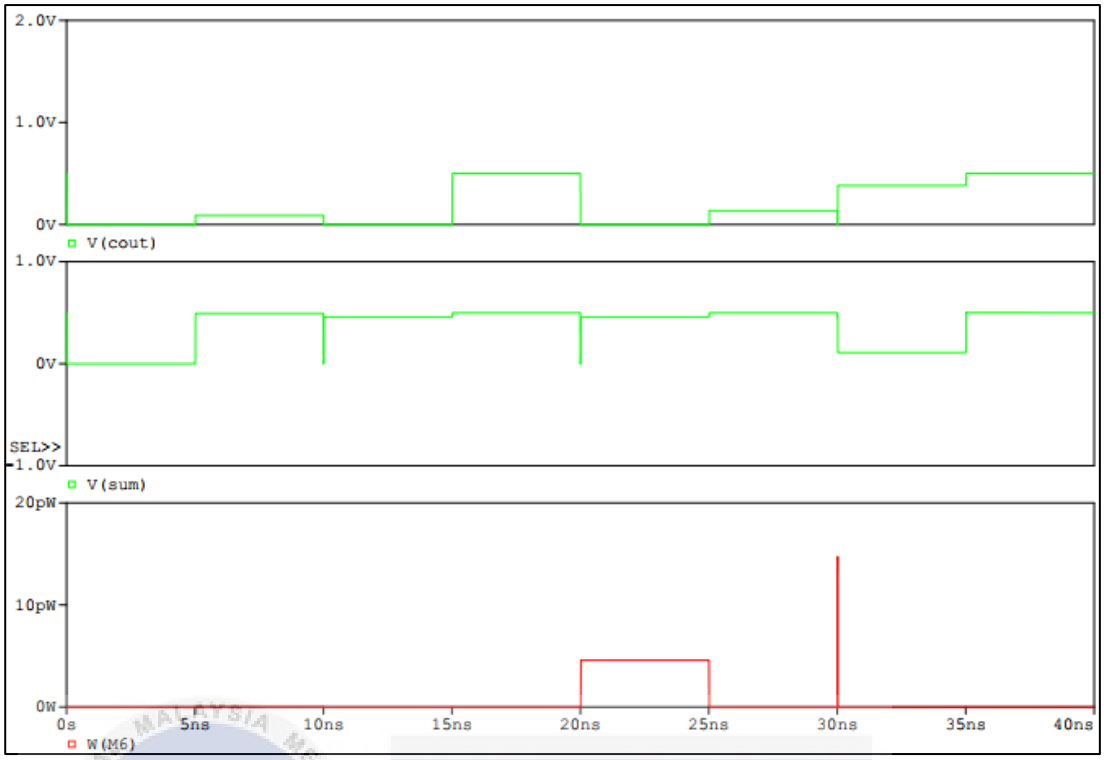


Figure 4.15: Power dissipation of double-gate MOSFET

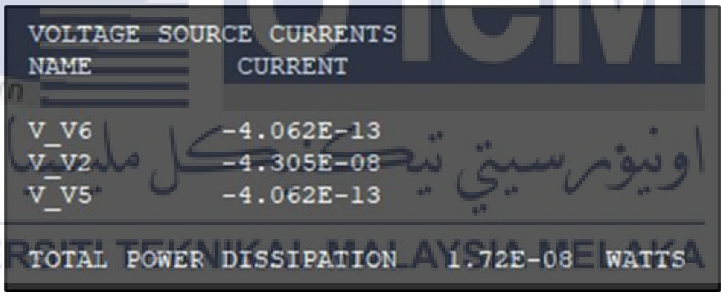


Figure 4.16: Average power dissipation of the double-gate MOSFET full adder

Meanwhile, for double-gate MOSFET, Figure 4.18 shows the power dissipation in the full adder circuit and Figure 4.19 shows the average power dissipated in the circuit is 17.2nW. It shows that full adder implementing double-gate MOSFET has lower power dissipation compared to single-gate MOSFET and it has been reduced by 39%. Lower power dissipation leads devices to operate longer on a single battery charge, enhancing energy efficiency and overall usability, especially for digital circuits.

Table 4.4: Result for power dissipation and switching delays at different supply voltages for single-gate MOSFET

Supply Voltage (V)	Power Dissipation (nW)	Switching delay (ps)
0.9	67.49	17.65
0.8	46.70	19.36
0.7	35.63	20.58
0.6	29.11	23.09
0.5	21.55	23.37
0.4	19.83	24.93

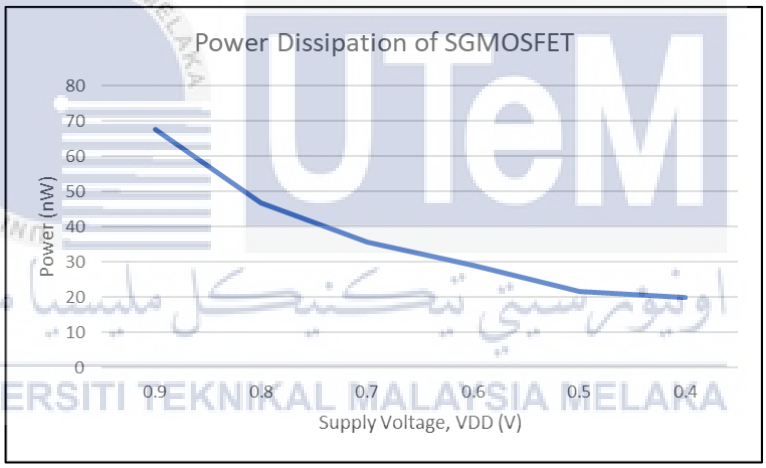


Figure 4.17: Illustration of single-gate MOSFET power dissipation

Table 4.4 and Figure 4.17 show that when the supply voltage decreases, there is a reduction in power dissipation. However, when the voltage drops below approximately 0.7V, there is an increase in switching delay. This phenomenon occurs because, at voltages below 0.7V, the system operates in the sub-threshold region, resulting in a lower drive current.

Table 4.5: Result for power dissipation and switching delays at different supply voltages for double-gate MOSFET

Supply Voltage (V)	Power Dissipation (nW)	Switching delay (ps)
0.9	53.71	6.93
0.8	45.70	7.15
0.7	30.14	8.25
0.6	25.39	8.79
0.5	19.77	9.33
0.4	17.20	9.89

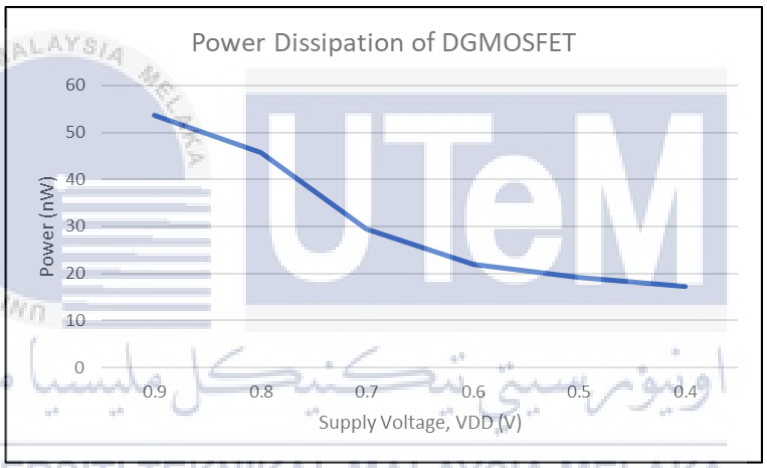


Figure 4.18: Illustration of double-gate MOSFET power dissipation

However, a lower power dissipation can be observed in Table 4.5 for double-gate MOSFET, which has been shown in Figure 4.18 and when the voltage drops below the range of 0.7 V to 0.6 V, there is an increase in delay times. This occurs because, within this voltage range, the system operates in the sub-threshold region, where the double-gate MOSFET exhibits optimal voltage transfer characteristics with reduced drive current.

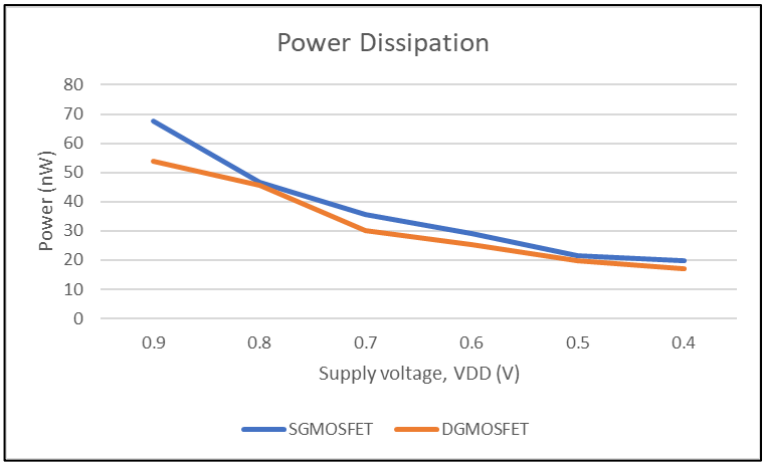


Figure 4.19: Comparison between single-gate MOSFET and double-gate MOSFET in power dissipation

Figure 4.19 shows the comparison between single-gate MOSFET and double-gate MOSFET in terms of power dissipation. It can be observed that when the supply voltage decreases, both types of MOSFET exhibit a decline in power dissipation. This indicates that reducing the supply voltage in these devices can result in decreased power consumption, which is a desirable characteristic for applications where power efficiency is crucial.

Initially, the single-gate MOSFET starts with a higher power dissipation value at 0.9V in comparison to the double-gate MOSFET. However, as the voltage decreases, the power dissipation of the single-gate MOSFET gradually approaches that of the double-gate MOSFET.

It can be suggested that at lower voltage levels, the difference in power dissipation between single-gate and double-gate MOSFET becomes negligible. It can be concluded that the dual-gate configuration offers more significant power-saving benefits at higher and lower voltages. Thus, the graph demonstrates that as the supply voltage decreases, both single-gate and double-gate MOSFET exhibit lower power

dissipation, with the double-gate MOSFET showing a more pronounced advantage in power savings.

4.4.2 Switching Delays

Switching delays in MOSFET are crucial to determine the speed and efficiency of electronic circuits. This is important in power electronics and high-frequency applications. These delays show the time a MOSFET takes to transition between its on and off states. There are two types of delay:

1. Turn-On Delay
   - Delay time - the interval from the application of the gate voltage to the onset of the drain current rise
   - Rise time - the duration for the drain current to increase from 10% to 90% of its maximum value
2. Turn-off delay
   - Delay Time - the period from the removal of the gate voltage to the start of the drain current fall
   - Fall Time - the time it takes for the current to decrease from 90% to 10% of its peak.

The total switching time is the aggregate of turn-on and turn-off times. Factors like gate charge, gate drive strength, internal parasitic capacitances and operating conditions like temperature and load significantly influence these delays. Reducing switching delays is essential for enhancing the performance and efficiency of circuits employing MOSFET.

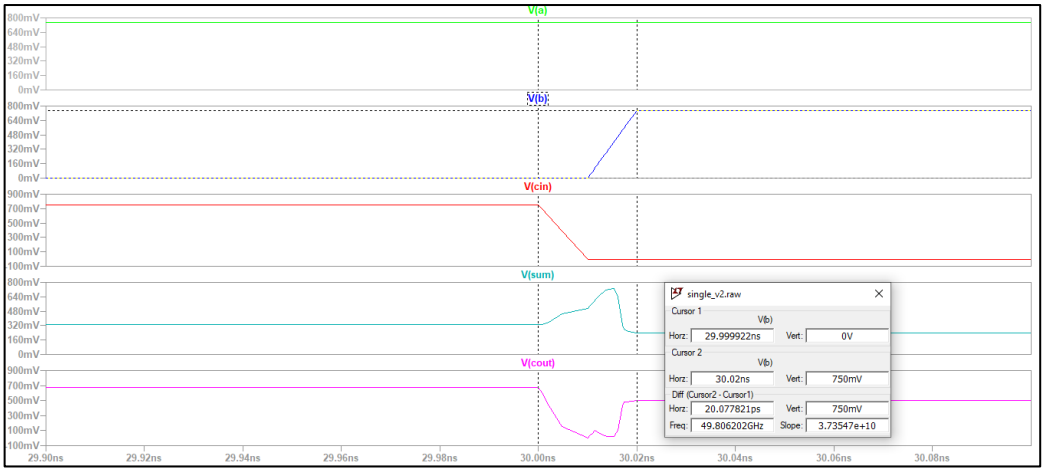


Figure 4.20: Switching delay in single-gate MOSFET switching

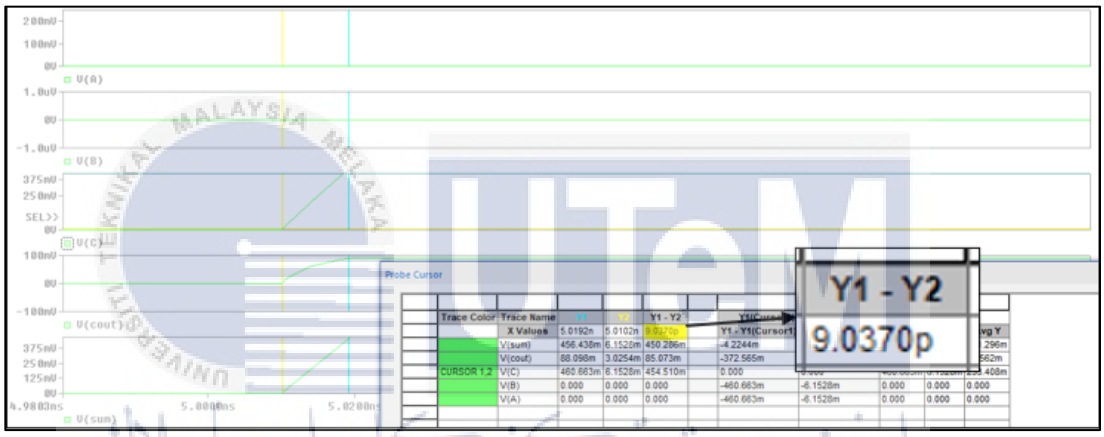


Figure 4.21: Switching delay in double-gate MOSFET switching

Figure 4.20 shows the switching delays for single-gate MOSFET, which is 19.98ps, compared to double-gate MOSFET, which is 9.04ps, shown in Figure 4.21. This shows that by applying double-gate MOSFET, the transition from one period to another is boosted by 50%. This allowed the circuits to enhance efficiency, performance and reliability.

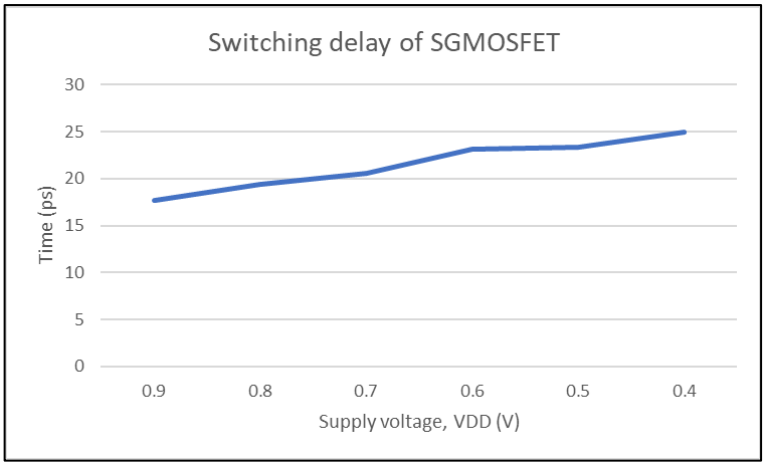


Figure 4.22: Illustration of single-gate MOSFET switching delays

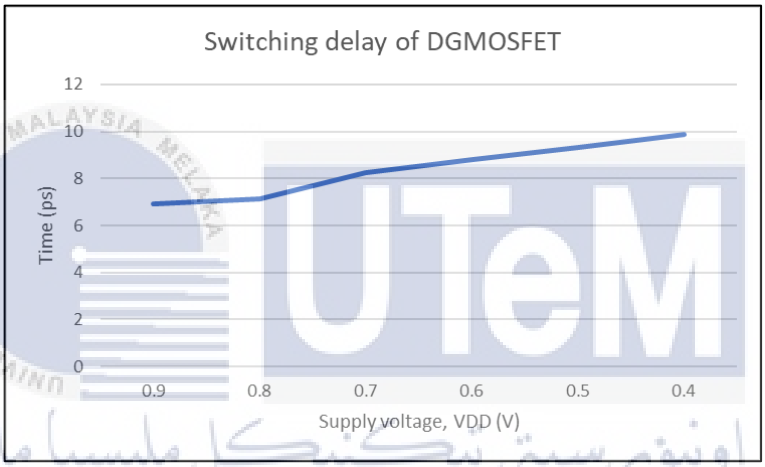


Figure 4.23: Illustration of single-gate MOSFET switching delays

Table 4.4 and Table 4.5 show the switching delays at different supply voltages and it can be seen that by increasing the supply voltage, the switching delays decrease in Figure 4.22 and Figure 4.23. This is because MOSFET gate functions act similarly to a capacitor. When the supply voltage is increased, this capacitance charges more rapidly, thus decreasing the duration required to switch the MOSFET from off to on and vice versa. This fast transition occurs as the gate voltage attains the necessary threshold voltage to activate the MOSFET more swiftly. Additionally, the overdrive voltage is enhanced with a higher supply voltage. The increase in overdrive voltage

shows a higher gate-source voltage compared to the threshold voltage letting transistor switch faster.

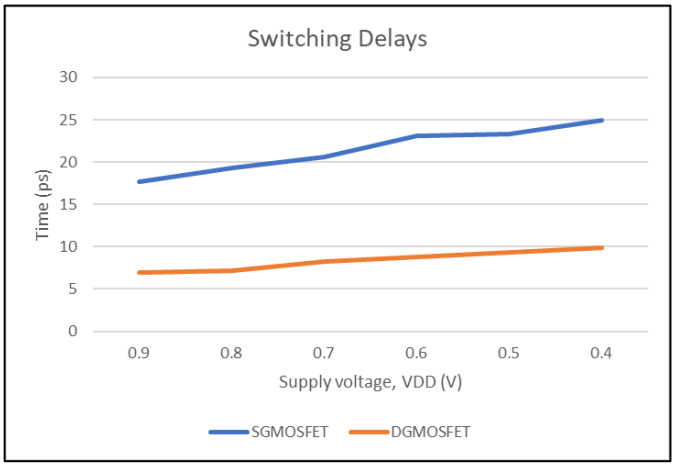


Figure 4.24: Comparison between single-gate MOSFET and double-gate MOSFET in switching delays

Figure 4.24 shows the comparison between single-gate MOSFET and double-gate MOSFET in terms of switching delays. The relationship between the supply voltage and the time it takes for transistors to switch is crucial for understanding transistor performance. When the supply voltage decreases from 0.9 V to 0.4 V, it can be observed an increase in switching delays for single-gate and double-gate MOSFET. This is because transistors tend to switch more slowly at lower voltages. Comparing the single-gate MOSFET and double-gate MOSFET, it is clear that the single-gate MOSFET experienced higher switching delays across different supply voltages, highlighting the double-gate MOSFET faster speed in Figure 4.24. Additionally, the single-gate MOSFET delay increase becomes more prominent as the voltage decreases. This is indicating that single-gate MOSFET more sensitive to voltage changes compared to the double-gate MOSFET.

These observations suggest that double-gate MOSFET is a good choice for applications that require faster switching speeds, especially at lower voltages. This is important for applications that need to reduce power consumption since lower voltages are used to minimize energy usage. The double-gate MOSFET improved performance at lower voltages shows a good energy efficiency for certain applications.

Switching delays play an important role in the design of digital circuits, impacting various critical aspects. Switching delays plays a fundamental role in determining timing and synchronization. These delays influence signal timing and error will occur if not handled properly. Additionally, the performance of a digital circuit heavily relies on its switching delays. A shorter delay allows faster operations, which are important in applications that need high speeds like processors and communication devices.

The total time taken for a signal to traverse a logic gate, known as propagation delay, is also influenced by switching delays. In complex circuits, these delays can affect the speed of the circuit. Thus, the management of switching delays is an important in ensuring the accurate, efficient and dependable operation of digital circuits, especially in high-speed and high-performance environments.

4.4.3 Area

The evolution of VLSI (Very Large-Scale Integration) technology, with the increasing preference of devices, has pushed designers to aim for reduced area in circuit design. The design of a full adder revolves around the number of transistors it contains. This will impact the complexity of designing various functional units like multipliers and algorithmic logic units in digital circuits.

The size of area in designing a digital circuit is crucial in the advancement of technology. The smaller circuit areas allow the miniaturization and integration to accommodate more components on a single small chip. This is important to produce a compact and a powerful electronic device. The miniaturization of device will have a faster processing speeds, shorter circuit paths with a faster signal transmission and reduced resistance and capacitance of device altogether enhance overall performance of the digital circuits.

Furthermore, smaller circuits are more energy-efficient, an important aspect for battery-powered devices such as smartphones. It consumes less power, leading to extended battery life and reduced heat generation. The trend toward decreasing circuit size aligns with Moore's Law, predicts the doubling of transistors on integrated circuits every two years. These advancements allow computing power and enable the development of more sophisticated electronics.

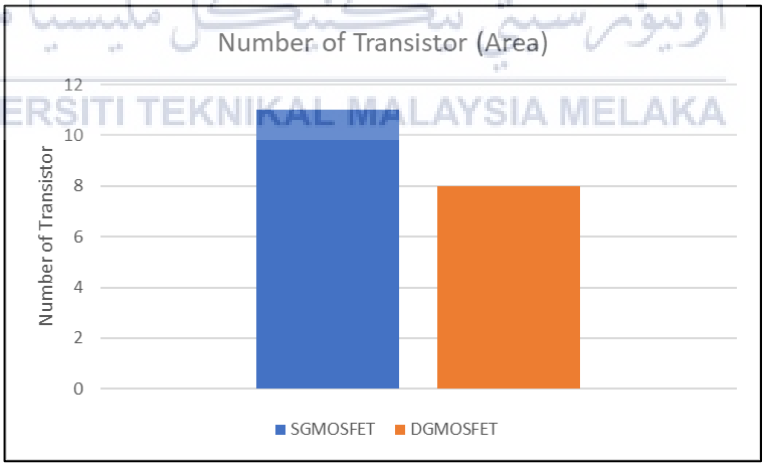


Figure 4.25: Number of transistors for single-gate MOSFET and double-gate MOSFET

Figure 4.25 shows the number of MOSFET used to design a full adder. For single-gate MOSFET, a total of 11 transistors (11T) are used to have a functioning full adder circuit. Meanwhile, double-gate MOSFET used only 8 transistors (8T) to have a

functioning circuit. It can be observed that double-gate MOSFET has a lower area size as it uses fewer transistors and benefits squeezing other digital circuits and analogue circuits into one small chip.

Double-gate MOSFET play a significant role in shrinking the size of digital circuits by offering enhanced control over the transistor channel. One of the defining attributes of double-gate MOSFET is their ability to operate with varying voltages applied to the top gate and bottom gate. This characteristic is harnessed to enhance the performance and versatility of digital circuits. It also effectively addresses short-channel effects, lowers power consumption, enhances packing density and boosts switching speed and overall performance. These advantages are essential for advancing microelectronics and facilitating the creation of smaller, swifter and more efficient electronic devices.

4.5 Summary

Table 4.6: Comparison between past and current project

Project Title	Power		Switching Delays		Area	
	Past	This Project	Past	This Project	Past	This Project
S. K. Gupta, G. G. Pathak, D. Das and C. Sharma, “Double Gate MOSFET and its application for efficient digital circuits,”	0.087µW	0.017µW	0.27ns	9.98ps	28T	8T
Liqiong Wei, Zhanping Chen and K. Roy, "Double gate dynamic threshold voltage (DGDT) SOI MOSFET for low power high performance designs,"	11.5mW	0.017µW	0.62ns	9.98ps	24T	8T
Abhinav Gupta, Manish Kumar Rai, Amit Kumar Pandey et al. A Novel Approach to Investigate Analog and Digital Circuit Applications of Silicon Junction less-Double-Gate (JL-DG) MOSFET	-	0.017µW	19.98ps	9.98ps	-	8T

Table 4.6 compares past work and this project analysis. This project has a reduction in power from 0.087µW to 0.017µW and a decrease in switching delays from 0.27ns to 9.28ps. The second project also showed the comparison with power dropping from 11.5mW to 0.017µW, switching delays decreasing from 0.62ns to 9.98ps and the area

reducing from 24 transistors to 8 transistors. This comparison shows a trend of reduced power consumption and switching delays with the designed double-gate MOSFET and digital circuit.

Three primary performance criteria to consider when analyzing digital circuit performance which is area, power and switching delay. In power, the distinction between energy consumption by the circuit and the energy dissipated as heat, with a specific emphasis on reducing switching activity in gates. This reduction affects both switching and short-circuit power, collectively referred to as dynamic power. It is worth noting that double-gate MOSFET demonstrate a 39% decrease in power dissipation compared to single-gate MOSFET, which results in longer battery life and improved energy efficiency.

Meanwhile, the analysis shows the crucial role of switching delays in determining the speed and efficiency of electronic circuits. The analysis shows that double-gate MOSFET displays a significant reduction in switching delays, making it 50% faster than single-gate MOSFET. This characteristic is recommended for applications that require faster switching, especially at lower voltages. Lower voltages are often used to minimize energy consumption and contribute to energy efficiency. In terms of the circuit's area aspect, double-gate MOSFET has smaller circuit sizes. This leads to faster processing speeds, lower power consumption and is on par with Moore's Law, which predicts the technology advancements in computing systems.

4.6 Sustainable Development Goal

4.6.1 Affordable and Clean Energy (SDG 7)

Figure 4.26: Affordable and clean energy (SDG 7)

Double Gate MOSFET play a crucial role in enhancing the efficiency of digital circuits, which directly relates to Sustainable Development Goal 7 - Affordable and Clean Energy. These transistors are renowned for their energy efficiency, owing to their ability to control the channel better and reduce leakage currents, thus lowering power consumption. This improvement in energy efficiency is in line with SDG 7's objective of promoting sustainable and affordable energy. The advancement in MOSFET technology, including double-gate MOSFET, allows for the miniaturization of electronic devices, which in turn leads to reduced power consumption and material usage, thereby decreasing the ecological footprint. Additionally, double-gate MOSFET are more effective at controlling heat dissipation than traditional single-gate MOSFET. This not only means less energy is wasted as heat but also reduces the need for energy-intensive cooling systems in facilities like data centers, directly contributing to the increased use of renewable energy. Continuous research and innovation in this field are paramount for developing cleaner energy technologies and solutions, aligning with the goals of SDG 7 to enhance global energy efficiency, promote sustainable industrialization and facilitate the transition to renewable energy sources.

4.6.2 Industry, Innovation and Infrastructure (SDG 9)

Figure 4.27: Industry, innovation and infrastructure (SDG 9)

Double-gate MOSFET technology plays a crucial role in efficient digital circuits, significantly contributing to Sustainable Development Goal 9 (SDG 9), which emphasizes industry, innovation and infrastructure. These transistors enhance energy efficiency by offering better control over the channel and minimizing leakage currents, thereby aligning with SDG 9's focus on sustainable industrial processes. The miniaturization capabilities of double-gate MOSFET, while maintaining high performance, directly supports the goal's emphasis on innovation. This miniaturization is essential for the advancement of technology, particularly in the computing and telecommunications sectors.

CHAPTER 5

CONCLUSION AND FUTURE WORKS

5.1 Conclusion

Continuous scaling in MOSFET devices leads to a decline in their performance due to issues such as leakage currents and short channel effects resulting from the reduction in device dimensions. To address these short-channel problems caused by downsizing, a new device called the double-gate MOSFET has been developed. A simplified simulated design of a 14nm double-gate MOSFET, which is suitable for investigating design parameters for performance analysis, has been presented. Despite some challenges, such as higher I_{OFF} (697.9 nA/μm) than projected and higher I_{ON} (1565 μA/μm) than projected in IRDS 2022, the V_{TH} value remains within 16% of the predicted value (0.225V). This device can serve as a starting point for further research and optimisation to enhance its overall functionality and performance, making the construction of a 14 nm gate-length transistor both feasible and practical.

Furthermore, in terms of digital circuit performance, it is an evident that the double-gate MOSFET full adder circuit outperforms the single-gate MOSFET full adder circuit when it comes to reducing transistor feature size. The double-gate full adder circuit can operate at significantly lower voltages and exhibits reduced power dissipation and switching delays compared to the single-gate MOSFET design by 50%. Additionally, the sub-threshold region displays lower power consumption and delay compared to the single-gate MOSFET design.

5.2 Future Works

The research conducted in this thesis has demonstrated the capability to mitigate short-channel effects and enhance device performance for digital circuit applications by carefully selecting device dimensions and suitable materials. While this thesis primarily focuses on the simulation and analysis of double-gate MOSFET, it is worth noting that there are numerous challenging research areas to explore as MOSFET device sizes continue to shrink. In the future, the channel length of MOS transistors is expected to reach the tens of nanometer range, approaching the carrier mean free path, which is also within the nanometer scale. This proximity between channel length and carrier mean free path, introduces correlations between local noise sources, a factor that has not been thoroughly investigated or measured as of now.

Although the current processes for manufacturing double-gate MOSFET are complex and time-consuming, it would be worth exploring the real-time fabrication and simulation of these devices. The objective of implementing double-gate MOSFET is to incorporate these devices into high-density configurations with many components. This would potentially revolutionize the design of CMOS circuits by

having less energy consumption, minimal power dissipation and smaller device sizes. These advancements are crucial for the development and manufacturing of circuits.

A SPICE model generated at Level 4 generation can be explored as no research has been conducted as for now. This package allows for the simulation of both analog and mixed-signal circuits and it includes features for making and recording sophisticated measurements of circuit performance compared to other generations. Other than that, an integration of double-gate MOSFET in mixed signal is an opportunity to study the performance of the device when both analogue and digital application integrated into one device. Therefore, research and development efforts must continue to progress in the field of double-gate MOSFET.

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LIST OF PUBLICATIONS AND PAPERS PRESENTED

APPENDICES

Appendix A: SPICE Parameter

Parameter	Description	Unit	Default value
LEVEL	Model Index	-	1
W	Channel length	meter	DEFL
L	Channel width	meter	DEFL
KP	Mutual conductance coefficients	amp/$volt^2$	2.00×10^{-5}
RS	Power supply ohm resistor	ohm	0
RD	Drain ohm resistor	ohm	0
VTO	Zero bias threshold voltage	volt	0
RDS	Drain-power supply shunt resistor	ohm	Infinite
TOX	Oxide film thickness	meter	*
CGSO	Gate-power supply overlap capacitance per unit channel width	farad/meter	0
CGDO	Gate-drain supply overlap capacitance per unit channel width	farad/meter	0

CBD	Bulk-drain p-n junction capacitance at zero bias	farad	0
RG	Gate ohm resistor	ohm	0
N	Bulk p-n junction emission coefficient	-	1
RB	Bulk ohm resistor	ohm	0
GAMMA	Bulk threshold parameter	$volt^{1/2}$	*
ETA	Static feedback	-	0
KAPPA	Saturation electric field factor	-	0.2
NFS	Fast surface-state density	$1/cm^2$	0
UO	Surface mobility	cm^2/volt · sec	600