A LOW NOISE AMPLIFIER AT 2.45GHz

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For my beloved family

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ABSTRAK

Projek ini membentangkan tentang merekabentuk, simulasi serta fabrikasi penguat rendah hingar(LNA) pada frekuensi 2.45GHz. Penguat rendah hingar ini menghasilkan gandaan melebihi 11dB dan faktor hingar pada 1.45dB. Simulasi untuk penguat rendah hingar ini akan menggunakan perisian Ansoft Designer SV2 dan difabrikasikan di atas papan mikrostrip.

ABSTRAK

This project presents the design, simulation and fabrication of low noise amplifier at 2.45GHz. The Low Noise Amplifier provide gain more than 11dB with the noise figure at 1.45dB. The simulation of the Low Noise Amplifier used the Ansoft Office software and be develop using the Microstrip board.

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LIST OF ABREVIATIONS

Γ -	Reflection Coefficient
AC-	Alternating Current
CF -	Center of constant noise circle
dB -	Decibel
DC-	Direct current
F -	Noise Figure
FET-	Field Effect Transistor
Fmin -	Minimum noise figure
Freq-	Frequency
G -	Gain
GA -	Available gain
GaAs-	Gallium Arsenide
GHz -	Giga Hertz
GHz-	Giga Hertz
GT -	Transducer gain
H -	Substrate thickness
IEEE-	Institute of Electrical and Electronic Engineering
Γ_{in} -	Input reflection coefficient
IP3-	Third order intercept point
K -	Rollet stability factor
L -	Length
l -	Length of quarter-wave transformer
LAN-	Local Area Network
LNA -	Low Noise Amplifier

mA - Milliampere
Mag - Magnitude
MESFET- Metal Semiconductor Field Effect Transistor
mm - Millimeter
MMIC - Monolithic Microwave Integrated Circuit
MOSFET- Metal Oxide Field Effect Transistor
N - Noise Figure Parameter
Ni - Noise parameter
P - Power
pF - Pico Farad
pHEMT - Pseudomorphic High Electron Mobility Transistors
R - Resistance
RF - Radio Frequency
RF - Radius of constant noise circle
rms - Root mean square
rn - Normalize noise resistance
V - Volt
Vd - Drain Voltage
Vgg - Gate Terminal Voltage
VSWR - Voltage Standing Wave Ratio
W - Width
WLAN - Wireless Local Area Network
Z - Impedance
Zin - Input impedance
zin - Normalize value of input impedance
ZL - Load impedance
zL - Normalize value of load impedance
Zo - Characteristic impedance
ZT - Transformer impedance
Γ_L - Load reflection coefficient
Γ_{opt} - Optimum reflection coefficient
Γ_{out} - Output reflection coefficient
Γ_S - Source reflection coefficient
Ω - Ohm

CHAPTER I

INTRODUCTION

1.1 Introduction

The function of low noise amplifier (LNA) is to amplify low-level signals with maintain a very low noise. Additionally, for large signal levels, the low noise amplifier will amplified the received signal without introducing any noise, hence eliminating channel interference. A low noise amplifier function plays an undisputed importance in the receiver[1].

The low noise amplifier consists of transistor, direct current (DC) bias circuit and matching circuit. Nowadays, there are numerous type of transistor that has this ability of low noise amplifier like BFP540, BFP640 and BFP620. In this project the LNA are designs using a Siemens wideband transistor BFP540 for a high frequency application with low current and low supply voltage.

1.2 Thesis Outline

i. Chapter 1 will explain the objective and introduction of the low noise amplifier.

ii. Chapter 2 will discuss the literature review for the low noise amplifier. The research and background study also include in this chapter.

iii. Chapter 3 will discuss the design and the process of the low noise amplifier.

iv. Chapter 4 will discuss on the result of the simulation for the low noise amplifier.

v. Chapter 5 will discuss on the analysis of project.

1.3 Objective

The objective of this research is to perform circuit level design, simulation and measurement, including circuit analysis and verification of a low noise amplifier circuit at 2.45GHz. This low noise amplifier will produce a gain more than 10dB and noise figure less than 3dB.

1.4 Scope of Project

This project will be divided into four parts, they:-

I. Literature Review
II. Simulation
III. Fabricate
IV. Analysis

The first part of this project is to get as much as possible information of low noise amplifier. The parameter like S-Parameter, gain and stability will be covered. In this part also the background study of the low noise amplifier will be discussed. The low noise amplifier will be designed at 2.45GHz. The low noise amplifier circuit used collector feedback bias to activate the transistor. Bipolar transistor BFP540 will be used to design this low noise amplifier circuit.

The second part of this project is to simulate the low noise amplifier circuit using Ansoft Designer SV2. The data will be collected during the simulation process. The value of noise figure, gain and the return loss will be observed through this procedure.

The third part of this project is to fabricate this low noise amplifier circuit. The FR4 board will be used to fabricate the low noise amplifier circuit. The analysis result will be observed from this circuit.

At the analysis part, the result from simulation and fabrication will be compared.

1.5 Methodologies

The project methodology present the implementing process for low noise amplifier. In early stage, the literature review and understanding of theory about the overall procedure in this project will be compared. Figure 1.1 shows the flow chart of the project.

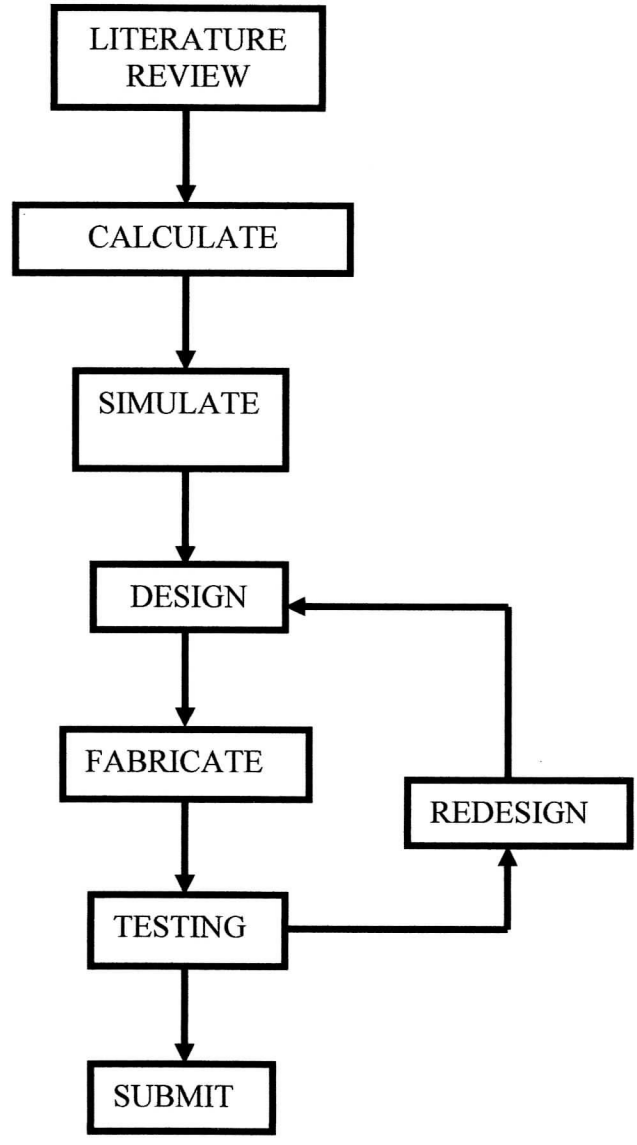

Figure 1.1 Flow chart of project

1.4.1 Literature review:-

The understanding parameter such as S parameter, VSWR, noise parameter and etc need to be covered. These parameters can be found from the data sheet of the transistor. Related topics need to be covered such as bias design, circuit stabilization, noise optimization, linearity optimization, load pull for gain and Third-Order Intercept Point (IP3) off improvement and complete circuit characterization[2]. The component that will be used in design the low noise amplifier circuit such as transistor, material and type of bias will be identified.

1.4.2 Calculate:-

All components will be calculated and selected using theoretical analysis.

1.4.3 Design and simulate:-

The low noise amplifier circuit is adapted into simulation software. The circuit will be simulated and the data will be collected. The important parameter for this low noise amplifier circuit is the gain and the noise figure.

1.4.4 Fabricate and testing:-

The low noise amplifier circuit will be constructed and fabricated on the microstrip board. The value of the hardware will be measured. It will be tested and analysed in this process.

CHAPTER II

LITERATURE REVIEW

2.1 Wireless LAN receiver

Behzad Razavi [3] reported the RF receiver design targeting spread-spectrum WLAN applications in the 2.4 GHz band. Based on direct-conversion architecture, the receiver employs partial channel selection filtering, dc offset removal and baseband amplification. The receiver was fully fabricated in a 0.6-μm CMOS technology in an area of 680μm x 980μm. The receiver achieved noise figure of 8.3 dB, IP3 of –9 dBm and system gain of 34 dB.

Charles Wenzel[4], have design a low noise amplifier for the ultra-low noise amplifier. He design the circuit using JFET as the transistor. The transistor is used because it is one of the suitable transistor for his application. He said that the amplifier should have some RF filtering at the input so that the carrier and sum frequencies from the phase detector do not reach the gain stages.

Muhammad Wasim[5] in his report have discuss and design a low noise amplifier using the CMOS transistor. He designed the low noise amplifier that suitable for the frequency from 1.8GHz to 2.4GHz. In his project, he has design multi-standard receiver front end. He has study the previous design of the Bluetooth low noise amplifier.

In case of an active mixer topology, the mixer input stage will contribute along with the LNA to the flicker noise level. Therefore, a resistive mixer should be the best solution in order to minimize the flicker noise level [6].

2.2 Transistor

There is three types of transistor that always being used to design the Low Noise Amplifier. The types of model are bipolar, FET and MMIC. In bipolar transistor, there are three regions collector, base and emitter.

The bipolar junction transistor was the first solid-state active device to provide practical gain and noise figure (F) at microwave frequencies. In the seventies, breakthroughs in the development of Field Effect Transistors (FETs) such as GaAs Metal Semiconductor Field Effect Transistor (MESFET) led to the higher gain and lower noise figure than bipolar transistors for the frequencies in the range of several gigahertz [7].

Currently, advanced FETs and bipolar transistors still compete for lower noise figure and higher gain at frequencies in excess of 100 GHz. Examples are the High Electron Mobility Transistor (HEMTs), such as Pseudomorphic High Electron Mobility Transistors (pHEMTs) [8], Metamorphic High Electron Mobility Transistor (MHEMTs) [9], as well as Heterojunction Bipolar Transistors (HBTs) [10], built using a variety of semiconductor materials likes GaAs, InP, Si, SiGe and many more.

Thomas L. Floyd[11] in his book has discuss about the circuit, component and application of electronic device. In the transistor chapter, his said that in order to operate properly a transistor as amplifier, the two pn junction must be correctly biased with external dc voltage. The emitter-follower is characterized by a high input resistance, which makes it a very useful circuit. This is because the high input resistance, the emitter-follower can be used as a buffer to minimize loading effects when one circuit is driving another.

Mike Wilson C.Eng.MIEE[12]. In his book, he discuss about the designing the receiver and transmitter for the wireless communication. He used the bipolar of low noise amplifier in his design. He said that would depend on cost and power supply considerations, as well as the application. FET/PHEMTdevices usually have a lower noise figure and higher IP3, but more expensive and may require a negative supply for the bias circuitry. MMIC's require very little design effort, but are usually the most expensive solution. Some MMIC's offer additional functionality in the same package (e.g. LNA+ mixer or two LNA stages), which may be an attractive option.

Gerard Wevers[13] had made the technical report for designing the low noise amplifier using the bipolar transistor. He discuss about the linearity, stability and including the way to design the bipolar Low Noise Amplifier. The design of his low noise amplifier is suitable for the wireless communication from 5 to 6 GHz. He said the bipolar transistor could give the high performance with the low cost budget.

T.K.K Tsang and M.N. El-Gamal[14] in their technical report, they had designed a double stages low noise amplifier. The gain for their low noise amplifier is 11.5dB and noise figure of 4dB. Since the design doesn't use any off-chip components, it can be easily integrated as part of a complete low-voltage transceiver.

In the national semiconductor technical report[2] they have design a very simple low noise amplifier using the discrete component. One of their last summary, they conclude that in order to improve the linearity of the Low Noise Amplifier, an inductor can be inserting on the transistor's emitter.

Ming-Chang Sun. Shing Tenqchen, Ying-Haw Shu. Wu-Shiung Feng[15] in their journal had design a 2.4 GHz CMOS Image-Reject Low Noise Amplifier. They use double stage of CMOS transistor in their project. The foundry provided device models are calibrated to incorporate the non-ideal properties of the CMOS process.

Gerard wevers[16] in Infineon technical report have design a low noise amplifier at 1900MHz using BFP640. In his technical report, he said that there is 4 element that need be considered to design low noise amplifier that is linearity,