# THRESHOLD VOLTAGE AND LEAKAGE CURRENT ANALYSIS ON 14NM DOUBLE GATE BI-GRAPHENE PMOS DEVICE

NURMISHYAR SHUHADA BINTI ABU BAKAR

UNIVERSITI TEKNIKAL MALAYSIA MELAKA

# THRESHOLD VOLTAGE AND LEAKAGE CURRENT ANALYSIS ON 14NM DOUBLE GATE BI-GRAPHENE PMOS DEVICE


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**This report is submitted in partial fulfilment of the requirements for the degree of Bachelor of Electronic Engineering with Honours**


**Faculty of Electronic and Computer Engineering**
**Universiti Teknikal Malaysia Melaka**



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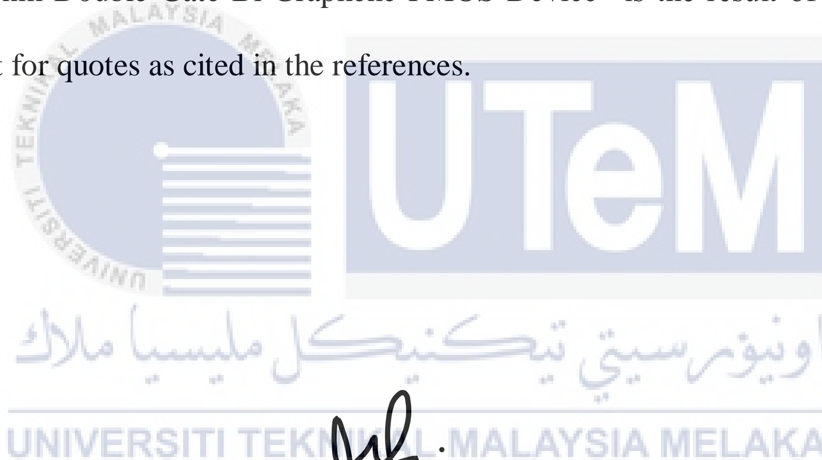


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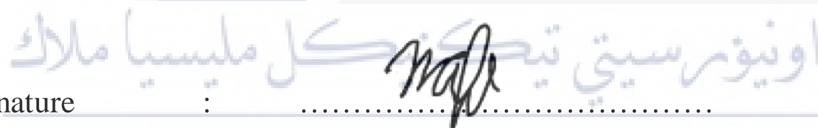


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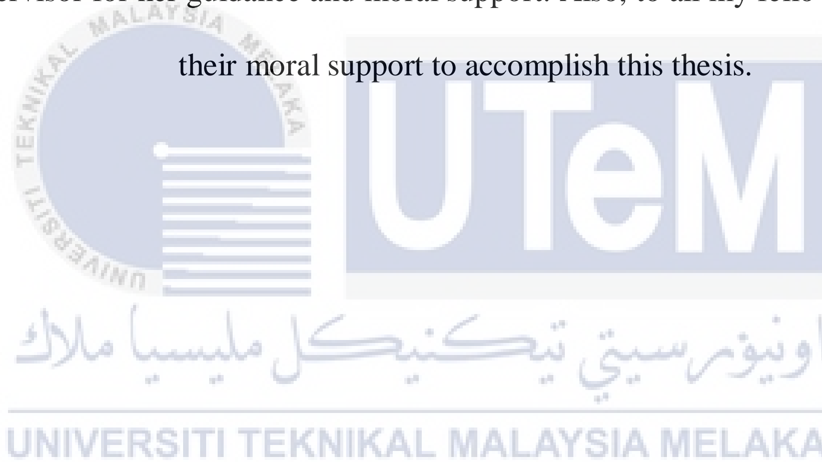
# DEDICATION

Special dedicate to my beloved family for encouragement. In addition, to my supervisor for her guidance and moral support. Also, to all my fellow friends for their moral support to accomplish this thesis.



# ABSTRACT

Metal Oxide Semiconductor Field Effect Transistor (MOSFET) is a semiconductor device are commonly used for switching and amplification of electronics signal in electronic devices. As the technologies growth faster, the MOSFET which allowing for compacting of the transistor on a single chip. It is very critical to producing a proper work to ultra-small transistors. In this research, the threshold voltage (VTH) and leakage current (IOFF) are the aim to meet nominal the best (NTB) and minimum the better (STB) according to International Technology Roadmap for Semiconductor (ITRS) 2013. Designing a 14nm double gate with added bi-graphene with Hafnium Dioxide (HfO2) which performs as the high permittivity material (high-k) dielectric in the gate structure of the PMOS device, and Titanium Silicide (TiSix), which acts as the metal gate, is deposited on top of the HfO2 high-k layer. By using Silvaco software to design and simulate the performance of devices through the ATHENA and ATLAS modules. The optimization method in this experimental were use Taguchi L9 orthogonal array strategy to improve the device process parameters for optimum VTH and minimum IOFF according to specifications of ITRS. Target of ITRS 2013 for nominal the best VTH is 0.191V ± 12.7% while the 100 nA/µm for smaller the better IOFF. The parameter process consists of VTH adjustment implant (A), VTH energy (B), VTH tilt (C), and S/D implantation (D), while for the noise factor which is S/D energy and S/D tilt. The simulations result shows the VTH adjustment implant and VTH tilt are the most dominant and adjustment factor that high possibilities to affect the VTH and IOFF respectively. Dominant factor is the unstable value which if there are minor changes of the doping value it will affect the majority process. Although, the best setting parameter for 14nm PMOS device VTH adjustment implant was obtained 9.12E10 Atom/cm3, VTH energy 11 KeV, VTH tilt 6 °C and S/D implantation 4.80E11 °C. Therefore, the average findings VTH and IOFF after optimization with the initial result has been observed for VTH through optimization are moving from 0.190867 V (6.96 % below the ITRS 2013 target) to 0.195049 V (2.12 % higher than ITRS 2013 target value) while for the IOFF from 4.35718 nA/µm to 4.940935 nA/µm.

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# ABSTRAK

*Transistor kesan medan semikonduktor oksida logam (MOSFET) ialah peranti semikonduktor yang biasa digunakan untuk menukar dan menguatkan isyarat elektronik dalam peranti elektronik. Memandangkan teknologi berkembang lebih pantas, MOSFET yang membolehkan pemadatan transistor pada satu cip. Ia sangat penting untuk menghasilkan kerja yang betul kepada transistor ultra-kecil. Dalam penyelidikan ini, voltan ambang (VTH) dan arus bocor (IOFF) adalah bertujuan untuk memenuhi nominal yang terbaik (NTB) dan minimum yang lebih baik (STB) mengikut Pelan Hala Tuju Teknologi Antarabangsa untuk Semikonduktor (ITRS) 2013. Mereka bentuk 14nm pintu berganda dengan tambahan graphene dwilapisan dengan Hafnium Dioxide (HfO2) yang berfungsi sebagai dielektrik bahan kebolehtepatan tinggi (high k) dalam struktur pintu peranti PMOS, dan Titanium Silicid (TiSix), yang bertindak sebagai pintu logam, dimendapkan. di atas lapisan HfO2 high-k. Dengan menggunakan perisian Silvaco untuk mereka bentuk dan mensimulasikan prestasi peranti melalui modul ATHENA dan ATLAS. Kaedah pengoptimuman dalam eksperimen ini adalah menggunakan strategi tatasusunan ortogon Taguchi L9 untuk menambah baik parameter proses peranti untuk VTH optimum dan IOFF minimum mengikut spesifikasi ITRS. Sasaran ITRS 2013 untuk nominal VTH terbaik ialah 0.191V ± 12.7% manakala 100 nA/µm untuk IOFF yang lebih kecil adalah lebih baik. Proses parameter terdiri daripada implan pelarasan VTH (A), tenaga VTH (B), kecondongan VTH (C), dan implantasi S/D (D), manakala bagi faktor hingar iaitu tenaga S/D dan kecondongan S/D. Hasil simulasi menunjukkan implan pelarasan VTH dan kecondongan VTH adalah faktor yang paling dominan dan pelarasan yang berkemungkinan tinggi untuk mempengaruhi prestasi VTH dan IOFF tersebut. Faktor dominan ialah nilai tidak stabil yang sekiranya terdapat perubahan kecil nilai doping ia akan menjejaskan majoriti prestasi peranti. Tuntasnya, parameter tetapan terbaik untuk implan pelarasan VTH peranti PMOS 14nm diperolehi 9.12E10 Atom/cm3, tenaga VTH 11 KeV, kecondongan VTH 6 °C dan implantasi S/D 4.80E11 °C. Oleh itu, keputusan optimum telah diperhatikan untuk VTH 0.191141 V manakala untuk IOFF 4.52747 nA/µm yang kedua-duanya hampir dengan ramalan ITRS 2013 yang disasarkan. Oleh itu, keputusan menunjukkan prestasi peranti cemerlang dengan nilai VTH 0.191141 V yang dicapai kepada sasaran ITRS 2013, juga nilai IOFF 4.52747 nA/µm.*

# ACKNOWLEDGEMENTS

Thankfulness to the All-Powerful, who is to be commended for being the Most Merciful and who I think has led me through these events. I have no chance without His direction.

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Last but not least, I would want to convey my sincere thanks to my parents and family for their unwavering support throughout this journey with both financially and morally. In addition, I want to thank all of my friends for their moral support. I'm hoping that this project will be useful.

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# TABLE OF CONTENTS


| | |
|---|---|
| **Declaration** | |
| **Approval** | |
| **Dedication** | |
| **Abstract** | **i** |
| **Abstrak** | **ii** |
| **Acknowledgements** | **iii** |
| **Table of Contents** | **iv** |
| **List of Figures** | **viii** |
| **List of Tables** | **x** |
| **List of Symbols and Abbreviations** | **xi** |
| **List of Appendices** | **xiii** |
| **CHAPTER 1 INTRODUCTION** | |
| 1.1 Introduction | 2 |
| 1.2 Problem Statement | 3 |
| 1.3 Objective | 4 |
| 1.4 Scope of work | 5 |


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UNIVERSITI TEKNIKAL MALAYSIA MELAKA

1.5 Importance of sustainability and impact 6

1.6 Thesis Organization 7

**CHAPTER 2 LITERATURE REVIEW**

2.1 Introduction 8

2.2 High Dielectric Constant (High K), Metal Gate 9

2.3 Graphene versus Bilayer Graphene 10

2.4 Difference between conventional MOSFET and double gate MOSFET 11

2.5 PMOS (P-Channel device) 13

2.5.1 Transistor Electrical Characteristics 15

2.6 Short Channel Effect (SCE) 16

2.7 Leakage Currents in MOSFET Device 17

2.8 Summary of literature review 18

**CHAPTER 3 METHODOLOGY**

3.1 Overview of project implantation 22

3.2 Flowchart of the project planning 24

3.3 Process flow and Device Simulation of PMOS Device 25

3.4 Process Virtual Fabrication 26

3.4.1 Step 1 Open DeckBuild in Silvaco software 26

3.4.2 Step 2 Running ATHENA under DeckBuild 27

3.4.3 Step 3 Start to program using ATHENA module inside DeckBuild 28

UNIVERSITI TEKNIKAL MALAYSIA MELAKA

3.4.3.1 Define an initial structure #non-Uniform grid 28

3.4.3.2 Define the initial substrate 29

3.4.4 Step 4 $V_{TH}$ Adjust Implant ($I_{ON}$ Implantation) 30

3.4.5 Step 5 Deposit Bilayer Graphene 31

3.4.6 Step 6 Deposit $HfO_2$ (High k) 33

3.4.7 Step 7 Conformal Metal Gate of TiSix Deposition 35

3.4.8 Step 8 S/D Implant ($I_{OFF}$ Implantation) 36

3.4.9 Step 9 Etch Silicon 37

3.4.10 Step 10 Aluminum Deposition 37

3.4.11 Step 11 Mirror (Right) Structure 40

3.4.12 Step 12 Etch at below Silicon 41

3.4.13 Step 13 Final Process 42

3.5 Taguchi-based L9 OA for optimization of process parameters 42

**CHAPTER 4 RESULTS AND DISCUSSION**

4.1 Design of 14nm Bilayer Graphene PMOS device 43

4.2 Result TonyPlot (ATLAS) 45

4.3 Result of 14nm Double Gate MOSFET 46

4.4 Determining the Process Parameters and Orthogonal Array 47

4.5 Process Parameters 48

4.6 Signal-to-noise Ratio (SNR) Analysis 49

UNIVERSITI TEKNIKAL MALAYSIA MELAKA

4.7 Analysis of Variance (ANOVA) 55

4.8 Conformation Test 56

**CHAPTER 5 CONCLUSION AND FUTURE WORKS**

5.1 Conclusion 60

5.2 Sustainability Development Goals (SDG) 61

5.3 Future Work 62

**REFERENCES** **63**

**APPENDICES** **70**

# LIST OF FIGURES


Figure 1.1 Shows the scope of work for the project. 5

Figure 2.1 Schematic diagram of DG MOSFET. 9

Figure 2.2 Illustrates monolayer Graphene and bilayer Graphene. 11

Figure 2.3 Conventional MOSFET and DG MOSFET. 12

Figure 2.4 Basic structure of PMOS. 14

Figure 2.5 P-type and N-type Majority/Minority carrier. 14

Figure 2.6 Electrical characteristic curve. 15

Figure 2.7 Various dielectric material graph. 17

Figure 2.8 Diagram of leakage currents in MOSFET transistors 18

Figure 3.1 Flowchart of the project 24

Figure 3.2 Process Simulation Flowchart 25

Figure 3.3 Open DeckBuild in Silvaco software tools. 27

Figure 3.4 Layout of the DeckBuild. 28

Figure 3.5 Initial Silicon substrates 29

Figure 3.6 Diffusion process and Ion implantation process. 31

Figure 3.7 The length of layer graphene x-direction. 32

Figure 3.8 Deposit of bilayer graphene. 32

Figure 3.9 The length of $HfO_2$ x-direction 0.0229. 34


UNIVERSITI TEKNIKAL MALAYSIA MELAKA

Figure 3.10 Deposit of Hafnium Dioxide ($HfO_2$). 34

Figure 3.11 The conformal TiSix deposition without etch. 35

Figure 3.12 The metal gate TiSix has been etched. 36

Figure 3.13 Etch unwanted Silicon 37

Figure 3.14 Deposit Aluminum layer. 38

Figure 3.15 Etch on the right side of Aluminum. 39

Figure 3.16 Etch Above side of Aluminum layer. 39

Figure 3.17 Mirror right side 40

Figure 3.18 Etch unwanted Silicon at below. 41

Figure 3.19 Mirror bottom of the structure. 42

Figure 4.1 The 14nm Bilayer Graphene PMOS device. 44

Figure 4.2 The measurement of gate length. 44

Figure 4.3 Relation between $V_{GS}$ versus $I_{DS}$ in ATLAS. 45

Figure 4.4 ATLAS result for $V_{DS}$ versus $I_{DS}$ for p-MOS transistor 46

Figure 4.5 Factor effect plot for SNR (Nominal the best) 54

Figure 4.6 Factor effect plot for SNR (Smaller the better) 54

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# LIST OF TABLES

Table 2.1 Summary based on previous researched 18

Table 4.1 Result of 14nm PMOS device 47

Table 4.2 Using a L9 Orthogonal Array for experimentation 48

Table 4.3 Process parameters and their levels 49

Table 4.4 Noise factors and their level 49

Table 4.5 Result for $V_{TH}$ value based on L9 Orthogonal Array 51

Table 4.6 Result for $I_{OFF}$ value based on L9 Orthogonal Array 52

Table 4.7 $V_{TH}$ and $I_{OFF}$ SNR level of Process Parameters 53

Table 4.8 Result of ANOVA for $V_{TH}$ 55

Table 4.9 Result of ANOVA for $I_{OFF}$ 56

Table 4.10 Best setting parameters for $V_{TH}$ and $I_{OFF}$ 57

Table 4.11 Confirmation results for $V_{TH}$ using L9 OA of Taguchi analysis 58

Table 4.12 Confirmation results for $I_{OFF}$ using L9 OA of Taguchi analysis 58

Table 4.13 Simulation results versus optimization 59

UNIVERSITI TEKNIKAL MALAYSIA MELAKA

# LIST OF SYMBOLS AND ABBREVIATIONS

| | | |
|---|---|---|
| MOSFET | : | Metal Oxide Semiconductor Field Effect Transistor |
| PMOS | : | Positive Metal Oxide Semiconductor |
| NMOS | : | Negative Metal Oxide Semiconductor |
| GFET | : | Graphene Field Effect Transistor |
| ITRS | : | International Technology Roadmap for Semiconductor |
| DG | : | Double Gate |
| DMG | : | Dual Material Gate |
| SOI | : | Silicon-On-Insulator |
| $SiO_2$ | : | Silicon dioxide |
| $HfO_2$ | : | Hafnium dioxide |
| $TiSi_X$ | : | Titanium Silicide |
| SCE | : | Short Channel Effect |
| OA | : | Orthogonal Array |
| EOT | : | Equivalent Oxide Thickness |
| IEEE | : | Institute of Electrical and Electronics Engineers |
| CD | : | Critical Dimension |
| CVD | : | Chemical Vapor Deposition |
| ALD | : | Atomic Layer Deposition |

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| | | |
|---|---|---|
| CF | : | Control Factor |
| NF | : | Noise Factor |
| SNR | : | Signal-to Noise Ratio |
| FE | : | Factor Effect |
| ANOVA | : | Analysis of Variance |
| NTB | : | Nominal the best |
| STB | : | Smaller the better |

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# LIST OF APPENDICES

Appendix A: International Technology Roadmap for Semiconductor (ITRS) 70
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# CHAPTER 1

# INTRODUCTION

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This chapter presents a brief introduction about the project. Basic introduction of Metal Oxide Semiconductor Field Effect Transistor (MOSFET) is a semiconductor device are commonly used for switching and amplification of electronics signal in electronic devices. The invention of transistor was challenging which to reduce the size. This chapter also provided background studies, which was followed by a statement of the problem and the project's goals. The scope of the project can be determined based on the problem statement and project objectives. Finally, the organization of the report is clarified.

## 1.1 Introduction

MOSFET's which have been scaled greatly due to Moore's Law since 1974. As the technologies growth faster, the MOSFET which allowing for compacting of the transistor on a single chip. It is very critical to producing a proper work to ultra-small transistors. For scaling smaller chips has been possible due to the technology that encourage potentially lower cost for production than it was, while improved in its speed as well as reduced in physical characteristics[1].

Simultaneously, the smaller devices may be implemented in smaller areas of integrated circuit (ICs), which resulting in higher number of transistors per wafer. According to earlier research, utilizing a high permittivity (high-k) gate dielectric and metal gate can overcome the problems[2]. In order to keep MOSFET devices on track, $SiO_2$ and polysilicon (poly-Si) are replaced with high k and metal gate materials, respectively, to solve the main issues with downscaling. Furthermore, to lowered size of MOSFET has influenced the transistor's doping as well as the dimensions in term of channel length, width, and oxide thickness.

The control of the $V_{TH}$ is the main challenge in the creation of a nanoscale transistor. The entire system of the device will be affected by doping fluctuations if the nominal $V_{TH}$ values are not reached. This study explores a variety of process variables that may affect the fabrication of 14nm-PMOS devices, including source/drain implantation and $V_{TH}$ adjustment implantation, which adjust the profile and electrical characteristics of the device by varying the dose, energy, and tilt of the implantation. Nonetheless, this project is to find the greatest combination of process

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parameters that would result in the nominal $V_{TH}$ value which lead to minimum leakage current.

In order to obtain analysis result of nominal $V_{TH}$ and, low $I_{OFF}$ which refer to ITRS 2013 prediction, by using Taguchi L9 orthogonal array method approach to investigate the effect of the process parameters through a small number of experiments. Other than that, by using Taguchi method able to significantly reduce time for experimental investigation.

Therefore, few reason that smaller size of MOSFETs are desirable because of the small size able to allow high current to pass and it has small gate thus lower the capacitance.

## 1.2 Problem Statement

The traditional MOSFET device have dominated the semiconductor industry for decades, keeping up with Moore's Law has become more difficult due to the numerous challenges provided by exceeding small feature sizes. The presence of short channel effects (SCEs) in ultra-small FETs, scaling of the oxide thickness might result in a high tunnelling current and a lower $I_{ON}/I_{OFF}$ ratio, resulting in poor power consumption. Other than that, Vth decreases as gate length (L) decreases, which is a well-known SCE. For shorter channel lengths, the value of $V_{TH}$ reduces[3]. A crucial fabrication step that might mitigate SCEs in MOSFET devices is source/drain (S/D) implantation[4].

Graphene field effect transistors (GFET) still challenging to be used in digital logic despite their outstanding electronic properties because graphene does not have a band gap in its normal form, making them difficult to turn off. As a result, bilayer graphene will be used in this research to measure this problem. With this method, the graphene

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channel in the transistor is able to induce a band gap leading to higher on-off ratio [5], [6].

The electrical parameters of the FET device, such as $V_{TH}$, $I_{OFF}$ may be deteriorated by changing the dose, energy, and rotation of these implants. Furthermore, one of the most common problems encountered while designing a small sized transistor is the switch $V_{TH}$, which affects the entire implement structure and causes the device to stop working. For instance, the statistical methods are often carried out to optimize device performance.

## 1.3 Objective

The main objective in this research is:

i. To design and simulate a double gate Bi-Graphene of $HfO_2$ and $TiSi_X$ on 14nm PMOS device using Silvaco software.

ii. To analyze and identify the significant process parameter to obtain nominal $V_{TH}$ and minimum $I_{OFF}$ using Taguchi L9 orthogonal array referring to ITRS 2013.

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## 1.4 Scope of work

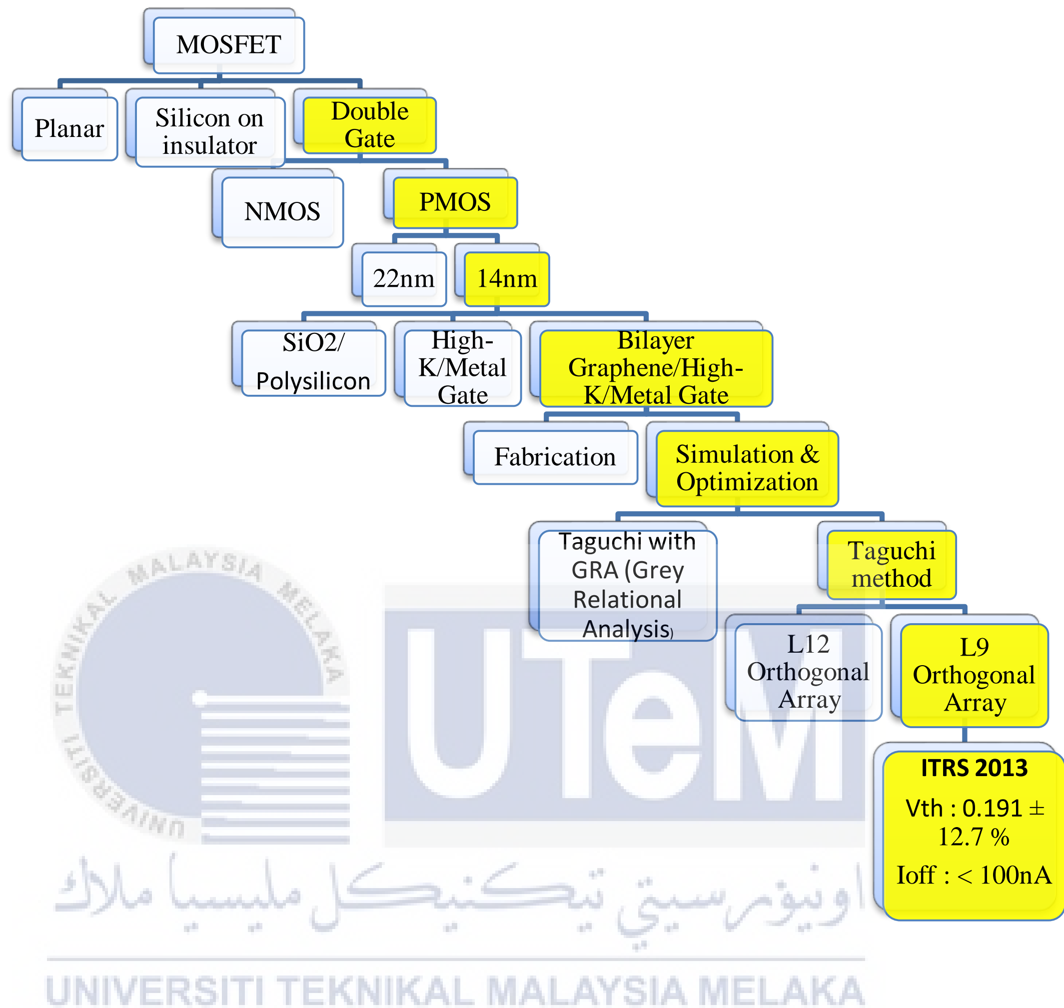


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**Figure 1.1 Shows the scope of work for the project.**