Faculty of Electrical Engineering

DESIGN AND DEVELOPMENT OF SINGLE PHASE CASCADED H-BRIDGE MULTI-LEVEL INVERTER

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A report submitted

in partial fulfillment of the requirements for the degree of Bachelor of Electrical Engineering

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DECLARATION

I declare that this report entitled “Design and Development of Single Phase Cascaded H-Bridge Multilevel Inverter” is the result of my own research except as cited in the references. The report has not been accepted for any degree and is not concurrently submitted in candidature of any other degree.

Signature : …….....

Name : Ahmad Firdaus Bin Roslan

Date : …….....

APPROVAL

I hereby declare that I have read through this report entitled “Design and Development of Single Phase Cascaded H-Bridge Multilevel Inverter” and found that it has comply the partial fulfillment for awarding the degree of Bachelor of Electrical Engineering.

Signature : …….....

Supervisor’s Name : En.Ahmad Aizan Bin Zulkefle

Date : …….....

DEDICATION

To my beloved parents

for their enduring love, motivation and support

ABSTRACT

Inverter is a power electronics device which is used to convert Direct Current (DC) into Alternating Current (AC). The conventional inverter that produces two voltage levels are no longer fulfils the requirement of reducing harmonic distortions. Therefore, Multi-Level Inverter (MLI) is implemented to solve the problem of high harmonic distortion. Instead of two levels of output, the MLI are used to produce multiple steps/stages of voltages levels to obtain a smoother and almost sinusoidal waveform. In addition, Multi-Level Inverter is treated as the one who used frequently and mostly in power converter topologies especially in handling high power and medium voltage industries. However, three of the most commonly used multi-level inverters topologies are Cascaded H-bridge Multi-Level Inverters (CHMLI), Diode Clamped Multi-Level Inverters (DCMLI), and Flying Capacitor Multi-Level Inverters (FCMLI). This project proposed a single phase cascaded h-bridge multi-level inverter (CHMLI) topology in which requires lesser number of components and it is easier to control if compared to the other methods. Inverter of different voltage levels (up to 11-Levels) are designed and simulated using MATLAB Simulink. Level Shifted Multi-Carrier PWM control scheme is used to control the operation of power switches for CHMLI in this project. The results are compared in terms of THD. These results are analyzed and discussed at the end of this report. The value of THD is found to be reduced as the number of voltage level of CHMLI increased. Besides, the hardware developing of single phase 5-Levels CHMLI is designed by using IGBTs that controlled by Field-Programmable Gate Array (FPGA) using the same PWM control scheme in simulation. Both the results from simulation and hardware are compared in the end of this project.

ABSTRAK

Inverter adalah peranti elektronik kuasa yang digunakan untuk menukar arus terus (DC) ke dalam arus ulang-alik (AC). Penyongsang konvensional yang menghasilkan dua tahap voltan tidak lagi memenuhi kehendakan pasaran iaitu mengurangkan kekacauan harmonik. Oleh itu, Multi-Level Inverter (MLI) dilahirkan untuk menyelesaikan masalah herotan harmonik tinggi. MLI digunakan untuk menghasilkan arus dalam bentuk tingkatan yang mana gelombangnya lebih serupa dengan arus ulang-alik. Di samping itu, kerap Multi-Level Inverter digunakan dan kebanyakannya dipakaiguna dalam pengendalian kuasa tinggi dan industri voltan sederhana. Walau bagaimanapun, tiga topologi yang terutamanya merupakan Cascaded H-bridge Multi-Level Inverters (CHMLI), Diode Clamped Multi-Level Inverters (DCMLI), dan Flying Capacitor Multi-Level Inverters (FCMLI). Projek ini mencadangkan Cascaded H-Bridge Multi-Level Inverter (CHMLI) topologi satu fasa yang memerlukan bilangan yang komponen yang kecil dan lebih mudah untuk mengawal berbanding dengan kaedah lain. Inverter tahap voltan yang berbeza (sehingga 11-Level) direka dan simulasi dijalankan mengguna MATLAB Simulink. Tahap teranjak skim kawalan Multi-Carrier PWM digunakan untuk mengawal operasi suis kuasa untuk CHMLI dalam projek ini. Keputusan dibandingkan dari segi THD. Keputusan ini dianalisis dan dibincangkan pada akhir laporan ini. Nilai THD didapati semakin berkurang apabila tahap voltan CHMLI meningkat. Bagi kerja perkakasan membangunkan satu fasa 5-Levels CHMLI akan direka dengan menggunakan IGBT yang dikawal oleh Field-Programmable Gate Array (FPGA) menggunakan skim kawalan PWM yang sama dalam simulasi seperti report ini. Perbandingan kedua-dua dapatan daripada simulasi dan perkakasan akan dikonklusikan dalam bahagian tamat projek ini.

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Alhamdulillah, first of all I would like to thank God as finally I was able to finish my Final Year Project. This project had been done with all afford even though I got problems to choose title or idea on my project. Luckily, the problem can be settling down and I was able to adapt properly and wisely.

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Finally, thanks to my beloved family and friends that always support and give contributions on ideas and help me during my hard time. Without them, I could not complete this report and project and special thank you to everyone who had been to the crucial parts of realization of this project.

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LIST OF ABBREVIATIONS

DC	: Direct Current
AC	: Alternating Current
UPS	: Uninterruptible Power Supplies
PWM	: Pulse Width Modulation
MOSFET	: Metal Oxide Semiconductor Field Effect Transistors
IGBT	: Integrated Gate Bipolar Transistors
THD	: Total Harmonic Distortion
MLI	: Multi-Level Inverter
FPGA	: Field Programmable Gate Array
CHMLI	: Cascaded H-Bridge Multilevel Inverter
PS	: Problem Statement
DCMLI	: Diode-Clamped Multi-Level Inverter
FCMLI	: Flying Capacitor Multi-Level Inverter
NPC	: Neutral-Point Clamped
DSTATCOM	: Distribution Static Compensator
PD	: Phase Disposition
POD	: Phase Opposition Disposition
APOD	: Alternative Phase Opposition Disposition
DFT	: Discrete Fourier Transform
HDL	: Hardware Description Language
IC	: Integrated Circuit
FFT	: Fast Fourier Transform
FYP	: Final Year Project
SPWM	: Sine Pulse-Width Modulation

CHAPTER 1

INTRODUCTION

1.1 Background

Inverter is an electronic device that converts direct current (DC) into alternating current (AC). Applications such as Uninterruptible Power Supplies (UPS), electric motor speed control, Power Grid, Solar and HVDC Power transmission are embedded with inverter in order to generate AC for their operation. The basic operation of an inverter is by switching on and/or off the transistors with Pulse Width Modulation (PWM) techniques. Transistors such as metal oxide semiconductor field effect transistors (MOSFET), thyristors and as integrated gate bipolar transistors (IGBT) are used for a more efficient output.

Efficiency of an inverter is very important in order to provide sufficient output for the entire system. Therefore, Total Harmonic Distortion (THD) is used to measure the quality of AC signal. The THD in an inverter is determined to prevent undesirable losses, malfunction of appliances hence increasing the efficiency of the inverter. While the conventional two-level inverter used today has drawback, where high harmonic distortions exist in its output [1]. The harmonics content or the quality of an AC signal can be determined in terms of total harmonic distortion (THD).

High level of harmonics can lead to undesirable losses, malfunctions of equipment, and some others critical consequences. To decrease the THD, the number of levels needs to be increased but it requires bulky hardware and it will be harder to control. However, the conventional two-level inverter has some disadvantages and restrictions to produce low THD and higher voltage level. Hence, the concept of multi-level inverter (MLI) has been introduced to overcome the situation since 1975 [12].

Therefore, Multi-level Inverter (MLI) is introduced due to the need of low distortion in the output voltage. Multi-level inverter is the new generation of power converter which complies to the demands of high power and medium voltage applications in the industry [2]. MLI is capable in reducing the Total Harmonic Distortion (THD) content in the generated output waveform. This could be done by implementing multiple level of DC Voltages which then leads to the creation of sinusoidal waveform. In the meantime, substituting most of the distortions in the output. Thus, a higher number of DC levels will result in a lower THD. Nevertheless, this improvement will result in a bulkier product and increases the difficulties in controlling the device.

Generally, the switching techniques that used in a MLI is called as Pulse Width Modulation (PWM). PWM is a modulation technique that used to encode messages into pulses signals to control the switches in a circuit. These pulses will trigger the state of switches either on or off. The switches in an inverter are triggered with PWM pulses to perform effective conversion of voltage and current from DC to AC. The generation of PWM requires a drive to encode the pulses required for the switches. Conventionally, the most popular brand of PWM drive in the market such as Allen Bradley, Altera, and Intel.

1.2 Problem Statement

Conventional inverter has been used since the past decades in the field of industrial applications and power systems of lower power usage. Problems appeared when it comes to high power and medium voltages usage. Conventional inverters are found that no longer fulfill the requirement due to the incapable of reducing harmonic contents. It has high switching losses, lower efficiency and the lifespan of systems due to long term constraining. This lead to the growth of Multi-Level Inverter (MLI), the creation of multiple DC levels that combined into sinusoidal wave with reduced harmonic distortion. MLI topologies are introduced to be functioning under high frequency with lesser switching losses and higher efficiency.

The PWM generation for the pulses that to trigger the switches of inverter are said to be slightly complicated and time consumed to be enhance. The Altera Cyclone IV Field Programmable Gate Array (FPGA) is used due to its programmable advantages. The programmable pulses generation could help to improve the efficiency and ease the repair action.

Therefore, this thesis presents the design and development of single phase Cascaded H-bridge Multilevel Inverter (CHMLI) using FPGA (pulse generator) to produce a sinusoidal output waveform.

Table 1.1: Summary of Problem Statement

PS	Problem Statement
PS1	Conventional inverter not capable when it comes to high power and medium voltages usage.
PS2	Conventional inverters are found that no longer full fill the requirement due to the incapable of reducing harmonic contents.
PS3	Conventional inverters have high switching losses, lower efficiency and the lifespan of systems due to long term constraining.

1.3 Motivation

With the invention of MLI topologies, it offers great advantages and imparts an alternative for high power applications over a conventional two-level inverter. However, there are few types of MLI topologies and several issues need to be concerned. As for a diode-clamped inverter, it needs voltage balance control and requires excessive amount of clamped diodes when the output voltage level increases which affects the structure of the circuit to become more complex. Similar to diode-clamped inverter, a flying capacitor inverter needs huge amount of capacitors when it has high voltage level and therefore increases the cost.

On the contrary, a h-bridge inverter does not require diodes and capacitors which reduces the complexity and cost of the circuit. On top of that, it solves voltage balancing problem by cascading several h-bridge inverters with separate DC sources [13]. On the other hand, analogue circuit is mostly used in MLI topology as pulse generator and controller for power switches in the circuit.

The micro-controller or field-programmable gate array (FPGA) is an alternative for the topology as it is capable of controlling complicated applications and it allows real-time operations [14]. Consequently, it gives faster response and simplicity in control as comparing to an analogue circuit. A micro-controller or FPGA also provides flexibility in controlling a system in which an analogue circuit does not offer advantage as it is a single purpose-built circuit to serve only single operation [15]. With FPGA, it can change to any controlling method by altering the coding of the program easily and even monitor the process.

As illustrated in Figure 1.1, Field-programmable gate array (FPGA) is an alternative device for pulse generation and controller for power switches in the circuit of a MLI.

Figure 1.1: Altera FPGA Cyclone IV Programmable Chip

Field-programmable gate array (FPGA) is an alternative device for pulse generation and controller for power switches in the circuit of a MLI. FPGA can control complicated applications and allows a real-time operation. FPGA has flexibility in modifying the states or conditions of power switches. Therefore, it can alter the program easily by programming the coding in it and even monitoring the process of device.

1.4 Objectives

The objectives of this project are:

a) To design a single phase cascaded h-bridge multi-level inverter up to eleven levels that provide nearly sinusoidal output voltage using MATLAB Simulink.

b) To analyze the simulation results of different number of level of Multi-Level Inverter and amplitude modulation in terms of Total Harmonic Distortions (THD).

c) To develop a Single Phase five Levels Cascaded H-Bridge Multi-Level Inverter circuit using FPGA.

d) To analyze the hardware result of Single Phase Seven Levels Cascaded H-Bridge Multi-level inverter and compare with the simulation result.

1.5 Scope

The scopes of the project are: -

a) This project focuses on the design of single phase h-bridge cascaded multi-level inverter up to eleven levels to reduce harmonic content as well as THD.

b) This multi-level inverter is built and tested with MATLAB Simulink to observe the changes in amplitude modulation with suitable level.

c) The single phase five levels cascaded h-bridge multi-level inverter will be built using FPGA.

d) The hardware results of single phase five levels CHMI will be compared to simulation results.

1.6 Conclusion

The background of this project will be discussed in this chapter. Explanation is made based on the problem statement found in researches. Besides, the objectives and scopes of this project is identified to ensure it meet its learning outcome at the end of this project.

CHAPTER 2

LITERATURE REVIEW

2.1 Introduction

In this modern world, Multi-level inverter (MLI) is introduced mainly due to the high demand of high power and medium voltages applications especially in the field of renewable energy sources. MLI topology is effective in replacing the conventional two-level inverter. MLI is producing stepped waveform which is similarly to the sine wave. The steps are formed by supplying with different DC levels supported by series connected input source [2]. As the number of levels increases, the more steps the inverter produced.

A higher number of levels will produce a smoother stair case wave that approaching closely to desired sine wave for AC-operated applications. The quality of output, Total Harmonic Distortion are measured using Fast Fourier Transform analysis tools in MATLAB Simulink.

2.2 Multi-Level Inverter Topology

Inverter is a power electronic circuit which converts the DC to AC power. Nowadays, Multi-Level Inverter are used in many applications under high power switching condition [5].

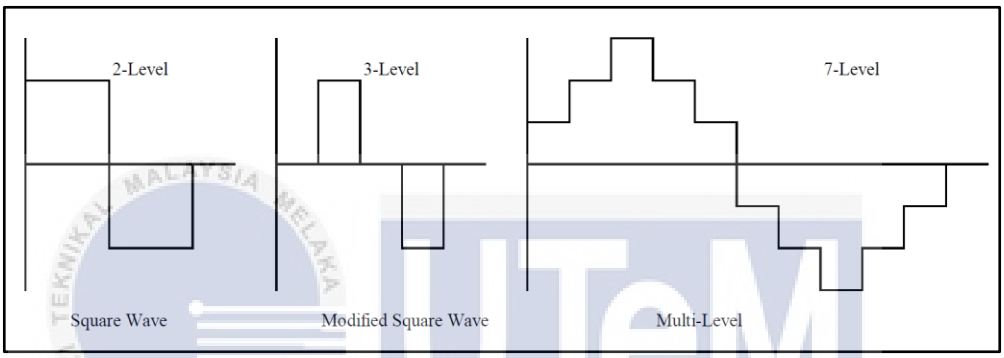


Figure 2.1: Differences of Waveforms

As shown in Figure 2.1, multiple voltage levels are used to create waveform in order to produce a waveform more likely to a sine wave. Therefore, Multi-Level Inverter is more frequently used today compared with another conventional 2-Level inverter.

The basic types of multi-level inverter topologies used are diode-clamped multi-level inverter (DCMLI), flying capacitor multi-level inverter (FCMLI), and cascaded h-bridge multi-level inverter (CHMLI). As exhibited in Figure 2.2, the topologies of MLI are classified into separated DC sources and common DC source.

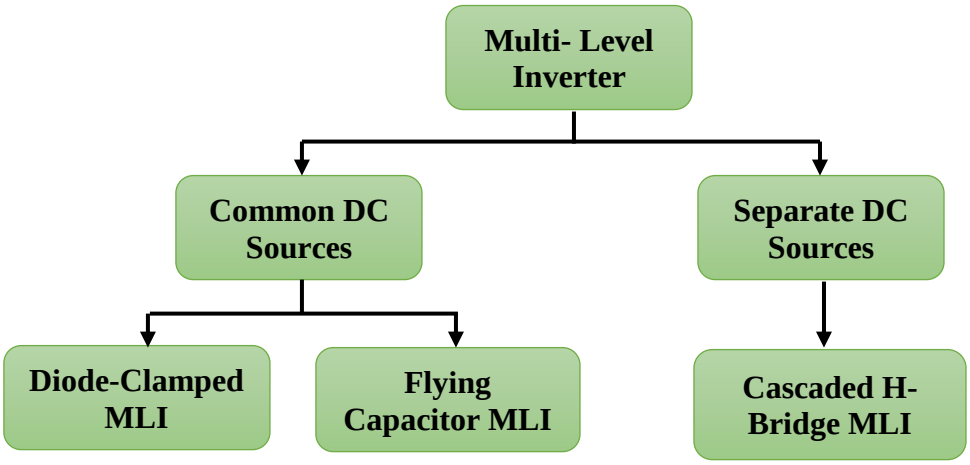


Figure 2.2: Classification of Multi-Level Inverter

2.2.1 Diode-Clamped Multi-Level Inverter (DCMI)

There are many past researches and studies about DCMI topology, one of them is on solar power system. This research focused on designing a power conditioned system for extraction of DC solar power and conversion of DC to AC power to be supplied to the load by using DCMI topology with PWM technique [16].

Diode-clamped Multi-Level Inverter (DCMLI) is also known as Neutral-Point Clamped Inverter (NPC) when initially introduced in 1981 [1]. A DCMLI is constructed with capacitor on the DC input and Diode switches to create Multi-Level Inverter. Figure 2.3 shown below is the basic structure of a single-phase 5-level Diode Clamped Inverter [4]. The output voltage is half of the input DC voltage. Therefore, simple control technique is required to solve this problem. Hence, the amount of component like switches and diode have to be increased.

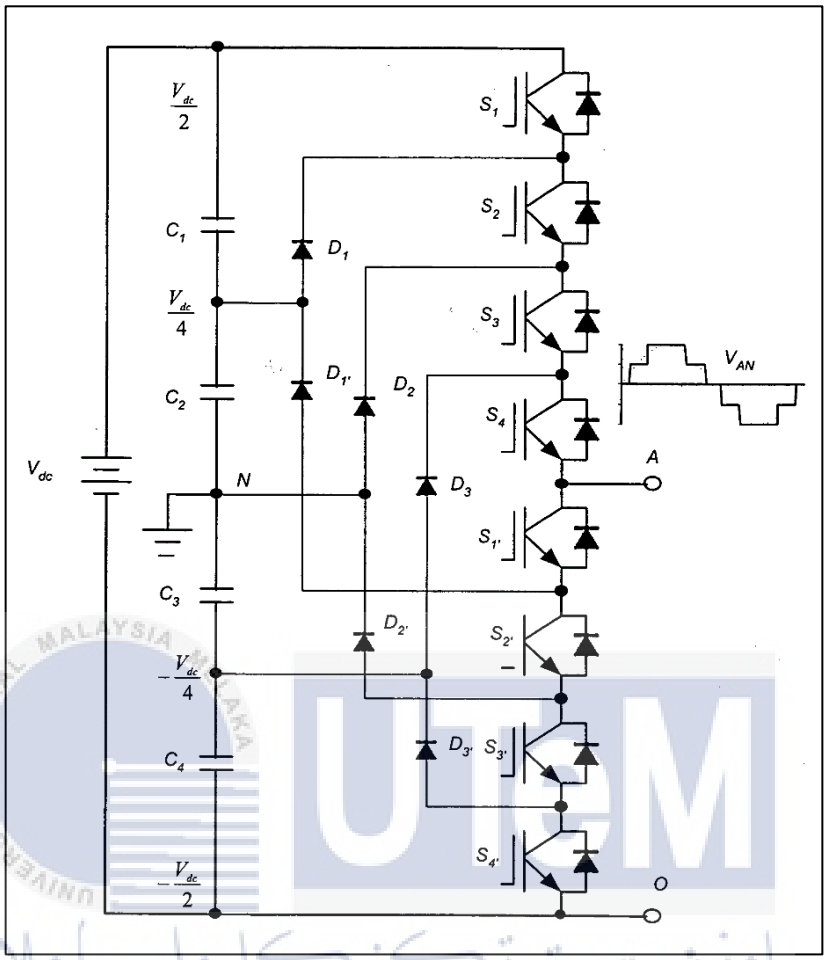


Figure 2.3: Single-Phase 5-level Diode Clamped Inverter

Principle of Operation

Figure 2.3 shows a single phase five-level DCMI that consists of four dc bus capacitors, six clamped diodes, and eight power semiconductor switches. The voltage across each of the capacitor is and the clamped diodes limits the voltage stress of each devices to a single capacitor voltage level of. The steps of synthesis of staircase voltage for a five-level DCMI are explained below [17,18]:

a) Voltage output $V_{AN} = \frac{V_{dc}}{2}$, turn on switches S_1, S_2, S_3, S_4.

b) Voltage output $V_{AN} = \frac{V_{dc}}{4}$, turn on switches $S_2, S_3, S_4, S_{1'}$.

c) Voltage output $V_{AN} = 0$, turn on switches $S_3, S_4, S_{1'}$ and $S_{2'}$.

d) Voltage output $V_{AN} = -\frac{V_{dc}}{4}$, turn on switches $S_4, S_{1'}, S_{2'}$ and $S_{3'}$.

e) Voltage output $V_{AN} = -\frac{V_{dc}}{2}$, turn on switches $S_{1'}, S_{2'}, S_{3'}$ and $S_{34'}$.

The number of capacitor that required for a certain level of inverter can be calculated as equation 2.1 [4].

$$N_C = N_L - 1 \tag{2.1}$$

As shown in the formula, the N_C represents the number of capacitors while N_L represents the number of level. For example, a 5-Level inverter will require 4 capacitors to complete the circuit. For a 5-Level inverter, the switching mode for each of the switches are tabulated as the Table 2.1.

Table 2.1: Switching condition of a single phase five-level DCMI

(Switching condition 1 = ON, 0 = OFF)

Output Voltage, V_O	**Switching State**							
	S_1	**S_2**	**S_3**	**S_4**	**S_1'**	**S_2'**	**S_3'**	**S_4'**
$\frac{V_{dc}}{2}$	1	1	1	1	0	0	0	0
$\frac{V_{dc}}{4}$	0	1	1	1	1	0	0	0
0	0	0	1	1	1	1	0	0
$-\frac{V_{dc}}{4}$	0	0	0	1	1	1	1	0
$-\frac{V_{dc}}{2}$	0	0	0	0	1	1	1	1

The switching state of a single phase five-level DCMI is summarized in Table 2.1. As it can be observed in Table 2.1 there is a drawback of the DCMI which is the optimum output voltage obtained is only half of the DC voltage source. The output waveform of DCMI is as shown in Figure 2.4.

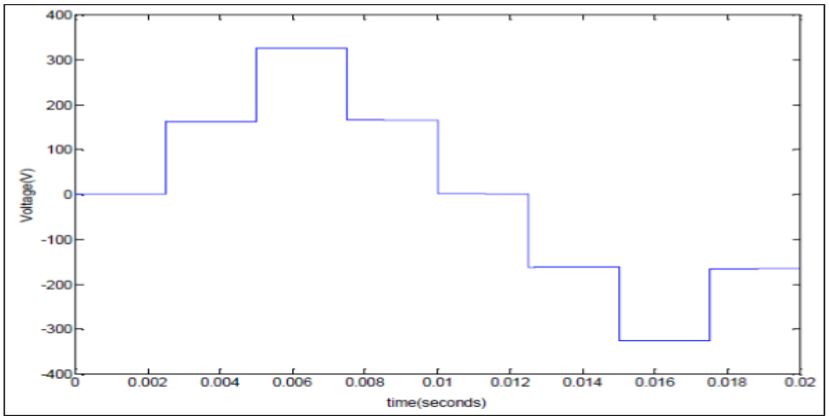


Figure 2.4: Example of five-level DCMI output waveform

Advantages of DCMI

One of the advantages of DCMI topology is simple to control due to its simple structure. It also utilizes only a DC source rather than multiple sources. Thus, it will be a better option when there is only single DC source applied for certain applications. Moreover, it is very efficient as its power switches are being controlled at first harmonic. It does not need filters when its harmonic content is low enough by increasing number of levels [19, 20].

Disadvantages of DCMI

Nevertheless, the controlling becomes complex when the voltage levels are increased where more components are required. The excessive clamping diodes are required when the number of levels is high where this will insult the difficulty in controlling the real power flow of the individual inverter in a Multi-Level Inverter system [4].

2.2.2 Flying Capacitor Multi-Level Inverter (FCMI)

Flying capacitor multi-level inverter is widely has been used in high power applications such as the distribution static compensator (DSTATCOM). FCMI is invented to improve the efficiency and ease the control of the compensator. The FCMI replaced the conventional inverter in term of providing better performance in power conversion. It can control both active and reactive power flow [5]. Previously, it is proposed to replace the old method that requires transformer in order to improve the efficiency and ease the control of the compensator. This FCMI technique was initially presented in 1992 in order to replace the conventional inverter for better power conversion performance purpose. It has capability of resolving the unbalanced capacitor voltage issues and excessive diode requirement in DCMI topology. This type of inverter includes power switches, diodes, DC bus capacitors and clamped-capacitors. Figure 2.5 shows the Single Phase 5-Level FCMI.

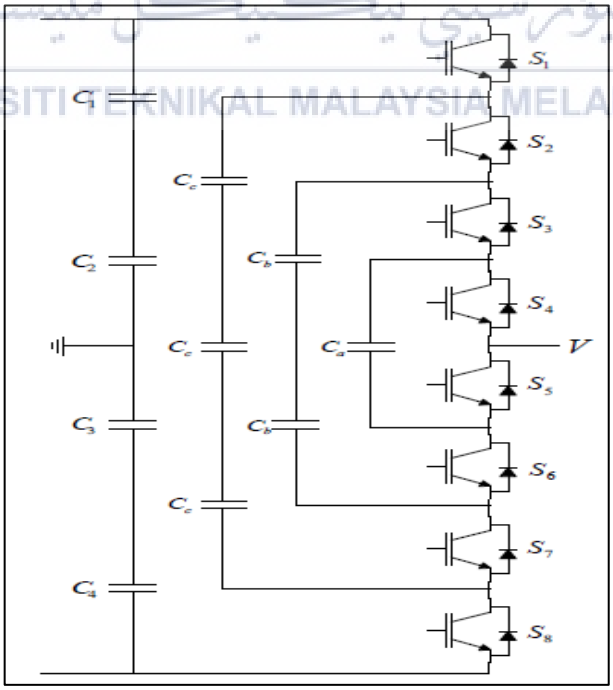


Figure 2.5: Single Phase 5-Level FCMI

Principle of Operation

The equation 2.1 introduced in FCMLI for calculating the number of Capacitors at the DC input. Similar to DCMI, N_C represents the number of capacitors while N_L represents the number of level. For a 5-Level inverter, the switching mode for each of the switches are tabulated in the Table 2.2.

Table 2.2: Switching state of five-level FCMI

Output Voltage, V_O	Switching State							
	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
$\frac{V_{dc}}{2}$	1	1	1	1	0	0	0	0
$\frac{V_{dc}}{4}$	1	1	1	0	1	0	0	0
0	1	1	0	0	1	1	0	0
$-\frac{V_{dc}}{4}$	1	0	0	0	1	1	1	0
$-\frac{V_{dc}}{2}$	0	0	0	0	1	1	1	1

Advantages

This topology used large amount of storage capacitors which will provide capabilities during power outages and switch combination redundancy in order to balance the different voltage levels. FCMI topology is capability of controlling real and reactive power flow for high voltage DC transmission. It does not require separate DC sources and extra clamped-diodes. As the other topology, the higher the voltage levels, the lower the harmonic content. For this topology, both the real and reactive power flow can be controlled.

Disadvantages

Hence, the excessive number of capacitors are required when the number of levels is increased where this will result in a bulkier power capacitor and becoming expensive [4]. Even tough, the inverter is able to control the real power transmission and yet this controlling method is complicated while the switching frequency and switching losses are high. The efficiency of FCMI decreases with the increase in real power transmission as the switching losses are high. It is also harder to control than DCMI topology.

2.2.3 Cascaded H-Bridge Multi-Level Inverter

Cascaded h-bridge multi-level inverter is slightly different as compared to DCMLI and FCMLI. CHMLI is constructed based on topology that cascading multiple h-bridge inverters to produce sinusoidal voltage waveform. Each phase of H-Bridge is connected with one separated DC source. Hence, the output voltage for a higher-level inverter will be higher. Besides, multiple level of cascaded h-bridge will result in a lower THD output voltage. Therefore, CHMLI is proposed as the solution for high distortion content in the output.

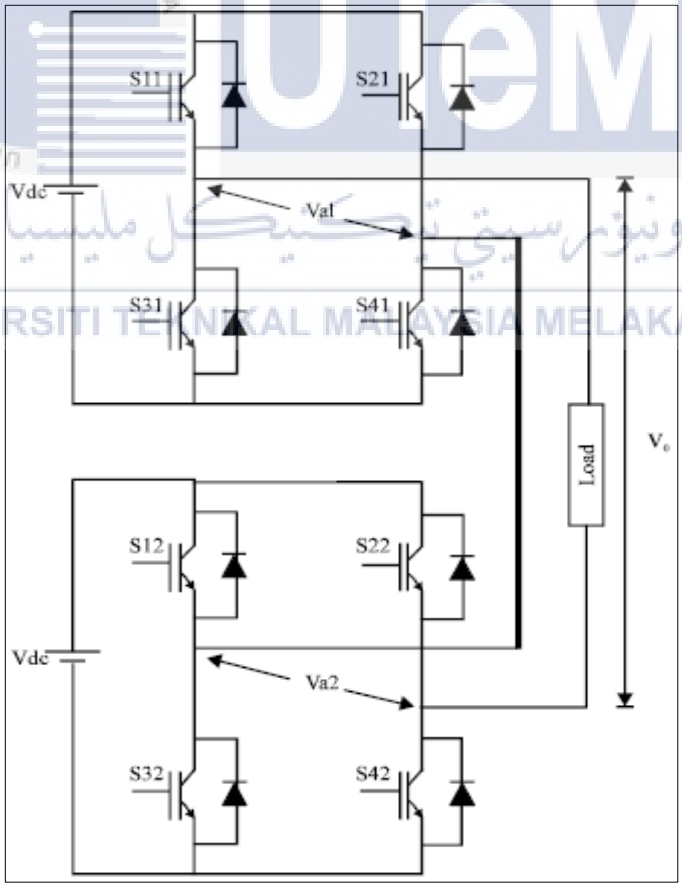


Figure 2.6: Single Phase 5-Level Inverter

Principle of Operation

Figure 2.5 shows a single-phase 5-Level Cascaded H-Bridge MLI. It consists of 2 separate DC sources and 2 cascaded H-bridge. Hence the output voltage is the sum of the input voltages.

Table 2.3: Switching States of each IGBTs in CHMLI

Voltage Level (V)	S1	S2	S3	S4	S5	S6	S7	S8
2VDC	1	1	0	0	1	1	0	0
VDC	1	1	0	0	0	1	0	1
0	0	1	0	1	0	1	0	1
- VDC	0	0	1	1	0	1	0	1
- 2VDC	0	0	1	1	0	0	1	1

As shown in Table 2.3, the maximum and minimum of output voltage are $\pm 2V_{DC}$, which is due to the 2 input voltages for the 2 cascaded H-Bridges.

Advantages

This topology solved the problems of extra diodes and capacitors as compared in the DCMLI and FCMLI topologies. Comparing to the DCMLI and FCMLI, this topology required the least amount of components. Due to its simple constructions, this topology is much easier to control.

Disadvantages

The advantages of CHMLI will be focusses on the sourcing part. This s due to its limitation of usage on some application that do not have an isolated DC sources. Besides, the separated sources effect on the inconvenience in which more sources are needed to produce a smoother graph using an inverter of greater voltage levels.

2.3 Pulse-Width Modulation

Pulse-Width Modulation is the process of modifying the width of pulses in direct proportion to control signal [3]. For generating pulses for an inverter, sinusoidal waveform is acting as the reference frequency for a PWM circuit. Therefore, the sinusoidal reference waveform is compared with the input waveform to produce the pulses for driving a circuit.

The advantages of the modulation technique are:

i. Increase the quality of reception with the help of modulation

ii. Avoid mixing of different frequency signal and increase the range of communication

iii. Allow the flexibility for adjusting bandwidth

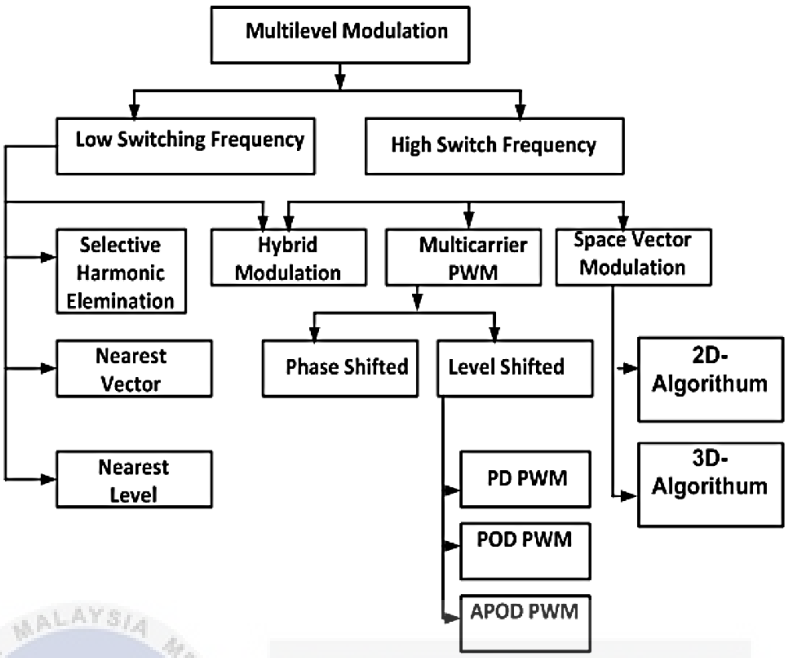


Figure 2.7: Classification of Modulation Technique

The Figure 2.7 shows the classification of modulation technique where the high switching frequency is considered above 1kHz.

2.3.1 Pulse-Width Modulation Consideration

Some definition and explanation should be considered when PWM is used in an inverter. The considerations are based on frequency modulation ratio, $\boldsymbol{m_f}$ and amplitude modulation ratio $\boldsymbol{m_a}$.

2.3.1.1 Frequency Modulation Ratio, m_f

The Fourier series of the PWM output voltage has the fundamental frequency which is the same as the reference signal, $\boldsymbol{m_f}$ should be an old integer. If $\boldsymbol{m_f}$ is not an integer, there may exist sub- harmonics at output voltage. Increasing the carrier frequency (increasing $\boldsymbol{m_f}$) increases the frequencies at which the harmonics occur. Frequency modulation ration is represented in Equation 2.2.

$$m_f = \frac{f\ carrier}{f\ reference} = \frac{f\ tri}{f\ stine} \tag{2.2}$$

2.3.1.1 Amplitude Modulation Ratio, m_a

The amplitude of the fundamental frequency of the PWM output is thus controlled by $\boldsymbol{m_a}$. Alternatively, $\boldsymbol{m_a}$ can be varied to change the amplitude of the output. However, if $\boldsymbol{m_a}$ is greater then 1, the of the output increases with $\boldsymbol{m_a}$ but not linearly. The amplitude modulation ratio is represented in Equation 2.3. if the $0 \leq \boldsymbol{m_a} \leq 1$, the fundamental output voltage will calculate as illustrated in Equation 2.3.

$$\boldsymbol{m_a} = \frac{V_m,references}{V_{c,}carrier} = \frac{V_m,sine}{V_{c,}tri}$$

$$V_1 = \boldsymbol{m_a}\, V_{dc}$$

(2.3)

2.3.2 Multi-Carrier Pulse-Width Modulation

Multiple Pulse-Width Modulation Technique is used in three level or higher. This technique is classified into two types which is the Phase Shift and Level Shift [5].

Phase Shifted Pulse-Width Modulation

The carrier signals of same amplitude and frequency are phase shifted by 90 degrees between one another and compared with the reference waveforms. The gate signals for the cascaded inverter can always be derived directly from the PWM signals [6]. The derivation is the comparison of carrier signals with the trapezoid signals.

The amplitude modulation index that defined for this technique is shown in equation 2.3.

$$\mathbf{m_a} = \frac{\mathbf{A_m}}{\left[\frac{\mathbf{A_c}}{\mathbf{2}}\right]} \tag{2.3}$$

Where

Am represents the peak amplitude of modulating wave

Ac represents the peak amplitude of each carrier wave

Level Shifted Pulse Width Modulation

Carrier signals are vertically shifted to each other. The Level-Shifted PWM is classified into Phase Disposition (PD-PWM), Phase Opposition Disposition (POD-PWM) and Alternative Phase Opposition Disposition (APOD-PWM) [5,7].

1. **Phase Disposition (PD-PWM)**

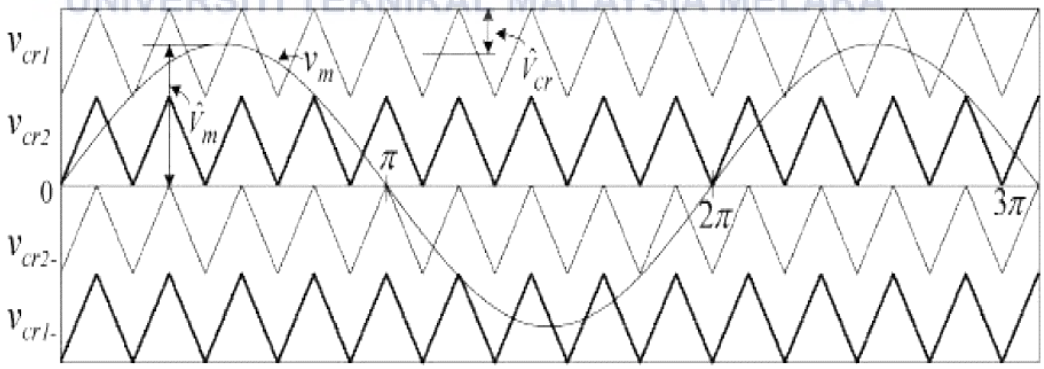


Figure 2.8: PD-PWM

Figure 2.8 illustrates the waveform of multiple carriers and reference sine wave of a PD-PWM. This scheme employs all carriers of same frequency in phase.

2. Phase Opposition Disposition (POD-PWM)

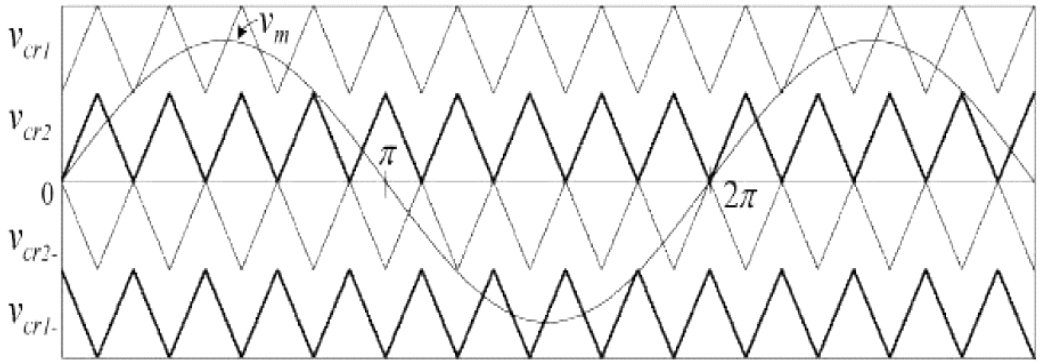


Figure 2.9: POD-PWM

Figure 2.9 shows the waveform of multiple carriers and reference sine wave of a POD-PWM. It carrier signals must above zero axis. All carrier wave has same frequency and amplitude. Then, all carrier wave has phase shifted 180 degrees below zero axis.

3. Alternative Phase Opposition Disposition (APOD-PWM)

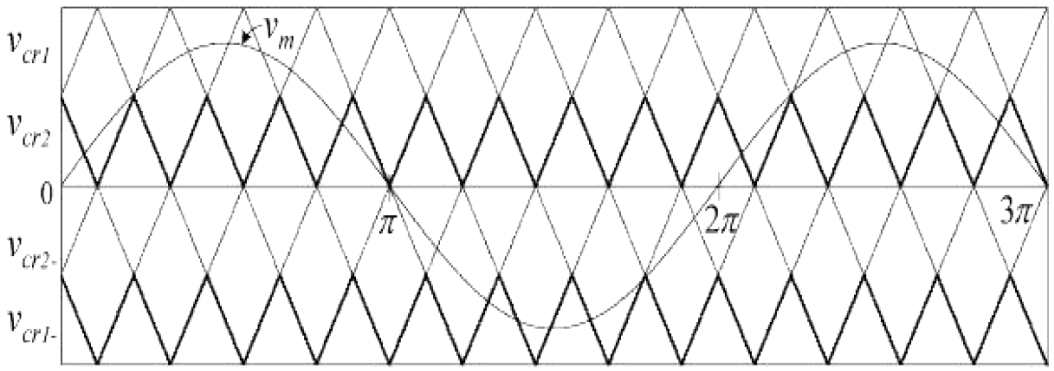


Figure 2.10: APOD-PWM

Figure 2.10 exhibits the waveform of multiple carriers and reference sine wave of a POD-PWM. This scheme employs all carriers of same frequency but phase shifted 180 degrees from its adjacent carrier.

For Multi-Carrier Level Shifted PWM, its amplitude modulation index is defined in equation 2.4.

$$\mathbf{m_a} = \frac{\mathbf{A_m}}{\mathbf{A_c(m-1)}} \text{ for } 0 \leq \text{ma} \leq 1 \tag{2.4}$$

Where

Am represents the peak amplitude of modulating wave

Ac represents the peak amplitude of each carrier wave

m represents the voltage level(s) of the inverter.

2.4 Total Harmonic Distortion

The Total Harmonic Distortion (THD), is a measurement of the harmonic distortion present and is defined as the ratio of the sum of the powers of all harmonic components to the power of fundamental frequency. Therefore, THD is the best method of measure of the quality of output waveform as defined in equation 2.5.

$$\mathbf{THD} = \frac{\sqrt{\sum_{n=2}^{\infty}(V_{n,rms})^2}}{V_{total,rms}} \tag{2.5}$$

Where the percentage of THD can be calculate as in equation 2.6.

$$\mathbf{THD\%\ of\ fundamental} = \frac{\sqrt{\sum_{n=2}^{\infty}(V_{n,rms})^2}}{V_{total,rms}} \times 100\% \quad (2.6)$$

The definition for THD equation above is based on the Fourier Series. Therefore, there is some bene fits that to determine the THD using the Fourier Series [8].

2.5 Fast Fourier Transform

Fourier analysis is a method used to convert time domain waveforms into frequency components and vice versa. Fourier series can be used to calculate the magnitudes and phases of the fundamental and its harmonic components [9].

The equation 2.7 shows the equation for Fourier Series [10].

$$F(t) = \int_{-\infty}^{\infty} f(t)e^{-j2\pi ft}dt \quad (2.7)$$

Fast Fourier Transform is implemented in order to performs better for estimation of periodic signals. This implementation improves the analysis by shorten the time used as compared to the Discrete Fourier Transform (DFT).

2.6 Field-Programmable Gate Array

Field-Programmable Gate Array (FPGA) is an integrated circuit (IC) designed to be configured by consumer repeatedly. The FPGA configuration can do by using Hardware Description Language (HDL). FPGA can be used as a processing of signals and data acquire tools. Processing of signals such as pulses generation while data acquire such as output value of both digital and analogue type [11].

2.7 Gate Driver

Gate driver is a power amplifier that receives low power input and produces high current at the output. Gate driver perform amplification and isolation of the pulses that received to ensure the pulses have an amplitude that are high enough to triggered the transistors. The gate driver is needed for every transistor to protect the circuit of combination of transistors. Usually, a gate driver consists of an optocoupler and a boost converter which results in a higher power of output that required by the circuit. An Optocoupler is used to receive and control the pulses at the output where connected in parallel to the DC boost converter.

Figure 2.11: Optocoupler

DC boost converter is used to step up the DC voltage from 5 Volts to 15 Volts. Where the output of the DC boost is connected in parallel such that the input pulses will triggered the 15 Volt as output pulses to reach the transistor.

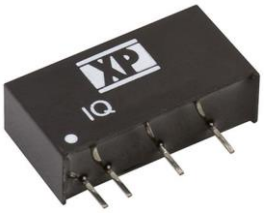


Figure 2.12: Boost Converter

2.7 Summary of Review

Cascaded H-Bridge MLI is the best topology among the others where It has a lesser number of switches (IGBTs). Therefore, the switches losses are lower compared to other topologies. Besides, the percentage of THD content in a Cascaded H-Bridge MLI is lower than the other two.

Pulse Width Modulation is important in order to generate pulses or signals to control the switches of inverter. Level-Shifted Multi-Carrier PWM will be the better choice where number of carriers tend to be increase easily. The increase of voltage level does not increase the complexity of the circuit.

The analysis of THD content will be perform using FFT method. This method can be trigger easily in the MATLAB-Simulink tools and require lesser time compare to manually calculations.

Hardware implementation is making use of Field-Programmable Gate Array (FPGA) where it is used to generate PWM pulses for the controlling of the switches in MLI. Gate Driver is used to perform amplification and isolation of pulses before sending to the switches in h-bridge.

CHAPTER 3

METHODOLOGY

3.1 Introduction

This chapter describes about the project methodology that is practiced in this project. Started with literature review which enables the understanding on the topology, behavior, and method/techniques used in designing a Multi-Level Inverter. The design on MLI is included the use of topology, switching technique, and the Total Harmonic Distortion content in the output voltage. The simulation of the circuit is run to record the results at the output of MLI. The details will be discussed further in this section.

3.2 Research Methodology

This section will cover information such as flow chart of the project, milestone allocated for this project, and Gantt Chart that illustrate the plan and flow for this project.

3.2.1 Flow Chart

The flow of the final year project 1 (FYP 1) is shown as in the flow chart designed in Figure 3.1. The development of this project started with the literature review of Multi-Level Inverter from the previous research journal. There are several topologies that had been used currently where the concepts are yet to be discover, in order to understand the concept and theory behind the circuit design. Based on the researches, the selected control schemes and switching technique are chosen to design the Multi-Level Inverter in this project. After that, there are topology of cascaded H-bridge multi-level inverter and sine pulse-width modulation (SPWM) switching technique and the design of Cascaded H-Bridge Multi-Level Inverter is simulated by using the MATLAB Simulink. The simulated result is verified, analyzed and compared based on the concept and theory. Lastly, the report is written and concluded with the hardware developments that will be continued in final year project 2 (FYP 2).

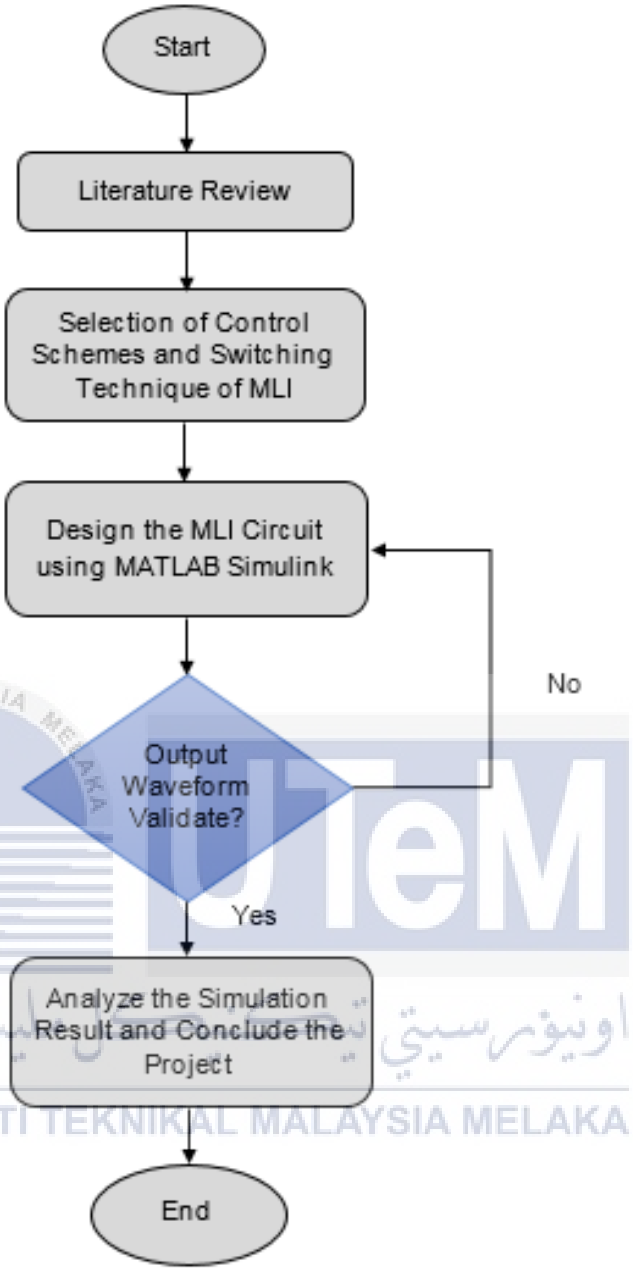


Figure 3.1 : Flow Chart for FYP 1

The development process of the hardware for final year project 2 (FYP 2) is as illustrated in Figure 3.2. Initially, the suitable components for the single phase five levels CHMI circuit are selected and purchased. The prototype is then started with the built of Gate Drivers followed by programming code for the pulses that will be programmed into FPGA chip. After the prototype is validated to be functioning well, the hardware results are obtained and analyzed. Last but not the least, the final report is completed for this project.

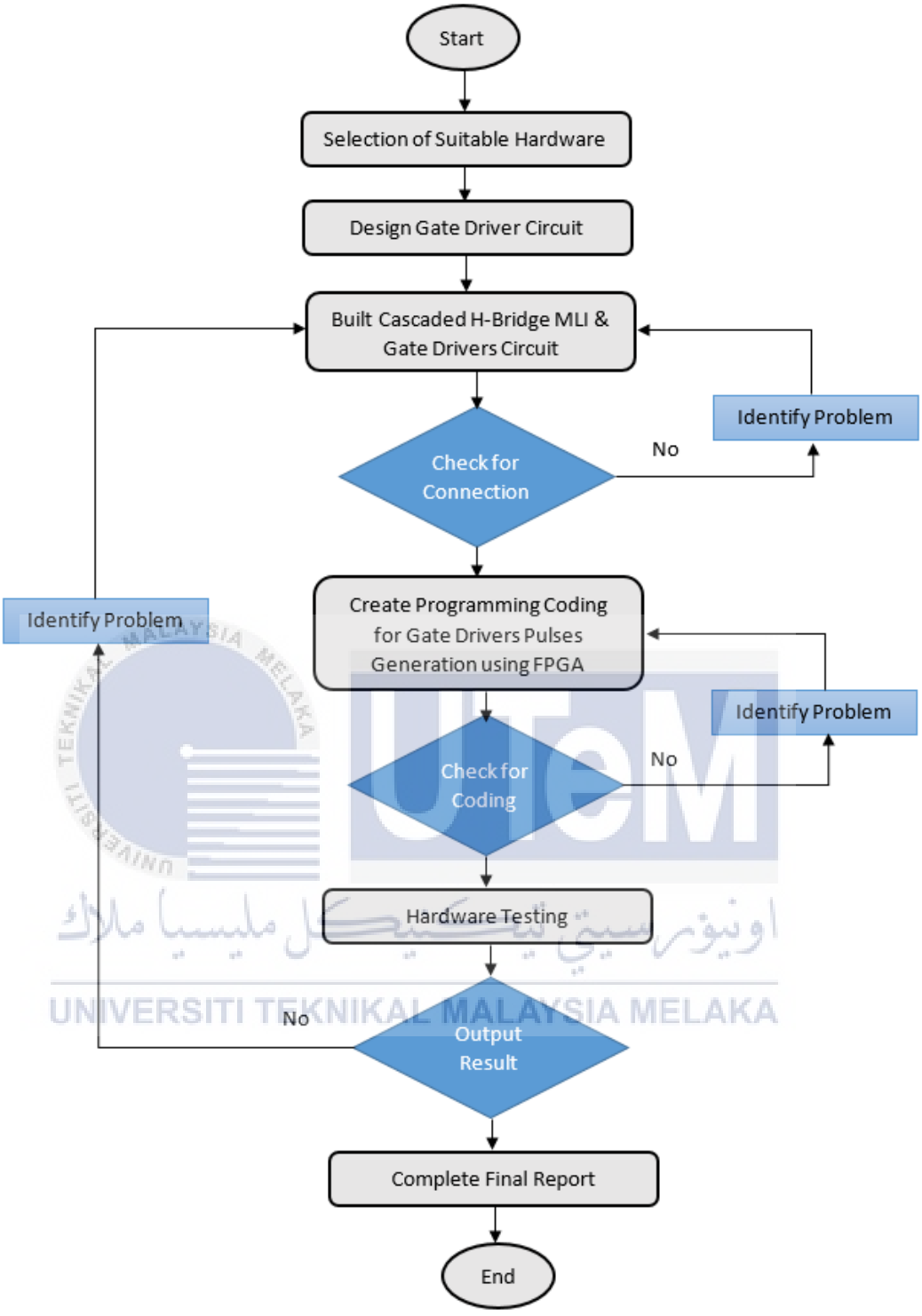


Figure 3.2 : Flow Chart for FYP2

3.2.2 Milestones

The milestones assigned for this project are as follows:

a) Milestone 1: Research on literature review.
b) Milestone 2: Design of single phase CHMI up to 11 levels.
c) Milestone 3: Simulation of single phase CHMI up to 11 levels and hardware implementation of 5 levels CHMI.
d) Milestone 4: Validate & analyze simulation output waveform obtained (simulation and hardware).
e) Milestone 5: Analyze the Total Harmonic Distortion content in the output (simulation and hardware).
f) Milestone 6: Final report writing.

3.2.3 Gantt Chart

A Gantt Chart is constructed that illustrates the flow of this project.

Table 3.1: Gantt Chart for FYP 1

Project Activity	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Literature Review	■	■	■	■	■	■									
Simulation of Multi-Level Inverter (MLI)				■	■	■	■	■	■	■					
Project Report Writing		■	■	■	■	■	■	■	■	■	■	■			
Project Report Correction													■	■	■
Final Year Project Presentation												■			

Table 3.2: Gantt Chart for FYP 2

Project Activity	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Hardware															
Coding (FPGA)															
Project Report Writing															
Project Report Correction															
Final Year Project Presentation															

3.3 Project Topology

The topology of Multi-Level Inverter that will be used in this project is the Cascaded H-Bridge. Cascaded H-Bridge is constructed with 4 switches (IGBTSs). Each of the H-Bridge represents an increment of 2 levels of the inverter. Therefore, the Table 3.3 shows the number of H-Bridges in an inverter of different number of voltage level.

Table 3.3: Number of H-Bridges in MLI

Voltage Level(s)	No. of H-Bridges
3	1
5	2
7	3
9	4
11	5

3.3.1 Control Switching Technique Used

There are many modulation control schemes in multilevel inverter systems. In this project, MATLAB simulation software is used to analyze of the MLI cascaded PWM multilevel inverter using SPWM.

The multilevel inverter used the multi-carrier base PWM as the modulation control schemes. The implementation of SPWM techniques for multilevel inverters are POD technique, PD technique and alternative phase APOD technique. This project used the PD technique to implement the SPWM switching schemes. The PD technique is easiest to implement compared to POD and APOD technique.

3.3.2 Switching States

Table of switches on-off state are constructed to clarify the output signal generation. All the levels are discussed further in the Table 3.4, 3.5, 3.6, 3.7 and 3.8. As all the tables shown, each switch has its own unique pulses. For every switch, there must be another switch which its' pulses are inverted from itself. For example, the inverted pulses of S1 will be the same as the S4's pulses. With all the information written in table, the modulation of signal is ready to take place.

3.3.2.1 3-Levels Inverter

For a 3-Levels Inverter, the voltage levels included are V_{DC}, 0, $-V_{DC}$. The table for switches states is shown in Table 3.4.

Table 3.4: Switching State of Switches of 3-Levels Inverter

Voltage Level	S1	S2	S3	S4	Output Voltage
1	1	1	0	0	V_{DC}
0	0	1	0	1	0
-1	0	0	1	1	$-V_{DC}$

3.3.2.2 5-Levels Inverter

For a 5-Levels Inverter, the voltage levels included are $2V_{DC}$, $1V_{DC}$, 0, $-V_{DC}$, $-2V_{DC}$. The table for switches states is shown in Table 3.5.

Table 3.5: Switching State of Switches of 5-Levels Inverter

Voltage Level	S1	S2	S3	S4	S5	S6	S7	S8	Output Voltage
2	1	1	0	0	1	1	0	0	$2V_{DC}$
1	1	1	0	0	0	1	0	1	V_{DC}
0	0	1	0	1	0	1	0	1	0
-1	0	0	1	1	0	1	0	1	$-V_{DC}$
-2	0	0	1	1	0	0	1	1	$-2V_{DC}$

3.3.2.3 7-Levels Inverter

For a 7-Levels Inverter, the voltage levels included are $3V_{DC}$, $2V_{DC}$, $1V_{DC}$, 0, $-V_{DC}$, $-2V_{DC}$, $-3V_{DC}$. The table for switches states is shown in Table 3.6.

Table 3.6: Switching State of Switches of 7-Levels Inverter

Voltage Level	**S1**	**S2**	**S3**	**S4**	**S5**	**S6**	**S7**	**S8**	**S9**	**S10**	**S11**	**S12**	**Output Voltage**
3	1	1	0	0	1	1	0	0	1	1	0	0	$3V_{DC}$
2	1	1	0	0	1	1	0	0	0	1	0	1	$2V_{DC}$
1	1	1	0	0	0	1	0	1	0	1	0	1	V_{DC}
0	0	1	0	1	0	1	0	1	0	1	0	1	0
-1	0	0	1	1	0	1	0	1	0	1	0	1	$-V_{DC}$
-2	0	0	1	1	0	0	1	1	0	1	0	1	$-2V_{DC}$
-3	0	0	1	1	0	0	1	1	0	0	1	1	$-3V_{DC}$

3.3.2.4 9-Levels Inverter

For a 9-Levels Inverter, the voltage levels included are $4V_{DC}$, $3V_{DC}$, $2V_{DC}$, $1V_{DC}$, 0, $-V_{DC}$, $-2V_{DC}$, $-3V_{DC}$, $-4V_{DC}$. The table for switches states is shown in Table 3.7.

Table 3.7: Switching State of Switches of 9-Levels Inverter

Voltage Level	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	S13	S14	S15	S16	Output Voltage
4	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	$4V_{DC}$
3	1	1	0	0	1	1	0	0	1	1	0	0	0	1	0	1	$3V_{DC}$
2	1	1	0	0	1	1	0	0	0	1	0	1	0	1	0	1	$2V_{DC}$
1	1	1	0	0	0	1	0	1	0	1	0	1	0	1	0	1	V_{DC}
0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
-1	0	0	1	1	0	1	0	1	0	1	0	1	0	1	0	1	$-V_{DC}$
-2	0	0	1	1	0	0	1	1	0	1	0	1	0	1	0	1	$-2V_{DC}$
-3	0	0	1	1	0	0	1	1	0	0	1	1	0	1	0	1	$-3V_{DC}$
-4	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	$-4V_{DC}$

3.3.2.5 11--Levels Inverter

For a 11-Levels Inverter, the voltage levels included are $5V_{DC}$, $4V_{DC}$, $3V_{DC}$, $2V_{DC}$, $1V_{DC}$, 0, $-V_{DC}$, $-2V_{DC}$, $-3V_{DC}$, $-4V_{DC}$, $-5V_{DC}$. The table for switches states is shown in Table 3.8.

Table 3.8 Switching State of Switches of 11-Levels Inverter

Voltage Level	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	S13	S14	S15	S16	S17	S18	S19	S20	Output Voltage
5	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	$5V_{DC}$
4	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	0	1	0	1	$4V_{DC}$
3	1	1	0	0	1	1	0	0	1	1	0	0	0	1	0	1	0	1	0	1	$3V_{DC}$
2	1	1	0	0	1	1	0	0	0	1	0	1	0	1	0	1	0	1	0	1	$2V_{DC}$
1	1	1	0	0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	V_{DC}
0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
-1	0	0	1	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	$-V_{DC}$
-2	0	0	1	1	0	0	1	1	0	1	0	1	0	1	0	1	0	1	0	1	$-2V_{DC}$
-3	0	0	1	1	0	0	1	1	0	0	1	1	0	1	0	1	0	1	0	1	$-3V_{DC}$
-4	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	1	0	1	$-4V_{DC}$
-5	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	$-5V_{DC}$

3.3.3 Modulation Technique

The switching technique can be defined as the controlling method of switches in the inverter's circuit. Pulses are needed to drive the switches (IGBTSs). Therefore, Multi-Carrier Pulse Width Modulation are used to trigger the switches.

Modulation of pulses are the process that comparing the Modulating Frequency (F_m) with the Carrier Frequency (F_c). The modulating frequency is the reference frequency (sinusoidal) while the carrier frequency is most-likely to information carrying frequency.

The one reference sinusoidal signal is made constant, the number of triangular carrier signal are varied according the number of DC source applied. When producing Nth number of level (output), N-1 of triangular carrier will be needed to be compared to the only sinusoidal signal. It is must be noted that the magnitude of N is an odd value.

As mentioned above, the modulation is the comparison of modulating frequency and the carrier frequencies. Therefore, the amplitude of carrier(s) will be reduced as the voltage level increases as the carriers will share the range within minimum and maximum amplitude of the modulating frequency. Table 3.9 to Table 3.13 shows the maximum and minimum amplitude of a MLI.

Table 3.9: Minimum & Maximum Amplitude of Carriers (3-Level Inverter)

Triangular Carrier No.	Min. Amplitude	Max. Amplitude
1	0	+1
2	-0.1	0

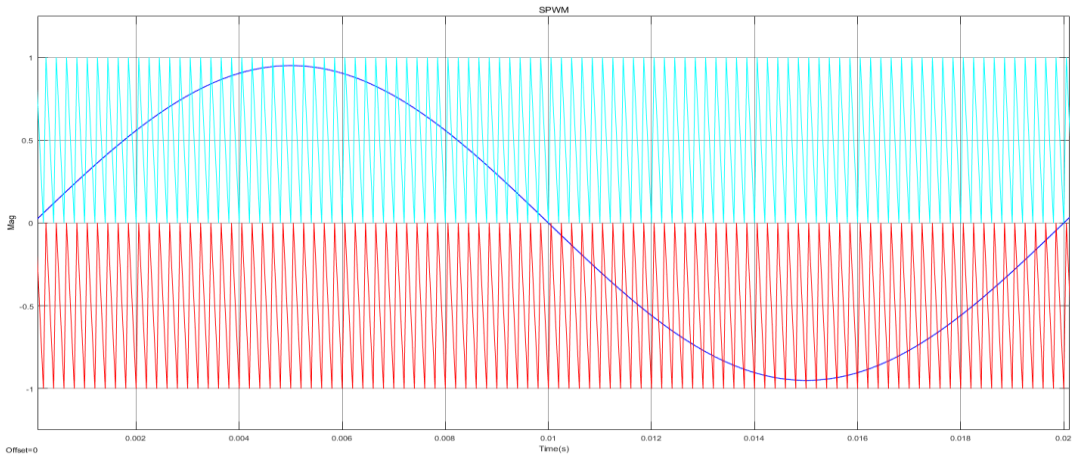


Figure 3.3: Phase disposition (PD) multicarrier PWM for a 3-level Inverter

Table 3.10: Minimum & Maximum Amplitude of Carriers (5-Level Inverter)

Triangular Carrier No.	Min. Amplitude	Max. Amplitude
1	+0.5	+1
2	0	+0.5
3	-0.5	0
4	-1	-0.5

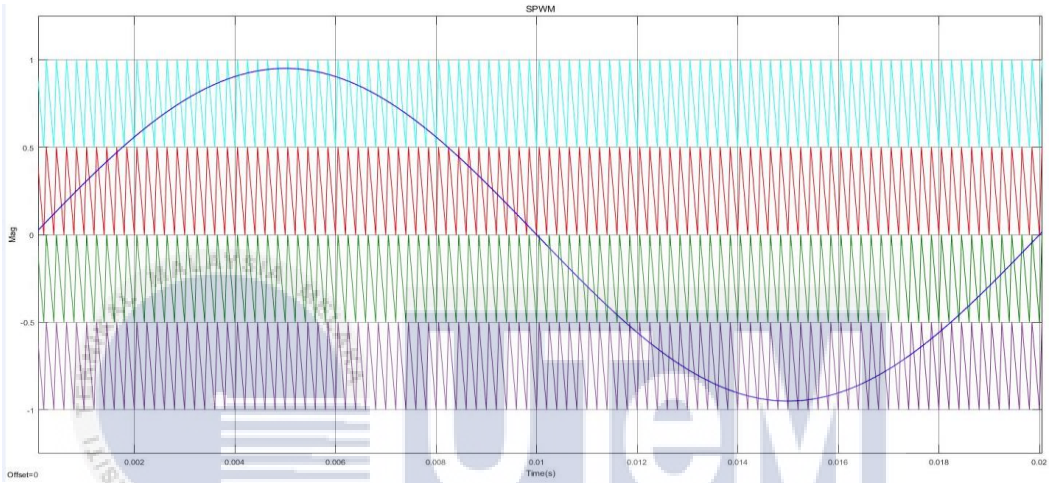


Figure 3.4: Phase disposition (PD) multicarrier PWM for a 5-level Inverter

Table 3.11: Minimum & Maximum Amplitude of Carriers (7-Level Inverter)

Triangular Carrier No.	Min. Amplitude	Max. Amplitude
1	+2/3	+1
2	+1/3	+2/3
3	0	+1/3
4	-1/3	0
5	-2/3	-1/3
6	-1	-2/3

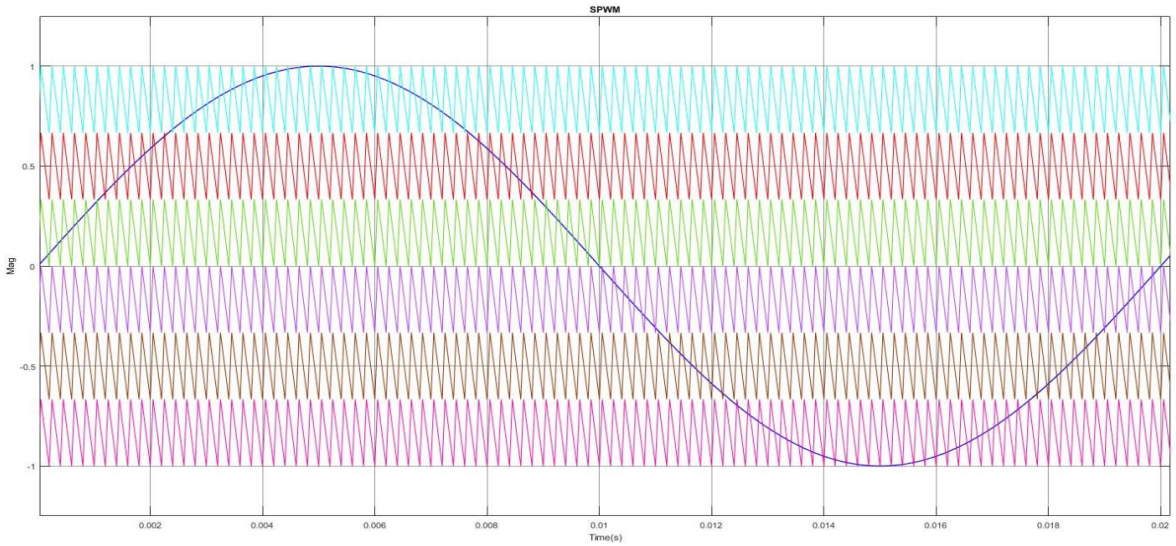


Figure 3.5: Phase disposition (PD) multicarrier PWM for a 7-level Inverter

Table 3.12: Minimum & Maximum Amplitude of Carriers (9-Level Inverter)

Triangular Carrier No.	Min. Amplitude	Max. Amplitude
1	+0.75	+1
2	+0.5	+0.75
3	+0.25	+0.5
4	0	+0.25
5	-0.25	0
6	-0.5	-0.25
7	-0.75	-0.5
8	-1	-0.75

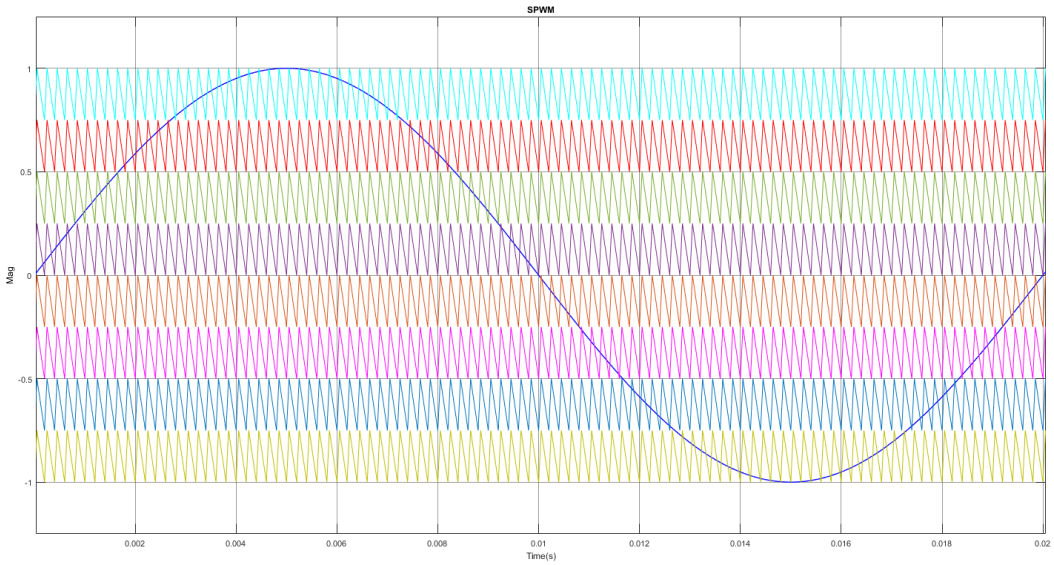


Figure 3.6: Phase disposition (PD) multicarrier PWM for a 9-level Inverter

Table 3.13: Minimum & Maximum Amplitude of Carriers (11-Level Inverter)

Triangular Carrier No.	Min. Amplitude	Max. Amplitude
1	+0.8	+1
2	+0.6	+0.8
3	+0.4	+0.6
4	+0.2	+0.4
5	0	+0.2
6	-0.2	0
7	-0.4	-0.2
8	-0.6	-0.4
9	-0.8	-0.6
10	-1	-0.8

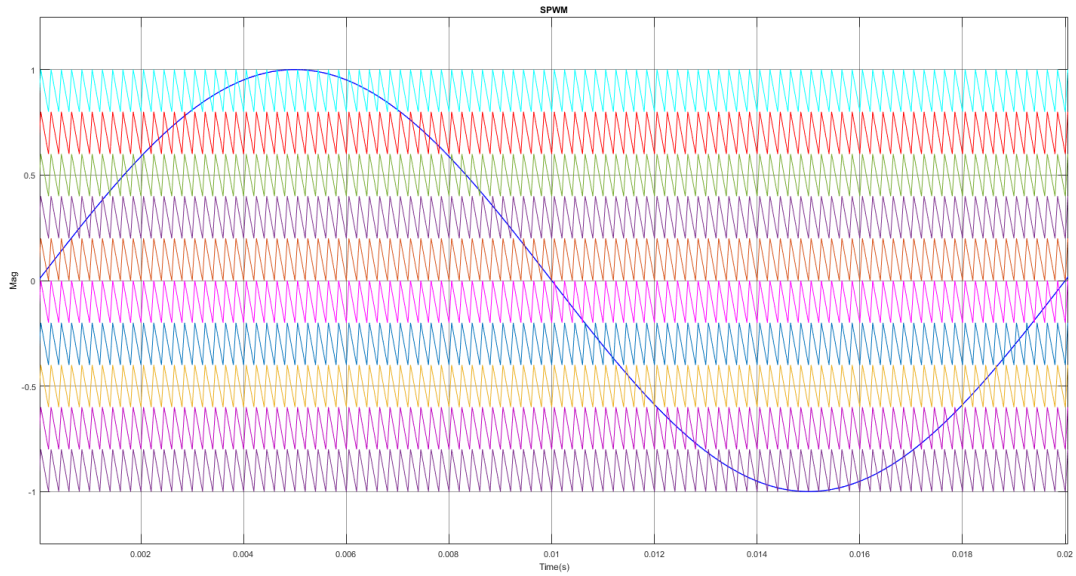


Figure 3.7: Phase disposition (PD) multicarrier PWM for a 11-level Inverter

Increases of level will increase the number of carriers in a comparing circuit where all the carriers will share equally the amplitude of the modulation waveform. The circuit that designed to generate the pulses using Multi-Carrier PWM are as shown in the Figures 3.8 to 3.12

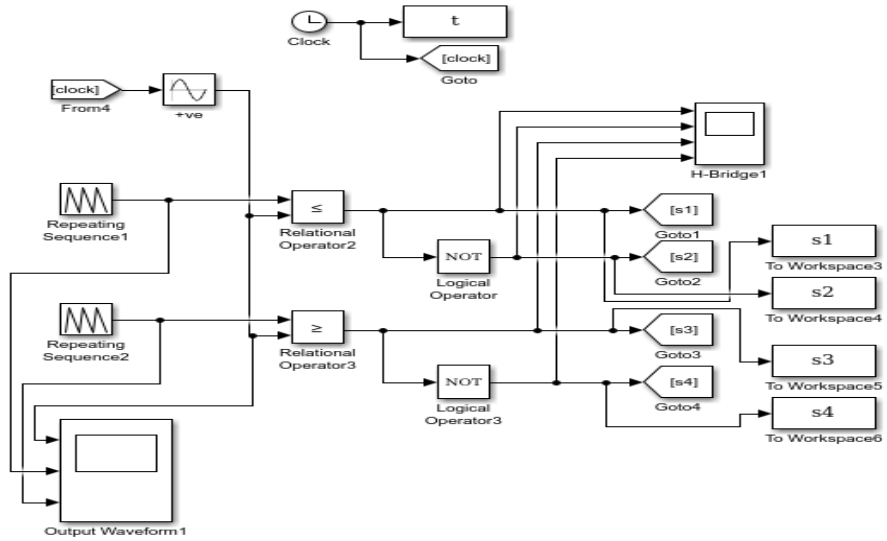


Figure 3.8: PWM Circuit for 3-Level Inverter

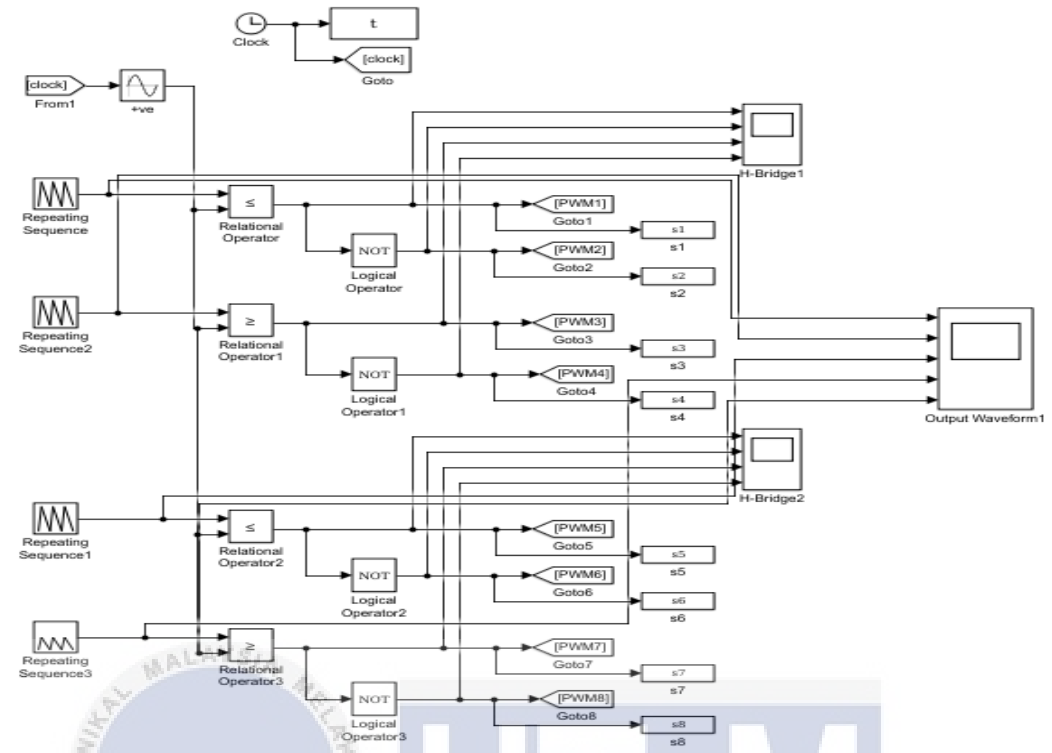


Figure 3.9: PWM Circuit for 5-Level Inverter

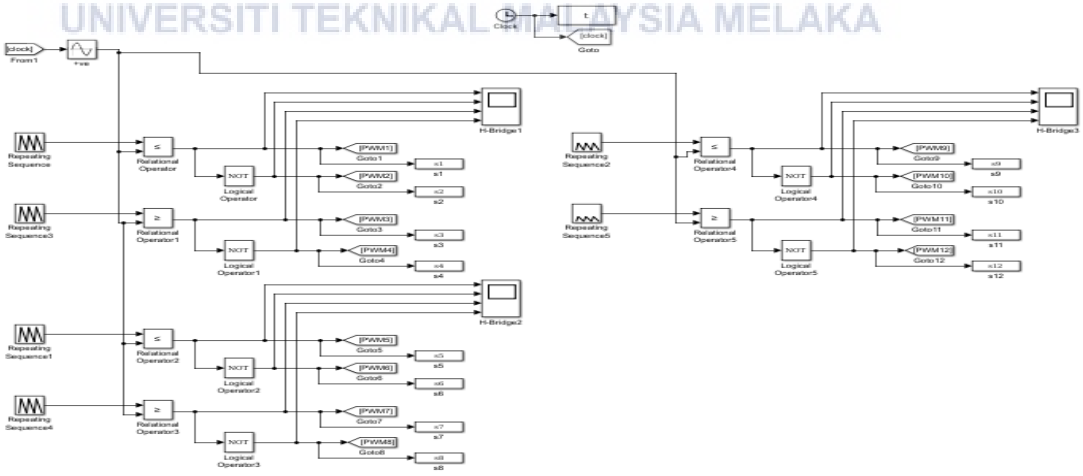


Figure 3.10: PWM Circuit for 7-Level Inverter

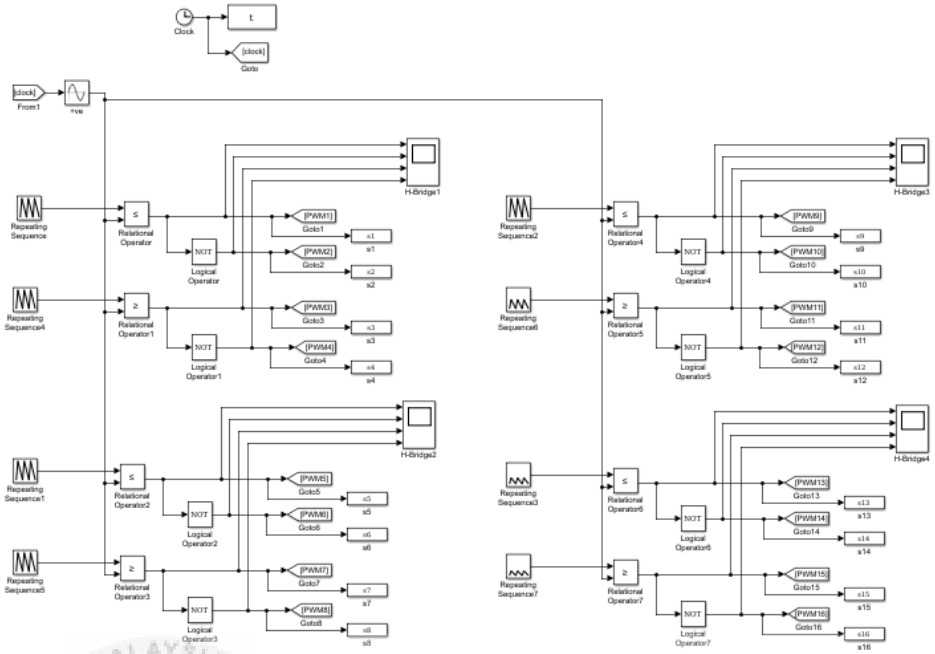


Figure 3.11: PWM Circuit for 9-Level Inverter

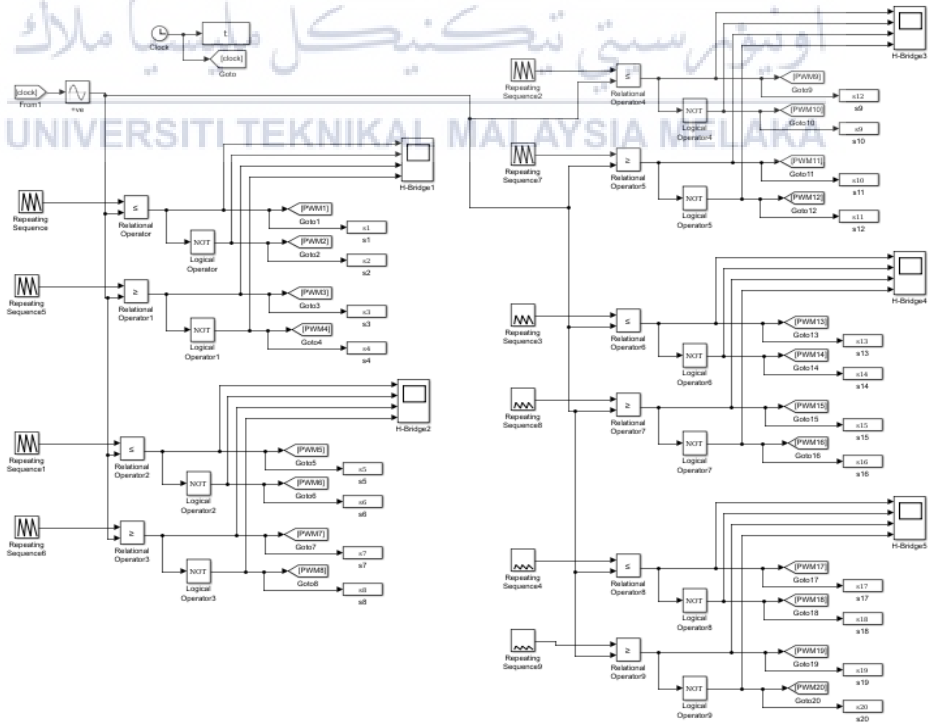


Figure 3.12: PWM Circuit for 11-Level Inverter

Figure 3.8 until Figure 3.12 shows the circuit connection for the modulation of pulses based on Multi-Carrier PWM technique. These simulated waveforms will be discussed further in next chapter.

3.3.4 Design of Multi-Level Inverter

The simulation of single phase CHMLI with several numbers of voltage levels is built using MATLAB Simulink. IGBTS power switches are opted to be used in the model for better performance in low to medium voltage applications. The waveform parameters assigned are stated as in the Table 3.14.

Table 3.14: Parameters for Single Phase CHMLI

Input Voltage, Vdc	Modulating Frequency, f_m	Carrier Frequency, f_c
20V	50Hz	5kHz

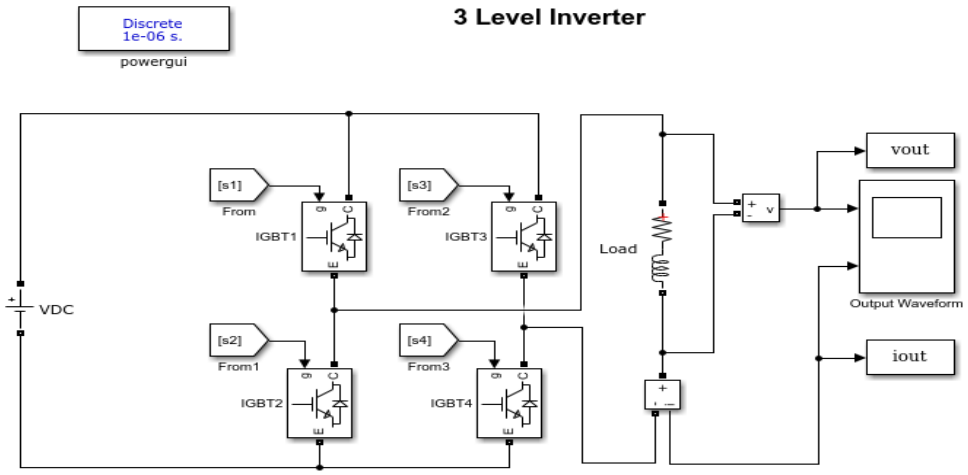


Figure 3.13: 3-Levels Inverter

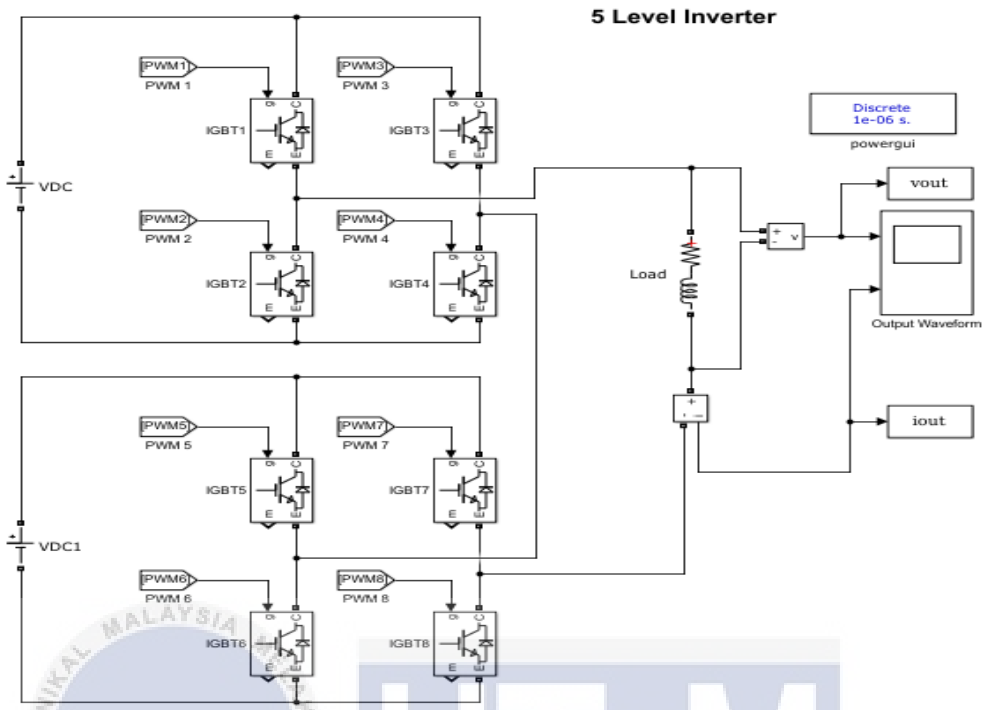


Figure 3.14: 5-Levels Inverter

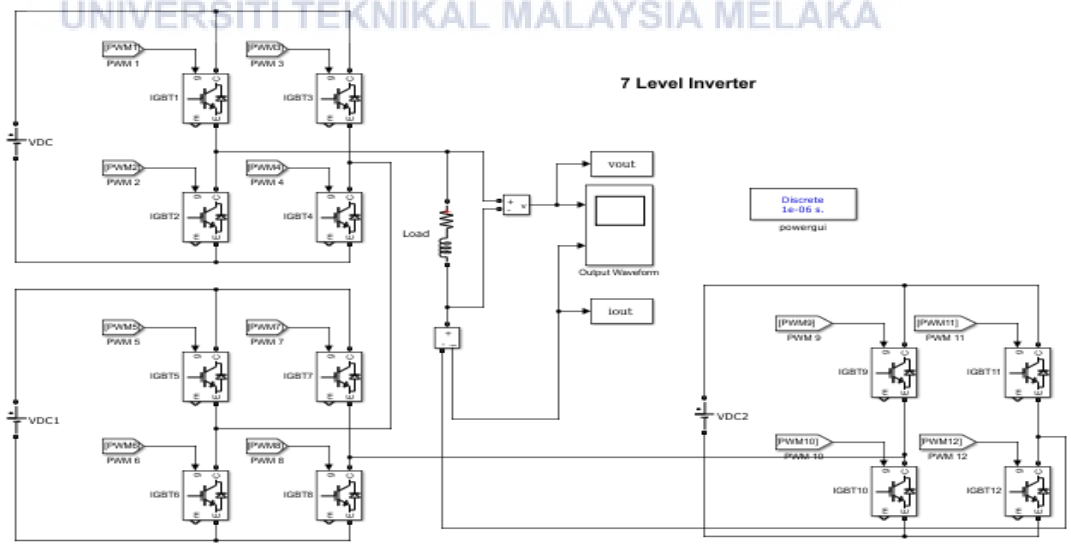


Figure 3.15: 7-Levels Inverter

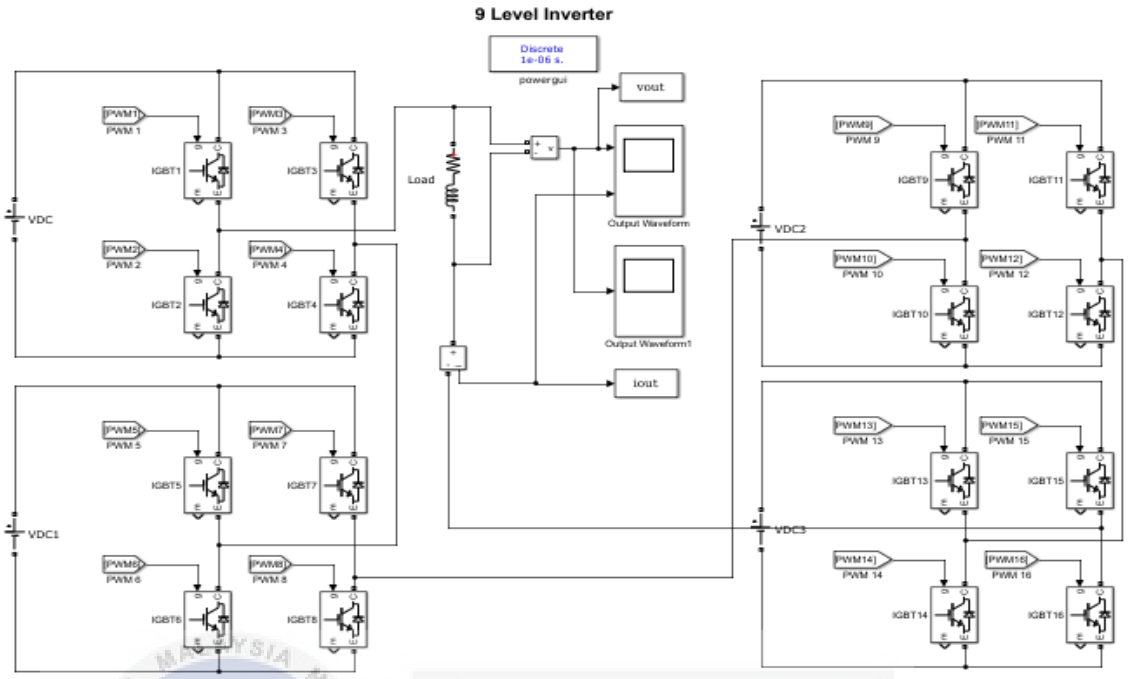


Figure 3.16: 9-Levels Inverter

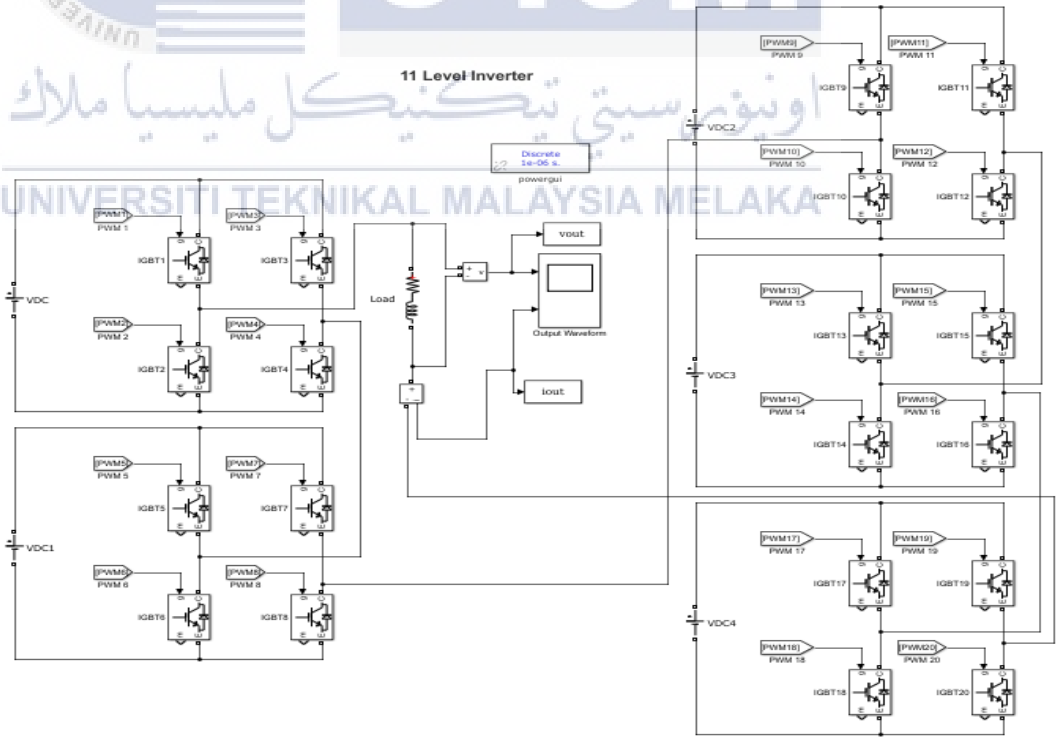


Figure 3.17: 11-Levels Inverter

As shown from Figure 3.13 to Figure 3.17, the number of Cascaded H-Bridge is increased as the voltage levels of the inverter increases.

3.4 Project Methodology on FYP 2

This section is going to develop the hardware of Multi-Level Inverter. The hardware that are implemented in this project is the Single Phase Cascaded H-Bridges 5-Levels Inverter. The switches are controlled by gate drivers and FPGA development board. This section will discuss on the procedure of enhancing these parts which includes the components and designs of the project.

3.4.1 Preparation of Components

The construction of the circuit is based on the schematic diagram designed in previous simulation during FYP 1. The components that are used in the hardware design are listed as shown in Table 3.15.

Table 3.15: List of components

No	Components	Quantity
1	IGBT (GP35B60PD)	8
2	Gate Drive Optocoupler (HCPL-3120 000E)	8
3	FPGA (Altera Cyclone IV DE0-nano)	1
4	1kΩ Resistor	16
5	10µF Capacitor (25V)	16
6	Boost Converter (IQ0515SA)	8

IGBT

Eight IGBTs are used for the development of this project. The controlling of the states of the switches are giving pulses through the Gate (G) of the IGBTs. The IGBT is as shown in Figure 3.18

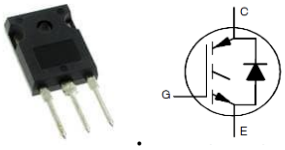


Figure 3.18: IGBT

DC-DC Converter (Boost)

Figure 3.19 shows the DC-DC converter (IQ0515SA) that is used to step up input voltage from 5V to 15V for the operation of gate drive optocoupler in which the gate drive optocoupler require 15V to be functioning in the gate drive circuit. As to coupling with optocoupler, twelve units of DC-DC Converter are prepared.

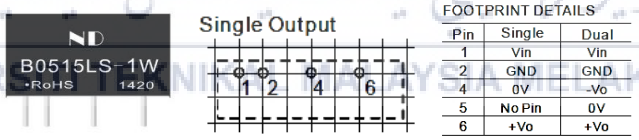


Figure 3.19: DC-DC Converter (Boost) IQ0515SA

Optocoupler

This gate drive optocoupler as shown in Figure 3.20 is used to provide the required amount of gate voltages for driving the IGBTs in the circuit. It also serves the protection purpose for FPGA from over voltage. The amount of optocoupler needed for the hardware development is eight units.

Figure 3.20: Optocoupler HCPL3120

Capacitor

A capacitor is a passive two-terminal electrical component that stores electrical energy in an electric field. A capacitor is stated with SI unit of Farad which is the measure of the capacitance. A capacitor is specifically designed to provide and enhance this effect for a variety of practical applications by consideration of size, shape, and positioning of closely spaced conductors, and the intervening dielectric material. A capacitor can be used as a filtering device to filter the ripple occurs.

Figure 3.21: Capacitor

FPGA Board

FPGA is selected over conventional microcontrollers because FPGA is more power efficient and flexible in terms of performance that provides a better output quality and it can be performed very well in real time applications. The FPGA (Altera Cyclone IV DE0-nano Board) is shown in Figure 3.22. The programming of FPGA coding is written and edited by using Quartus II.

Figure 3.22: FPGA Cyclone IV DEO-nano Board

3.4.2 Hardware Circuit Connection

The hardware of this project is separated into 3 sections which include the Gate Driver, IGBT H-Bridge and FPGA section. Each of the Section will be discuss further below.

FPGA

This is the section where programming codes is needed to be processed. Programming code are tested and transferred to the FPGA development board to provide or generate pulses into the Gate Driver to control the IGBT performances. The coding can be referred in Appendix.

Gate Driver

The Gate Driver section perform task to ensure the pulses entering the IGBT without faulty. These including the secure of the circuit that to prevent more than 1 switches are on at the same time. The connection for each gate driver is as shown in Figure 3.23. The Figure 3.24 shows schematic diagram that designed using Orcad Pspice Layout Plus.

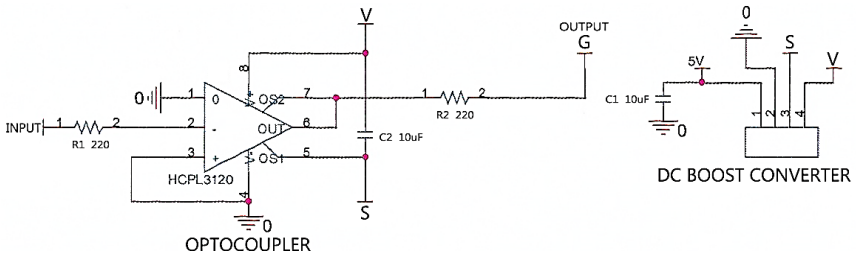


Figure 3.23: Connection of Gate Driver

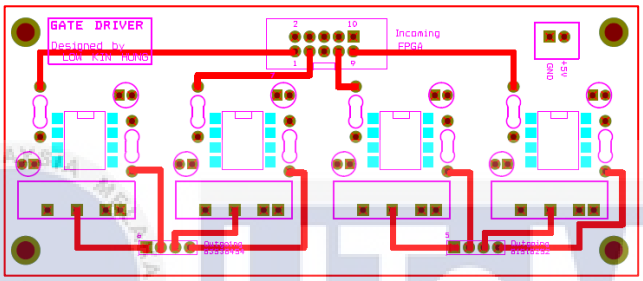


Figure 3.24: Schematic Diagram for Gate Driver (Bottom Connection)

IGBT H-Bridge

This section is the cascaded h-bridge which includes only the IGBT switches that attached and screwed on the heat sink that to prevent over heating of the switches. The figure below shows the completed hardware.

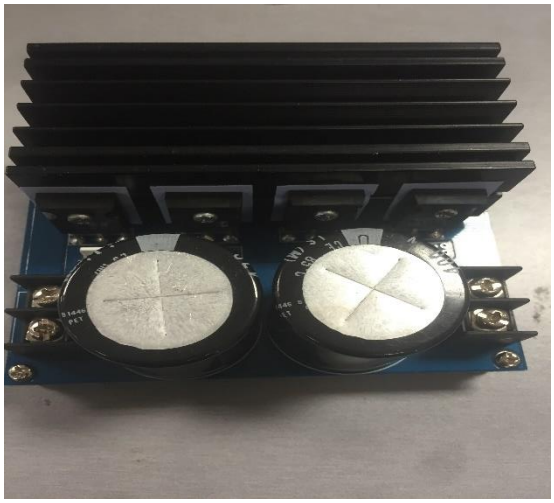


Figure 3.25: IGBT Cascaded H-Bridge

3.4.3 Hardware Testing

The testing of hardware of this project included the 3 sections: The Gate Driver, IGBT H-Bridge and FPGA.

FPGA

Only Oscilloscope is needed for the testing of FPGA board. This step is needed to test on the output of FPGA. In this project, FPGA is served as a pulses generator that controlling all the switches. VHDL programming code should be checked and compile as to ensure the correct output of FPGA, the output is connected to the Oscilloscope to observed the amplitude and timing of each pulses. The Figure 3.26 shows the testing of 2 pulses from the FPGA.

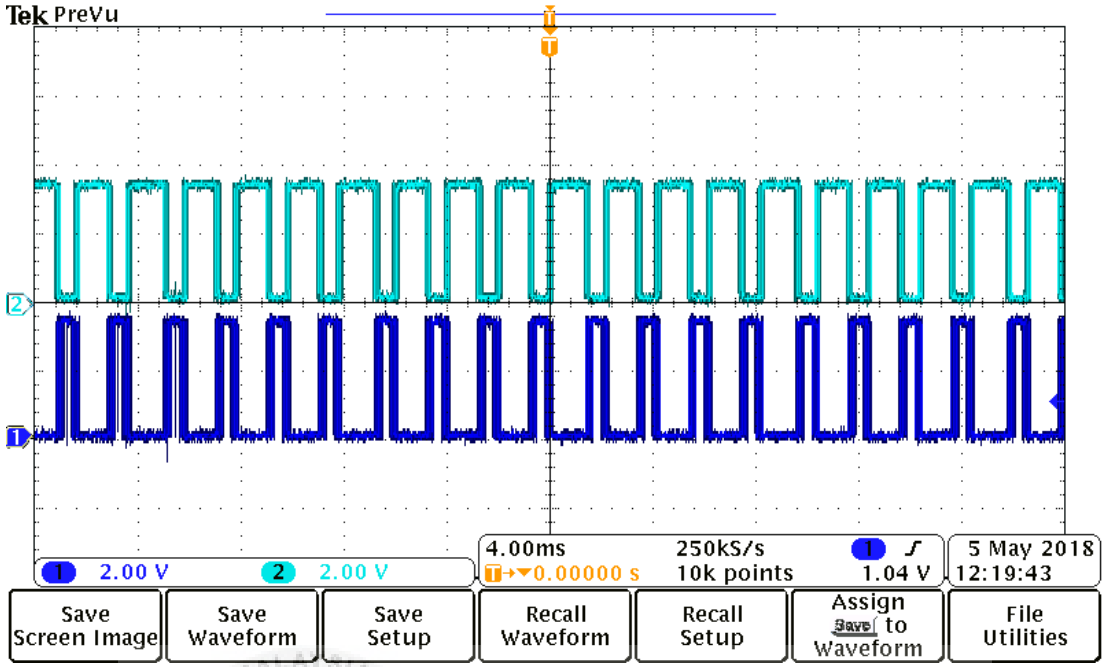


Figure 3.26: FPGA Output Pulses

Gate Driver

The instruments that are required to test the Gate Driver are the Function Generator, Oscilloscope and DC Power Supply. The Function Generator is used to generate pulses to be send into the gate driver. The DC power Supply is used to supply power of 5 Volts to the gate driver circuit. While, the Oscilloscope is used to observed the output of the gate driver. The output is expected to be the same as the pulses from Function Generator but different in just amplitude where the output is expected to has a range of amplitude within 12 to 15 Volts.

IGBT H-Bridge

The testing of each Cascaded H-Bridge required the full connection from FPGA Board to the Gate Driver until the IGBT H-Bridge. The output at H-Bridge is observed by using Oscilloscope. The output of each bridges should have an output similar to a 3-level inverter waveform.

3.4.4 Final Hardware Testing

After the testing of hardware, the end hardware that combined all the 2-cascaded h-bridges and gate drivers are going for the last testing. There are 2 variable DC voltages from the power supplies that connected to the input port of each of the H-Bridges. Besides, all the gate driver circuit is connected parallel to a constant 5V/3A to enable the amplification and isolation of pulses that send from FPGA. The FPGA is loaded with programming coding and connected to the gate drivers. Lastly, Oscilloscope is connected at the output terminal of the prototype.

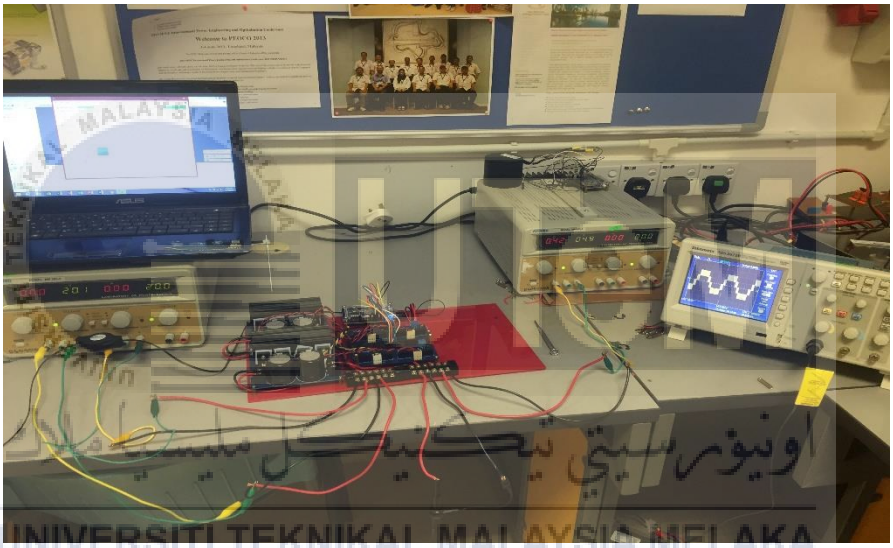


Figure 3.27: Connection for Final Hardware Testing

THD Content in Output Voltage

The output of final hardware is observed with fluke meter and the waveform data is saved and analyzed. By using the data of fluke view obtained from the hardware oscilloscope, THD is analyzed.

3.5 Conclusion

This chapter will discuss about the methodology that is practiced in order to complete this project. The duration taken for this project is one semesters which is around 30 weeks. The overall procedure undergone throughout the whole project from the beginning in which study previous research, designing circuit, simulating, constructing hardware and analyzing results until the writing final report are all discussed in this section. The presence of this chapter is to ensure the project is simulated efficiently.

CHAPTER 4

RESULTS

4.1 Introduction

This chapter will discuss about the results for this project. This will include the simulation of different amplitude modulation, m_a and level(s) of Multi-Level Inverter such that up to 11-Level. Every output of the simulation is observed and the Total Harmonic Content (THD) is studied. Then, the THD for each simulation is compared and analyzed. Results for the design and development of single phase 5-levels inverter are compared with the simulation results.

4.2 Simulation Results

The simulations for this project includes the 3-levels, 5-levels, 7-levels, 9-levels and 11-levels inverter using 20V input voltage value. These results of different levels of MLI and amplitude modulation, m_a will be discussed in terms of Total Harmonic Distortion (THD).

4.2.1 Pulse Width Modulation

Based on the theory from the researches, the number of carrier(s) is depending on the H-Bridges and construction of the PWM generator. Level Shifted Multi-Carrier PWM is used in this project. PD technique to implement the SPWM switching schemes.

The generation of pulses can be defined as the comparison of modulating and carrier frequencies which is in term of greater than or less than. The pulses generated for different level of MLI are shown in figures below. The PWM parameters assigned are stated as in the Table 4.1.

Table 4.1: PWM parameter

Modulating Frequency, f_m	Carrier Frequency, f_c	Amplitude Modulation Ratio, ma
50Hz	5kHz	1

4.2.1.1 Pulses for 3 Level Inverter

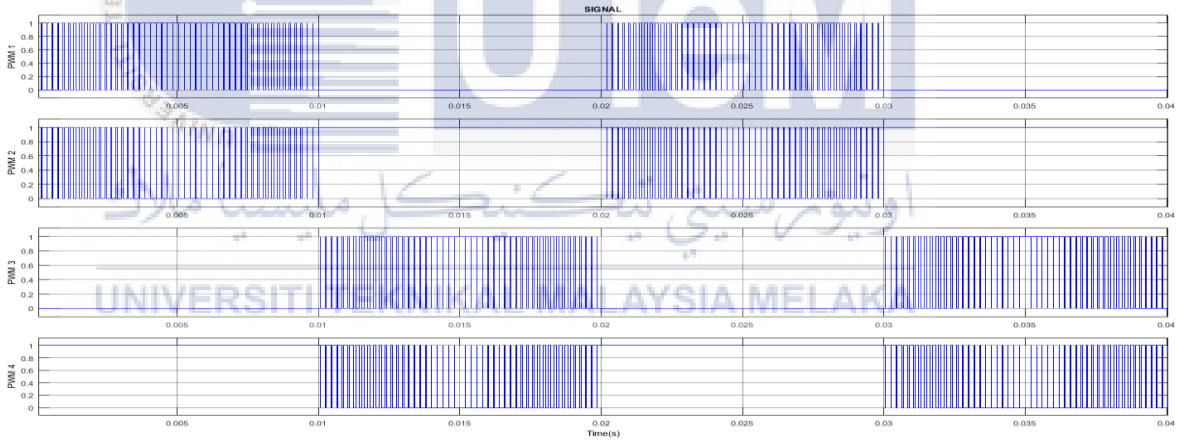


Figure 4.1: Pulses for 3 Level Inverter (1 H-Bridge)

From the comparison between the reference wave and the carrier wave will produce the PWM switching pulse. The pulse is also known as PWM compensator signal. For two-triangle wave will produce the four PWM switching signal for SPWM switching technique. Figure 4.1 show the PWM compensator signal for SPWM. The PWM signal is used to turn ON and OFF the IGBT power switch.

4.2.1.2 Pulses for 5 Level Inverter

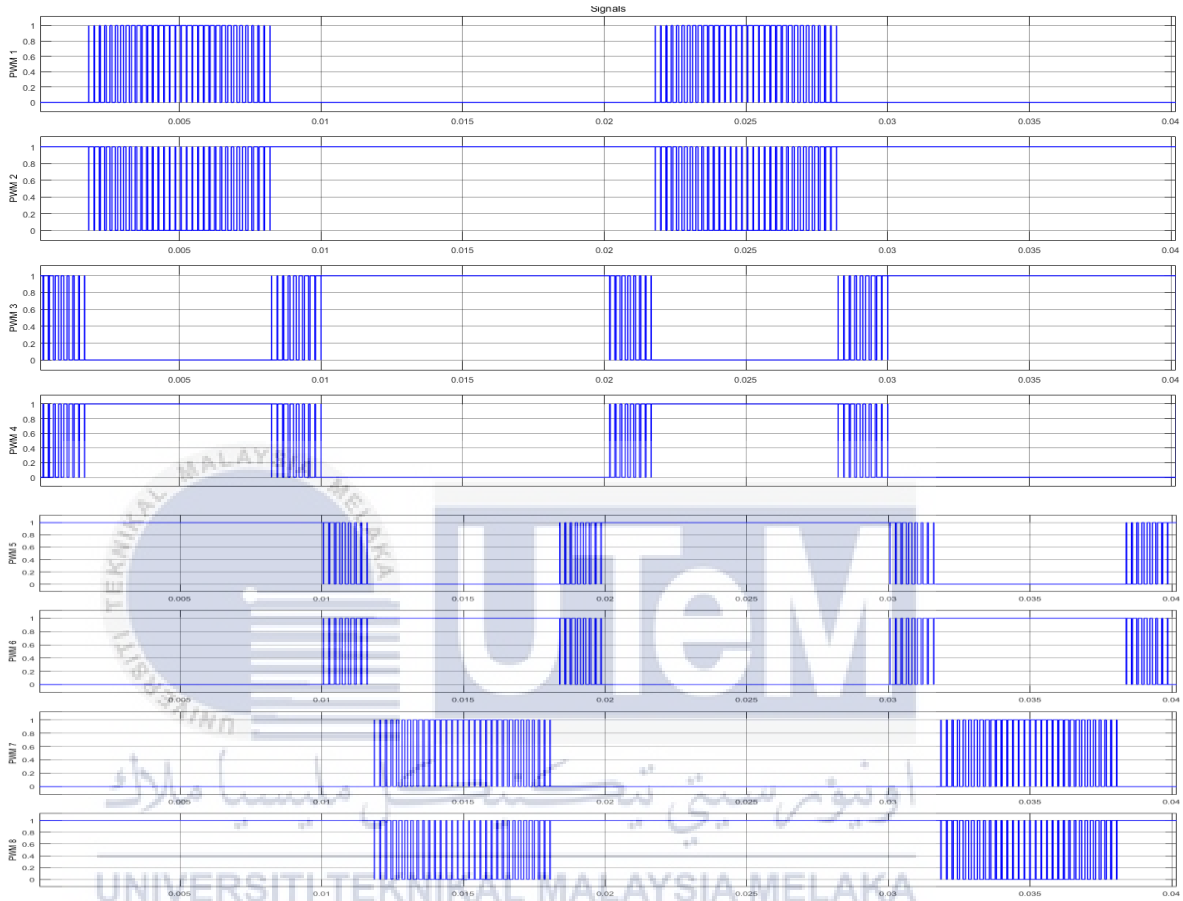


Figure 4.2: Pulses for 5 Level Inverter (2 H-Bridge)

For four-triangle wave will produce the eight PWM switching signal for SPWM switching technique. Figure 4.2 show the PWM compensator signal for SPWM. The PWM signal is used to turn ON and OFF the IGBT power switch.

4.2.1.1 Pulses for 7 Level Inverter

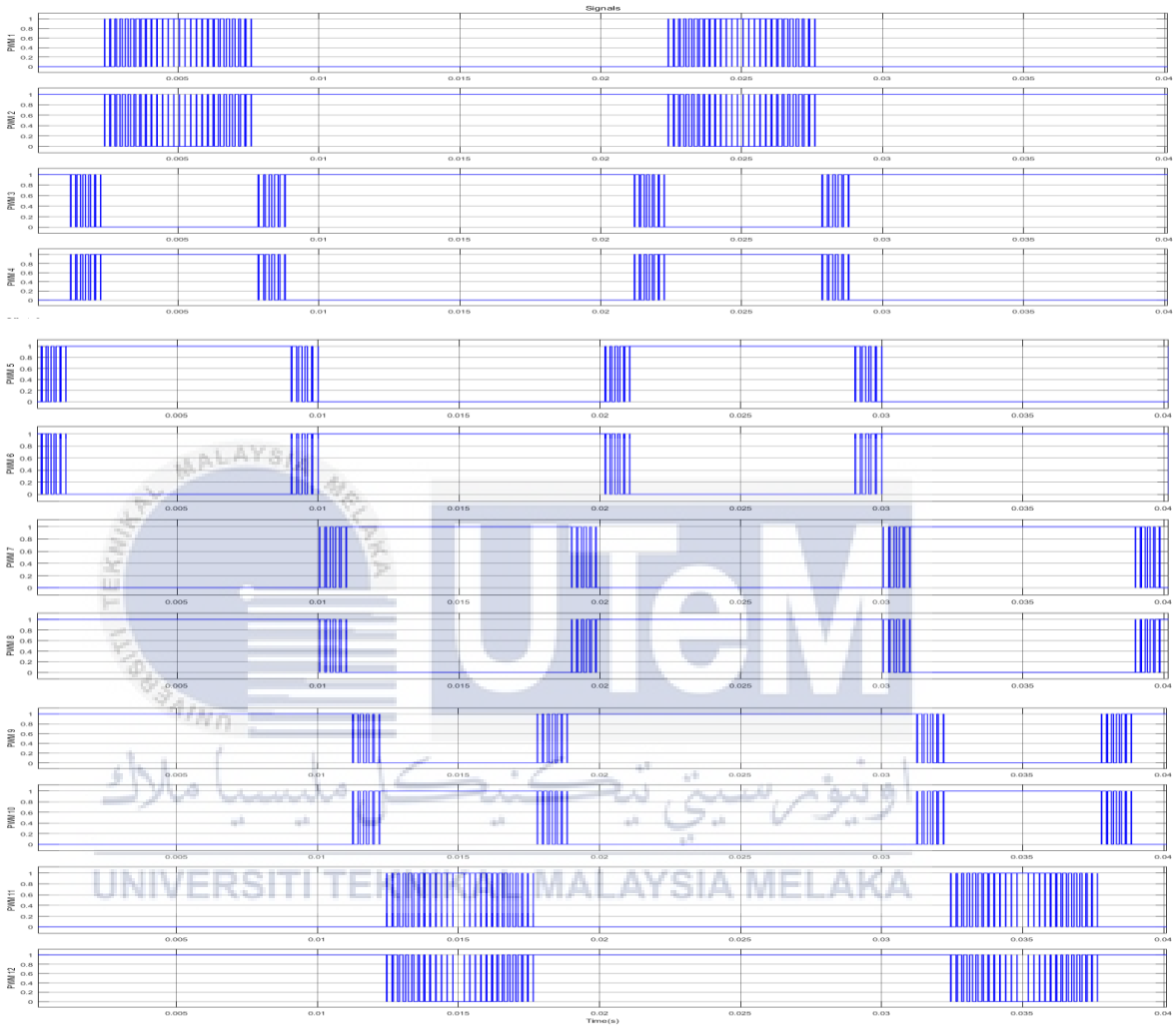


Figure 4.3: Pulses for 7 Level Inverter (3 H-Bridge)

For six-triangle wave will produce the twelve PWM switching signal for SPWM switching technique. Figure 4.3 show the PWM compensator signal for SPWM. The PWM signal is used to turn ON and OFF the IGBT power switch.

4.2.1.1 Pulses for 9 Level Inverter

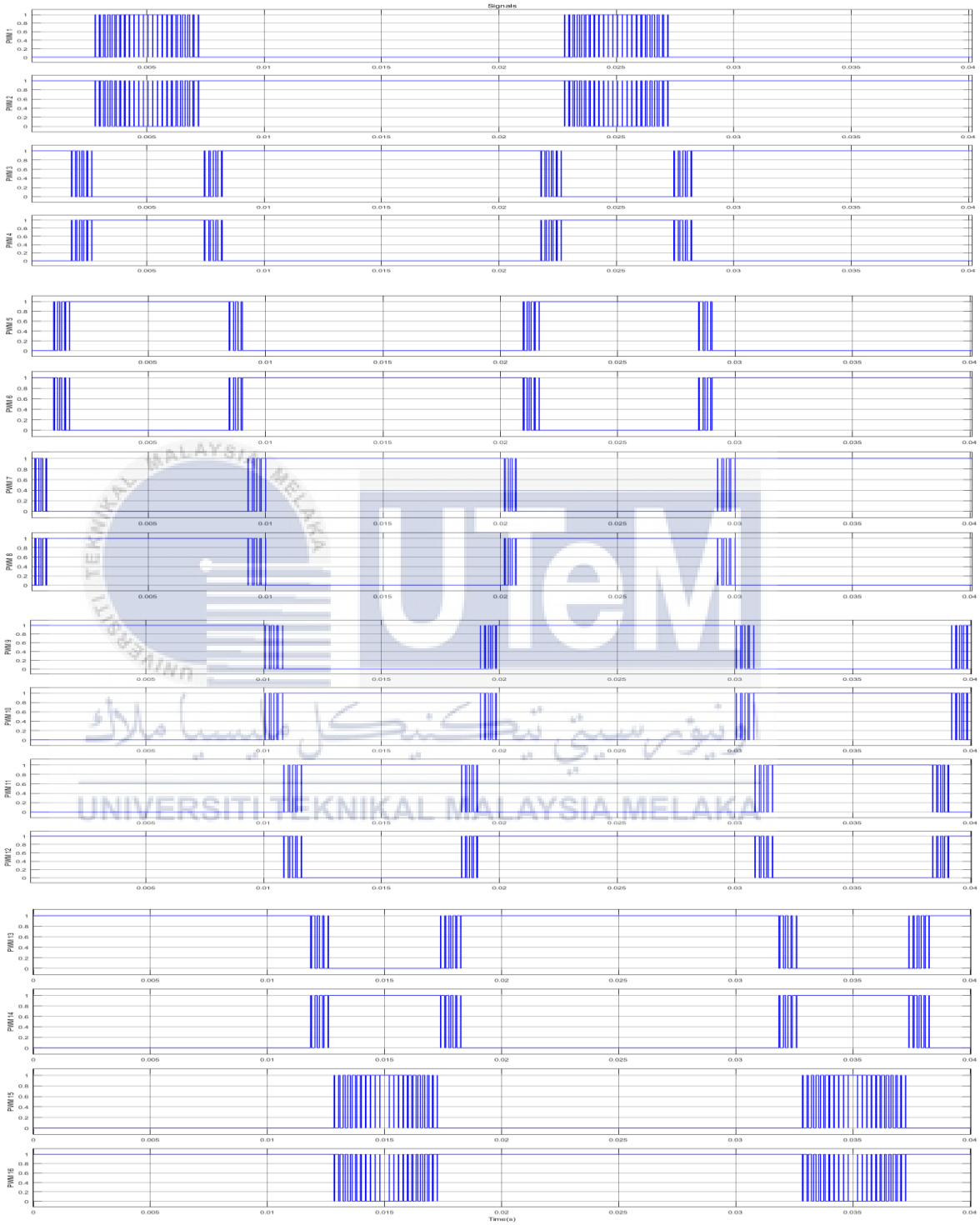
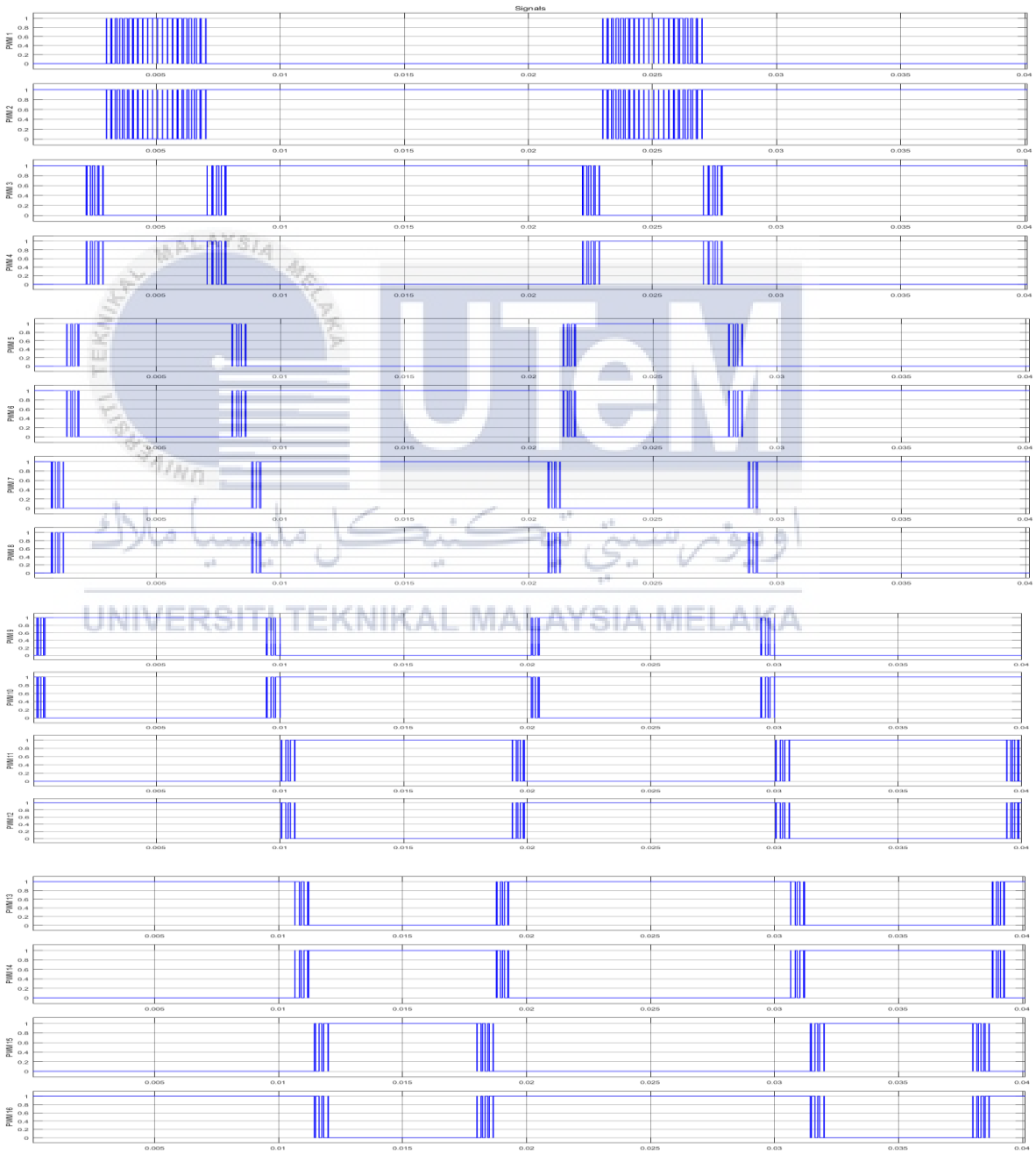


Figure 4.4: Pulses for 9 Level Inverter (4 H-Bridge)

For eight-triangle wave will produce the sixteen PWM switching signal for SPWM switching technique. Figure 4.4 show the PWM compensator signal for SPWM. The PWM signal is used to turn ON and OFF the IGBT power switch.

4.2.1.1 Pulses for 11 Level Inverter



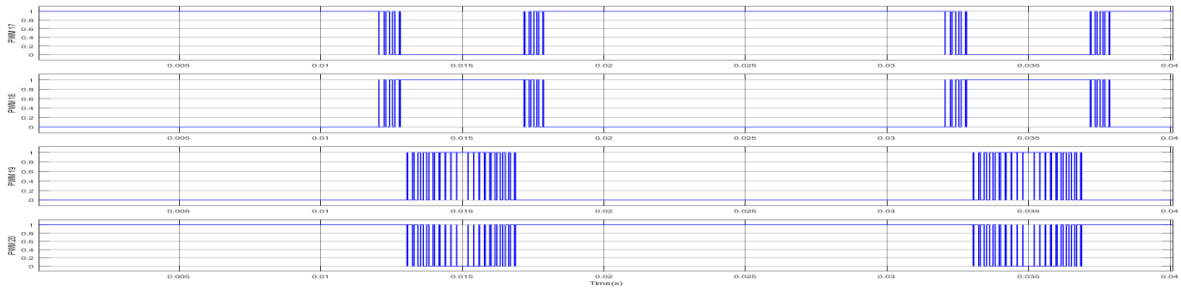


Figure 4.5: Pulses for 11 Level Inverter (5 H-Bridge)

For ten-triangle wave will produce the eight PWM switching signal for SPWM switching technique. Figure 4.5 show the PWM compensator signal for SPWM. The PWM signal is used to turn ON and OFF the IGBT power switch.

Figure 4.1 to Figure 4.5 shows different number of pulses generated for each level of the MLI.

4.2.2 Simulation of different Level of MLI

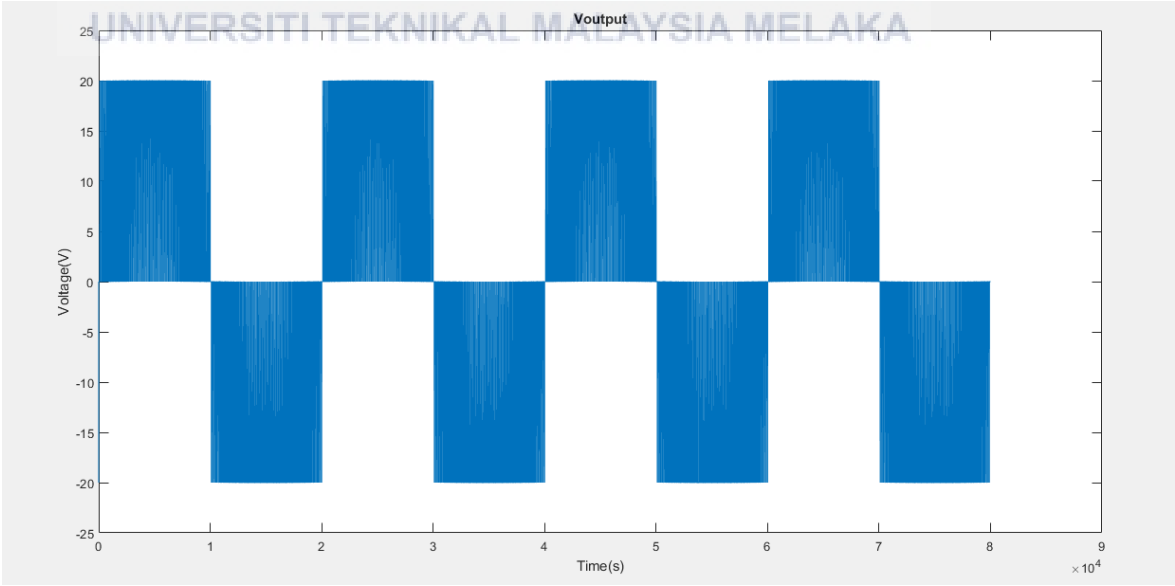
The MLI operates with the PWM switching pulse to turn ON the power switching device IGBT. The PWM switching pulse was generated by the comparison between two waves which are the sinusoidal wave reference and the triangle wave carrier. The number of carrier wave will affect the number of output voltage level. The Cascaded H-Bridge Multilevel Inverter (CHB-MLI) was supplied with 20 V DC voltage and the inverter was connected with RL loads. The value of R load is 1200 Ω, L load is 0.8H. The frequency of the triangle wave carrier that used in this simulation is 5 kHz and the fundamental frequency for the reference sinusoidal is 50 Hz. Table 4.2 show the parameter that was fixed for this simulation.

Table 4.2: Fixed Parameter for MLI Level Simulation

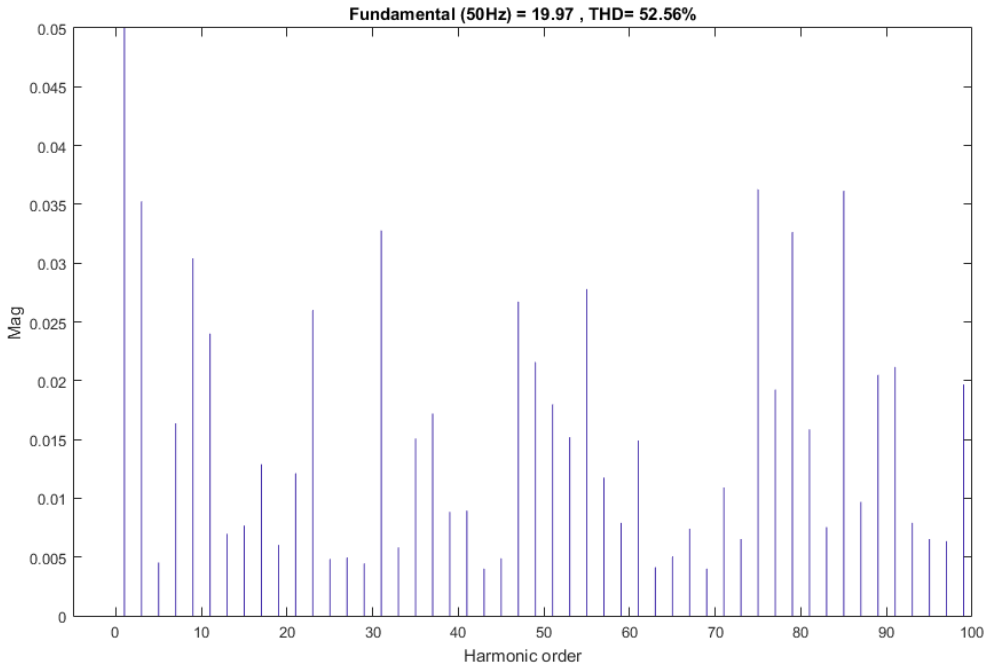
Parameter	**Value**
Input Voltage, Vdc	20V
Carrier Wave Frequency	5 kHz
Reference wave Frequency	50 Hz
R load	1200Ω
L load	0.8H
Frequency Modulation Ratio, m_f	100
Amplitude Modulation Ratio, m_a	1

4.2.2.1 Simulation of 3-Level Inverter

The cascaded H-Bridge Multilevel (CHB-MLI) was applied with the two-triangle wave carrier. The Multilevel inverter was connected to RL load. The result simulation was show in figure 4.6



(a)

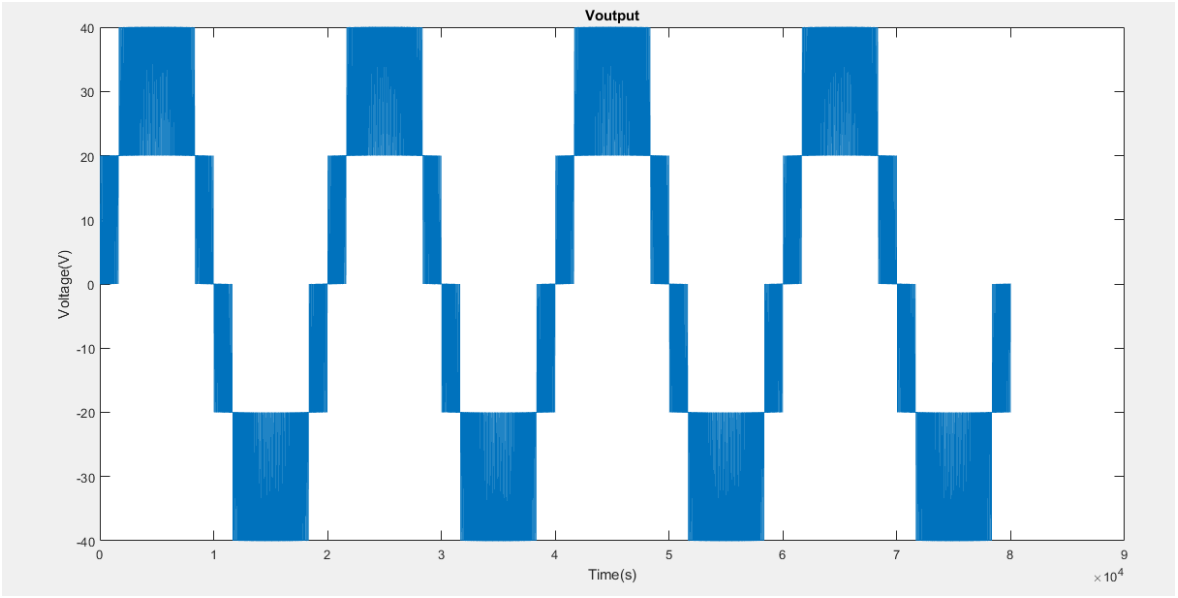


(b)

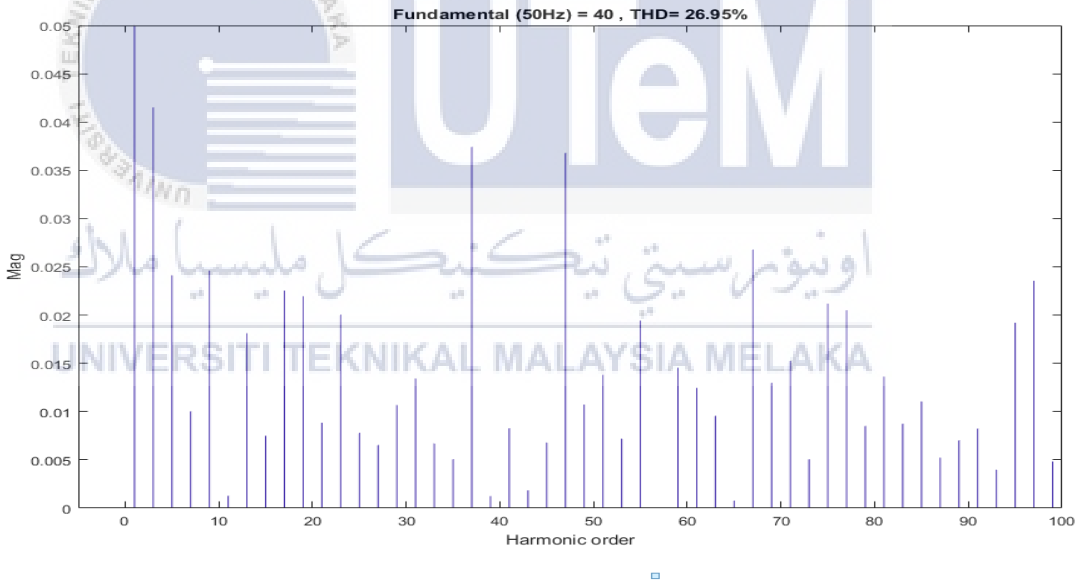
Figure 4.6: (a) Output Voltage for 3 Level Inverter, (b) THD Content in 3 Level Inverter.

4.2.2.2 Simulation of 5-Level Inverter

The cascaded H-Bridge Multilevel (CHB-MLI) was applied with the four-triangle wave carrier. The Multilevel inverter was connected to RL load. The result simulation was show in figure 4.7



(a)

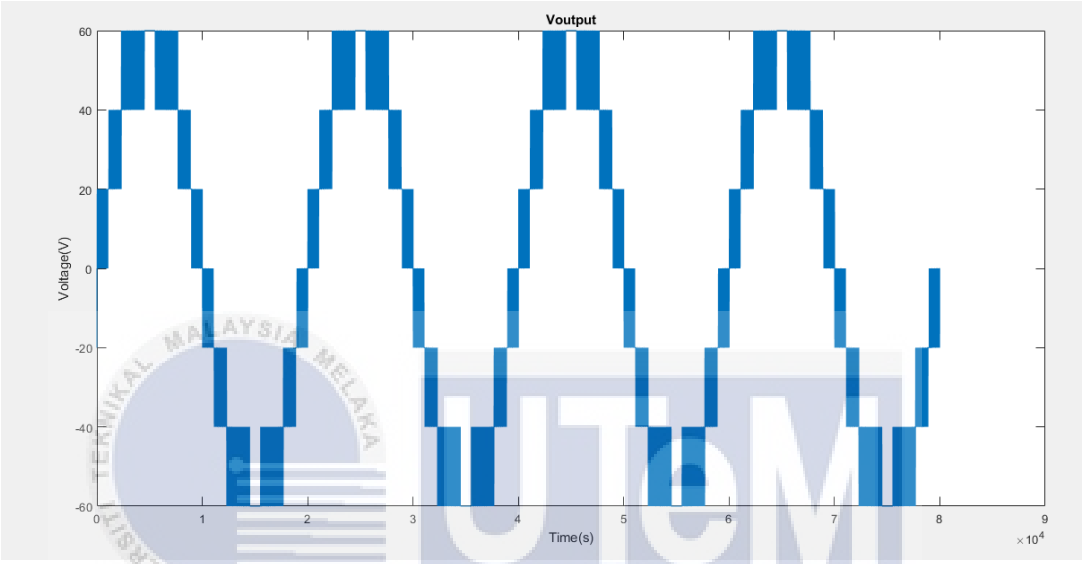


(b)

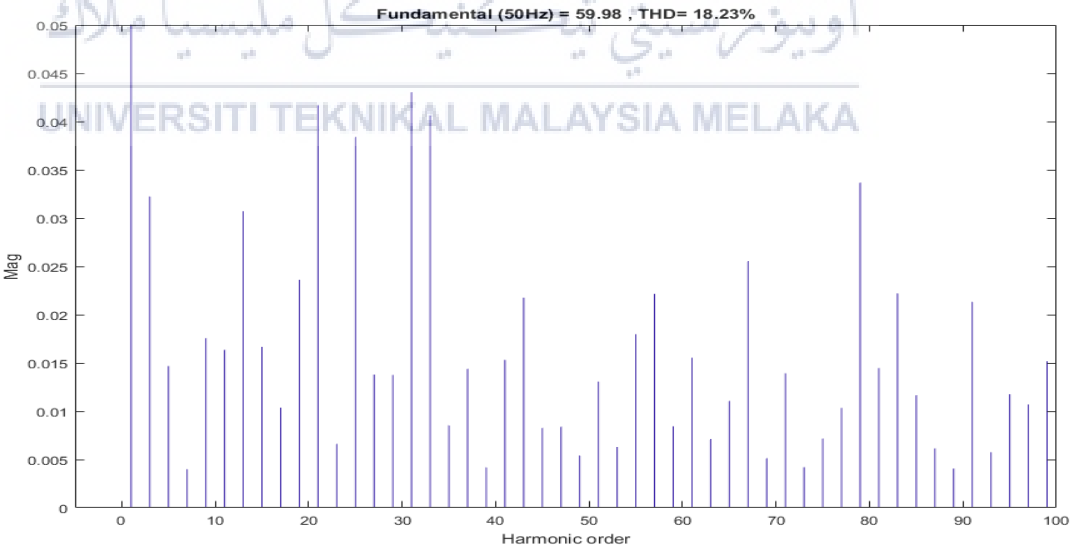
Figure 4.7: (a) Output Voltage for 5 Level Inverter, (b) THD Content in 5 Level Inverter.

4.2.2.3 Simulation of 7-Level Inverter

The cascaded H-Bridge Multilevel (CHB-MLI) was applied with the six-triangle wave carrier. The Multilevel inverter was connected to RL load. The result simulation was show in figure 4.8.



(a)

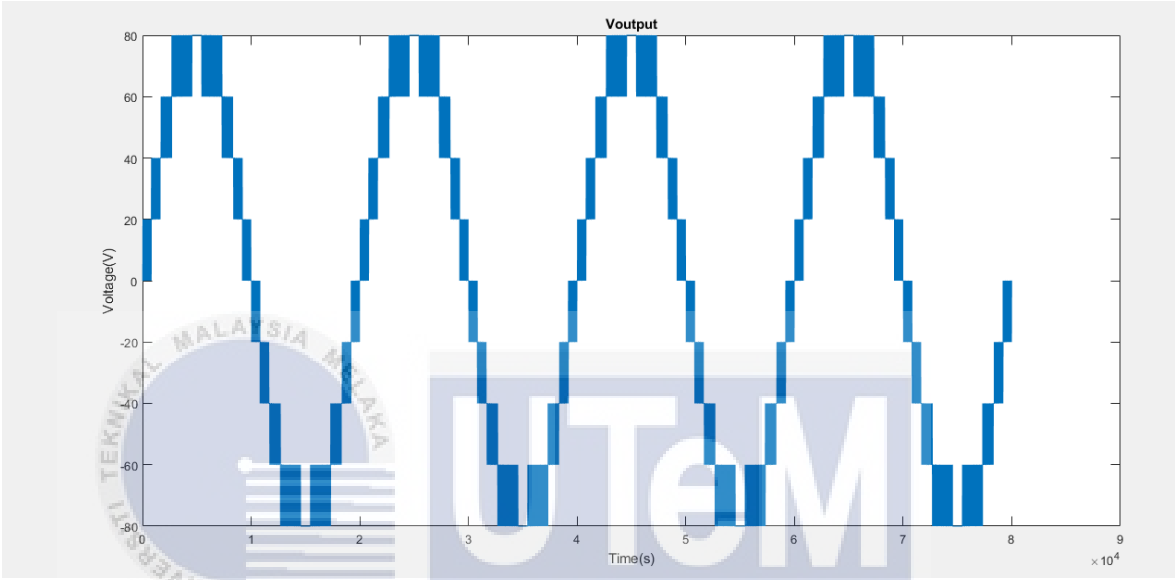


(b)

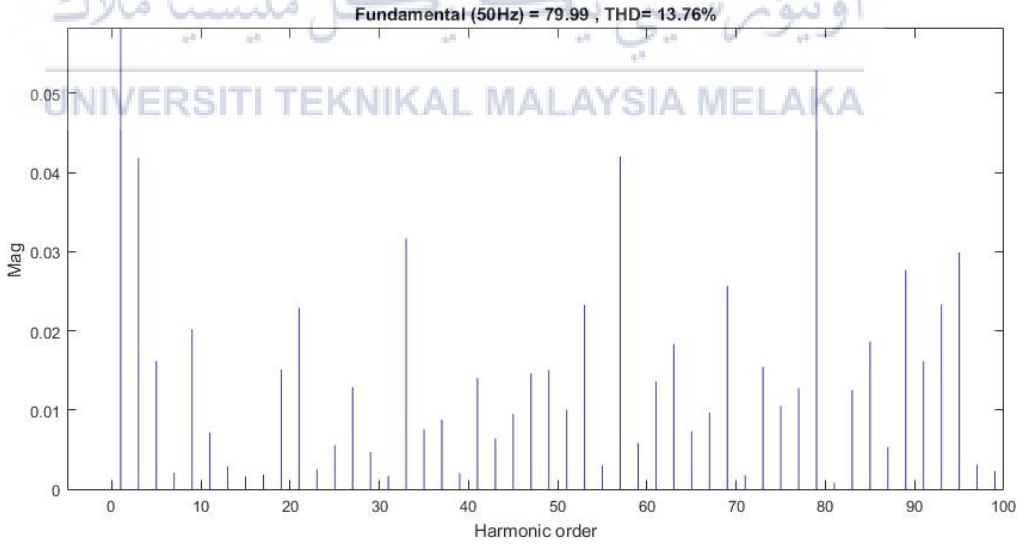
Figure 4.8: (a) Output Voltage for 7 Level Inverter, (b) THD Content in 7 Level Inverter.

4.2.2.4 Simulation of 9-Level Inverter

The cascaded H-Bridge Multilevel (CHB-MLI) was applied with the eight-triangle wave carrier. The Multilevel inverter was connected to RL load. The result simulation was show in figure 4.9.



(a)

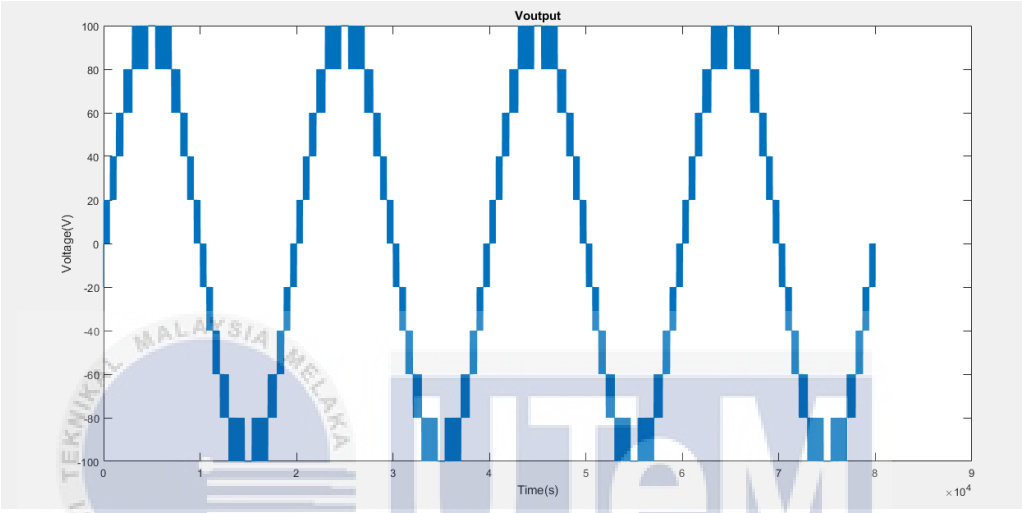


(b)

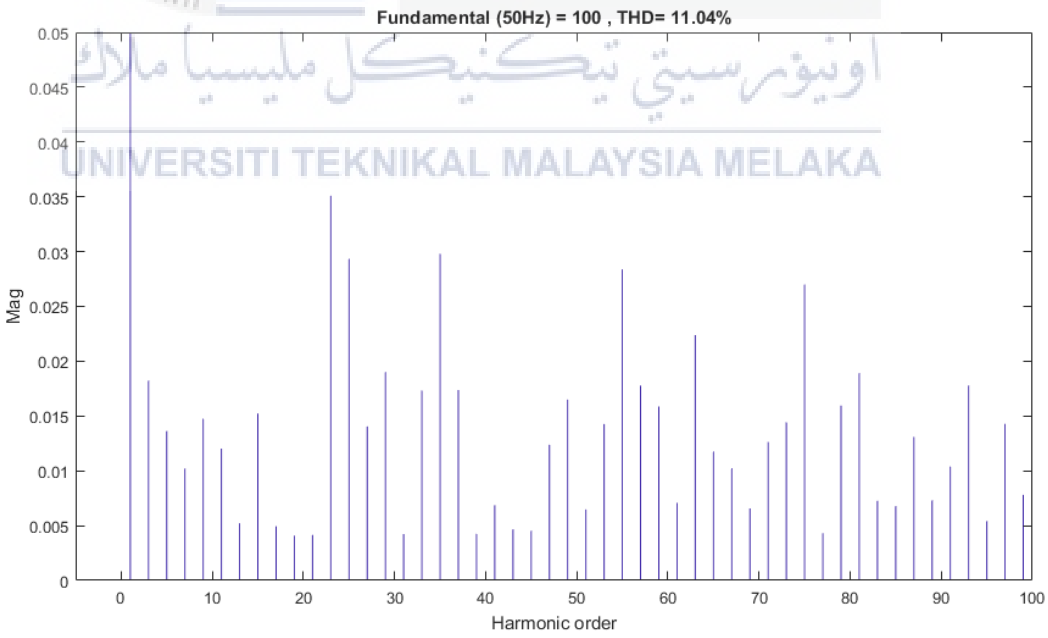
Figure 4.9: (a) Output Voltage for 9 Level Inverter, (b) THD Content in 9 Level Inverter.

4.2.2.5 Simulation of 11-Level Inverter

The cascaded H-Bridge Multilevel (CHB-MLI) was applied with the ten-triangle wave carrier. The Multilevel inverter was connected to RL load. The result simulation was show in figure 4.10



(a)



(b)

Figure 4.10: (a) Output Voltage for 11 Level Inverter, (b) THD Content in 11 Level Inverter.

4.2.2.6 Summary of the different MLI level

The Cascaded H-Bridge Multilevel Inverter was simulated with multiple number of carrier wave and the inverter was connected with RL load. This section will present summary of overall result for multicarrier simulation. The result will be present in the percentage of total harmonic distortion (THD) and it will present in the table and the graph

Table 4.3: Total Harmonic Distortion (THD) Content in MLI

Level	Percentage of THDv (%)
3	52.56
5	26.95
7	18.23
9	13.76
11	11.04

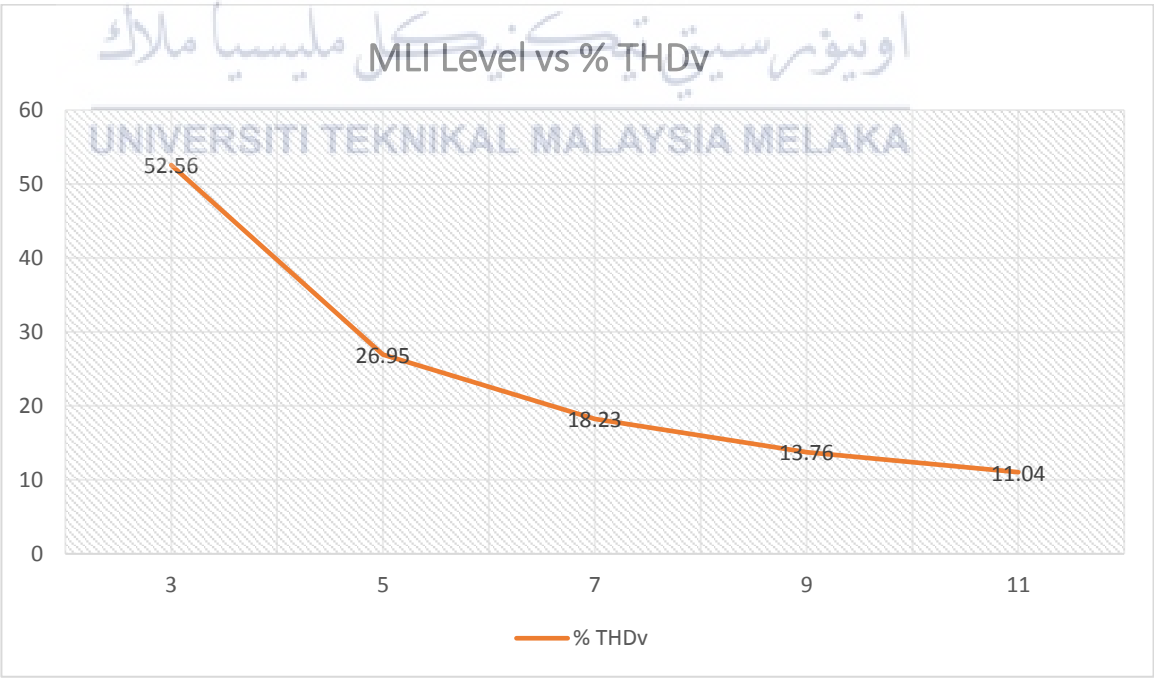


Figure 4.11: Relationship of Levels vs %THDv

The Table 4.3 show the simulation result. The result also illustrated in graph form. From the table and illustrated graph, the lowest percentage of THD for all the simulation result is 11.04% for 11-level MLI. From the graph, it can conclude that the THD will decrease if the number of carrier wave increased. On the other hand, the THD also decrease with the higher output level of inverter.

4.2.3 Simulation of Various Amplitude Modulation Ratio, m_a.

The second parameter that has been manipulated to analyzed the performance of the Cascaded H-Bridge Multilevel Inverter is the is the amplitude modulation ratio, m_a. This simulation is focus to the performance of 11-level MLI with five-carrier. The m_a is the ratio between the amplitude of the sinusoidal reference wave with the triangle carrier wave. The value of m_a can be determined by using equation 4.1.

$$m_a = \frac{Vm,refference}{Vc,carrier} \quad (4.1)$$

There are several parameters that has been fixed to operate the simulation. The Table 4.4 show the fixed parameter for simulation.

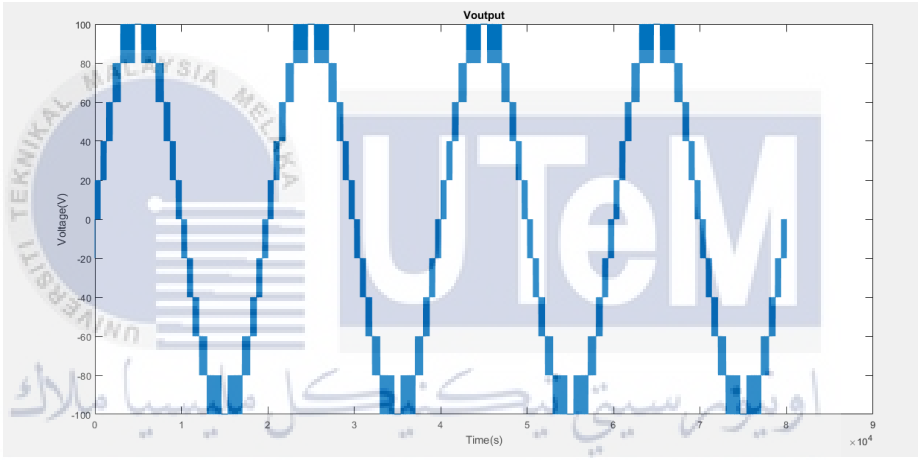
Table 4.4: Fixed Parameter for Various value of m_a Simulation.

Parameter	**Value**
Input Voltage, Vdc	20V
Carrier wave Frequency	5kHz
Reference wave Frequency	50Hz
R load	1200Ω
L load	0.8H
Frequency Modulation Ratio, m_f	100

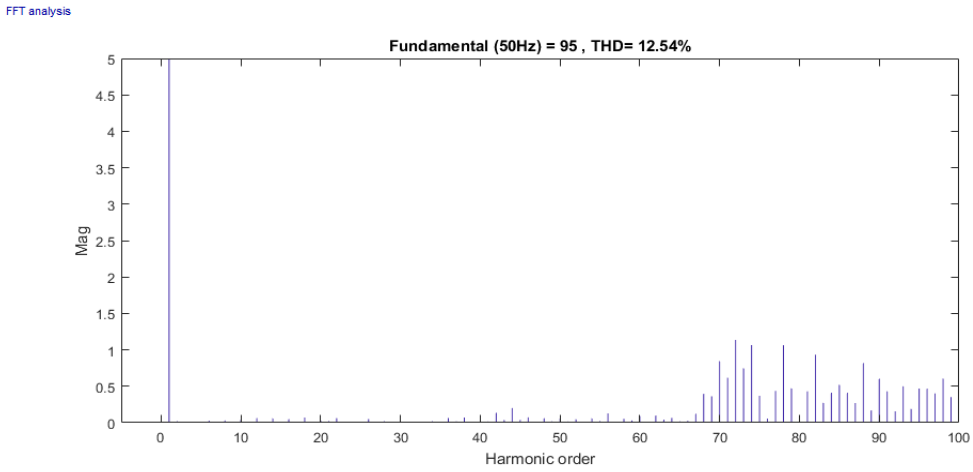
4.2.3.1 Amplitude Modulation Ratio, m_a=0.95.

The amplitude modulation ratio, m_a was adjusted to the value 0.95. The value of the carrier wave is fixed at 1V peak voltage and the peak value of the sinusoidal wave is varied. To get the m_a equal to 0.95, the value of peak voltage of sinusoidal wave was adjusted to 0.95Vp.

The Multilevel inverter output was applied to the RL load. The result of the simulation was show in figure 4.12.



(a)



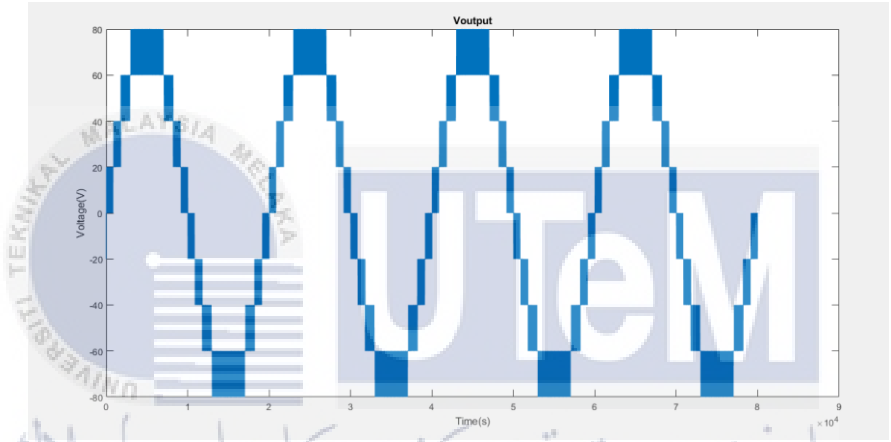
(b)

Figure 4.12: (a) Output Voltage for m_a= 0.95, (b) THD for m_a= 0.9

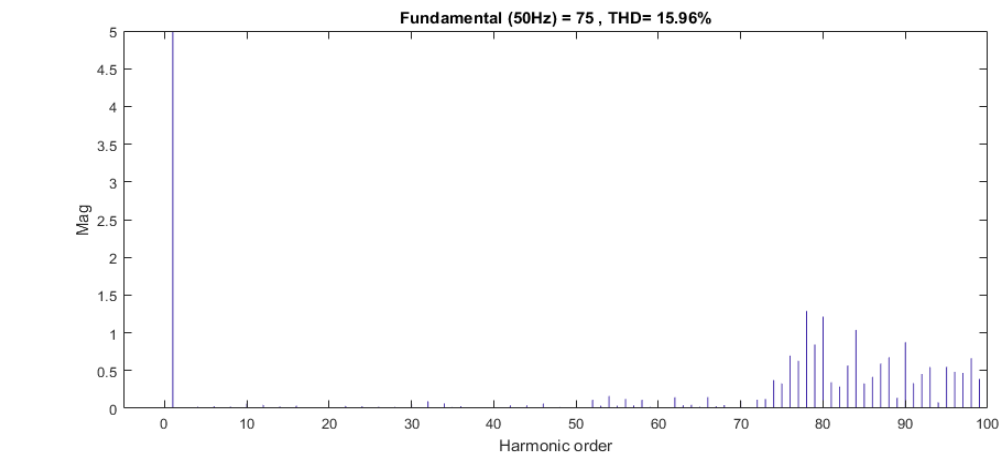
4.2.3.2 Amplitude Modulation Ratio, m_a=0.75.

The amplitude modulation ratio, m_a was adjusted to the value 0.75. The value of the carrier wave is fixed at 1V peak voltage and the peak value of the sinusoidal wave is varied. To get the m_a equal to 0.75, the value of peak voltage of sinusoidal wave was adjusted to 0.75Vp.

The Multilevel inverter output was applied to the RL load. The result of the simulation was show in figure 4.13.



(a)



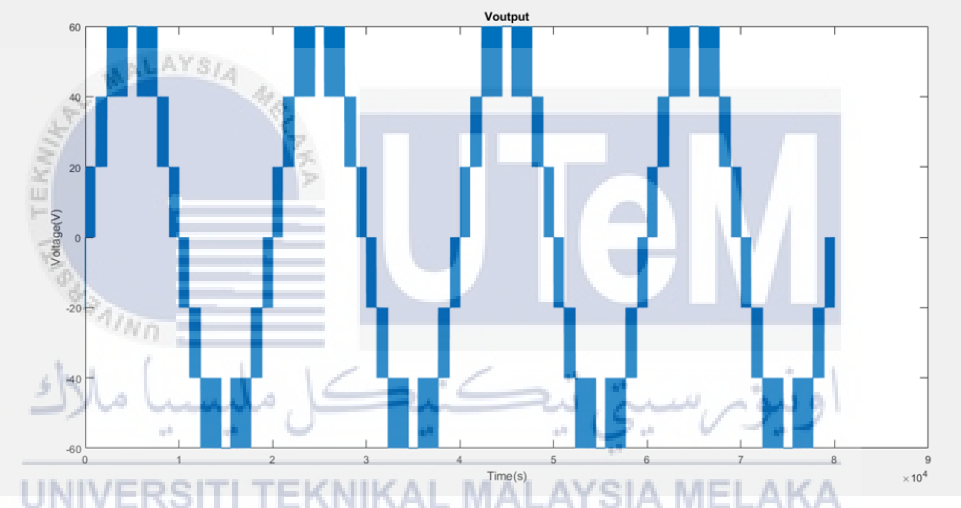
(b)

Figure 4.13: (a) Output Voltage for m_a= 0.75, (b) THD for m_a= 0.75.

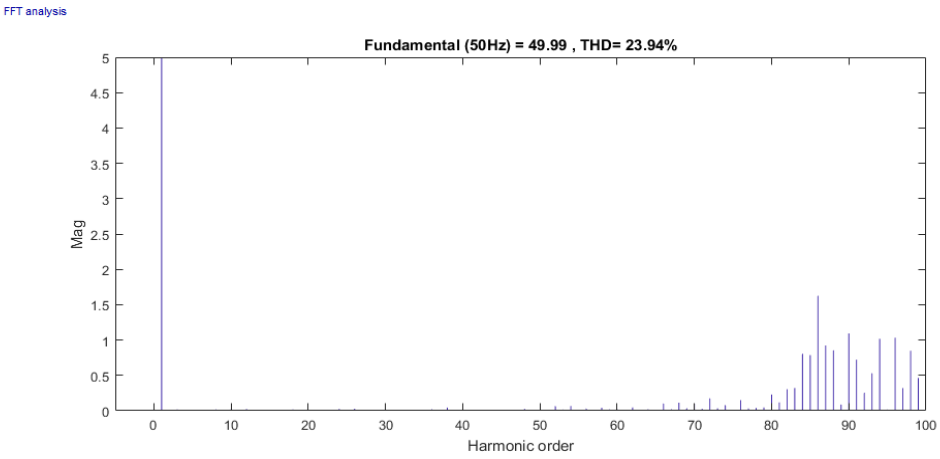
4.2.3.3 Amplitude Modulation Ratio, m_a=0.5.

The amplitude modulation ratio, m_a was adjusted to the value 0.5. The value of the carrier wave is fixed at 1V peak voltage and the peak value of the sinusoidal wave is varied. To get the m_a equal to 0.5, the value of peak voltage of sinusoidal wave was adjusted to 0.5Vp.

The Multilevel inverter output was applied to the RL load. The result of the simulation was show in figure 4.14



(a)



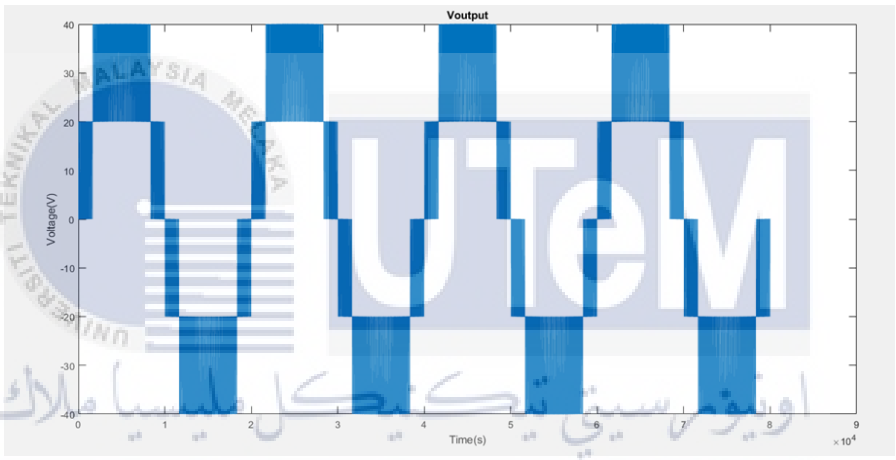
(b)

Figure 4.14: (a) Output Voltage for m_a= 0.5, (b) THD for m_a= 0.5.

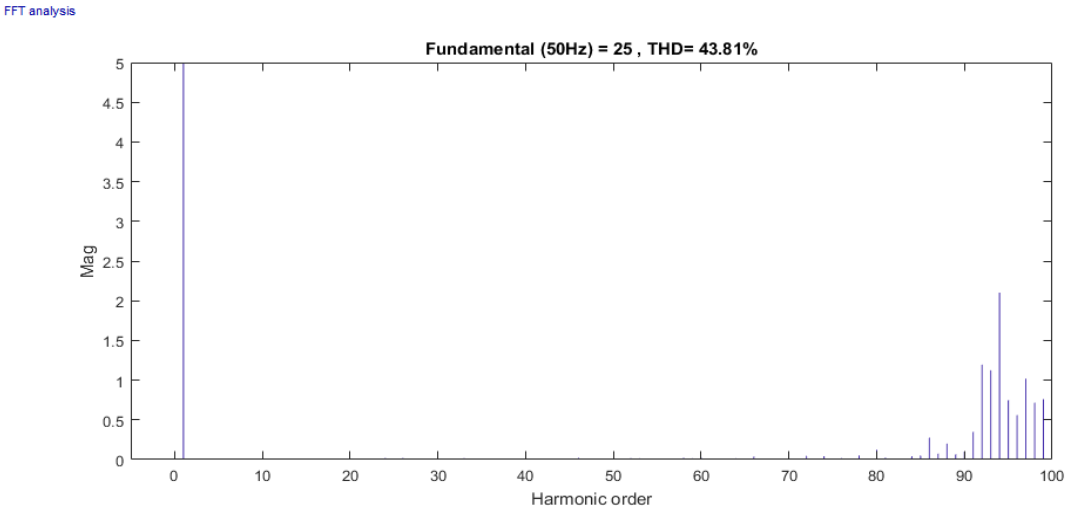
4.2.3.4 Amplitude Modulation Ratio, m_a=0.25.

The amplitude modulation ratio, m_a was adjusted to the value 0.25. The value of the carrier wave is fixed at 1V peak voltage and the peak value of the sinusoidal wave is varied. To get the m_a equal to 0.25, the value of peak voltage of sinusoidal wave was adjusted to 0.25Vp.

The Multilevel inverter output was applied to the RL load. The result of the simulation was show in figure 4.15.



(a)



(b)

Figure 4.15: (a) Output Voltage for m_a= 0.25, (b) THD for m_a= 0.25.

4.2.3.5 Summary of the Amplitude Modulation Ratio, m_a Simulation.

The two-carrier Cascaded H-Bridge Multilevel Inverter was simulated with various value of Amplitude Modulation Ratio, m_a. this section will present the summary of overall result for Amplitude Modulation Ratio, m_a simulation. The result will represent in percentage of the total harmonic distortion (THD) and it will present in the table and the graph.

Table 4.5: The THD of MLI for various m_a

Amplitude Modulation Ratio, m_a	Percentage of THDv (%)
0.95	12.54
0.75	15.96
0.5	23.94
0.25	43.81

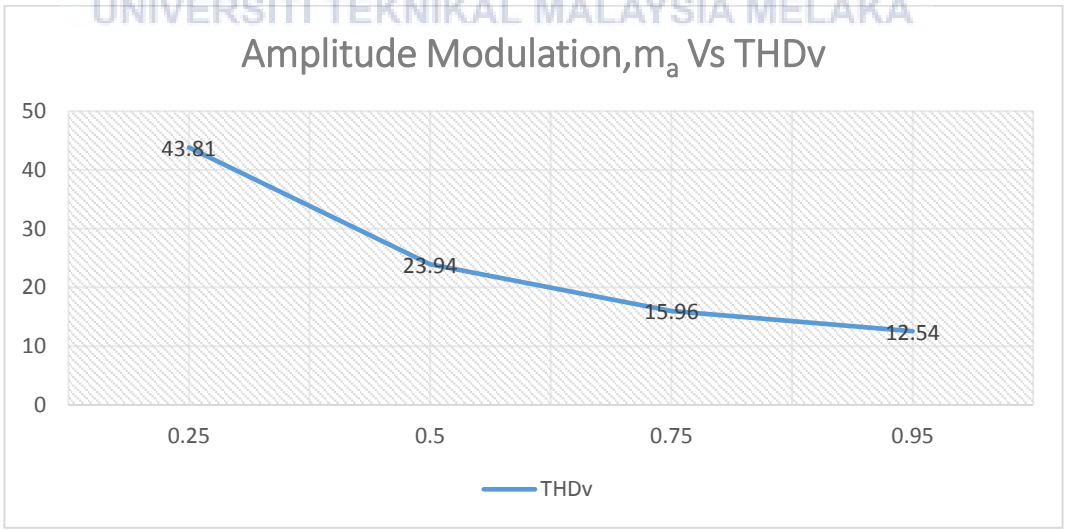


Figure 4.16: The THD with Various Value of Amplitude Modulation Ratio.

Table 4.5 show the THD with various value of m_a. From the table and the illustrated graph, the lowest percentage of THD for all simulation result is 12.56% for 0.95 value of m_a. From the graph, it can be concluded that the THD will decrease if the value of m_a increased. On the other hand, the THD also decrease with the higher output level of the inverter. The level of the voltage can be control by increasing or decreasing the value of amplitude modulation ratio, m_a.

4.3 Summary on Preliminary Results

The number of level of the inverter will results in different output voltage, output current and the percentage of Total Harmonic Distortion in the output where this changes will affect the quality of the output of MLI.

The simulations show that the increase of level of inverter will require a higher number of sources. Hence, this will increase the number of carriers to generate PWM pulses for the switches (IGBTs). This will increase the complexity of the circuit, but produces a better and smoother output.

Total Harmonic Distortion (THD) is a quality measure of the output. As the level of the inverter increases, the percentage of THD in the output decreases. It also decreased THD if the value of amplitude modulation ratio, m_a increased. This shows that the better quality of the output as the level of inverter increases.

4.4 Design and Development of Hardware

The design and development of Multi-Level Inverter started with the design of gate driver. The Orcad Pspice Layout Plus are used to design the circuit of gate driver. The circuit of Gate Driver are then sent to the factory for the final fabrication. The Printed Circuit Board (PCB) that designed for the gate driver are double layered which has connection on both the top and bottom layer. The Figure 4.17 shows the complete fabricated PCB.

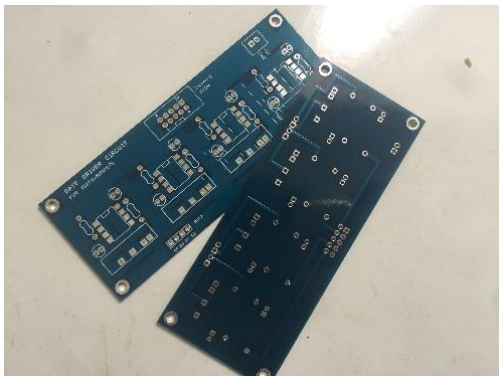


Figure 4.17: Fabricated PCB for Gate Driver

The Figure 4.18 shows the complete soldered gate driver.

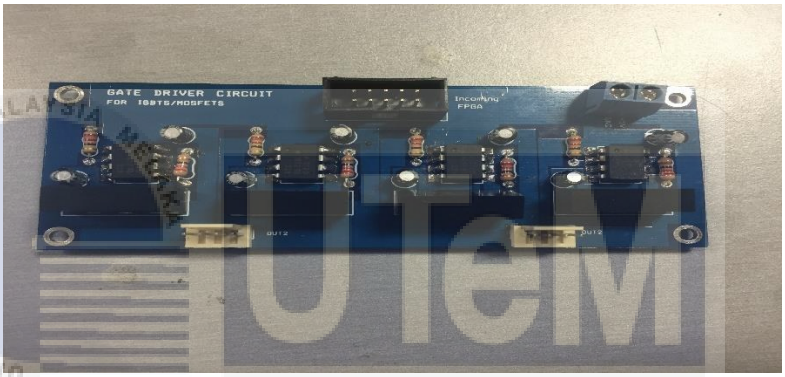


Figure 4.18: Gate Driver

4.4.1 Hardware Testing

The hardware such as IGBT H-Bridge, Gate Driver and FPGA coding are tested and the result of testing is shown in Figures 4.19, 4.20, 4.21 and 4.22.

FPGA Coding Testing

The completed programming codes (refer Appendix) of VHDL format is tested in the Quartus II software by using the compiler. The compiling results is completed as shown in the Figure 4.19 below.

	Task	Time
✓	Compile Design	00:00:36
✓	Analysis & Synthesis	00:00:07
✓	Fitter (Place & Route)	00:00:15
✓	Assembler (Generate programming files)	00:00:04
✓	TimeQuest Timing Analysis	00:00:06
✓	EDA Netlist Writer	00:00:04
	Program Device (Open Programmer)	

Figure 4.19: Compiling Result

The completed compiling codes are then uploaded into the Cyclone IV DE0-nano board and the pulses are check at the pins that assigned earlier in the software

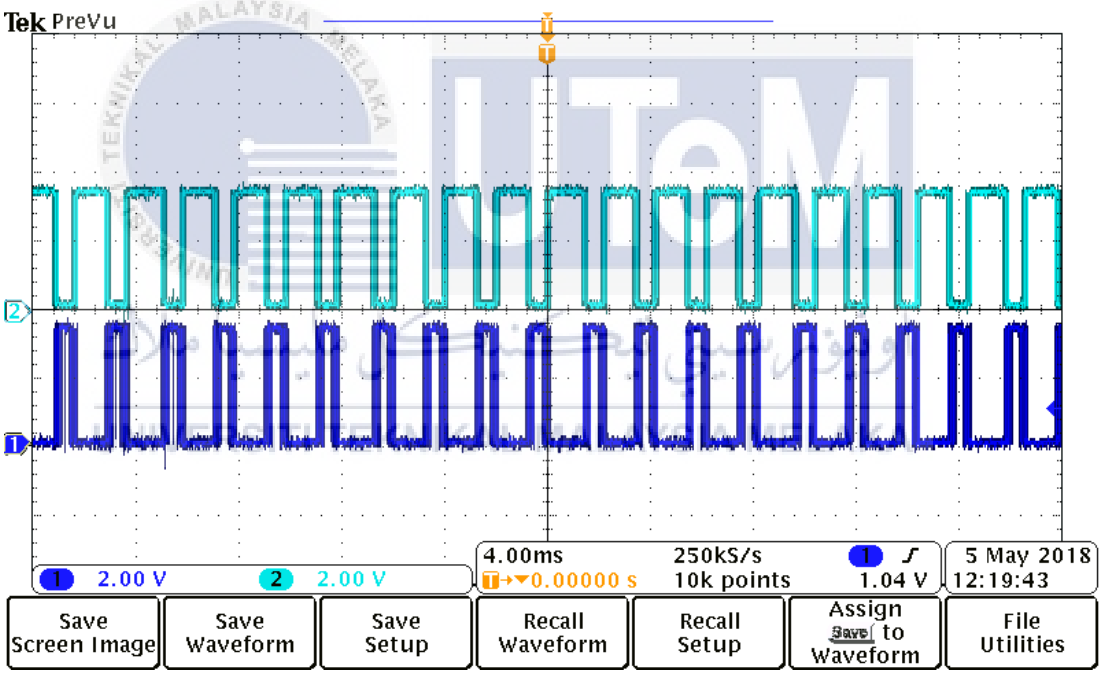


Figure 4.20: Checking for Pulses

Gate Driver Testing

The gate driver is then fed in pulses from the DE0-nano Board. The output was tested and observed by using the oscilloscope. The output of the gate driver should

have a pulse of amplitude around 15V. The Figure 4.21 shows the output testing for gate driver.

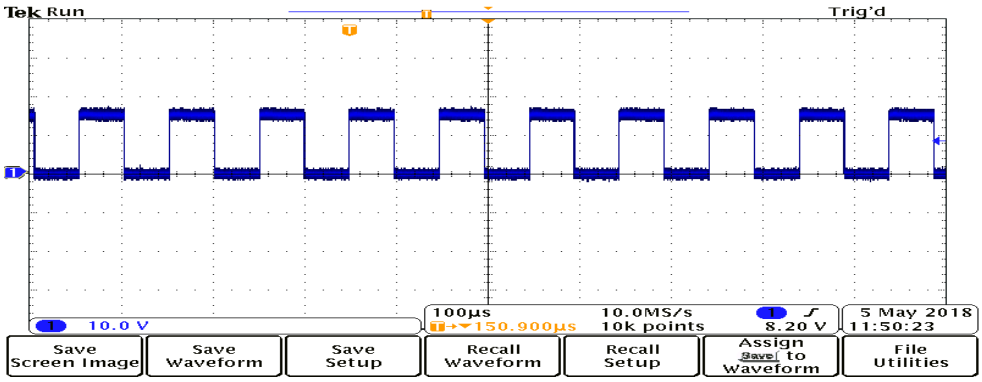


Figure 4.21: Output of Gate Driver Testing with FPGA

The output is at the gate driver is same as the output at the FPGA DE0-nano Board. Malfunctioned Optocouplers and DC-DC converter are replaced and tested again to ensure the functionality of the Gate Driver.

IGBT H-Bridge Testing

Once the FPGA coding and Gate Driver were tested, IGBT cascaded H-Bridge is connected to perform another testing. This testing has the exactly same output as the 5-Level MLI. The Figure 4.22 shows the output of 2 cascaded h-bridge (5-Level MLI).

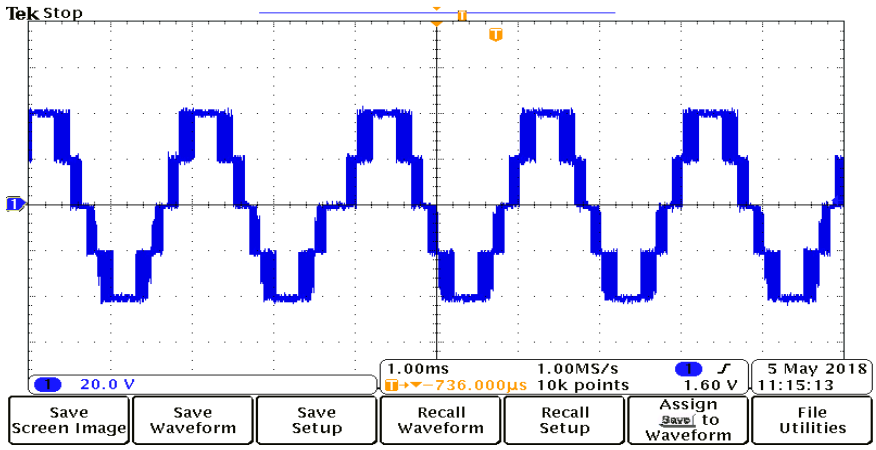


Figure 4.22: Output of H-Bridge

Once the H-Bridge testing were done, it brings the development of hardware to the step of combining 2 Cascaded H-Bridge to complete the final prototype of 5-Levels Single Phase Cascaded H-Bridge Multi-Level Inverter.

4.4.2 5-Levels Multi-Level Inverter

The 5-Levels single phase cascaded h-bridge multi-level inverter is the combination of 2 h-bridge which generating an output of seven different voltage level. The hardware development of the 5-Levels Cascaded H-Bridge MLI is as shown in the Figure 4.23.

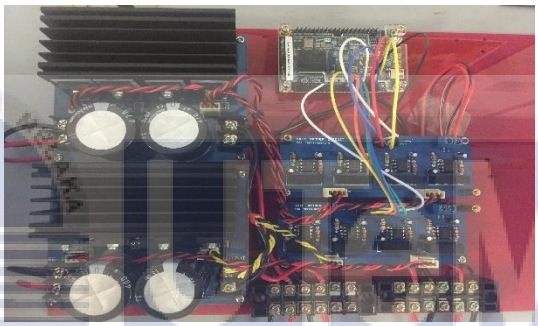


Figure 4.23: 5-Levels Cascaded H-Bridge MLI

End-to-End Hardware Testing

The 5-Levels VHDL programming codes are compiled and tested using oscilloscope to ensure all the pulses has the required pulses waveforms. Secondly, the pulses output from the FPGA Cyclone IV DE0-nano Board are fed into the gate drivers. While, the outputs at Gate Drivers are then connected the IGBTs at each of the H-Bridge. Figure 4.24 shows the setup of testing equipment for the end-to-end hardware testing of 5-Levels MLI.

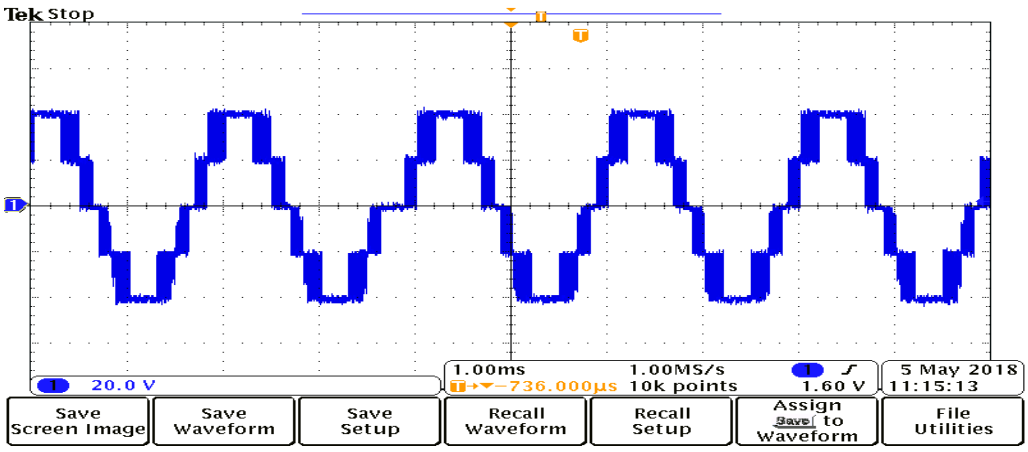


Figure 4.25: Output Voltage Waveform of 5-Levels MLI

The waveform of the output voltage is saved and THD analysis are performed using fluke meter. By using the data from the fluke meter, the data are saved in a fluke view. The Figure 4.26 the output analysis for the THD content in the output voltage of the end-to-end hardware in fluke view.

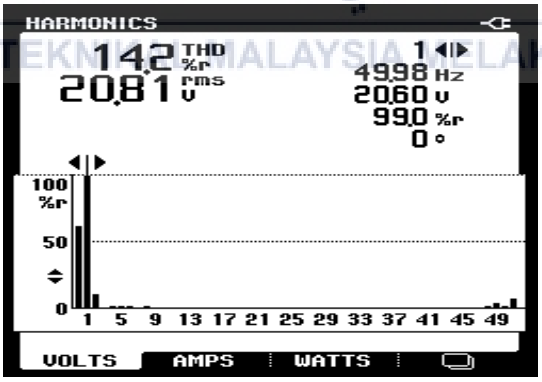


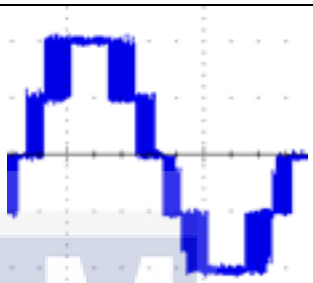
Figure 4.26: THD Content in Output Voltage

The output voltage THD content for the hardware were determined to be 14.2% for the 5-Levels MLI. Comparison are then made between simulation and hardware developed in terms of the output voltage value and the THD content.

4.5 Comparison of Simulation and Hardware Development Results

The comparison of both the simulation and hardware development results are shown in the Table 4.6.

Table 4.6: Comparison of Simulation and Hardware Development Results

	Simulation	**Hardware**
Waveform		
Voltage (max)	40.00V	42.00V
Frequency (Hertz)	50.00	49.98
%THD	26.95	14.20

As shown in Table 4.6, the results for both the simulation and hardware are same in terms of waveform and frequency. As comparison in the table, the maximum voltage and percentage of THD content has a slightly different where the voltage of hardware are greater with a different of 2.00 Volts while the percentage of THD content of the hardware are lower than the simulated result.

Based on the Table 4.6,

$$\% \text{ error} = \left| \frac{\text{Actual Value} - \text{Measured Value}}{\text{Actual Value}} \right| \times 100\%$$

$$\% \text{ error} = \left| \frac{26.95 - 14.20}{26.95} \right| \times 100\% = 47.30\%$$

From the hardware result, it shows that the single phase five levels cascaded h-bridge MLI hardware produces a THD value of 14.20% and it is lesser than the simulation result of single phase seven levels cascaded h-bridge MLI which is 26.95%. The calculated percentage error of THD value between simulation and hardware results is 47.30%. The hardware developed a better THD content output. This is due to the implementation of capacitors in the IGBT H-Bridge circuits where it acts as a filter to provide better quality of output voltage waveform.

CHAPTER 5

CONCLUSION

5.1 Conclusion

In conclusion, the simulation of single phase cascaded h-bridge multi-level inverter for 3-levels, 5-levels, 7-levels, 9-levels and 11-levels are developed using MATLAB Simulink. The Level Shifted Multi-Carrier PWM is designed for Cascaded H-Bridge Multi-Level Inverter to yield signals for power switches operation. The output voltage for all the simulations are yield correctly. Then, the simulation results are analyzed in terms of THD content. The THD content of the output is analyzed using FFT analysis in MATLAB Simulink tool in which based on the Fourier Series Transform. According Table 4.4, the percentage of THD for 3-levels, 5-levels, 7-levels, 9-levels and 11-levels are found to be 52.56%, 26.95%, 18.23%, 13.76% and 11.04%. Moreover, the percentage of THD for amplitude modulation ratio, m_a for 0.95, 0.7, 0.4, and 0.2 are found that 0.95 value is the least percentage of THD. It shows that the percentage of THD decreases drastically when the number of level increases and the amplitude modulation ratio, m_a increase. This meant that the harmonic distortion is decreased as the voltage level of a Cascaded H-Bridge MLI increases. This also shows that the performance of the Cascaded H-Bridge MLI is depending on the voltage levels and amplitude modulation ratio, m_a in terms of THD content. As the staircase waveform produced is more closely like a sinusoidal waveform, the harmonic contents are lesser. In other way, a higher level CHMI can produce a more sine-like waveform to produce lesser harmonics. For the development of hardware, the 5-Levels single phase cascaded h-bridge multi-level inverter, a FPGA Cyclone IV DE0-nano board and gate driver were used before connections to IGBT h-bridges. DE0-nano is used as

the pulses generator and gate driver is used for the purpose of isolation and amplification of pulses. Based on Table 4.6, the percentage THD of five levels output voltage of hardware developed has significant difference of 47.30% which the hardware developed has a lower THD content. Therefore, the hardware is said to have a better efficiency than the simulation. This is due to the implementation of capacitors in the circuit which acts as a filtering for the distortion of input voltages. Finally, the objectives of this project are achieved with no doubt.

5.2 Recommendation

The great advantages of MLI is that to produce an output that is almost sinusoidal waveform compared to the conventional one. As the simulations done in this project, the output waveforms are satisfied and the THD content are reduced by increasing the level. Simulations is simulating the best performance of the components which is the most ideal condition without any losses or distortion. However, the development of the hardware in this project has proved that the importance of the filtering on the waveform produced. Filters can always be used to refine the output quality of single phase MLI. The MLI is then going to produce an output waveform with less harmonic distortion, but there are still a lot improvement and elimination techniques are required to produce a smoother waveform. Hence, the number of components needed such as gate drivers and boost converters is recommended to be reduced as to reduce cost and complexity of the Cascaded H-Bridge Multi-Level Inverter. Furthermore, parameter such as Switches Losses should have aware with besides the THD content.

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APPENDIX A1

```
LIBRARY ieee;
USE ieee.std_logic_1164.all;
USE ieee.numeric_std.all;

entity pwm5level8001 is
port(
    clk: in std_logic;
    rst: in std_logic;

    s1up, s1low: out std_logic;
    s2up, s2low: out std_logic;
    s3up, s3low: out std_logic;
    s4up, s4low: out std_logic

    --x:out std_logic_vector (15 downto 0)

);
end entity;

architecture rtl of pwm5level8001 is

    signal address : std_logic_vector (12 downto 0);
    signal clk_1000k: std_logic;
    signal s1, s2, s3, s4: std_logic_vector (0 downto 0);

begin

   process (clk, rst) is
   begin
      if (rst = '0') then
        address <= (others =>'0');
      elsif (rising_edge(clk)) then
        if (clk_1000k = '1') then
          if (unsigned(address) < 8001) then
            address <= std_logic_vector(unsigned(address) + 1);
          else
            address <= (others =>'0');
          end if;
        end if;
      end if;
   end process;

   --=========================================
   -- instantiate SPWM table (ROM) to the code
   --=========================================
   lut_s1:
   entity work.s1 (SYN) port map (address => address, clock => clk, q => s1);
   lut_s2:
   entity work.s2 (SYN) port map (address => address, clock => clk, q => s2);
   lut_s3:
   entity work.s3 (SYN) port map (address => address, clock => clk, q => s3);
   lut_s4:
   entity work.s4 (SYN) port map (address => address, clock => clk, q => s4);


   --=========================================
   -- generating sampling clock with f = 1000 KHz
   --=========================================
   gen_1000KHz_clk:
   entity work.clk_div (rtl) port map (clk => clk, rst => rst, clkout => clk_1000k);

   --=========================================================
   --Generating blanking time function for induction machine
   --=========================================================
   blanking_time_2microsec:
   entity work.blankingtime_main (behavioral) port map (clock =>clk, sa1 => s1, sb1 =>s2, sc1 => s3, sd1 => s4,
   --x <= address;

end rtl;
```

APPENDIX A2

```
--Blanking Time Generator

library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;

entity blankingtime_main is
    port ( clock : in std_logic;
            --rst: in std_logic;

           --INPUT PORT--
           sa1, sb1, sc1, sd1: in std_logic_vector (0 downto 0);

           --OUTPUT PORT--
           s1upper, s2upper, s3upper, s4upper: out std_logic;

           s1lower, s2lower, s3lower, s4lower: out std_logic);
end blankingtime_main;


                --blanking_time_signal--
architecture behavioral of blankingtime_main is
signal a1,a2, b1, b2, c1, c2, d1, d2: std_logic_vector (14 downto 0);

--clock_out
signal T : std_logic;
```

```
begin
--=========================================================
--clock_divide
--=========================================================
u1 : entity work.blanking_mod18(behavioral) port map (clk => clock, clkout => T);
--=========================================================
--upper_counter
--=========================================================
u2 : entity work.blanking_upper_counter(behavioral) port map (clk => T, clear1 => sa1, clear2 => sb1, clear3 => sc1, clear4 => sd1,
--=========================================================
--lower_counter
--=========================================================
u3 : entity work.blanking_lower_counter(behavioral) port map (clk => T, clear1 => sa1, clear2 => sb1, clear3 => sc1, clear4 => sd1,
--=========================================================
--Comperator
--=========================================================
u4 : entity work.blanking_comparator(behavioral) port map (Cin1 => a1, Cin2 => b1, Cin3 =>c1, Cin4 => d1, Cin13 => a2, Cin14 => b2,

end behavioral;
```

APPENDIX A3

```
1  --================================================================================
2  -- Entity: Mode 20
3  -- Author: FIRDAUS ROSLAN
4  -- Date: 1/4/2018
5  -- Brief: to generate 1MHz clock from 50MHz sys_clk
6  --================================================================================
7
8   LIBRARY ieee;
9   USE ieee.std_logic_1164.all;
10  USE ieee.numeric_std.all;
11
12 entity clk_div is
13   port (
14     clk : in std_logic;
15     rst : in std_logic;
16     clkout : out std_logic
17   );
18 end entity;
19
20 architecture rtl of clk_div is
21
22   constant cnt_max : integer range 0 to 500 := 500;
23   signal   cnt     : integer range 0 to cnt_max-1;
24
25 begin
26
27   process (clk, rst) is
28   begin
29     if (rst = '0') then
30        cnt <= 0;
31     elsif rising_edge (clk) then
32       if (cnt = cnt_max-1) then
33          cnt <= 0;
34       else
35          cnt <= cnt + 1;
36       end if;
37     end if;
38   end process;
39
40   -- divide by 5, result a pulse in every 250 cycles
41   --250/5=50MHz
42   --each clk 5u
43   clkout <= '1' when (cnt = cnt_max-1)  else '0';
44
45 end rtl;
```