A MODIFIED PID CONTROLLER DESIGN FOR 3-PHASE SPWM MULTILEVEL INVERTER

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A report submitted
in partial fulfillment of the requirements for the degree of
Bachelor of Electrical Engineering with Honours

Faculty of Electrical Engineering

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2019

DECLARATION

I declare that this thesis entitled "A MODIFIED PID CONTROLLER DESIGN FOR 3-PHASE SPWM MULTILEVEL INVERTER is the result of my own research except as cited in the references. The thesis has not been accepted for any degree and is not concurrently submitted in candidature of any other degree.

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APPROVAL

I hereby declare that I have checked this report entitled "A MODIFIED PID CONTROLLER DESIGN FOR 3-PHASE SPWM MULTILEVEL INVERTER" and in my opinion, this thesis it complies the partial fulfillment for awarding the award of the degree of Bachelor of Electrical Engineering with Honours

Signature : .....

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DEDICATIONS

To my beloved mother and father

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Beyond everything else, I thank to The One, The Supreme Creator for giving me all that is necessary in order to complete this project, a strong heart and a mental fortress mind.

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ABSTRACT

Multilevel inverter is an evolved version of the conventional inverter and have risen in favour by many in industries out of its capability to operate for medium to high rating power equipment. It boast several advantages over inverter such as generating higher voltage using low rating equipment, produce a more pure sinusoidal voltage wave with increasing levels and less losses from the switching frequency. This project is to analyse a 3-phase 5-level multilevel inverter with sinusoidal pulse width modulation (SPWM) by using a PI and modified PID controller as a method to maintain desire output by using MATLAB and MATLAB Simulink. The gating component applied are the MOSFETS that acts as the switching component. The feedback controller of PI and modified PID are also designed and calculated and then tuned on MATLAB with trial and error through proper procedure an applied to ensure a steady voltage output of the 3-phase 5-level cascaded h-bride multilevel inverter. The results are analysed in the form of total harmonic distortion (THD) and power factor where the CHMI have low THD and power factor of ~1. The performance of both controller are also analysed and compared where modified PID is slight better as it have better response which ia average at 0.126s compare than that of PI at 0.157s and more robust if there is disturbance or voltage change.

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ABSTRAK

Inverter bertingkat adalah versi evolusi dari inverter konvensional dan telah menjadi pilihan kepada banyak industri disebabkan keupayaannya untuk beroperasi untuk peralatan kuasa sederhana hingga tinggi. Ia mempunyai beberapa kelebihan berbanding inverter seperti menghasilkan voltan yang lebih tinggi menggunakan peralatan penarafan yang rendah, menghasilkan gelombang voltan sinusoidal yang lebih tulen dengan peningkatan tingkat dan mengurangkan kehilangan kuasa dari kekerapan peralihan suis.Tujuan projek ini adalah menganalisis inverter bertingkat 5 tahap 3 fasa dengan modulasi lebar denyut sinusoidal (SPWM) dengan menggunakan pembawa tunggal dan 4 bentuk gelombang rujukan sebagai kaedah kawalan untuk menghasilkan output keinginan dengan menggunakan MATLAB. Komponen 'gating' yang digunakan adalah MOSFET yang bertindak sebagai komponen pensuisan. Pengawal maklum balas PI dan PID juga adalah direka dan diubahsuai untuk digunakan untuk memastikan output voltan mantap bagi inverter h-jambatan berbilang peringkat 5 tingkat. Hasilnya dianalisis dalam bentuk total distorsi harmonik (THD) dan faktor kuasa. Hasil dari implementasi kedua-dua sistem kawalan juga akan dianalisis dan perbandingan akan disertakan.

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LIST OF SYMBOLS AND ABBREVIATIONS

THD	-	Total Harmonic Distortion
PF	-	Power Factor
SPWM	-	Sinusoidal Pulse Width Modulation
SDLC	-	System Development Life Cycle
VSI	-	Voltage Source Inverter
CSI	-	Current Source Inverter
MLI	-	Multilevel Inverter
AC	-	Alternating Current
DC		Direct Current
CHMI		Cascaded H-Bridge Multilevel Inverter
PWM		Pulse Width Modulation
PD		Phase Disposition
POD		Phase Opposition Disposition
APO		Alternate Phase Disposition
PI		Proportional-Integral
PID		Proportional-Integral-Derivative

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CHAPTER 1

INTRODUCTION

1.1 Background

As the nation and its people are evolving into a new age of technology advancement so does the requirement for such task. The consumption of energy and resource alone are exceptionally high and resulting numerous of side effect such as burning of fossil fuel of which lead to the emission of greenhouse gas, which in turn lead to global warming. As culmination from such wanton cases, renewable energy has been a popular choice nowadays and simpler design for many electronic and more efficient controllers must be implemented.

An inverter is used to convert DC source into an AC source. Among its output commonly known are usually of 3 types of forms which is the square wave usually applied for some resistive loads, quasi/modified sine wave for inductor, capacitor, resistive loads and pure sine wave for prevalent application, thus classifying all of it into 3 types of inverter output waveform[1]. The inverter are also known to have been classified into 2 operation mode which is the voltage source inverter (VSI) and current source inverter (CSI), however, (VSI) have several distinct advantages over (CSI) such as being more efficient, highly dependable and quick dynamic response[2]. Which is why of it being implemented in this project.

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However, as the growth renewable energy approached equipped with high power equipment and high power rating machineries are ever increasing, the topologies of inverter too must evolve to suits the need of the industry. Thus, a multilevel inverter is invented with design evolved from the existing one. A multilevel

inverter(MLI) is suitable for energy control of medium to high power rating equipment. With its topologies, a MLI is preferable purely because of its performance in generating a higher voltage from a lower rating powered device,

better voltage waveform ,using pulse width modulation control its switching frequency is reduced and smaller total harmonic distortion (THD)[3].

The focus however would be on the method of controlling section as a good controller can contribute a significant effect on the efficiency of the inverter, such as the switching frequency, minimizing the switching loss, steady state with fast transient response from control point of view. Variety of controller are available such as neural network and PID controller. Artificial neural network is such information etiquette is implement the way of brain processing work, involving the neural connection and mimicking it which is differ from conventional controllers[4]. For PID controller, it is a type feedback controller famous among controllers, PID stands for proportional, integral, derivative. In each application, coefficient of these three actions are varied to get optimal response and control. Controller input is error signal and output is given to the plant/process. Output signal of controller is generated, in such a way that, output of plant is try to achieve desired value[5].

However, among the controllers, PID is chosen because of its simple topology to implement such as a simple equation, require low amount of resource, more robust to tuning any discord, easier to calibrate by normal trial and error and better response to unmeasured disturbances. Model-based controllers recover from unmeasured disturbances with only an integral type of action, while PID has also the proportional and derivative action that immediately act on an unknown disturbance[5]. However, despite its advantageous characteristic, PID controller still have a setback. Which is the set point kick phenomenon from the derivative action. To avoid this, modification is made with an example PI-D and I-PD scheme where derivative action is only operated on feedback path so as to avoid any differentiation.

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1.2 Motivation

Development of renewable energy are rapidly expanding. Large scale renewable power plant are higher than ever and should not be neglected by the fact in 2018 the global solar installation only will be 109GW [6] .Thus, the needs of inverter are now more popular than ever and are an integral to the power distribution system. Application of inverter would bring much advantages to the industry especially of that multilevel inverter, famed for its capability to operate in medium to high power energy control equipment or grid. Moreover, as shown in Table 1.1 below 5 level inverter shown more efficiency than that of the 2 level.

Table 1.1 Comparison between 2 level and 5 level CHMI inverter

	Three phase 2-Level Inverter	**Three phase 5-level CHMI using SPWM**
THD value after filter	14.54%	0.75%
Power Factor(PF)	~1	~1
Voltage output (V_{rms})	88.89V	415.47V

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From Table 1.1 above it can be stipulated that 3 phase 5-level CHMI using SPWM give a better result as it have lower value of THD and higher value of voltage output than that 2 level inverter that have significant higher amount of THD.A modified controller is devised and simulate in this paper using MATLAB Simulink to inquire of its ability to operate under designated load and giving the intended voltage output not to mention smaller amount of total harmonic distortion.

1.3 Problem Statement

With the advancement of our technology development, the growth of electricity are also exponential, corresponding with the demand. Thus, multitudes of power distribution have been created and innovated to handle electricity distribution properly. One of the core component in the system is the inverter which is crucial in converting DC signal to AC signal and control the power flow in the distribution system. However, despite the commendable advancement in this field, setback and predicament are bound to occur.

The latter are usually in the form significant switching losses, voltage-balancing concerns and raised number of components. The needs of multilevel inverter however is undeniable as the growth of energy control of medium to high power rating equipment in renewable energy sector increase. For practical approach, in Power grid system, there are usually change of load where voltage drop may occur under certain condition so to speak. Thus, to maintain the purity of sine wave, a feedback controller need to be implemented so that the voltage output is maintained. This project is to research on the feedback controller implemented. Typical PID feedback controller however usually have set point kick phenomenon which is a condition where if the reference input is a step function, the manipulated variable will involve an impulse function, such set point kick phenomenon can cause equipment to be damaged. This project suggest modification to the PID controllers.

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1.4 Objective

This project endeavour to:

1. Simulate three phase Cascaded H-bridge Multilevel Inverter with MATLAB-Simulink software using SPWM technique with one carrier.
2. Analyse the performance of CHMI in terms of total harmonic distortion (THD) and the power factor for open loop system.
3. Design a feedback PI and modified PID controller and implement it into CHMI.
4. Analyse the performance of both controllers on the three phase Cascaded H-bridge Multilevel Inverter.

1.5 Scope

The scope for this project are:

- Resolved on the cascaded H-bridge for 5-level 3 phase
- Simulate the 3 phase H-bridge multilevel inverter by employing MATLAB Simulink.
- The voltage output (V_{rms}) is 400V which is standard grid voltage, from the peak voltage sine wave output.
- Modified PID and PI are implemented as the controller.

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CHAPTER 2

LITERATURE REVIEW

2.1 Introduction

This chapter will discuss the topology of typical multilevel inverter available and frequent applied in the industries. This literature review will enhance understanding about component used in final year project. Moreover, this chapter will also discuss about the sinusoidal pulse width modulation (SPWM) technique used in order to reduce harmonic load voltage.

This chapter will also include literature review of controller being used and available, the working principle of controller.

2.2 Inverter & Multilevel Inverter

Designed of many electrical device is progressively being upgraded and applied in an industrial application which utilize large amount of power. Significant amount of appliances in industries however need medium or low power for their operation. The Multilevel inverter is like an inverter and it is used for industrial applications as alternative in high power and medium voltage situations.

As the industries is getting bigger and larger for production and technological advancement, multilevel inverter is being chosen for it advantageous characteristic such as multilevel inverters produce common mode voltage, reducing the stress of the motor and do not damage the motor, it also can operate at both fundamental switching frequencies that are higher switching frequency and lower switching frequency. It should be noted that the lower switching frequency means lower switching loss and higher efficiency is obtained[7]. Variety of multilevel inverter topology have been suggested in this review, three main topologies of multilevel inverters are the diode clamped inverter, flying capacitor inverter, and the cascaded h-bridge inverter[8].From table 2.1 below, it is shown and can be inferred that which among the 3 multilevel inverter comprised of the lowest number of component.

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Table 2.1 Comparison of number of components utilised by each multilevel inverter topologies[9]

Multilevel Inverter Topology	Number of level	Power Switches	Power Diodes	DC Bus Capacitors
Flying Capacitor	5	8	-	10
Cascaded-H Bridge	5	8	-	-
Diode-clamped	5	8	12	4

From table 2.1 above, it is shown that cascaded h-bridge multilevel inverter have the lowest number of component employment than the other 2 at only 13 component. This shows that cascaded h-bridge is the most convenient to be used. This is further validated by the table above as more component will only resulting higher cost to build and more complex to handle the operating mechanism.

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2.2.1 Flying Capacitor Multilevel Inverter

This type of multilevel inverter requires capacitor to be pre-charged. It is quite the same in term of topology with diode clamped multilevel inverter, however the capacitor is instead used to separate the input DC voltage. The capacitor near to the source have higher voltage while the one near to the load have lower voltage. They are known as Flying Capacitor Multilevel Inverter, purely from reason of the capacitors float with respect to earth's potential[10]. For each voltage output level, 4 switches are turned on. The amount of component needed is correlate with the formula (n-1) for the voltage sources,2(n-1) for switching devices and(n-1)x ((n-2))/2 for capacitor. n is the number of level[11].

Flying capacitor have its own advantages where the capacitors allow extra energy during long energy discharge transient when 'n' level is high and lower THD when the 'n' is high. It also, however posed significant disadvantages where the topology can be bulky and more expensive from the large number of capacitor used and complex control to maintain capacitor's voltage balance[12]. Figure 2.1 below shown the topology flying capacitor multilevel inverter.

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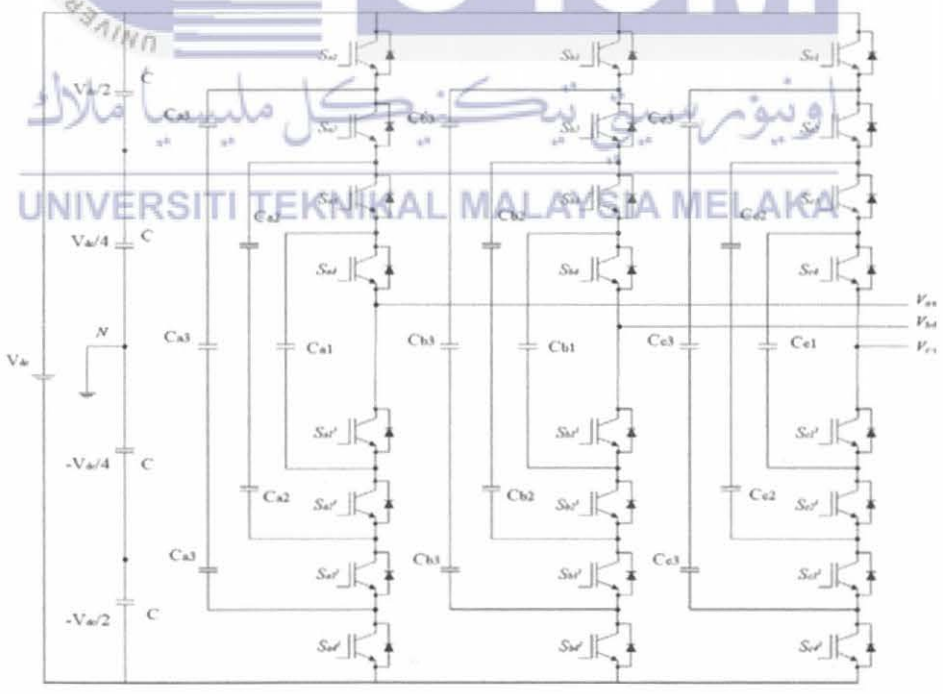

Figure 2.1 3-phase 5 level of flying capacitor multilevel inverter [13]

2.2.2 Diode-Clamped Multilevel Inverter

The implementation of diodes which is to produce multiple voltage level through different phases to the capacitor banks that are arranged in series is the main idea for diode clamped inverter. It also reduced stress on other electrical devices by a diode that transfer limited amount of voltage. However, this topology also has its own drawback where its maximum output voltage is only half of the input DC voltage. This weakness can be countered by increasing the level of the inverter, thus increasing the switches, diodes and capacitors[7]. The design however is limited 3 level out of capacitor balancing issues. This problem can be resolved by using a two times voltage source or cascading two diode clamped multilevel inverters[11]. Figure 2.2 below shown 5-level topology for diode-clamped multilevel inverter.

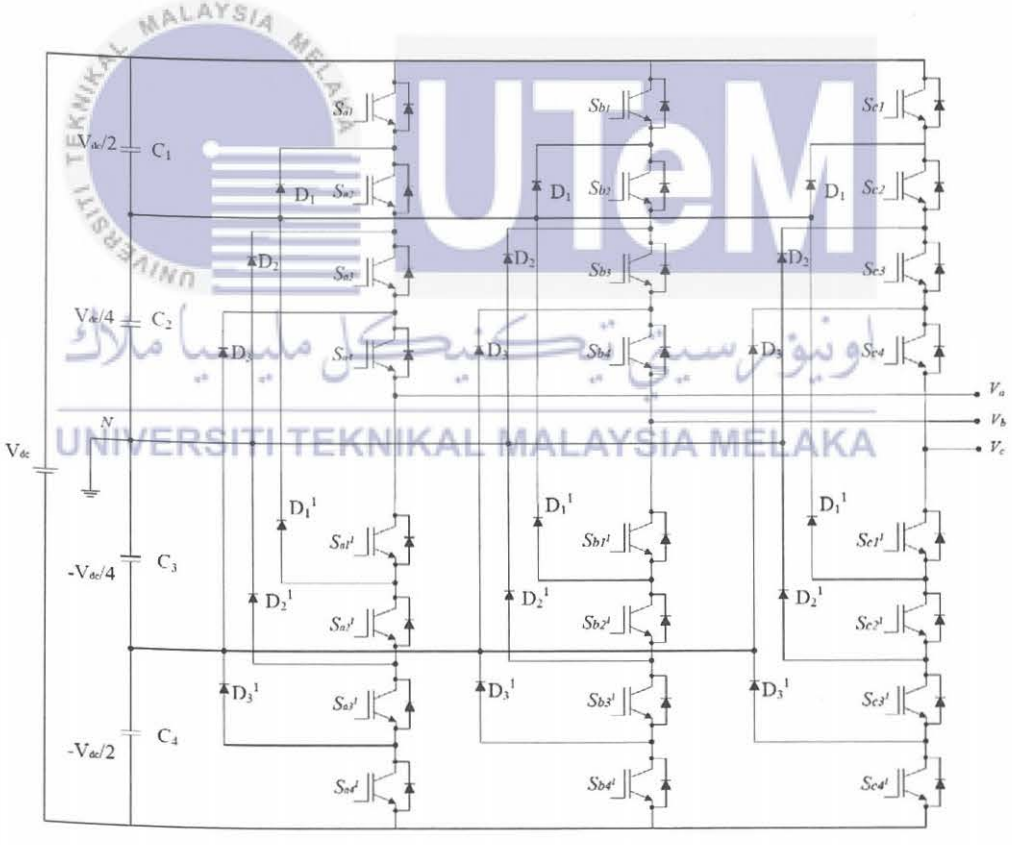

Figure 2.2 3-phase 5 level topology of Diode-Clamped multilevel inverter [13]

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2.2.3 Cascaded H-Bridge Multilevel Inverter

For CHMI, it is composed of two series connected H-bridge which are also fed by an independent voltages sources. Thus, the synthesized voltage waveform is the sum of all of the individual cell outputs mainly because the outputs of the H-bridge cells are arranged and connected in series. The output voltage is given by.

$$V = V1 + V2 \tag{2-1}$$

Where the output voltage of the first cell is known as V1 and the output voltage of the second cell is signified by V2. There are five level of output voltage which is 2V, V, 0, -V, -2V. The main advantages of cascaded H-bridge inverter are that it needs least number of components, modularized circuit and soft switching can be utilized. But the main disadvantage is that when the voltage level increases, the number of components such as switches increases and also the sources. Thus resulting the cost and weight to be increased. Field where high power and power quality are crucial is where the cascaded H-bridge multilevel inverters have been employed for example, static synchronous compensators, active filter and reactive power compensation applications, photo voltaic power conversion, continuously power supplies, and magnetic resonance imaging[13]. Figure 2.3 below shown topology 5-level cascaded h-bridge multilevel inverter.

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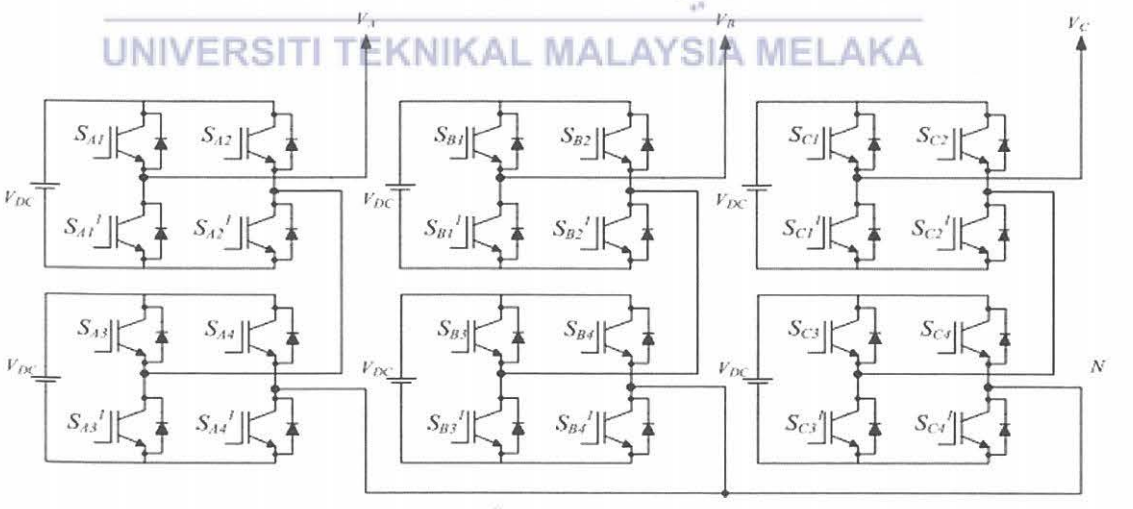

Figure 2.3 3-phase 5 level topology of Cascaded H-Bridge multilevel inverter [13]

2.3 Sinusoidal Pulse Width Modulation (SPWM)

Sinusoidal Pulse Width Modulation (SPWM) is a widely known control method widely used in power electronic inverter circuit. Menial switching losses, fewer harmonic from the output and easy implementation are among the advantageous trait of SPWM[14]. The sinusoidal pulse-width modulation (SPWM) technique produces a sinusoidal waveform by filtering an output pulse waveform with varying width [15]. SPWM technique advantage and disadvantages is as shown in Table 2.2 below.

Table 2.2 Advantage and Disadvantage of SPWM [16]

Advantage	Disadvantage
More efficient which is at 90% efficiency	Attenuation of the required fundamental component of the waveform
Improved control on the process	Drastically amplified switching frequencies that resulting to greater stresses on associated switching devices and therefore dreading of those devices
Reduced energy consumption	High-frequency harmonic components is generated.

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2.3.1 SPWM for Multilevel Inverter

For the principle working of SPWM, a sinusoidal reference voltage waveform is compared with a triangular carrier waveform to generate gate signals for the switches of inverter. Several multicarrier techniques have been developed to reduce the THD ratios, based on the classical SPWM with triangular carriers. The fundamental frequency SPWM control method was proposed to minimize the switching losses[17].

It is inferred that the significant difference between pulse width modulation and sinusoidal pulse width modulation is the width of each pulse is varied in proportion to the amplitude of a sine wave evaluated at the centre of the same pulse for SPWM compared to than that of PWM [18].

Multilevel inverter have various control strategy, however there are 2 most prominent and mainly used. That said is high switching frequency and fundamental switching frequency. SPWM, Selective Harmonic Elimination PWM (SHEPWM), Space Vector PWM (SVPWM) are the one for high switching frequency. From the aforementioned method above SPWM is the commonly used for the multilevel inverter because of its simple principle to grasp and easy to implement[19]. Figure 2.4 and 2.5 below show basic principle of SPWM.

For multilevel inverter however, to reduce the distortion from the topology of MLI, an improvisation is made where variety of multicarrier technique is developed, although it is still based from the existing traditional SPWM with triangular carriers. where (n-1) carrier formula is used for n level of MLI. Among the methods that is employed is carrier disposition while there is also the phase shifting of multiple carrier signals[20].

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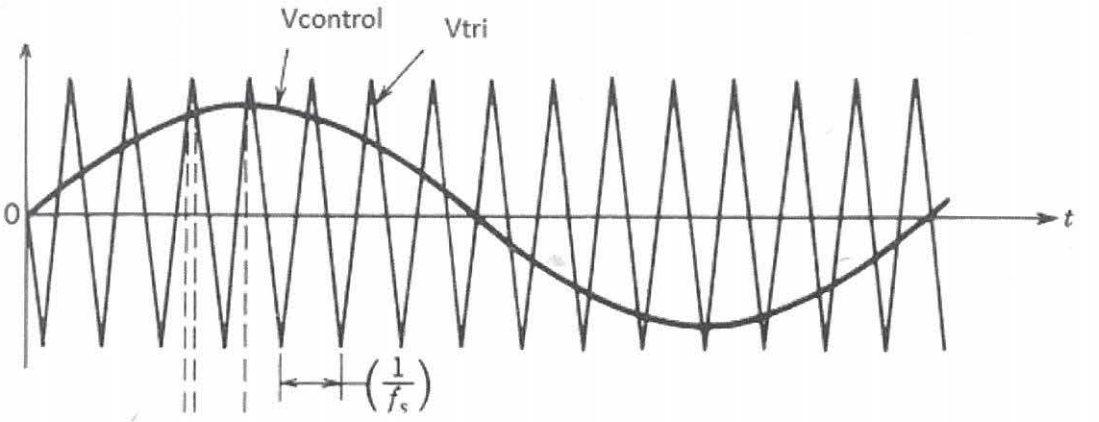

Figure 2.4 Example of SPWM principle where carrier waveform is compared with reference waveform [18]

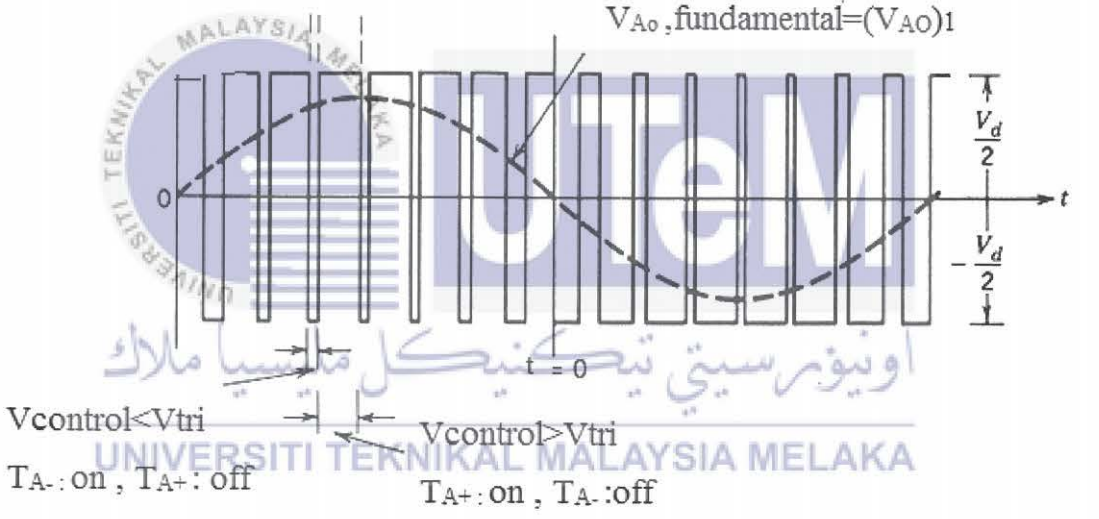

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Figure 2.5 Gating from the comparison between 2 signals [18]

2.3.2 Types of SPWM Techniques

For an inverter or a multilevel inverter of which their topology incorporated of 3 level or more than that, a multiple pulse width modulation technique is applied. This technique are arranged into level shift and phase shift. For level shifted, there are 3 types of technique.

- Phase disposition (PD-PWM): these phase employed multiple carrier waveform that are in same phase. Figure 2.6 below are the waveform for phase disposition.

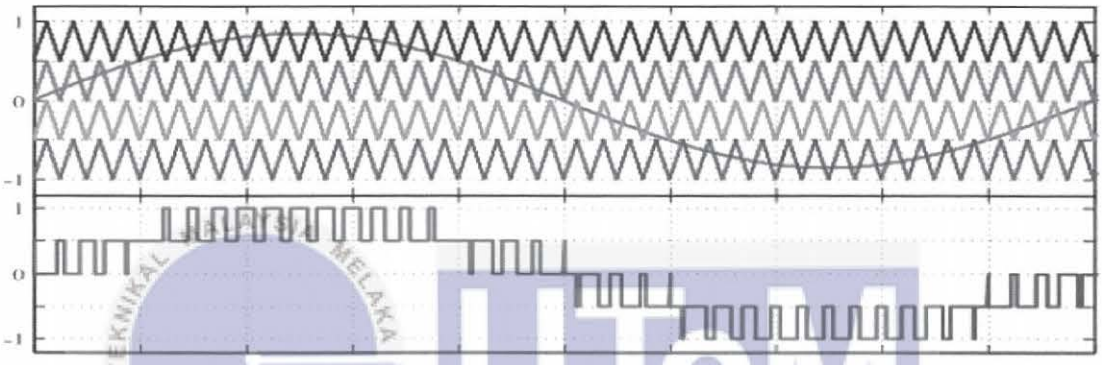

Figure 2.6 Phase Disposition[21]

- Phase opposition disposition (POD-PWM): for this type, carrier signal for the above zero and below zero are not synchronised or out of phase to each other by 180 degree. Figure 2.7 below are the waveform so as to speak.

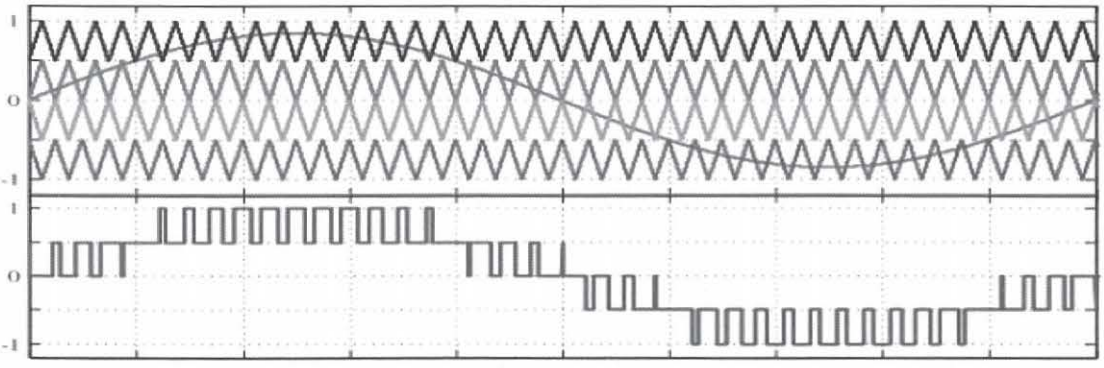

Figure 2.7 Phase Opposition Disposition[21]

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- Alternative phase disposition (PWM-APO): Apo type is where all the carriers have different phase shift by 180 degree between them. Figure 2.8 below shown the waveform for PWM-APO.

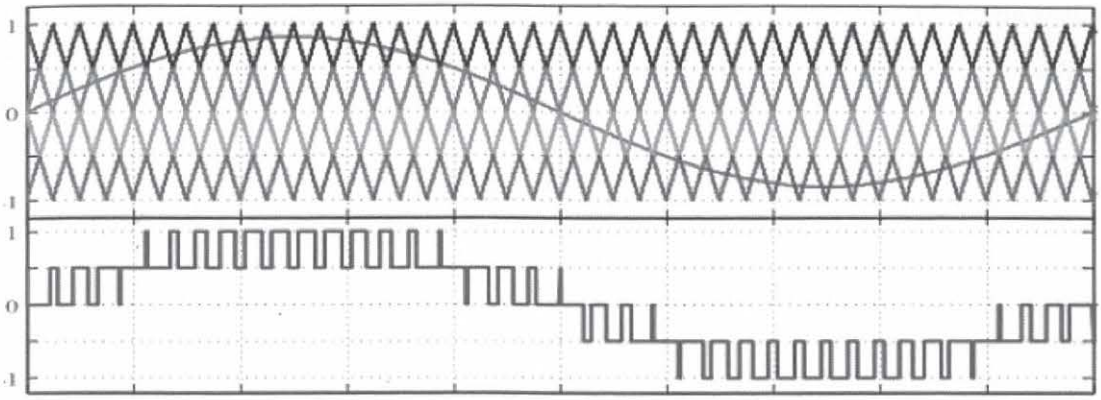

Figure 2.8 Alternative Phase Disposition[21]

Among the 3 disposition it have also been concluded from past research that phase disposition is the better one[21].

2.4 Proportional Integral Derivative Controller

A PID controller computes a slip esteem as the contrast between an intended procedure variable and a wanted set point. By adhering to the procedure through utilization of a controlled variable, the lapse is able to be minimized by the controller.

This controller calculation incorporates three different steady parameters, and as of lately and again being called the three-term control: the relative, the vital and subsidiary parameters, designated P, I, and D[22]. Basically, these parameters can be interpreted and explain in analogy as time: P relies on upon the present error, I on the amassing of past mistakes, and D is an expectation of future lapses, taking into consideration of current rate of change. All of these parameter are taken into account and used to improve the procedure via a control component. The force supplied to a warming component, the position of a control valve or a damper are among the examples.

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As a controller, PID only need to rely on the intended procedure inconsistency instead of the information on the fundamental procedure. Thus, making it a really beneficial controller[22].By manipulating any of the 3 parameters in the controller computation, the controller can give the deliberate control activity for any designated prerequisite procedure. Tuning any of the three parameters in the PID controller calculation, the controller can give control activity intended to particular procedure necessities. PID controller is can be tuned until the response of the controller is exhibited up to the point it reaches fault, a point of which the controller overshoots from its set point where the framework is quivering.

Mind that an ideal control of the framework or framework soundness cannot be guaranteed by implementation of the PID calculation[22]. From figure 2.9 shown below, the whole principle of PID can be observed.

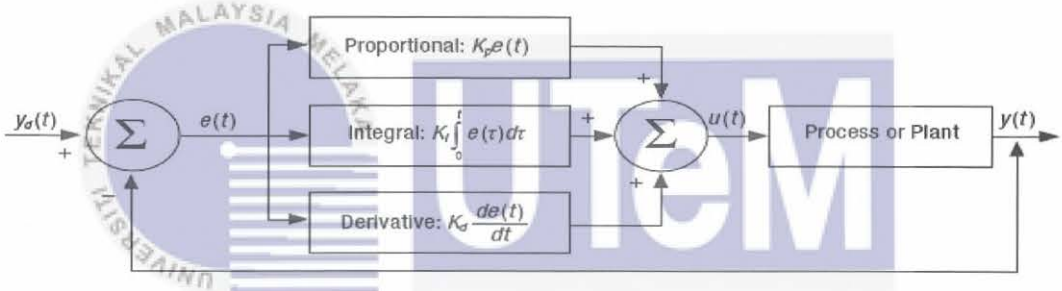

Figure 2.9 General concept of PID controller

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2.5.1 Proportional Integral (PI)

PI controller is most generally received in modern application because of its basic structure, simple to plan and minimal effort. In spite of these favorable circumstances, the PI controller falls flat when the controlled question is exceedingly nonlinear and dubious[23]. PI controller will wipe out forced oscillation and steady state error bringing about activity of on-off controller and P controller individually. Be that as it may, presenting integral mode will negatively affect speed of the reaction and generally speaking steadiness of the system. This is expected since PI controller is incapable to anticipate occurring of error in future. This issue can be unravel by presenting derivative mode which has capacity to foresee what will occur with the error in future and therefore to minimize the response time of the controller[23].

The working principle of PI can be observed from figure 2.10 next page as it shown the block diagram

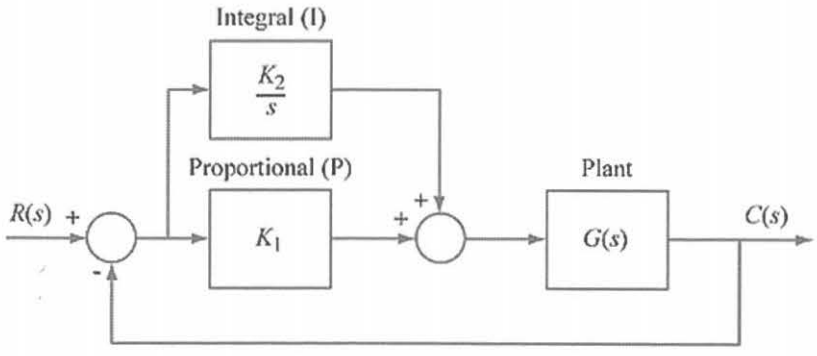

Figure 2.10 Basic principle of PI in block diagram[24]

2.5.2 Advantages and Disadvantages of PID Controller

PID controller has all the necessary dynamics: fast reaction on change of the controller input (D mode), increase in control signal to lead error towards zero (I mode) and suitable action inside control error area to eliminate oscillations (P mode) [23].Below are Table 2.3 for advantages and disadvantages of PID controller.

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Table 2.3 Advantages and disadvantages for PID and PI controller

	Advantages	Disadvantages
PI	-Basic structure. -Minimal effort required	-Require excessive stabilization. -It takes longer time to stabilize the controller gain.
PID	-Use lower resources. -Feasibility and easy to implement.	-if not tuned properly the outputs may lead to aggressive gains which may damage the whole system -Low robust ability

2.5.3 Modification of PID Controller (PI-D)

Despite the resourcefulness of PID controller. They are also bound with certain drawback. In a system where the reference input is in a step input function, there will be presence of the derivative function the manipulated variable *u(t)* of which will involve an impulse function (delta function). In an actual PID controller, instead of the pure derivative term T_{ds}, this is employed[24].

$$\frac{T_{ds}}{1+\gamma T_{ds}} \tag{2-1}$$

Where the value of γ is somewhere around 0.1.Therefore, when the reference input is a step function, the manipulated variable u(t) will not involve an impulse function, but will involve a sharp pulse function. Such a phenomenon is called set-point kick[24].

To compensate for this drawback, the derivative parameter is manipulated in the feedback path. This ensured the differentiation transpire only on the feedback signal instead of reference signal. Figure 2.11 below shown the block diagram for PI-D.

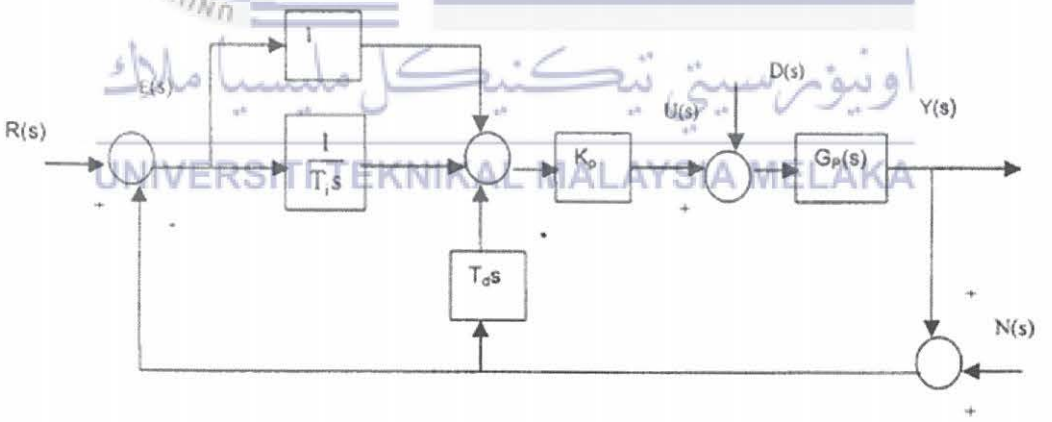

Figure 2.11 Block diagram of PI-D with derivative feedback

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2.5.4 Modification of PID Controller (I-PD)

There are variety of altered version for PID controller, one of them is the I-PD controller. The deviation from original design is to minimize the significant drawbacks of the parallel PID controllers of which are mainly contributed from proportional and derivative or set-point kick and reduce undesirable overshoot[25].

By implementing this design significant change from the reference input R(s) will not affect the proportional K_p and derivative K_d since only the integral term Ki responds on the error signal E(s). The different in time domain function and block diagram is shown in figure 2.12 and 2.13 equations below. Table 2.4 next page shown result from both controllers PID and I-PD[25].

$$u(t)\Big|_{PID} = K_p e(t) + K_i \int e(t)dt + K_d \frac{de(t)}{dt}$$

$$u(t)\Big|_{I-PD} = K_i \int e(t)dt - \left(K_p c(t) + K_d \frac{dc(t)}{dt} \right)$$

Figure 2.12 Time domain equation for PID and I-PD controller [25].

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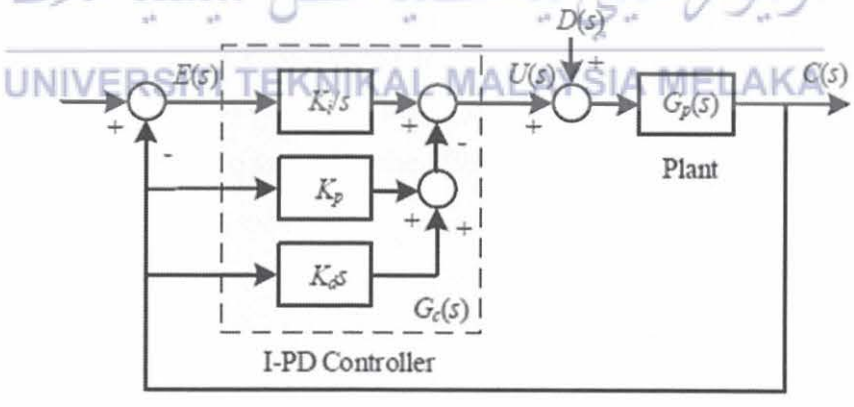

Figure 2.13 Block diagram for I-PD controller

Table 2.4 Result from PID and I-PD controller [25]

Controllers	Parameters			System responses				
	K_p	K_i	K_d	t_r(sec.)	t_s(sec.)	M_p(%)	E_{ss}(%)	t_{reg}(sec.)
PID	59.6745	464.4714	1.2445	0.0202	0.2029	9.4367	0.0000	0.2245
I-PD	24.7789	542.7411	0.3704	0.0841	0.2141	4.2264	0.0000	0.1654

From table 2.4 above, it is shown that I-PD give significant better response than that of parallel PID with smaller overshoot and rapid regulating time [25].

2.6 Summary

As shown from all of the above literature review above there are variety of multilevel inverter with its own aspect of topology and distinct features. The most common being applied in industry are the cascaded H-Bridge, Diode clamp and Flying capacitor multilevel inverter of which all have been discussed in this chapter about its basic feature in term of topology, significant difference between each other. All of this MLI also posed their own pros and cons. SPWM control technique is also the preferable technique mainly because of its advantageous trait that have been discussed in this chapter. PI controller is utilizing because of its straightforward and robustness. Modified PID is also employed out of its practicality than that of conventional PID and also to reduce the effect of set-point kick.

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CHAPTER 3

METHODOLOGY

3.1 Introduction

This chapter discussed the method applied for the completion of this project and the flow throughout of project being enacted until completion. From past journal studies and fundamental theory, reviews. Cascaded H-bridge multilevel inverter is implemented in this project. From past journal, working principle of each component and the role it played the project are also discussed.

The controlling technique for the multilevel inverter is also suggested in the methodology where a sinusoidal pulse width modulation (SPWM) with single carrier but 4 sinusoidal wave is applied. SPWM is implement as a control and gating system for the metal-oxide-semiconductor field-effect transistor (MOSFETs) from the CHMI

In order to achieve the result as per required, a simulation need to be made so as to inquire the voltage output waveform. For that, MATLAB/Simulink is applied so that all of the circuit can be design and simulate. From the output waveform analysis can be made on the performance based on total harmonic distortion and power factor. This is particularly applied for objective 1 and 2 in this project which is also mainly on the open loop system.

For objective 3 and 4, a closed system is used where there is feedback controller applied. The feedback that have been suggested are the PI and the modified PID controller. All of the controller will be analyse it its performances and compared with each other.

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3.2 Project Procedure

For this project, system development life cycle which is a system used to ensure a flow when doing a project or experiment is embedded into the project so as to ensure a structured methodology. It is a series of phases activity arranged in cyclic circle so that any improvement can be made. The phases are analysis, design, implementation, maintenance and planning. However, maintenance phase is redundant for this project, therefore only 4 phase are implemented into this project.

Planning phase are the phase where groundwork project is being lay upon. This is phase where journal reading, past research studies is being done. This is crucial as the data from past studies can be employed for this project. Next phase is the analysis phase. This is where the performance of 5-level cascade h-bridge multilevel inverter (CHMI) with sinusoidal pulse width modulation (SPWM) is analysed based on the total harmonic distortion and power factor. This is also where the phase where the feedback controller of PI and modified PID performance analysed.

Design phase is the phase where designing or improvement of CHMI topology being made along with calibration of the parameter such as the switching specification. This is also the phase where feedback controller is designed and tuning for the system or if the result in the analysis is not achieved accordingly with the objective, the project cycle will return to this phase so that an improvement can be made.

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Implementation are where the phase where feedback controller being implemented into the CHMI system and their respective performance can be analysed. Figure 3.1 below shown the system development cycle.

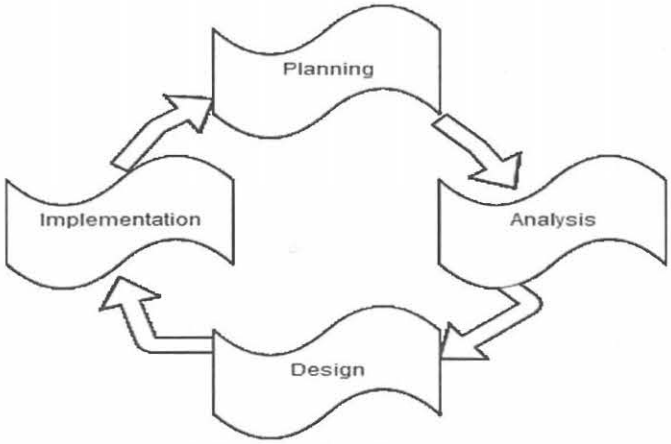

Figure 3.1 System development life cycle

For figure 3.1 from previous page shown that system development life cycle has 4 phases which is planning, analysis, design and implementation all in a cycle so that any improvement can be made.

3.3 Project Process Background and Flow

From the flowchart in figure 3.2 shown above, the project can be reviewed in a few steps, the first one would past research, basic fundamental understanding of the whole working principle involved in the project. From all of that, the working principle of CHMI is enacted. Next implementation of the modulation/control technique where SPWM with one carrier waveform and multiple vertically shifted sinusoidal waveform method is applied into 3-phase 5 level CHMI using MATLAB/Simulink software, from the output of Simulink simulation, THD output of the voltage and the power factor analysed from the comparison of voltage and current waveform.

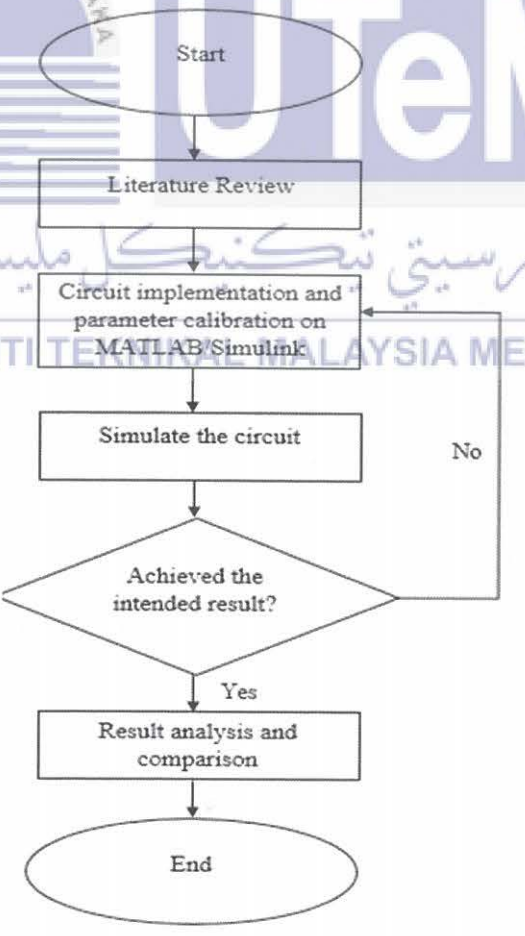

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Figure 3.2 Project Flow and Summary

As shown from Figure 3.2, a feedback controller will then be designed and implemented into the circuit. The performance of the system will then be analysed and compared along with PID and PI controller performance. All of the simulation will be done by using MATLAB/Simulink.

3.4 System Flowchart for Open Loop and Close Loop

Figure 3.3 below shown the flowchart for open loop system which is without the feedback controller the system for open loop without the feedback controller. The system begins with project research, designing the circuit and parameter implementation. The circuit is then simulating and the result is analysed.

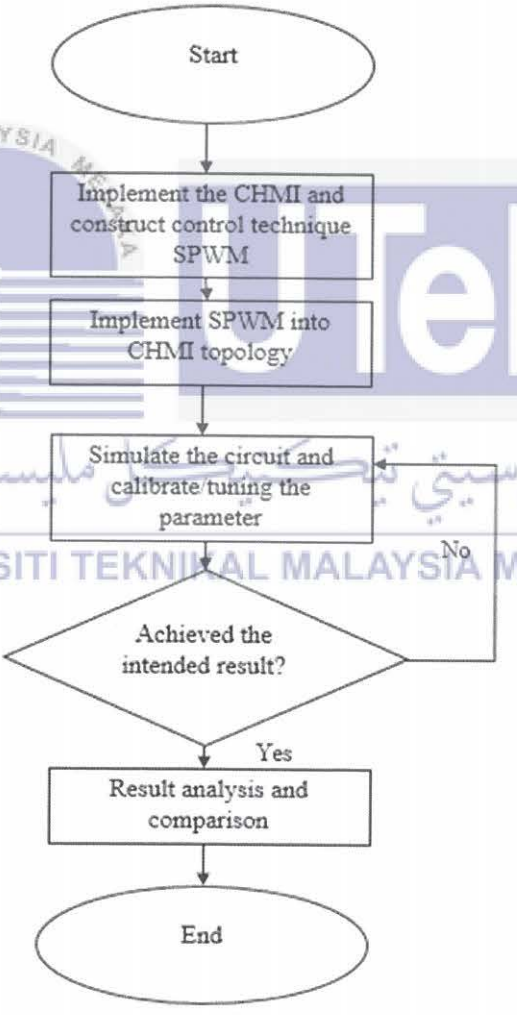

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Figure 3.3 Project flow without feedback control

For flowchart from figure 3.4 shown below, it is almost the same except it have a feedback controller which is the PI and the modified PID controller, both of the performance with respective controller are analysed and compared.

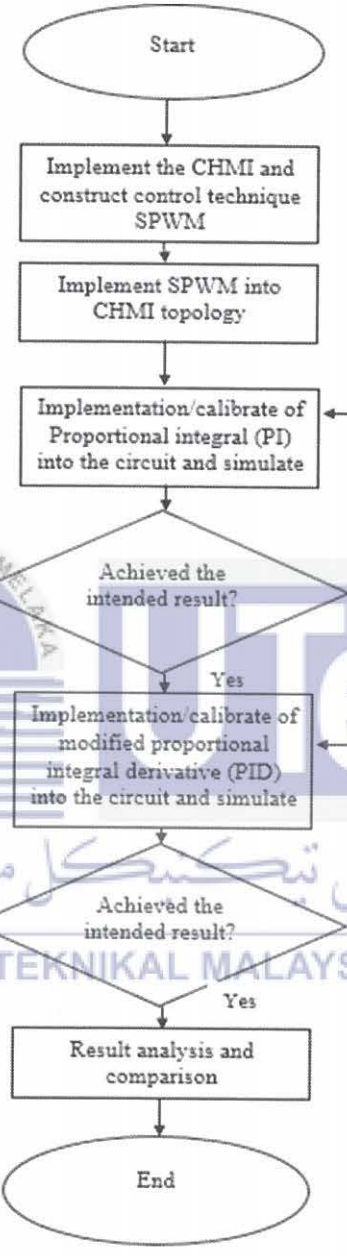

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Figure 3.4 Project flow with feedback control

3.5 Basic Working Principle of Cascaded H-Bridge Multilevel Inverter (CHMI)

Basically inverter is a device that convert power from dc to ac. In this project however 3 phase 5-level CHMI is implemented as shown in figure 3.5 below using MATLAB/Simulink to acquired voltage output, total harmonic distortion (THD) and power factor. Topology of CHMI are 2 H-bridge cells that are arranged in series. The structure of H-bridge consists of 4 switches and separated dc source. For this project however there will be 3 phase 3 H-bridge with each of the bridge having separate dc source. Since it have 2 separated dc source, voltage output of CHMI is the resulting of $v_1 + v_2$ or

$$V_{output} = V_1 + V_2 \tag{3-1}$$

Where v_1 is the upper leg of output voltage and v_2 is the lower leg of output voltage. The structure of the leg is as shown in figure 3.5.

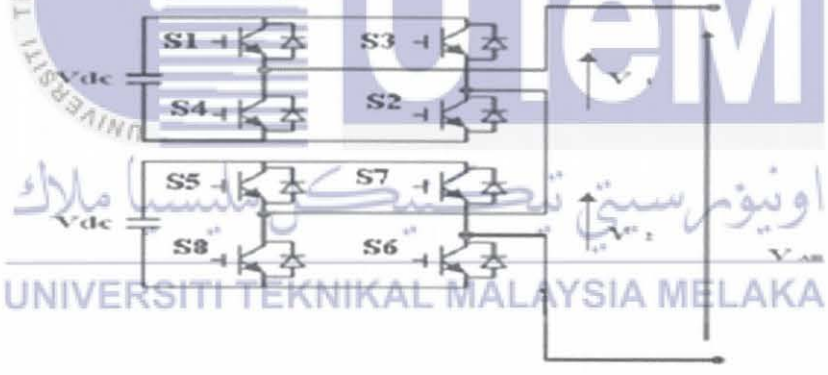

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Figure 3.5 Single phase 5-level CHMI

Noted that since this is a 5-level multilevel inverter, its voltage output would be in a 5 level waveform forming a staircase like waveform for its line to line voltage where the voltage are as follow $v_1, v_2, v_3, -v_1$, and $-v_2$. The output voltage v_1 for upper H-bridge and v_2 for lower H-bridge is shown in table 3.1 below. It is also the switching for the 5-level multilevel inverter.

Table 3.1 Voltage level and switching for 5-level CHMI.

Switches turned on	Voltage level
S1 and S2	V_{dc}
S1 , S2 and S5 , S6	$2V_{dc}$
S4 , S2 and S8 , S6	0
S3 and S4	$-V_{dc}$
S3 , S4 and S7 , S8	$-2V_{dc}$

Figure 3.6 below shown the design for 3-phase 5-level with SPWM for CHMI in this project where the switching of SPWM is in the 3 mask. Each of the inverter block consist of 4 switches. The circuit are also a resistive circuit since it has resistor as load and also consist of low pass inductance and capacitance filter.

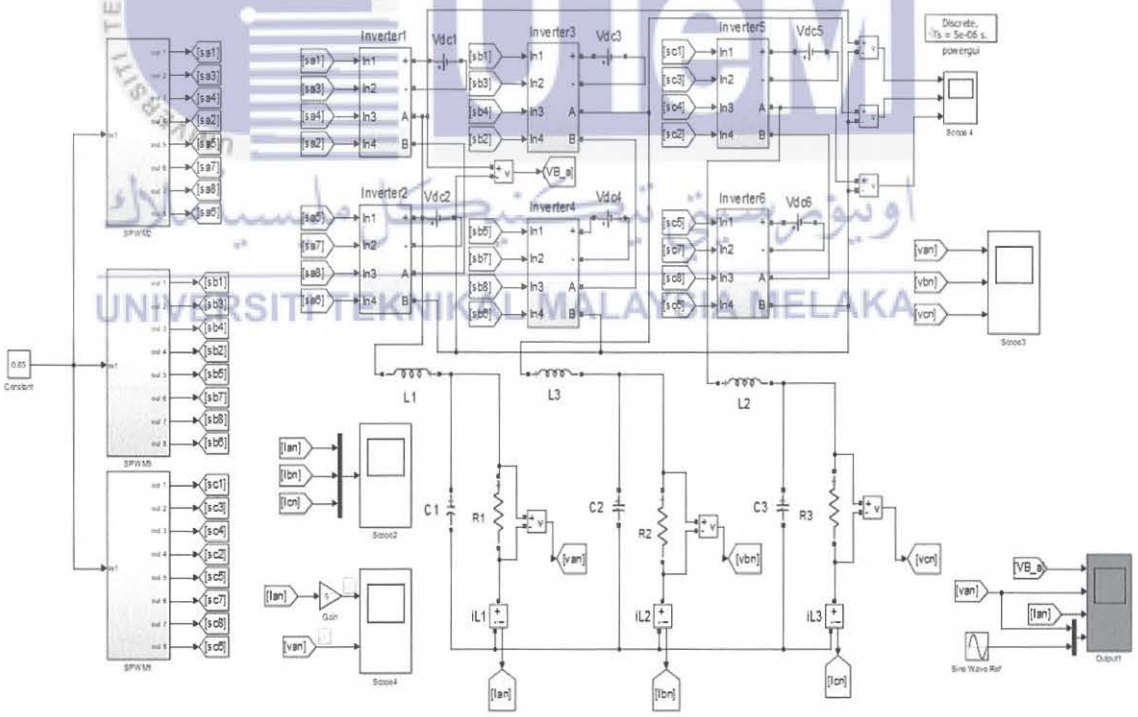

Figure 3.6 3 phase 5 level Cascaded H-Bridge Multilevel Inverter Design

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The upper leg structure and lower leg structure for H-bridge is as shown in figure 3.7 and figure 3.8 below.

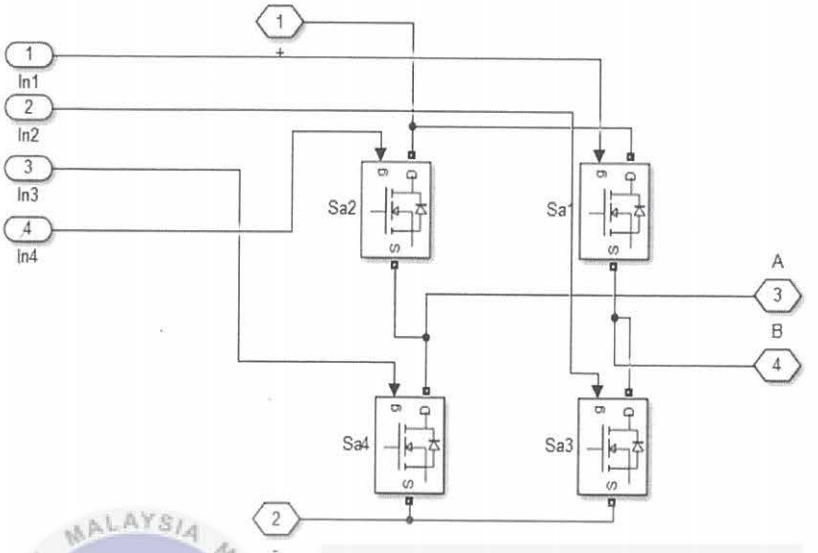

Figure 3.7 Upper leg H-Bridge for 5 level CHMI

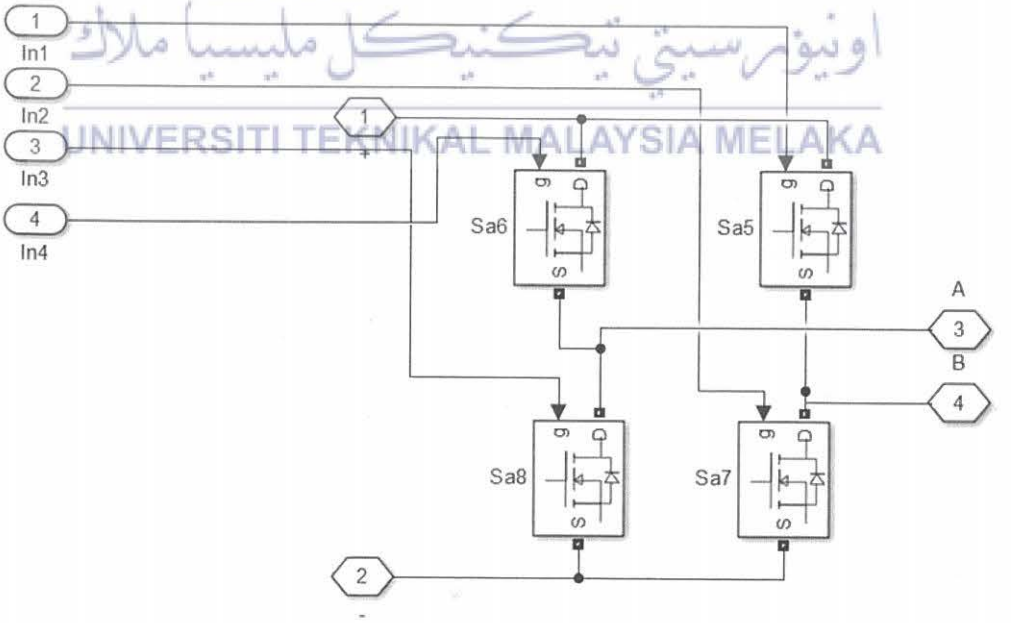

Figure 3.8 Lower leg H-Bridge for 5 level CHMI

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3.6 .The Switching Strategy for 3-phase 5-level CHMI

For CHMI in this project, modulation/control technique applied is the sinusoidal pulse width modulation (SPWM) technique where the on and off of the pulse logic gate is based on the comparison of triangular wave and sinusoidal wave. For this project however, single triangle waveform will be compared with 4 sinusoidal waveforms. All of the switching waveform is shown in figure 3.9, 3.10 and 3.11 below. To calculate the number of output voltage levels, formula shown below can be used.

$$n = 2m + 1 \tag{3-2}$$

Where m is the voltage dc source,

The sinusoidal waveform is vertically shifted with 2V, +1V and -1V. For this project the triangular carrier is compared with 4 sinusoidal waveforms, however the basic principal for the switching are still the same. The switching and comparison between of the triangular and sinusoidal waveform can also be expressed as the following below.

The pulse logic gate will be '0' if $V_{r,1} \leq V_{tri}$

The pulse logic gate will be '1' if $V_{r,1} \geq V_{tri}$

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Table 3.2 and 3.3 below shown the parameter used in this project and the parameter for the switching method. All of the respective component parameter is tuning in the MATLAB/Simulink.

Table 3.2 Parameter of the system

Parameter (load)	**Value**
Resistance, R (R_1, R_2, R_3)	10Ω
Parameter (Filter)	Value
Inductance, L (L_1, L_2, L_3)	150mH
Capacitance, C (C_1, C_2, C_3)	220μF

Table 3.3 Parameter for the switching method (SPWM)

Parameter	Value
Switching frequency	1kHz
Frequency reference signal	50Hz
Phase(rad)	0, -120*$\frac{\pi}{180}$, -240*$\frac{\pi}{180}$
Modulation index	0.85

Figure 3.9 below shown the switching scheme SPWM for the CHMI applied in this project and Figure 3.10, 3.11, 3.12 below shown the carrier wave which is the triangular wave with the reference wave or the sinusoidal wave in 3 phases.

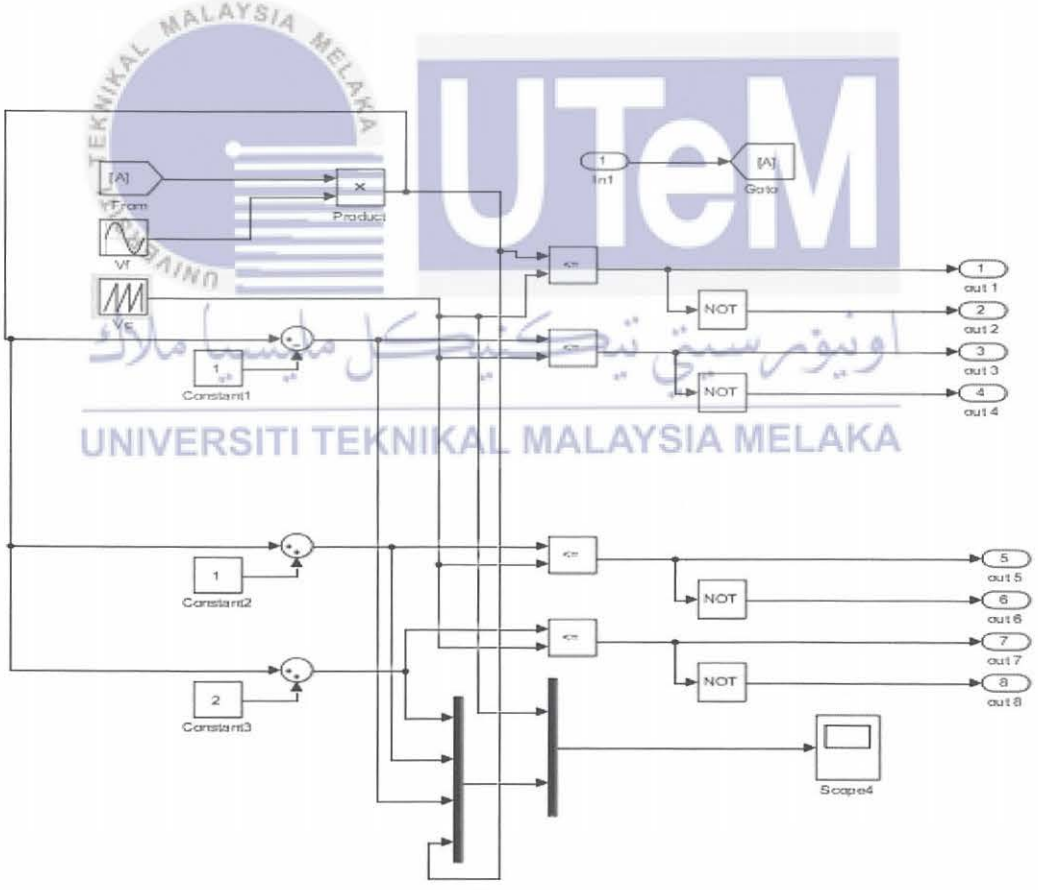

Figure 3.9 MATLAB/Simulink circuit for switching scheme

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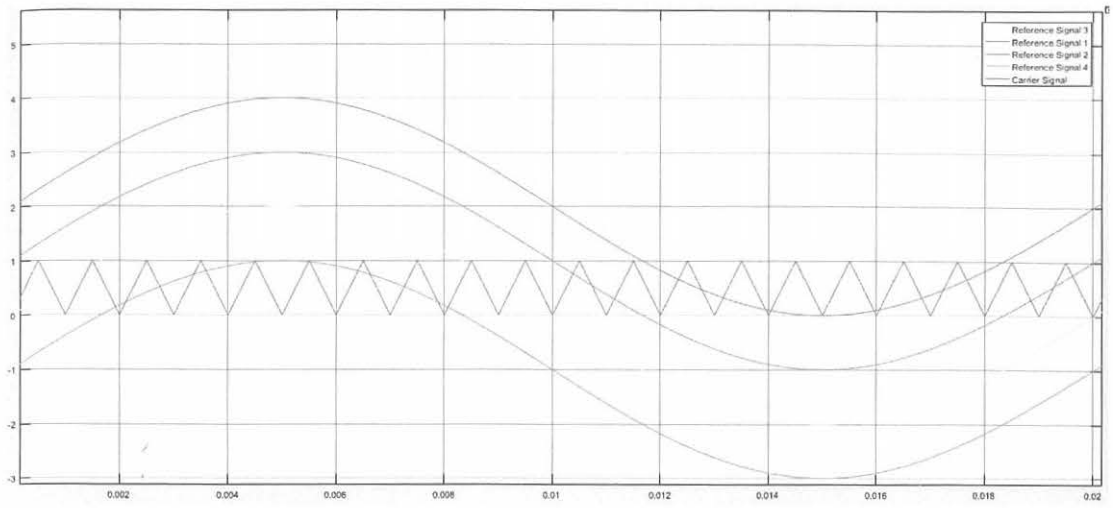

Figure 3.10 The sinusoidal waveform and the single traingular carrier waveform for $V_{a,1}$

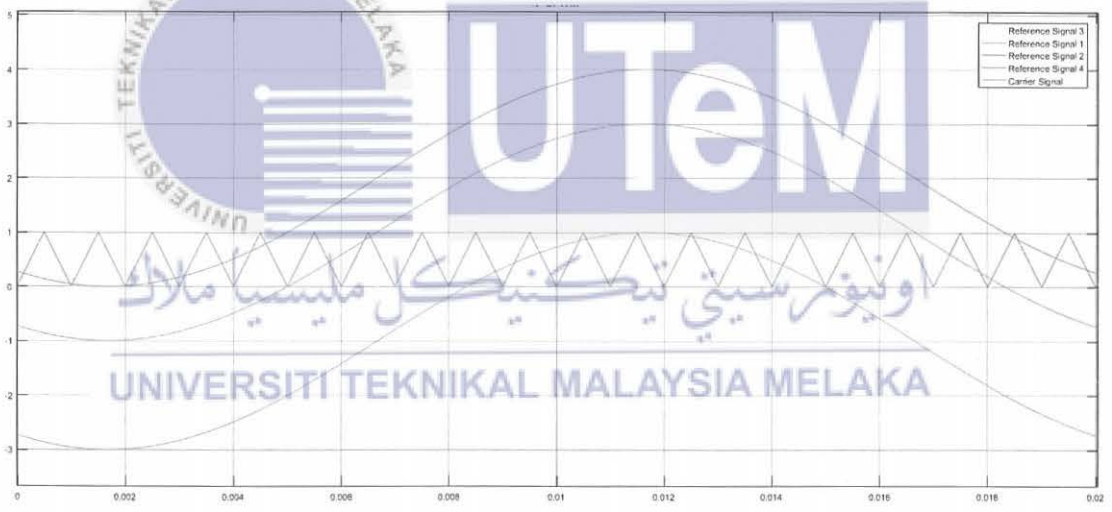

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Figure 3.11 The sinusoidal waveform and the single triangular carrier waveform for $V_{b,1}$

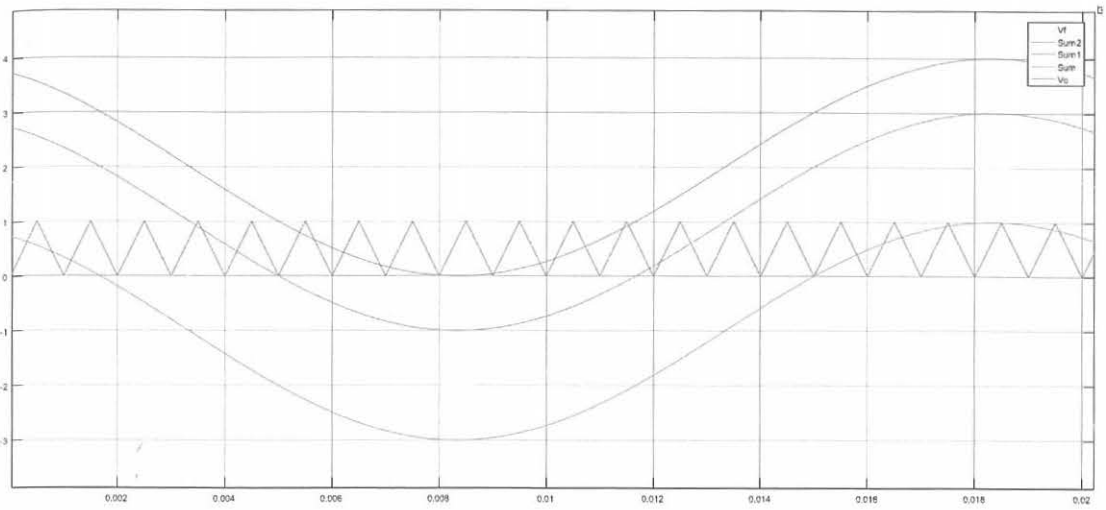

Figure 3.12 Thes sinusoidal waveform and the single triangular carrier waveform for$V_{c,1}$

3.7 Designing of Proportional Integral (PI) Controller

Designing of the PI controller began with the obtaining of the transfer function from the system circuit diagram through using the general equation of the second order system. From the acquired and calculated transfer function, it is then simulate on the MATLAB to observe the transient response of the uncompensated system. After observing the transient response, the system will then be tuned to obtain the desired state. Mostly involving a trial and error to obtain the most suitable state. Then, the compensated system is obtained by adding a zero pole to obtain the compensated system equation for PI controller. Figure 3.13 below shown the circuit involved to obtain the transfer function.

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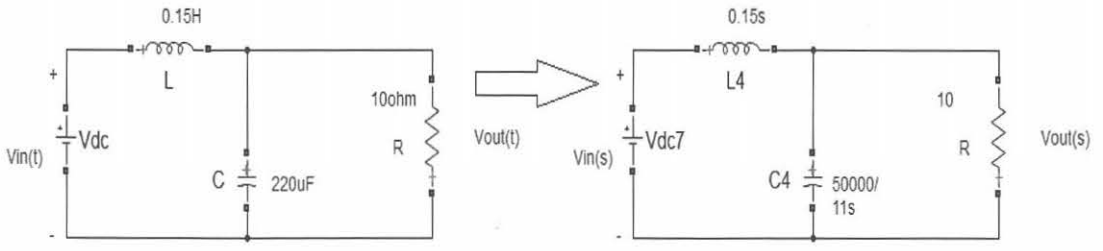

Figure 3.13 Simplified circuit used to obtain the transfer function

The circuit are then calculated by using the general equation for second order system as shown in the equation 3-3, 3-4 and 3-5 which is then obtained and calculated of which can be observed as transfer function below.

$$G(s) = \frac{V_2(s)}{V_1(s)} \tag{3-3}$$

$$G(s) = \frac{\omega_n^2}{S^2 + 2\xi\omega_n S + \omega_n^2} \tag{3-4}$$

$$G(s) = \frac{50000}{1.65S^2 + 750S + 50000} \tag{3-5}$$

From the calculated equation. The transfer function is then run through MATLAB using the root locus tool (RLTOOL) to observed the transient response of the uncompensated system. Figure 3.14 and 3.15 below shown the transient response with rltool and the designing of the compensated system.

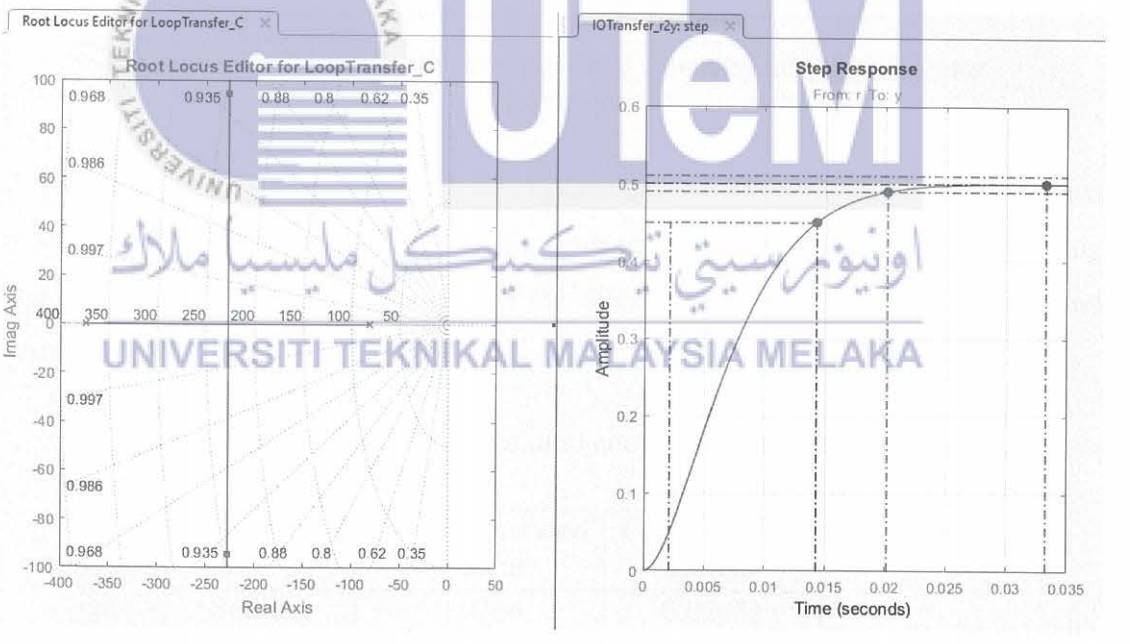

Figure 3.14 Root locus tool editor for the transfer function of the system

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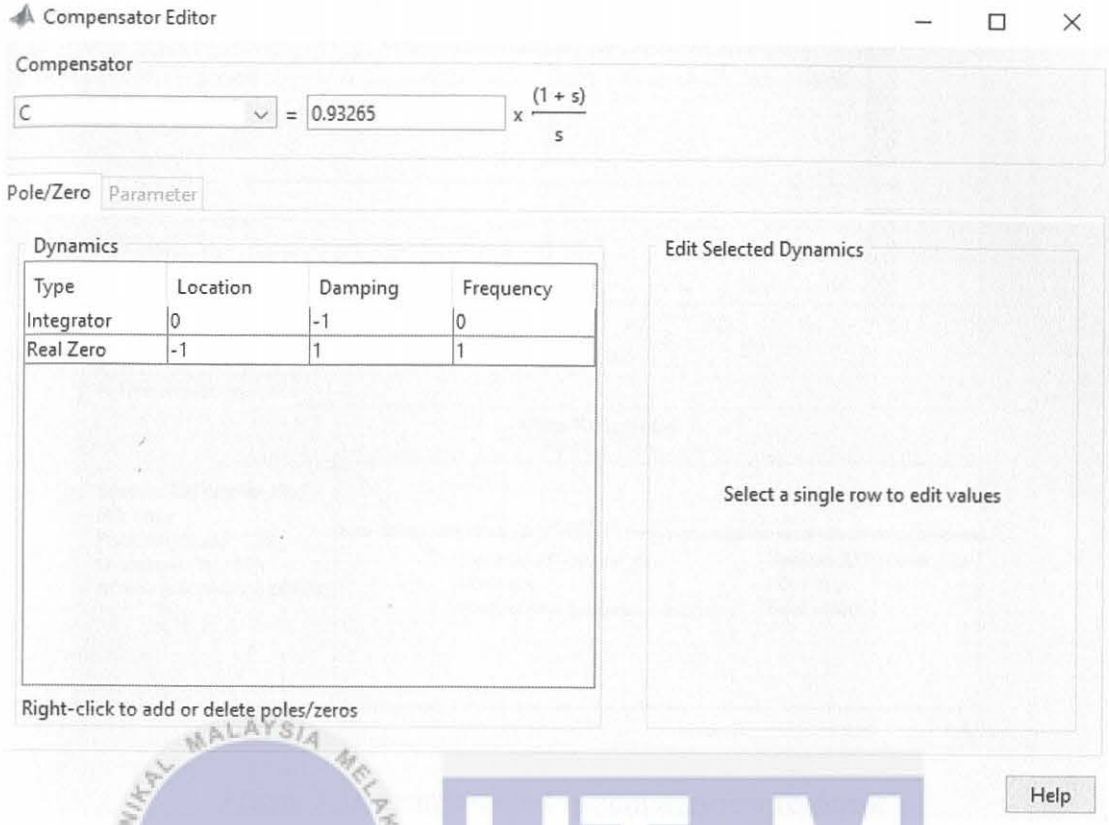

Figure 3.15 Designing the compensated sytem by adding integrator and zero pole

For designing of the compensated system several characteristic of the intended is set up such as the settling time, steady state error and overshoot from the existing one condition. Table 3.4 below shown the difference between uncompensated and compensated system.

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Table 3.4 Uncompensated system and compensated system

	Uncompensated system	**Compensated system**
Settling time,T_s	0.0246	0.0203s
Steady state error,e_{ss}	0.57	0
Overshoot	0%	37.1%

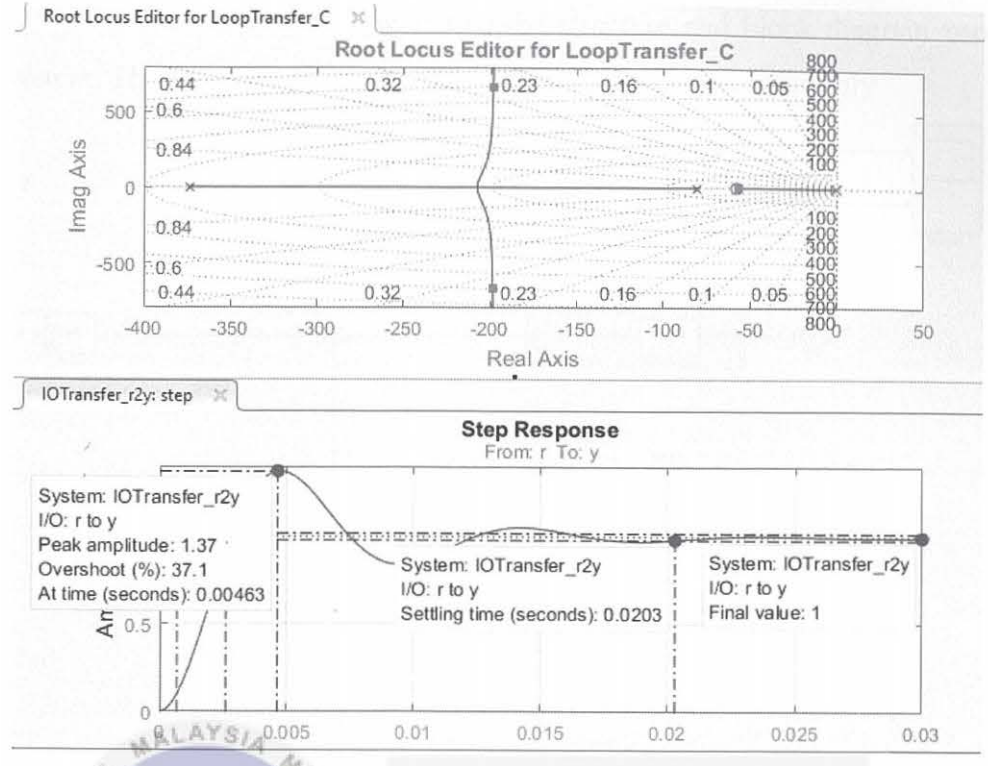

Figure 3.16 Compensated system transient response

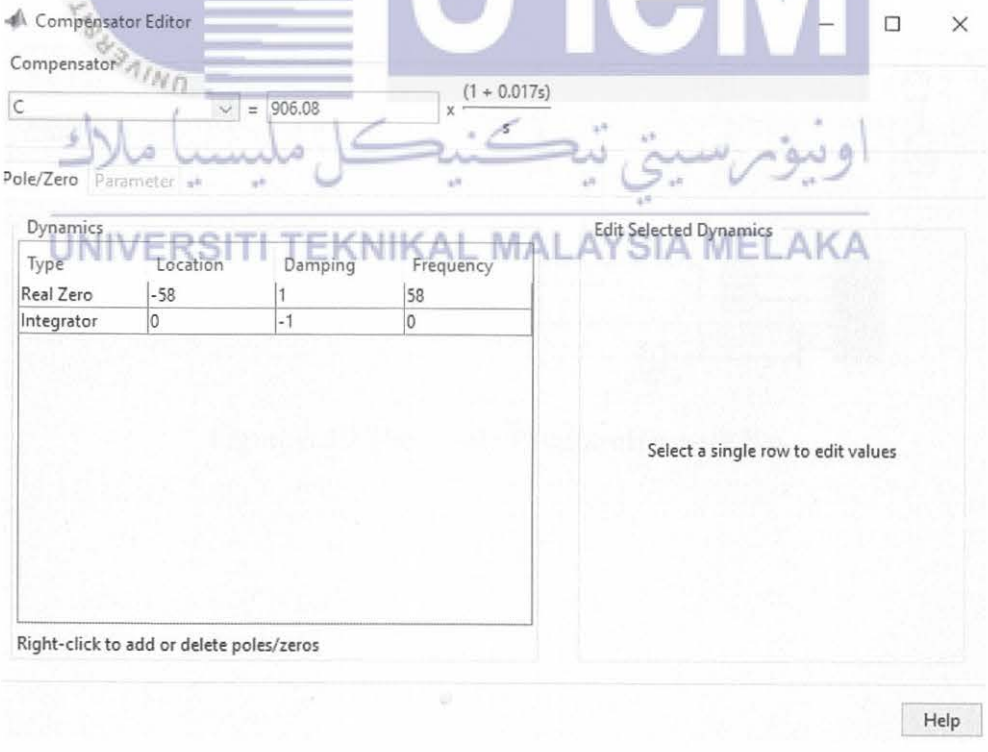

Figure 3.17 Compensator editor for the system with the calculated real zero

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Figure 3.18 and 3.19 below shown the structure and block diagram used for this system. The rms block diagram are to ensure the value are rms only

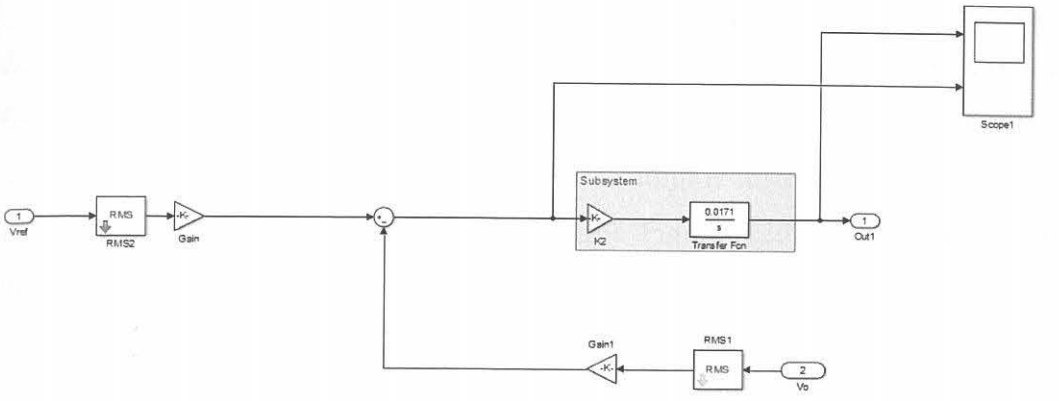

Figure 3.18 Ki and integrator of PI controller inside the subsystem

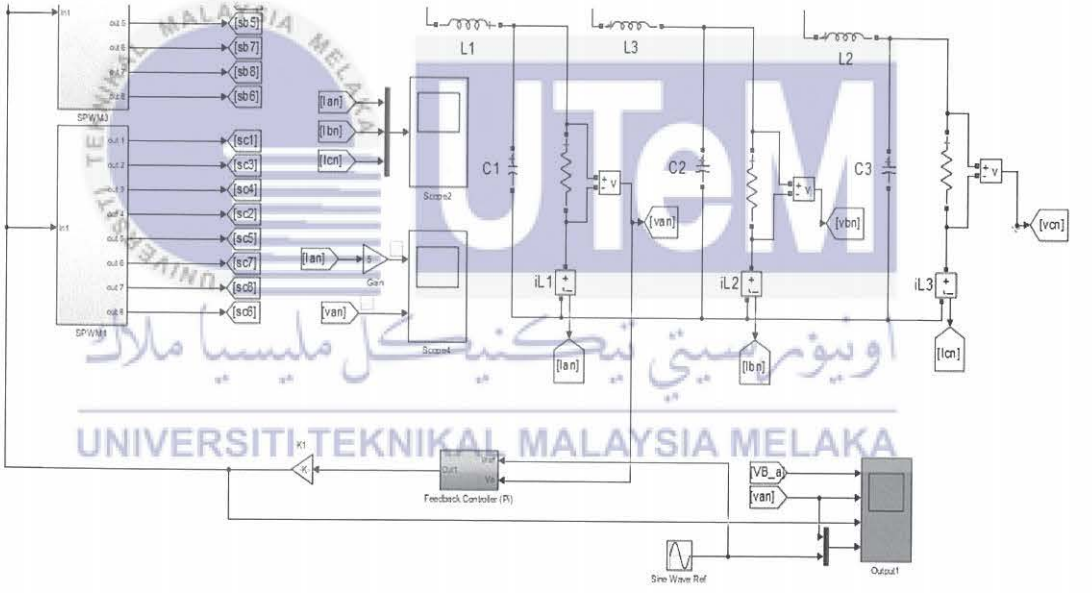

Figure 3.19 The whole Pi controller with Kp

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3.8 Designing of I-D Controller

To avoid the set-point kick phenomenon, it is important to operate the derivative action only in the feedback path so that differentiation occurs only on the feedback signal and not on the reference signal. In an actual PID controller instead of the pure derivative term $T_d s$, below equation is employ instead. The control scheme arranged in this way is called the PI-D control. Figure 3.20 and 3.21 below shown the block diagram for PID system.

$$\frac{T_{ds}}{1 + \gamma T_{ds}} \tag{3-6}$$

Where the value of γ is somewhere around 0.1

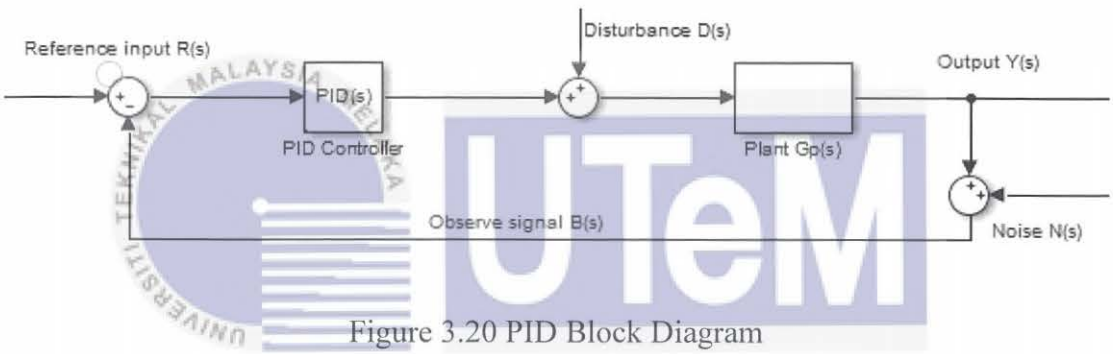

Figure 3.20 PID Block Diagram

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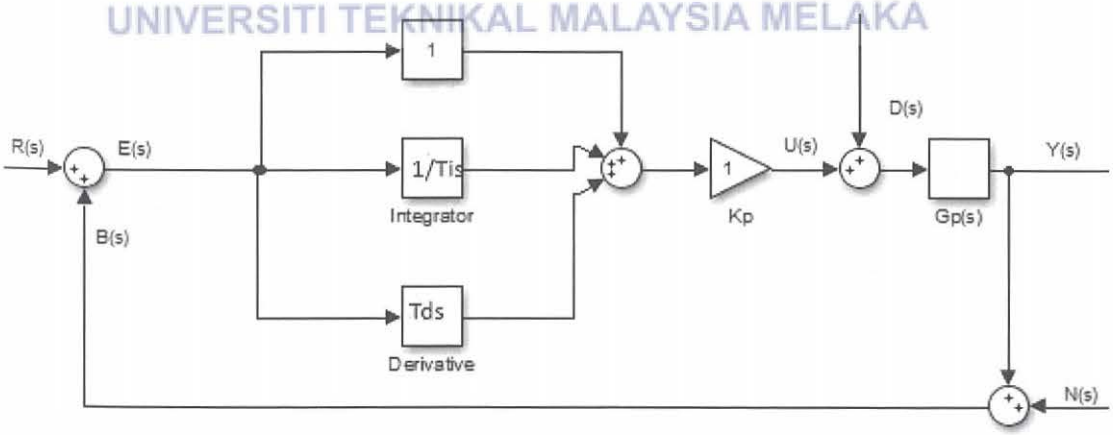

Figure 3.21 Equivalent Block diagram

In the absence of the disturbances and noises, the closed-loop transfer function of the fundamental PID control system as shown in figure 3.21 above and the PI-D control system as shown in figure 3.22 below are given respectively by

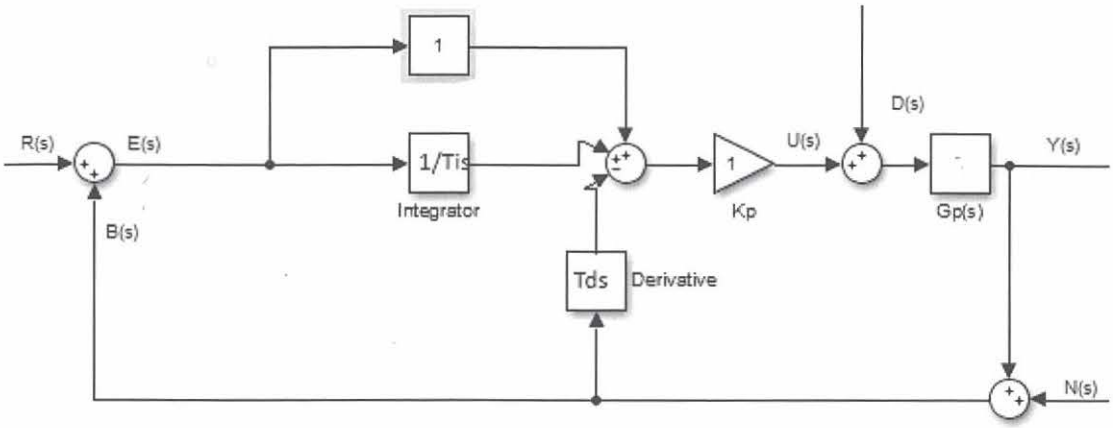

Figure 3.22 PI-D control system

$$\frac{Y(s)}{R(s)} = (1 + \frac{1}{T_i s} + T_d s)\frac{K_p G_p(S)}{1+(1+\frac{1}{T_i s}+T_d s)K_p G_P(s)} \quad (3\text{-}7)$$

And

$$\frac{Y(s)}{R(s)} = (1 + \frac{1}{T_i s})\frac{K_p G_p(S)}{1+(1+\frac{1}{T_i s}+T_d s)K_p G_P(s)} \quad (3\text{-}8)$$

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It is crucial to identify that in the absence of the reference input and noises, the closed-loop transfer function between the disturbance D(s) and the output Y(s) in the either case is the same and is given by.

$$\frac{Y(s)}{D(s)} = \frac{G_p(S)}{1 + K_p G_P(s)(1 + \frac{1}{T_i s} + T_d s)} \quad (3\text{-}9)$$

Figure 3.22 and 3.23 below shown the modified PID block diagram employ in the project

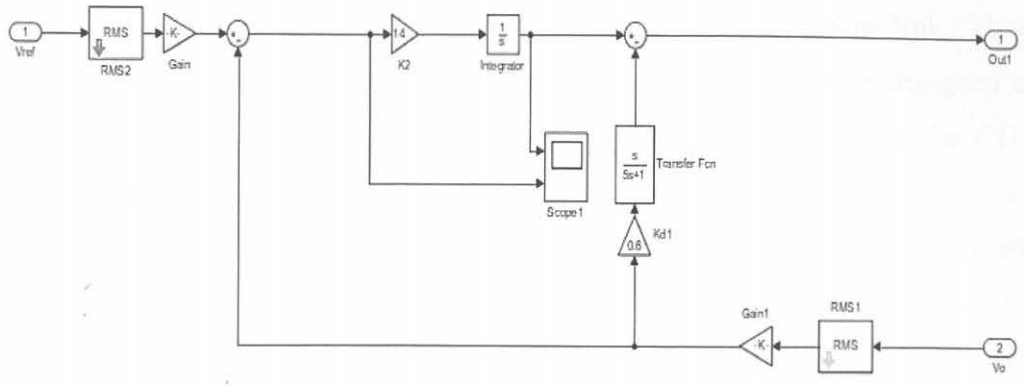

Figure 3.23 Modified PID structure

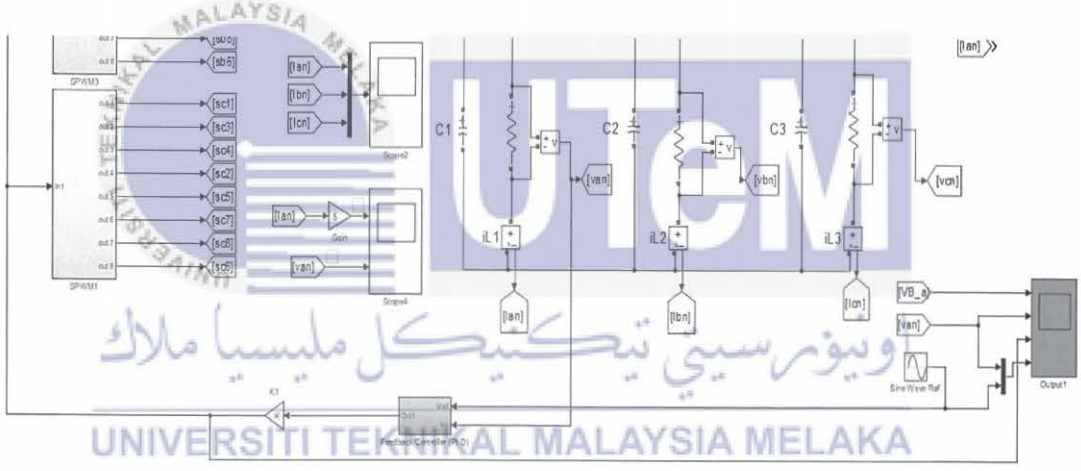

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Figure 3.24 Whole modified PID structure

The whole designing of the modified PID is a trial and error process that are involving several step. The first one is to choose the value of the T_d. Then the value of T_d will be multiplied with the γ which is a constant value of around 0.1. Next the tuning value of K, the effect of increasing K will be a faster response but also having high overshoot while decreasing the K will have a slow response and low overshoot. The steps are repeated until a proper output is obtained.

3.9 Summary

This chapter discuss the flow and how the project being executed. Which are the circuit and block diagram set up and built with MATLAB/Simulink. This is where the 3-phase 5-level cascaded h-bridge multilevel inverter were designed and implemented into the Simulink. There is also basic working principle for CHMI being explained in this chapter.

Next, with the implementation of Sinusoidal Pulse Width Modulation (SPWM) into CHMI as it controls technique for the gating signal. Basic working principle of the technique is explained such as the comparison of the single triangular wave and the 4 sinusoidal wave. Circuit for the SPWM are also shown in this chapter along with the parameter of the load, system and the SPWM.

The controller is lastly implemented in this chapter where the PI controller are designed, calculated and tuning in order to obtain the desired condition for the system. Then a modified version of the PID controller, which is the PI-D controller are designed where its working principle are explained and its structure are also shown in this chapter.

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CHAPTER 4

RESULTS AND DISCUSSIONS

4.1 Introduction

This chapter shown the result from all of the software implementation of the 3 phase 5-level CHMI with SPWM control technique by using MATLAB/Simulink. The result without feedback and with feedback control are also shown and discussed in this chapter. The results are in the form of voltage output, THD of the voltage output and voltage. All of the result of which will be analysed accordingly with the objective

4.2 Modulation Technique Using SPWM Switching Strategy by Comparing 1 Carrier and 4 Sinusoidal Wave

This switching strategy fundamental working principle is by comparing sine wave with carrier wave. For this project this switching technique is implemented into 3-phase 5-level CHMI where,V_c,V_r as the triangular wave and the reference wave, these are the signals involved for this switching method. However, in this project, there are 4 reference signals being compared with carrier signal. The 3 reference signal is the result of the original reference signal being shifted along the y-axis. V_{r2} is the result of V_r being shifted positively along y-axis by 2 units while V_{r3} is the result of V_{r2} being shifted positively by 1 unit along y-axis. V_{r4} is the only quite different as it is shifted negatively along y-axis by 1 unit. Figure 4.1 below exhibit the switching strategy and the 4 signal is represented as in the equation below.

$$V_{r2} = V_{r1} + 2 \quad (4\text{-}1)$$

And,

$$V_{r3} = V_{r2} + 1 \quad (4\text{-}2)$$

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And

$$V_{r4} = V_{r1} - 1 \tag{4-3}$$

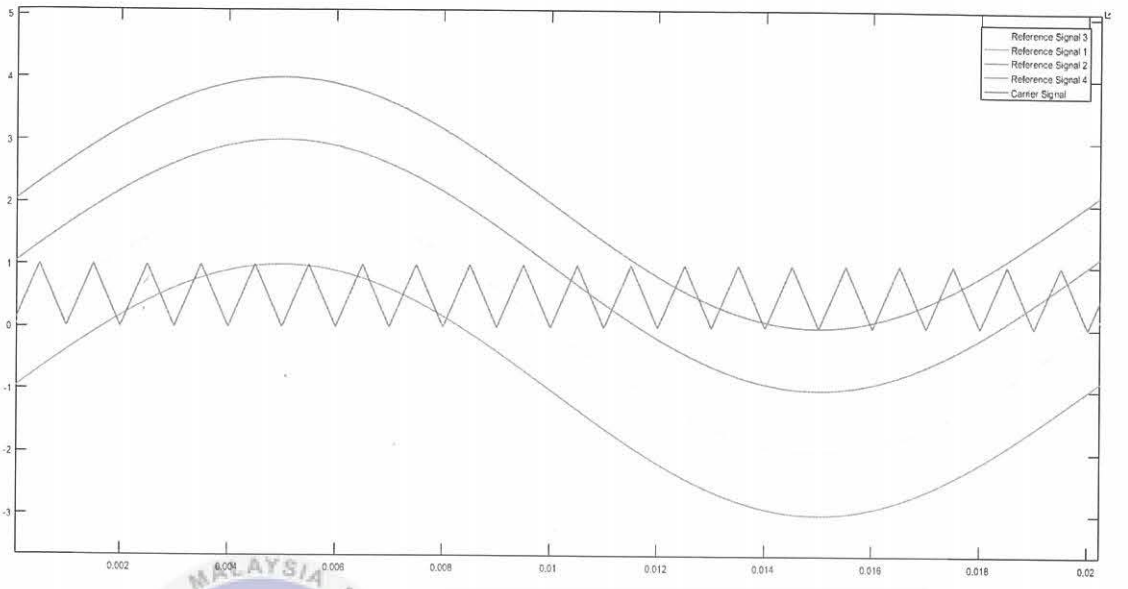

Figure 4.1 Switching Used for 3 phase 5 level CHMI

4.3 Simulation Result

This section present detailed description of the simulation output. In this project, the CHMI is simulated using MATLAB/Simulink. The result shown are the voltage output of the system with filter and without filter. Moreover, total harmonic distortion (THD) and power factor are also shown. The simulation shown 3-phase 5-level multilevel inverter with SPWM switching strategy and simulation of the CHMI with feedback controller.

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4.3.1 3-Phase 5-level Cascaded H-bridge Multilevel Inverter (CHMI)

From the implementation of the topology applied and the SPWM switching scheme. Figure 4.2 below the switching for all switches available which is S1 to S8. All of it are from the 2 cell connected in series with each cell consists of 4 switches. Since there are 8 switches, it is inferred that 8 signals are required to activate and triggering the switch.

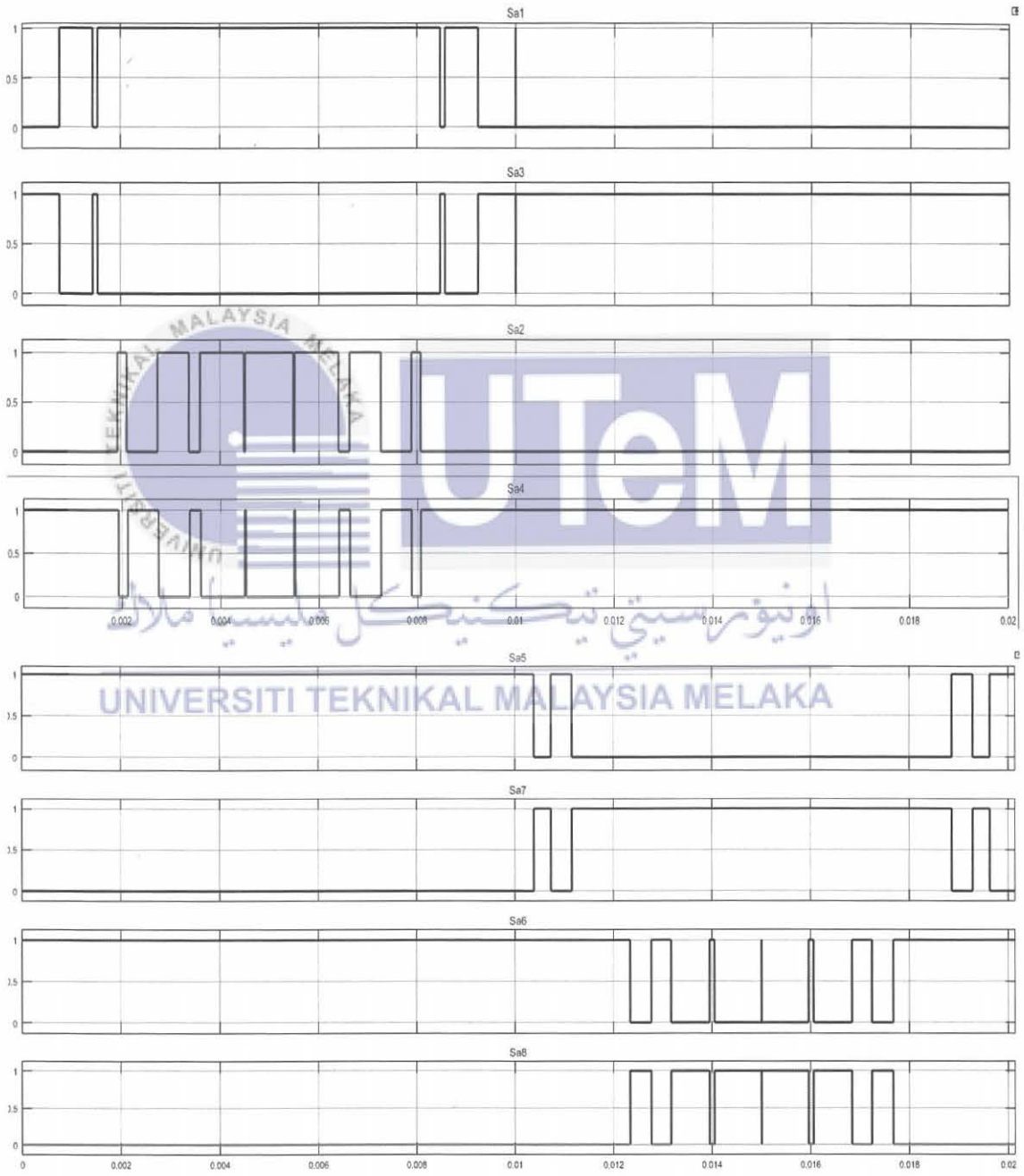

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Figure 4.2 Switches result from SPWM control structure

For the first half of the cycle switches S1 and S2 need to operate at the same time while for the next half cycle S5 and S6 will simultaneously operate. The working principle is the same for the second cell

4.3.2 3 Phase 5 Level CHMI Without Low Pass Filter

Figure 4.3 below shown the result for 3-phase 5-level CHMI. Since this is 5 level multilevel inverter, there are five output voltage level forming a staircase look-alike pattern. The voltage are V_0, V_1, V_2, $-V_1$, $-V_2$ where each of the respective voltage have their own value. The value each of the voltage level are as follow $V_0 = 0, V_1 = 1527V$, $V_2 = 3040V$. This however, is the waveform without filter. A filter is added to minimise THD and produce a more sinusoidal waveform. The THD shown without LC filter and load is 16.83%.

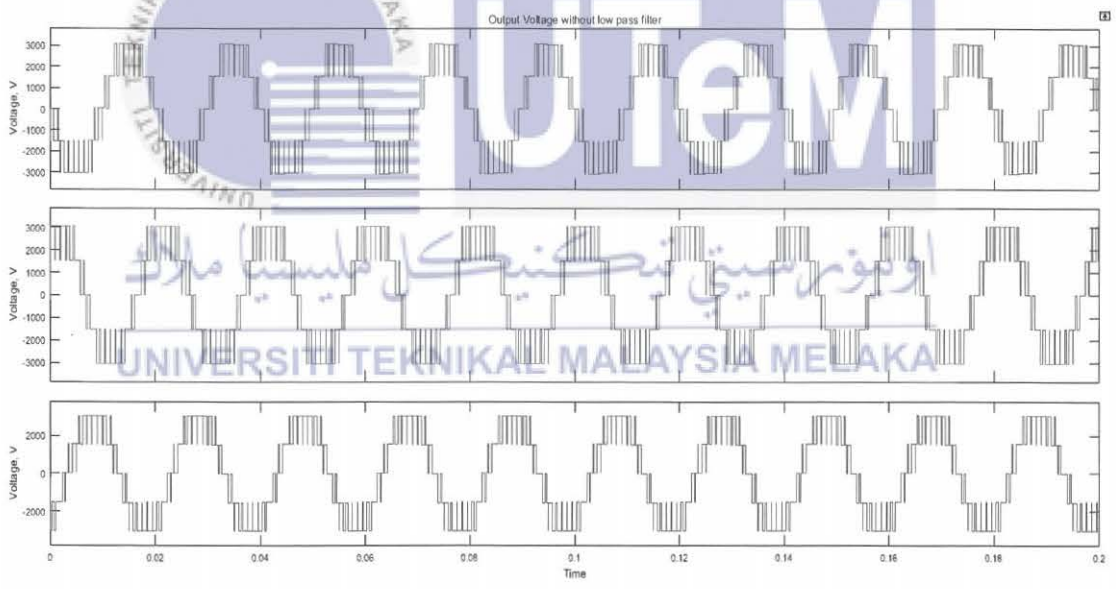

Figure 4.3 Output voltage without lowspass filter

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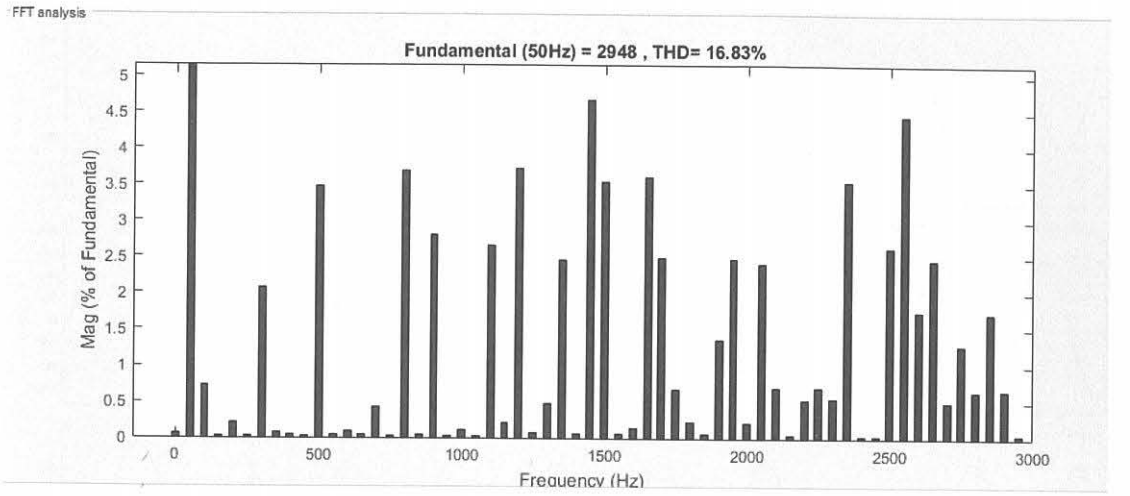

Figure 4.4 THD value for 3 phase 5 level CHMI without filter

4.3.3 3 Phase 5 Level CHMI With Low Pass Filter

With the implementation of filter, unwanted noise or the high frequency signals is filtered, thus less distortion and resulting a more pure sinusoidal wave. The LC filter is comprised of inductance of 150mH and capacitance of $220\mu F$ with both of the elements are arranged in series. From the result, voltage output shown $V_{rms} = 415V$ when modulation index, M is being set at 0.85. This can observed from figure 4.5 below. From the figure 4.6 below, the power factor are also in phase since this is resistive circuit the voltage and current are in phase where PF ~1. As shown in figure 4.7 below, THD value after implementation of filter and M=0.85 is 0.27%. This shown considerable decrease from 16.83%.

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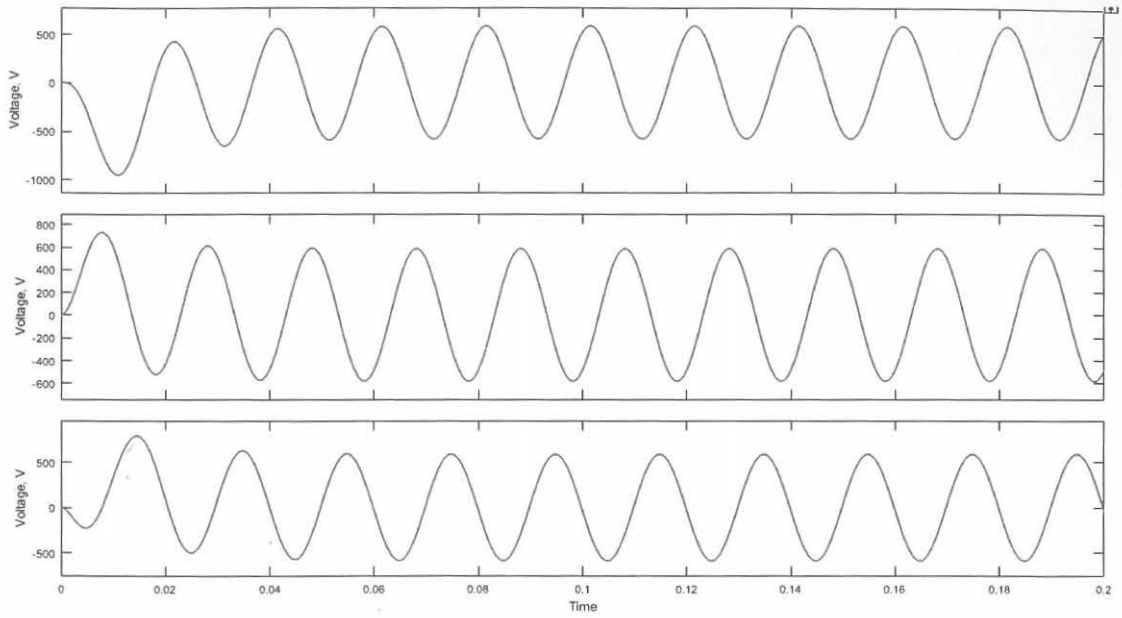

Figure 4.5 Output voltage with modulation index at 0.85 at all phase

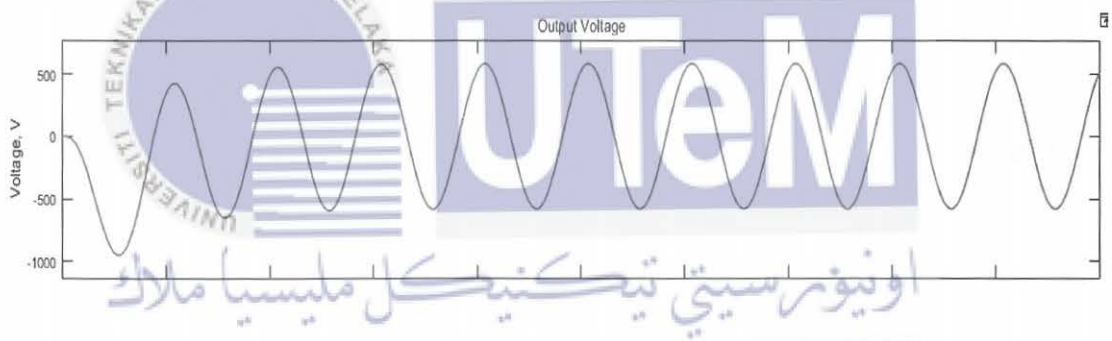

Figure 4.6 Output voltage 3 phase for phase 0 when M=0.85

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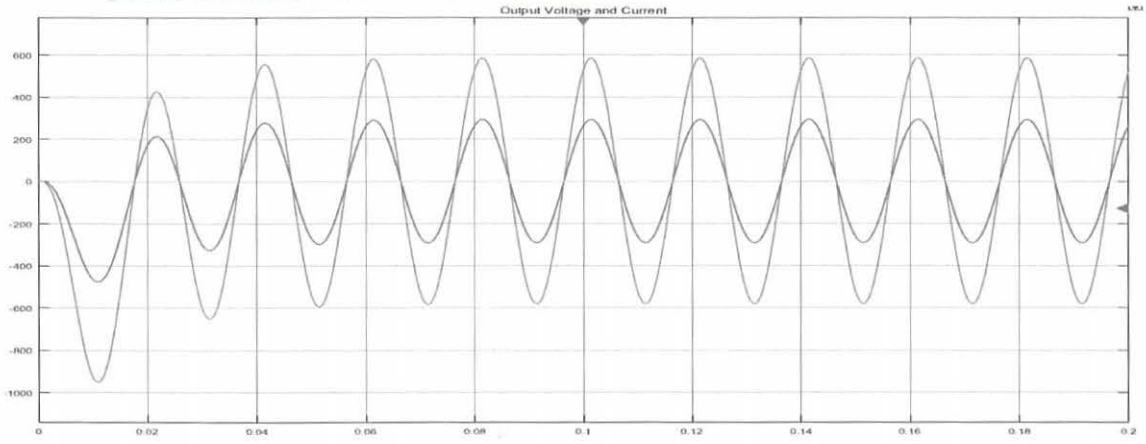

Figure 4.7 Output voltage and current 3 phase for phase 0 when M=0.85

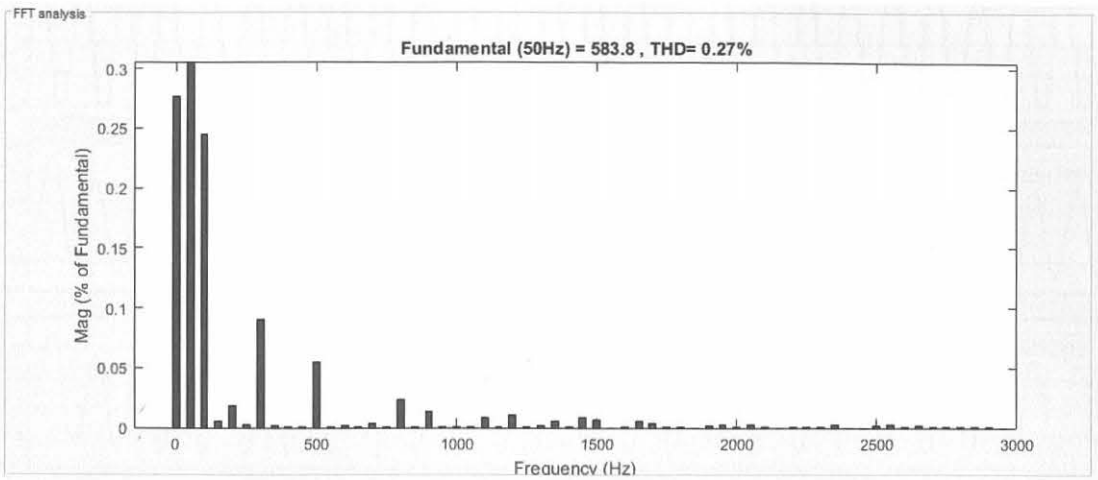

Figure 4.8 THD for H-Bridge CHMI value after implementation of filter

4.3.4 Range of Modulation index for the 5 level Multilevel Inverter

The 3 phase 5 level CHMI has range of modulation index at 0.6 – 1.2 as any below than 0.6 will resulting the voltage bridge level to be only 2 level and if the modulation index is set more than 1.2. The system will no longer able to functioning efficiently. Figure 4.9 and figure 4.10 below shown the voltage bridge results when modulation index is exceeding and below the range is implemented

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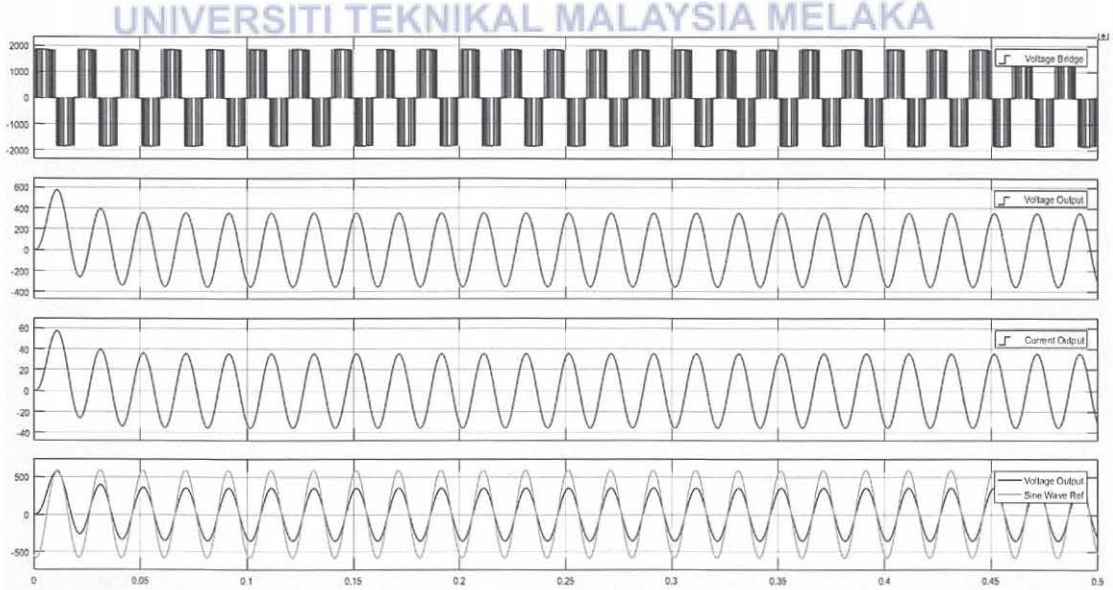

Figure 4.9 3 Phase 5 level CHMI at MI 0.5

Figure 4.10 3 phase 5 level CHMI with MI at 1.3

As shown in figure 4.9 and figure 4.10 the results shown the 2 level when MI is at 0.6 and the system is not giving reliable result when modulation index is 1.3

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4.3.5 Modulation Index and Its Effect on Total Harmonic Distortion

From table 4.1 below the value of modulation index is optimum from 0.6-0.85 with 0.65 being with the most optimum. Any less than that or more that will have rendered the THD to be higher and not reliable anymore. For 3-phase 5 level CHMI the modulation index is 0.6-1.2.

Table 4.1 Modulation Index and The Correlating Total Harmonic Distortion

Modulation Index	Total Harmonic Distortion (%)
0.60	0.13
0.65	0.12
0.70	0.13
0.75	0.13
0.80	0.13
0.85	0.13
0.90	0.14
0.95	0.15
1.00	0.17
1.05	0.20
1.10	0.26
1.15	0.31
1.20	0.38

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In this section Figure 4.11 and 4.6 below will shown the result of voltage output of an open loop system for 3-phase 5 level CHMI and when there is disturbance of voltage drop in the system.

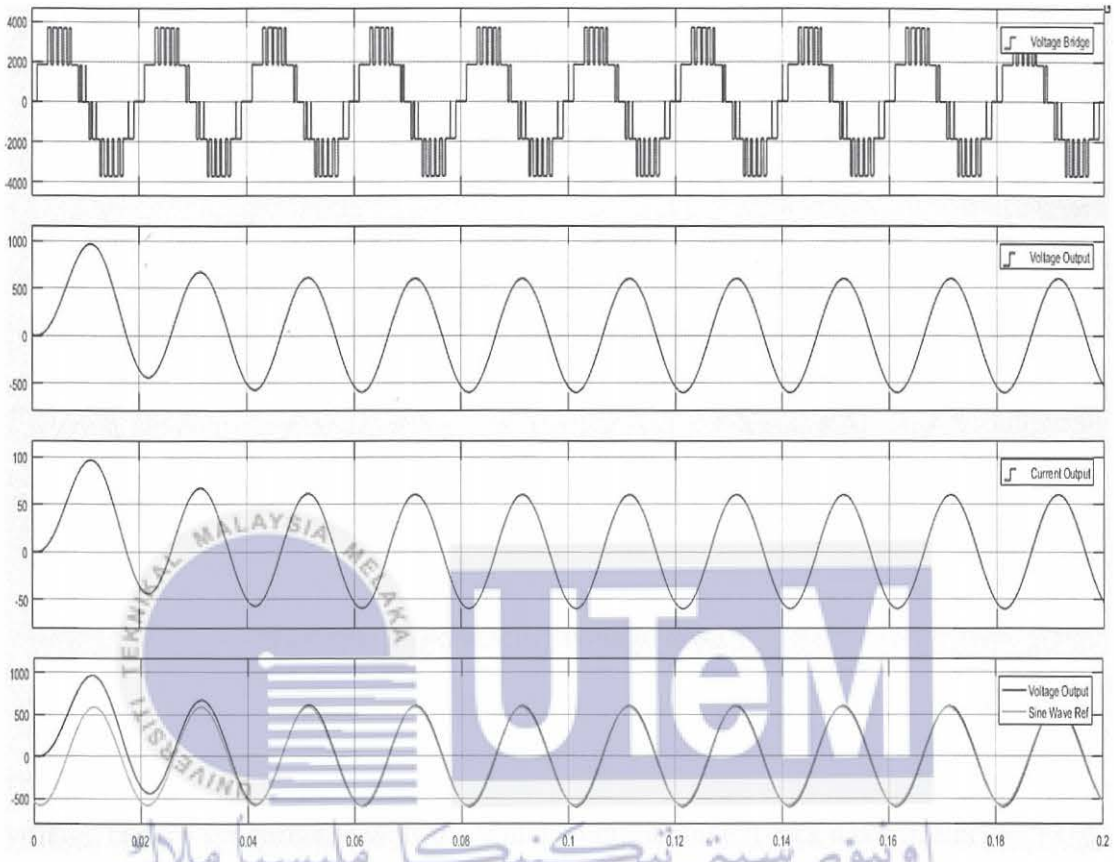

Figure 4.11 Uncompensated system 3 phase 5 level CHMI

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From figure 4.11 the 4 wave shown the voltage of the bridge, the voltage output, the current output and the voltage output comparing with voltage reference. The system is running with modulation index at 0.85 which is the optimum since it has low amount of total harmonic distortion (THD).

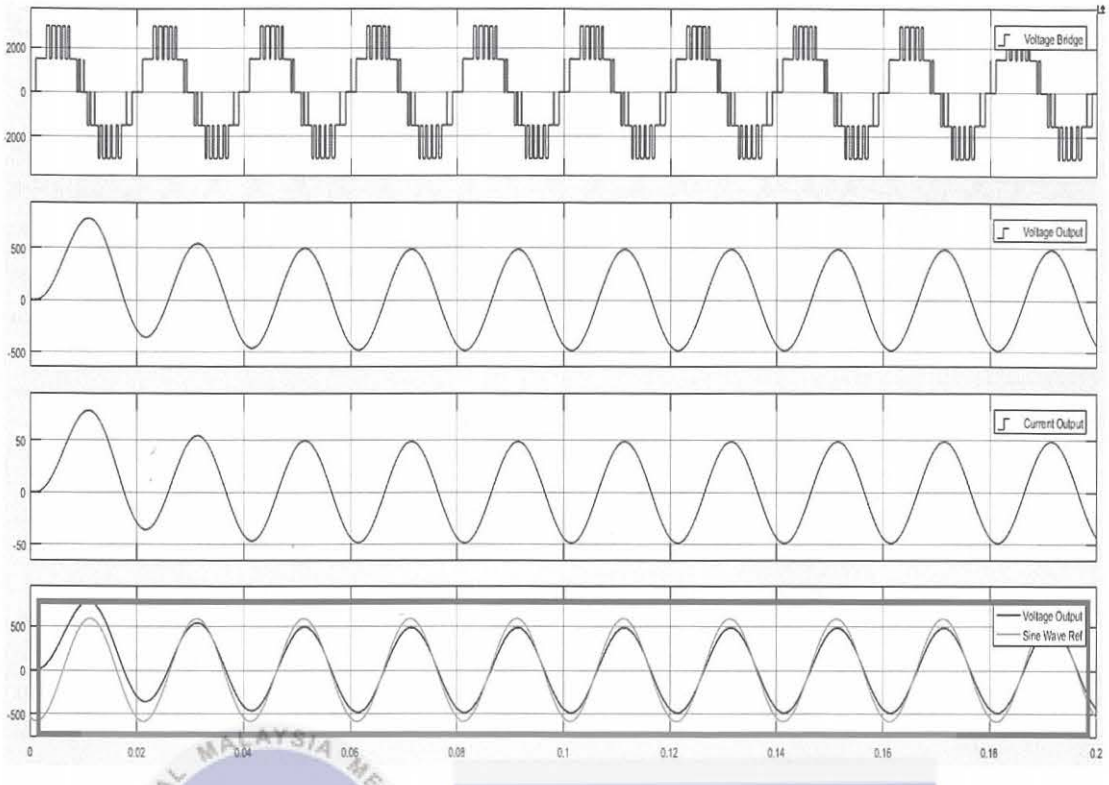

Figure 4.12 Uncompensated system of 3 phase 5 level CHMI experiencing voltage drop

Figure 4.12 above shown uncompensated system of 3 phase 5 level CHMI experiencing a voltage drop from its original supply. From the figure, the reference voltage cannot synchronise with the voltage output since it lack a controller.

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4.3.6 Close-loop System of Proportional Controller (PI)

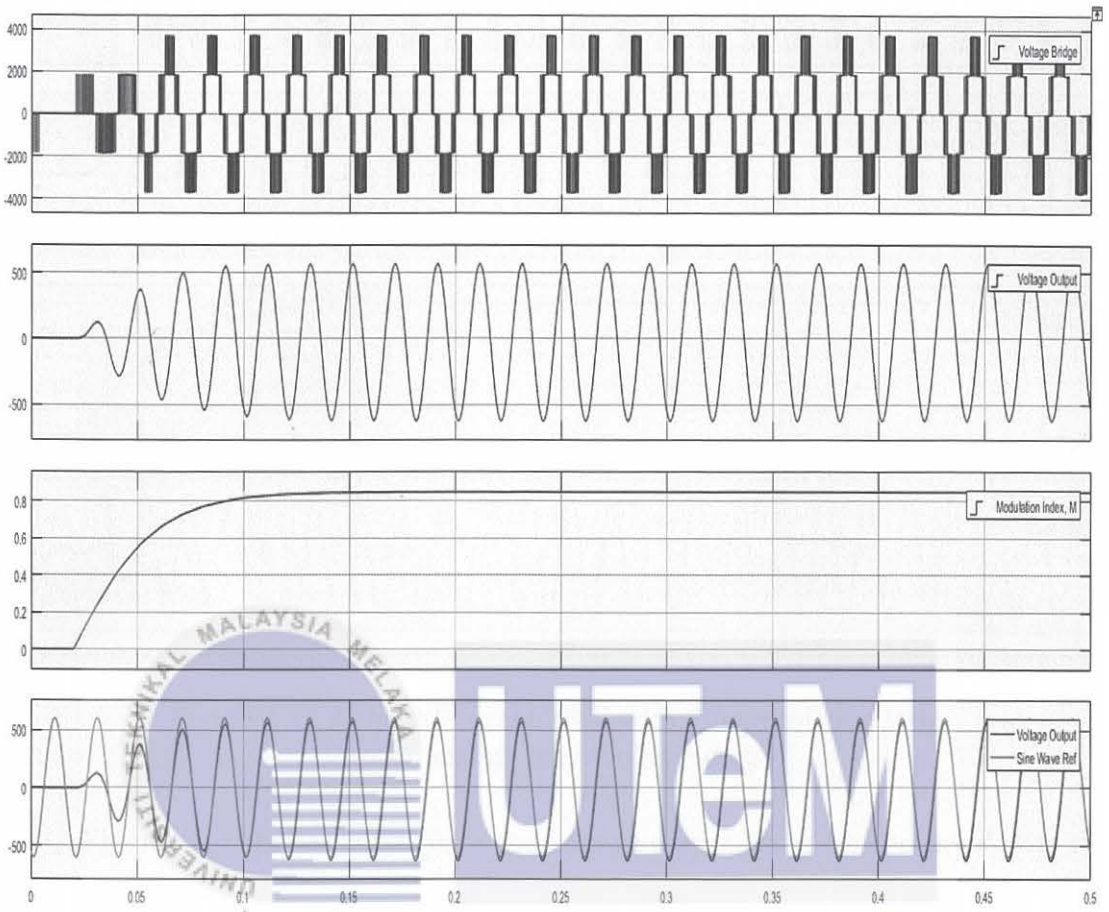

Figure 4.13 3 phase 5 level CHMI with PI controller system

Figure 4.13 above shown show the voltage output being synchronised with the reference voltage until they are in phase with the implementation of the proportional integral (PI) controller as shown above. Thus the voltage output is stabilise where the value of modulation index, m is 0.847 and the V_{rms} is 397.1V

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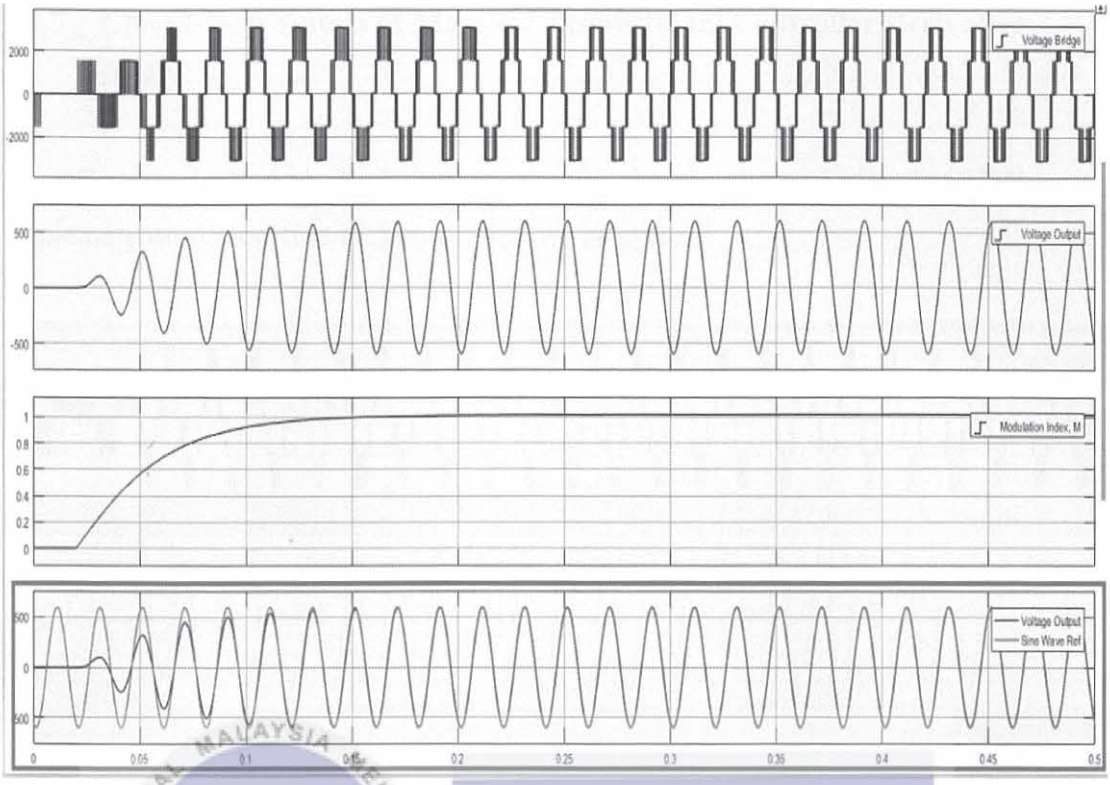

Figure 4.14 3 phase 5 level CHMI with PI controller system experiencing input voltage drop

Figure 4.14 above shown show the voltage output being synchronised with the reference voltage until they are in phase with the implementation of the proportional integral (PI) controller as shown above where there is voltage drop occur in the system. Thus the voltage output is stabilise where the value of gain, M is calculated by the PI at 1.017 and V_{rms} is 391.9V

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4.3.7 Closed-loop System of Modified Proportional Controller Derivative (PID)

Figure 4.15 and 4.16 below shown the 3 phase 5 level CHMI with implementation modified PID controller on the system.

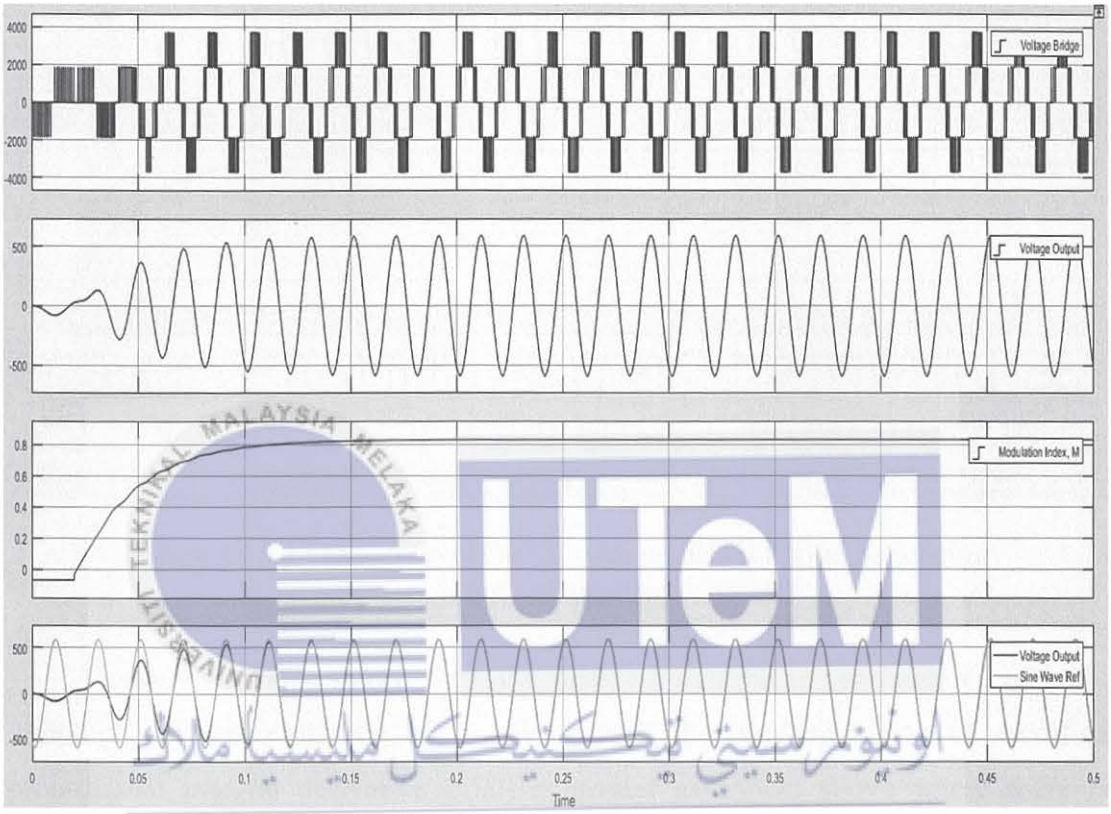

Figure 4.15 3 phase 5 level CHMI with modified PID controller

Figure 4.15 above shown show the voltage output being synchronised with the reference voltage until they are in phase with the implementation of modified proportional integral derivative (PID) controller as shown above where there is voltage drop occur in the system. Thus the voltage output is stabilise where the value of modulation index, M is calculated by the PID at 0.8326 and V_{rms} is 387.0V

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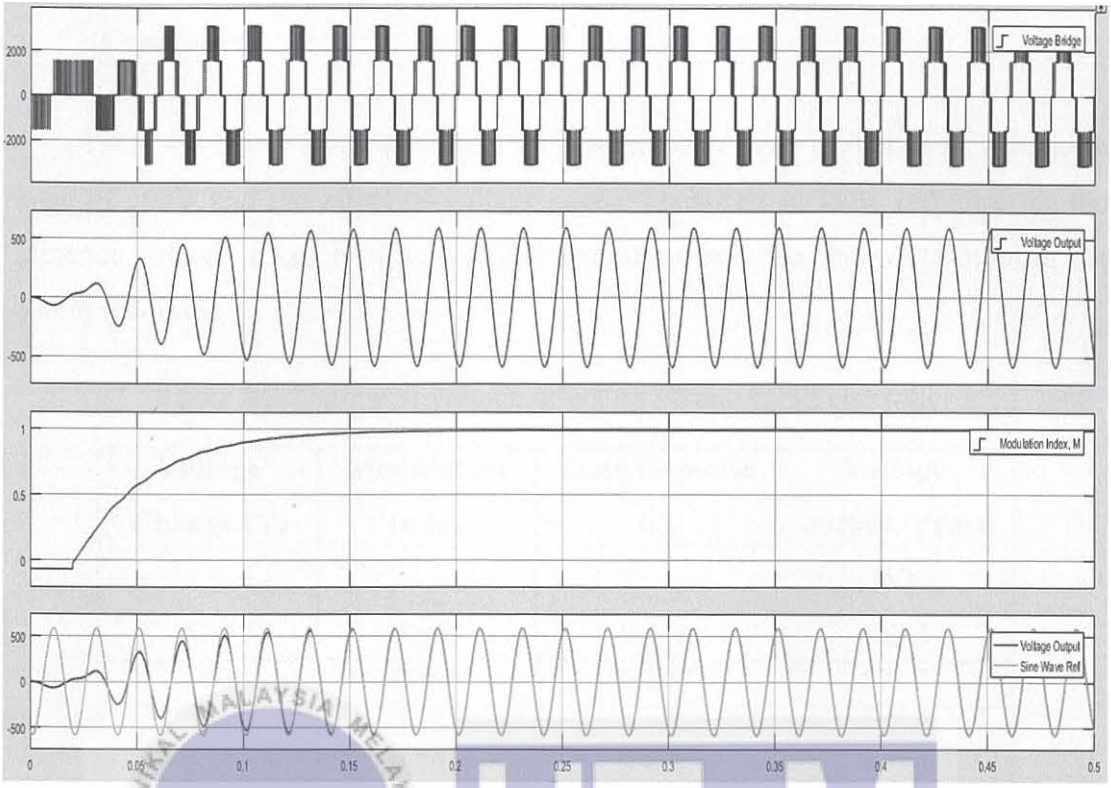

Figure 4.16 3 phase 5 level CHMI with modified PID experiencing input voltage drop

Figure 4.16 above shown show the voltage output being synchronised with the reference voltage until they are in phase with the implementation of modified proportional integral derivative (PID) controller as shown above where there is voltage drop occur in the system. Thus the voltage output is stabilise where the value of modulation index, M is calculated by the PID at 0.9935 and V_{rms} is 383.0V

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4.3.8 Table on Data of Voltage Change Effect on System PI and Modified PID Controller

Table 4.2 below show the effect on system when there is change in voltage in range of 500V and the effect of voltage output consistency. Time response for the reference voltage to synchronise with voltage output are also observe to monitor the system readiness.

Table 4.2 Change of voltage effect on system by PI controller

Voltage Change (V)	Modulation Index	Time response (s)	Voltage output, Vrms (V)
500	0.669	0.110	402.5
400	0.699	0.100	401.7
300	0.731	0.110	402.0
200	0.766	0.170	399.7
100	0.805	0.170	398.7
-100	0.897	0.180	396.0
-200	0.952	0.183	393.0
-300	1.017	0.184	391.0
-400	1.141	0.209	386.9
-500	1.378	0.172	377.2
-600	1.727	0.140*	363.2
		Average=0.157	

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From table 4.3 the data shows that the PI controller are functioning as to recalculate the value of modulation index according to the change of the voltage level although the change in modulation index is quite significant, the asterisk at 0.140s shown that the PI controller could no longer maintain the voltage output efficiently.

Table 4.3 below shown the voltage change effect on system by modified PID controller, the observed parameters is the modulation index, time response and the voltage output of the system. Modified PID shown a slight better performance as it has average time response of 0.126s than that of PI at 0.157s. Moreover, it also shown more robustness as the voltage output did not change much as the PI controller system

Table 4.3 Voltage change effect on system by modified PID controller

Voltage Change (V)	**Modulation Index**	**Time response (s)**	**Voltage output, Vrms (V)**
+600	0.628	0.070	391.9
+500	0.655	0.080	391.3
+400	0.684	0.090	390.3
+300	0.716	0.090	389.0
+200	0.751	0.102	389.0
+100	0.789	0.105	398.6
-100	0.880	0.130	385.0
-200	0.933	0.130	384.0
-300	0.994	0.130	383.0
-400	1.098	0.150	380.0
-500	1.327	0.170	372.0
-600	1.783	0.170	368.0
		Average=0.126	

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As shown in table 4.4, the modulation index is recalculated by the modified PID controller whenever there is a voltage change. When the voltage is increased the controller counter it by lowering the modulation index and when there is voltage drop, the controller counter it by increasing the modulation index.

4.3.9 Discussion of The Result

Table 4.2 below shown the summary of the performance of 3-phase 5-level CHMI with SPWM control without filter and with filter at modulation index 0.85

Table 4.4 Result from the simulation for 3 phase 5 level CHMI

	3-Phase 5-Level CHMI using SPWM
THD value before filter	16.83%
THD value after filter	0.27%
Power factor (PF) before and after filter	~1.0

Result from table 4.1 above shown result simulation for 3-phase 5-level multilevel inverter. The result from simulation of CHMI without filter shown THD with value of 16.83% and 0.27% after filter. Low THD is a good indication since it means more efficiency, higher power factor and low peak currents which is good for equipment as it ensured longer lifespan. The power factor can also be observed between the voltage output and the current out output which shown that both are in phase because the nature of the circuit which is the resistive circuit. Thus, it can be assumed that the value of power factor is ~1. This shown that the CHMI is quite efficient multilevel inverter.

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For the controller of multilevel inverter is previously an open loop system, thus the value of the output is expected. However, under certain circumstances such as noise or disturbance, there can be a rather unpredictable result. Moreover, the calculation will not always be similar with value from simulation. Therefore, a feedback controller of PI and modified PID is designed to counter the circumstances and PI controller is chosen as a controller to eliminate the steady state error in the system.

The results are as shown expected as it can eliminate the steady state error for the system, however there are still some drawback which is the settling time. Thus, an alternate feedback controller is coming up with, which is the modified PID controller. With its implementation, there is an additional parameter which is the derivative. Not only the steady state error is eliminated, the settling time is also reduced as shown in table 4.4 where the average for system readiness is only 0.126s compare to than that of PI controller at 0.157s. The voltage output also does not shown any abrupt change when there is voltage change occur.

4.4 Summary

By analysing the performance of the 3-phase 5-level CHMI in aspect of THD value of the CHMI and its power factor. It is shown that the CHMI have a low THD, which signifying it as quite efficient inverter.

The CHMI is also implemented with control technique of SPWM to produce more sinusoidal wave. This shown a correlation with the theoretical studies where it can be inferred that what has been shown in theoretical studies is validated with simulation using MATLAB/Simulink.

The performance of the PI and modified PID shown that PID is a slight better than that of PI as it's have faster response and more prone to adapt any change such change of voltage or load.

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CHAPTER 5

CONCLUSION AND RECOMMENDATIONS

5.1 Conclusion

Multilevel inverter has been a capable successor to normal inverter since it can withstand load for medium to high voltage application with significant minimum in switching losses and lower THD. The different topology available for multilevel inverter have been researched and studied in chapter 2 and it is shown that CHMI have some upper hand over the flying capacitor and diode-clamped which less component is required.

Moreover, all the block diagram and circuit of 3-phase 5-level CHMI have been implemented as shown in the methodology of chapter 3. From the circuit, SPWM is also implemented to minimise the harmonic of the voltage output from CHMI. SPWM are also crucial to ensure sinusoidal voltage output waveform.

From the performance, it is shown that 3-phase 5-level CHMI is an efficient system with THD at 0.27% and a power factor ~1 with resistive load.

For the feedback controller, which is the PI and modified PID, both of the controller have been designed into 3 phase 5 level CHMI and have been implemented successfully. The performance also has been analyse with modified PID controller slight better response than that of the PI controller.

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5.2 Recommendation

For future reference, designing of PI controller and modified PID need to be even more accurate to ensure a reliable result.

Moreover, the trial and error when tuning the proper value for the system need to be done frequently so that the PI and PID is functioning exactly and efficiently without any error or miscalculation

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APPENDICES

Gantt Chart

	Final Year Project 1														Semester Break					Final Year Project 2											
Week	1	2	3	4	5	6	7	8	9	10	11	12	13	14	1	2	3	4	5	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Title Registration																																	
Discussion with supervisor																																	
Research of topics with journal, paper and internet																																	
Study of multilevel inverter																																	
Study of SPWM technique																																	
Study of PI, PID and modified PID																																	

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Report Preparation																																
	Final Year Project 1														**Semester Break**					**Final Year Project 2**													
Week	1	2	3	4	5	6	7	8	9	10	11	12	13	14	1	2	3	4	5	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Final Year Project 1 presentation																																	
Final Year Project 1 report submission																																	
PI and modified PID controller designing																																	
Final Year Project 2 presentation																																	
Final Year Project 2 report submission																																	

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