MULTI-RESPONSE OPTIMIZATION IN 16NM WSI_2/TIO_2 N- CHANNEL MOSFET DEVICE USING TAGUCHI METHOD WITH GRA

NOR FAZILAH BINTI SHAMSUDIN

UNIVERSITI TEKNIKAL MALAYSIA MELAKA

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NOR FAZILAH BINTI SHAMSUDIN

This report is submitted in partial fulfilment of the requirements for the degree of Bachelor of Electronic Engineering with Honours

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DEDICATION

To my beloved parents and siblings,

To my supportive supervisor,

And to all my friends.

ABSTRACT

The aim of this research is to optimize the process parameters variations of 16nm WSi_2/TiO_2 n-channel MOSFET device using Taguchi-based Grey Relational Analysis (GRA). The process of the device was initially stimulated by using ATHENA module of Silvaco TCAD. The electrical characterization was carried out using an ATLAS module of Silvaco TACAD. The electrical characteristics that being calculated were threshold voltage (Vth), drive current (Ion), leakage current (Ioff), current state ratio (Ion/Ioff) and sub-threshold slope (SS). The L_9 Orthogonal Array (OA) method, signal-to-noise ratio (SNR) and Analysis of Variance (ANOVA) were used to analyze the effect of the process parameters. The process parameters that used were halo implant dose, halo implant energy, S/D implant dose and S/D implant energy with noise factor which were anneal and nitride temperature. All the experimental values were converted to Grey Relational Grade (GRG) and the level of process parameter with the highest GRG are selected as the most optimal level. The values of Vth, Ion, Ioff, Ion/Ioff and SS after optimization approaches were 0.547V, 471.78 µA/µm, 3.25 pA/µm, 145.17E+06 and 76.06 mV/dec respectively. Most of the results obtained were within the range and meet the requirement of low power (LP) technology for the year 2017 as predicted by International Technology Roadmap Semiconductor (ITRS) 2017. As a conclusion, the design 16nm WSi_2/Tio_2 n-channel MOSFET device has successfully been created and through the Taguchi-based GRA, the optimal solution for the robust design of the devices has successfully been achieved.

ABSTRAK

Tujuan penyelidikan ini adalah untuk mengoptimumkan variasi parameter proses peranti MOSFET n-saluran 16nm WSi2 / TiO2 menggunakan analisis hubungan Grey (GRA) berasaskan Taguchi. Proses bagi peranti disimulasikan dengan menggunakan modul ATHENA Silvaco TCAD sementara pencirian elektrik dijalankan adalah voltan ambang (Vth), arus pacu (Ion), arus bocor (Ioff), nisbah arus (Ion / Ioff) dan sub-threshold slope (SS). Kaedah L9 Orthogonal Array (OA), nisbah isyarat-kepada-bunyi (SNR) dan variasi analisis (ANOVA) telah digunakan untuk menganalisis kesan kepada parameter proses. Parameter proses yang telah digunakan adalah halo implant dose, halo implant energy, S/D implant dose dan S/D implant energy dengan faktor bunyi yang merupakan suhu anneal dan nitrida. Semua nilai eksperimen telah ditukar kepada Grey Relational Grade (GRG) dan paras parameter proses dengan GRG tertinggi dipilih sebagai tahap yang paling optimum. Nilai Vth, Ion, Ioff, Ion / Ioff dan SS selepas dioptimumkan adalah 0.547V, 471.78 μA / μm, 3.25 pA / μm, 145.17E + 06 dan 76.06 mV / dec. Kebanyakan keputusan yang diperolehi adalah dalam julat yang dibenarkan dan memenuhi keperluan yang telah ditetapkan oleh teknologi kuasa rendah (LP) untuk tahun 2017 yang telah ditetapkan oleh International Technology Roadmap Semiconductor (ITRS) 2017. Sebagai kesimpulan, reka bentuk 16nm WSi2 / Tio2 n-channel MOSFET sebagai peranti telah berjaya direka dan melalui kaedah GRA berasaskan Taguchi, penyelesaian optimum untuk reka bentuk yang teguh bagi peranti telah berjaya dicapai.

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LIST OF SYMBOLS AND ABBREVIATIONS

MOSFET	:	Metal Oxide Semiconductor Field Effect Transistor
MOS	:	Metal Oxide Semiconductor
NMOS	:	N-channel Metal Oxide Semiconductor
PMOS	:	P-channel Metal Oxide Semiconductor
SCE	:	Short-Channel Effect
DIBL	:	Drain Induced Barrier Lowering
TiO_2	:	Titanium Dioxide
SiO2	:	Silicon Dioxide
WSi_2	:	Tungsten Silicide
CMOS	:	Complementary Metal Oxide Semiconductor
S/N or SNR	:	Signal-to-Noise Ratio
GRA	:	Grey Relational Analysis
S/D	:	Source/Drain
TCAD	:	Technology Computer Aided Design
FET	:	Field-Effect-Transistor
ITRS	:	International Technology Road Map for Semiconductors
VLSI	:	Very Large-Scale Integration
LSI	:	Large-Scale Integration
ULSI	:	Ultra Large-Scale Integration

EOT	:	Gate Oxide Thickness
I_{ON} or Ion	:	Drive Current
Ioff or I_{OFF}	:	Leakage Current
V_{TH} or Vth	:	Threshold Voltage
SS	:	Sub-threshold Slope
Ion/Ioff	:	Current State Ratio
SOI	:	Silicon in Insulator
L_{eff}	:	Effective Channel Length
SS_T	:	Total Sum of Squared Deviation
VG	:	Gate Voltage
Al_2O_3	:	Aluminium Oxide
ZrO_2	:	Zirconium Dioxide
HfO_2	:	Hafnium Dioxide
Lg	:	Gate Length
OA	:	Orthogonal Arrays
WEDM	:	Wire Electrical Discharge Machining
MRR	:	Metal Removal Rate
VWF	:	Virtual Wafer Fab
LPT	:	Low Power Technology
Bf_2	:	Difluoride
DC	:	Direct Current
AC	:	Alternating Current
SSQ	:	Sum of Squares
DF	:	Degree of Freedom
IC	:	Integrated Circuit

MSSQ	:	Mean Sum of Squares
GRC	:	Grey Relational Coefficient
GRG	:	Grey Relational Grade
ANN	:	Analysis Neural Network