OPTIMIZATION OF 19 NM SOI MOSFET WITH HIGH-K MATERIAL AS GATE SPACER USING STATISTICAL METHOD

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UNIVERSITI TEKNIKAL MALAYSIA MELAKA

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OPTIMIZATION OF 19 NM SOI MOSFET WITH HIGK-K MATERIAL AS GATE SPACER USING STATISTICAL METHOD

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This report is submitted in partial fulfilment of the requirements for the degree of Bachelor of Electronic Engineering with Honours

Faculty of Electronic and Computer Engineering
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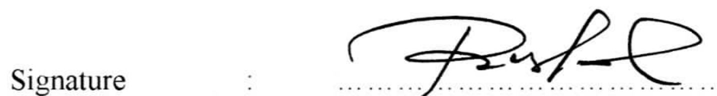
Signature : 

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DEDICATION

I dedicated this thesis to my beloved parents, Sahul Hameed Bin Raj Mohamed and Saniyah Binti Junid and my siblings whom always support and encourage me.

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ABSTRACT

As scaling down MOSFET device degrade the device performance in term of leakage current and short channel effect (SCE). To overcome the problem, the SOI MOSFET device with high-k material such as titanium dioxide (TiO2) as gate spacer has been introduced. However, the fluctuation and variation of ion implantation process will impact the overall power dissipation and performance. Therefore, analysis of variability has become a very important tool to predict the response variation very early in the design cycle due to process parameter spreads. This project execution is based on simulation and program development of the device. Simulation of this device fabrication will be performed by using ATHENA module while for simulation of electrical characteristics will be implemented by using ATLAS module from semiconductor TCAD tools. Semiconductor TCAD tools are computer programs which allow for the creation, fabrication and simulation of semiconductor devices. These 2 modules will be combined with Taguchi method to aid in design and optimizer the process parameter. The parameters that will be considered in this project are the drive current (Ion), leakage current (Ioff), threshold voltage (Vth), current state ratio (Ion/Ioff ratio), subthreshold swing (SS), halo implant energy, halo implant dose, Source/Drain (S/D) implant dose and S/D implant energy. These parameters must achieve the most optimum value that accepted by Low Power (LP) technology by International Technology Roadmap for Semiconductor (ITRS).

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ABSTRAK

Pengecilan peranti MOSFET merendahkan prestasi peranti dari segi kebocoran arus dan kesan saluran pendek (SCE). Untuk mengatasi masalah ini, peranti SOI MOSFET dengan bahan high-k seperti Titanium dioksida (TiO2) sebagai "gate spacer" telah diperkenalkan. Walau bagaimanapun, turun naik dan variasi proses implantasi "ion" akan memberi kesan kepada pelesapan kuasa dan prestasi kuasa keseluruhannya. Oleh itu, analisis kebolehubahan telah menjadi alat yang sangat penting disebabkan oleh penyebaran parameter proses. Pelaksanaan projek ini berdasarkan kepada simulasi dan pembangunan program peranti. Simulasi fabrikasi peranti ini akan dilakukan dengan menggunakan modul Athena sementara untuk simulasi ciri-ciri elektrik akan dilaksanakan dengan menggunakan modul Atlas dari alat TCAD semikonduktor. Peralatan TCAD semikonduktor adalah program komputer yang membolehkan penciptaan, fabrikasi dan simulasi peranti semikonduktor. Kedua-dua modul ini akan digabungkan dengan kaedah Taguchi untuk membantu dalam reka bentuk dan pengoptimum parameter proses. Parameter yang akan dipertimbangkan dalam projek ini ialah arus pemacu (Ion), kebocoran arus (Ioff), voltan (Vth), nisbah Ion/Ioff, sub-ambang voltan (SS), tenaga implan halo, dos implan halo, Imun implan (S/D) implan dan tenaga implan S/D. Parameter ini mesti mencapai nilai paling optimum yang diterima oleh teknologi Kuasa Rendah (LP) oleh Roadmap Teknologi Antarabangsa untuk Semikonduktor (ITRS).

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LIST OF SYMBOLS AND ABBREVIATIONS

Al_3O_2		Aluminium oxide
ANOVA	:	Analysis of Variance
BJT		Bipolar junction transistor
BOX	:	Buried oxide
BPSG	:	Boron Phosphor Silicate Glass
CMOS	:	Complementary Metal Oxide Semiconductor
CVD	:	Chemical Vapor Deposition
D	:	Drain
DIBL		Drain-Induced Barrier Lowering
FD		Fully depleted
FET		Field effect transistor
I_D		Drain current
I_{OFF}		Leakage current
I_{ON}		Drive current
I_{ON}/I_{OFF}	:	Current state ratio
ITRS		International Technology Roadmap for Semiconductor
HfO_2	:	Hafnium oxide
k		Dielectric constant
La_2O_3		Lanthanum Oxide

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L_G		Gate Length
MOSFET	:	Metal Oxide Semiconductor Field Effect Transistor
nm		Nanometer
NMOS		N-channel MOSFET
PECVD		Plasma Enhanced Chemical Vapor Deposition
PD		Partially depleted
S	:	Source
SCE	:	Short Channel Effect
Si_3Ni_4		Silicon nitride
S/N		Signal-to-noise
SNR		Signal-to-noise ratio
SiO_2		Silicon dioxide
SOI		Silicon-on-insulator
SS		Sub-threshold voltage
STI		Shallow trench isolation
TCAD		Technology Computer Aided Design
TiO_2		Titanium Dioxide
$TiSi_2$	:	Titanium Silicide
V_D		Drain voltage
V_{DS}		Drain-to-source voltage
V_G		Gate voltage
V_{GS}		Gate-to-source voltage
V_{TH}		Threshold voltage
Y_2O_3		Yttrium Oxide
ZrO_2		Zirconium Dioxide

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CHAPTER 1

INTRODUCTION

This chapter presents the brief introductory of project background which contains the problem statement, objectives, scope and significance of the project.

1.1 Background of Project

As technology is advancing by years, demand of high performance and accuracy of digital chips is increasing as well. Faster the switching rate can indicate the performance of the transistor is at its best and the microprocessor able to operate at a high speed. This could be achieved by scaling the dimension of MOSFET by using nanometer technology [1]. However, minimization of the gate dimensions increases the short channel effect (SCE) and the extension for drain (D) and source (S) junctions. A major obstacle of SCE is the gate current leakage that occurs when channel attached

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together as drain (D) and (S) are too near due to scaling the MOSFET dimension. This resulting a static power current leaks through transistor even when device is turned off. Besides, scaling limits the driving current of MOSFET device because increased in parasitic resistances and capacitances.

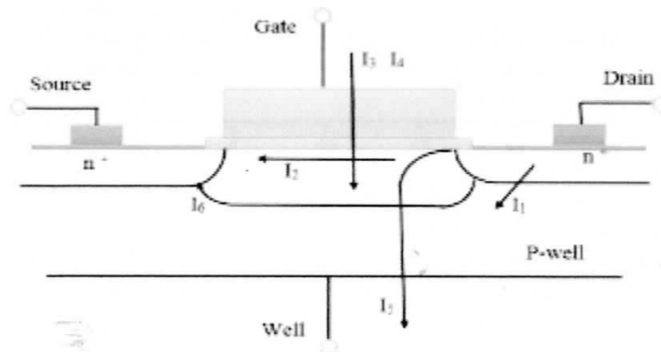

Figure 1.1: Leakage current mechanism in nanoscale MOSFET

Through a study of leakage reduction techniques for CMOS in 2015, a 22nm NMOS was designed and simulated by using ATHENA and the electrical characteristics were simulated by using ATLAS modules from Silvaco software [2]. Here, they emphasized the use of high-k materials as the dielectric metal gate in improving the current state ratio (I_{ON}/I_{OFF} ratio). Higher I_{ON}/I_{OFF} ratio indicates the device is suitable for low power application. Titanium silicide ($TiSi_2$) has been used as the metal gate while silicon nitride (Si_3Ni_4) and hafnium oxide HfO_2 are chosen as the gate dielectrics. The simulation result has shown that HfO_2 was the best dielectric material when $TiSi_2$ became the metal gate, which indicates that high-k dielectric is a possible candidate to replace SiO_2. Hence, it is proven that high-k materials could be one of the best mechanisms to limit leakage current in CMOS devices. Figure 1.2 shows the variation in I_{OFF} with SOI thickness (T_{SOI}).

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