

**FPGA IMPLEMENTATION OF HOG ALGORITHM
USING SDSOC**

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UNIVERSITI TEKNIKAL MALAYSIA MELAKA

**FPGA IMPLEMENTATION OF HOG ALGORITHM
USING SDSOC**

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APPROVAL

I hereby declare that I have read this thesis and in my opinion this thesis is sufficient in terms of scope and quality for the award of Bachelor of Electronic Engineering with Honours.

Signature :

Supervisor Name : Profesor Dr. Zulkalnain Bin Mohd Yussof

Date : 31/05/2019

DEDICATION

I dedicate this research work to my beloved father and mother who always support and encourage me through my education journey, my beloved lecturers, supervisor who do not stop giving knowledge and my beloved friends who always provide assistance.

ABSTRACT

In today modern world, a precise and rapid pedestrian detection is an extremely important job for a wide range of applications in automotive and personal identification. One of the most reliable and common use algorithms of computer vision for object detection and human detection is Histogram of Oriented Gradients (HOG) algorithm. HOG is also a high complexity and compute intensive task for human detection. This project implementations of HOG algorithm using an embedded platform, that is the Zedboard development kit board which contains the Xilinx Zynq R-7000 All Programmable system on chip (SoC) that is comprised of both an ARM-platform processing system and an FPGA based programmable logic. This platform gave us the ability to execute different parts of the algorithm simultaneously both on the CPU and the FPGA. The platform has the advantages of being portable and small size high computing speed, low cost and able to be built with small cameras for monitoring purposes.

ABSTRAK

Dalam dunia moden hari ini, pengesanan manusia yang tepat dan cepat adalah tugas penting bagi pelbagai aplikasi seperti pengenalan diri automotif dan orang. Algoritma “Histogram of Gradients Oriented (HOG)” adalah salah satu algoritma pengimejan yang paling dipercayai dan digunakan penglihatan komputer untuk pengesanan objek dan pengesanan manusia. Walau bagaimanapun, algoritma HOG juga merupakan kerumitan tinggi dan mengira tugas intensif untuk pengesanan manusia. Pelaksanaan projek algoritma HOG ini menggunakan platform terbenam, iaitu papan pengembangan Zedboard yang mengandungi sistem “Xilinx Zynq R-7000 All Programmable” pada cip (SoC) yang terdiri daripada sistem pemproses “ARM-platform” dan programmable berbasis FPGA logik. Platform ini memberi kita kemampuan untuk melaksanakan bahagian-bahagian algoritma yang berlainan secara serentak pada CPU dan FPGA. Sistem ini memberikan kelebihan saiz kecil, kos rendah, kelajuan pengkomputeran tinggi, dan mudah alih dan boleh dibina dalam kamera kecil untuk aplikasi pengawasan.

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LIST OF SYMBOLS AND ABBREVIATIONS

HOG	:	Histogram of Oriented Gradients
FPGA	:	Field-Programmable Gate Array
SDSoC	:	Software-Defined System-On-Chip
ARM	:	Advanced RISC Machines
SIFT	:	Scale-invariant Feature Transform
SVM	:	Support Vector Machine
PD	:	Pedestrian Detection
USB	:	Universal Serial Bus
RGB	:	Red Green Blue
ASIC	:	Application Specific Integrated Circuit
HDL	:	Hardware Description Language
PC	:	Personal computer
IDE	:	Integrated development environment
API	:	Application programming interface
NMS	:	Non-maximum Suppression
IoU	:	Intersection over Union

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CHAPTER 1

INTRODUCTION

This chapter explained about the introduction of this project following by the the problem statement. For the project background, an explanation about the lightning has been described. Project objectives, scopes and preliminary results from this project also discussed in this chapter. All the details for each section of the project have been discussed in this chapter.

1.1 Introduction of the Project

Object detection is a hot research topic over the last two decades and the real-time processing speed are also important especially in automotive sector that involve pedestrian detection, vehicle detection and traffic signal in the surrounding. [1] The HOG algorithm is a feature extraction that commonly used for object detection. This

project is using a heterogeneous Field programmable gate array FPGA/ARM processor and Xilinx SDSoC (Software-Defined System on Chip) for object detection. Xilinx Zynqa is a hybrid system and features a dual ARM Cortex-A9 processor and a FPGA processor that provides the adaptability of processing pace on a single chip.[2] In this project, evaluation on Zedboard with histogram of oriented gradients (HOG) algorithm for object detection will be analyze. For object classification, linear support vector machine (lnSVM) will be use. This system provides a more efficient implementation of HOG algorithm in FPGA, by considerably reducing the area, low cost, high computing speed, while maintaining accuracy compared to the original algorithm, portable and able to build in small cameras for surveillance applications. Finally, the project able to build for many applications of object detection including human detection, car detection etc.

1.2 Problem Statement

Object detection is one of the key problems in emerging self-driving car industry for example pedestrian and human detection, vehicle detection and traffic signal detection. However, object detection will need large memory capacity because of the size of input image issue. The high complexity of object detection needed longer processing time or even causing delay. [3] The size of network input is limited by the amount of memory; therefore, poor performance will also occur due to network latency. This will affect the accuracy and efficiency on object detection. On the same time, a graphics processing unit (GPU) is a computer chip which need higher cost, large area and large energy. Therefore, this project is implementing HOG algorithm in FPGA using SDSoC will reduce the problem and it is simplicity and mobility. [4]

1.3 Project Objectives

The objective of this project is:

- To implement of Histogram of Oriented Gradients HOG algorithms onto Field-programmable gate array (FPGA) platform for object detection
- To evaluate and analyze the performance of SDSoC implemented HOG algorithm in terms of accuracy and speed.

1.4 Scope of Work

The scope of work in this project is to study and evaluate FPGA implementation of HOG algorithm using SDSoC. The literature review of FPGA SDSoC and HOG algorithm from the journal using as a reference to get the information about this project. The final project is focus on object detection and classification. The algorithms will be coded by C programming language in Visual Studio 2017. First, study HOG algorithm and C programming language. Later, HOG algorithm in C programming language for HOG is implement and compile in software. After the code is successfully built, Xilinx SDSoC software platform is using to assess the performance of system when implemented HOG algorithm in terms of speed. The performance analysis will help on decision making for better performance. FPGA SDSoC Xilinx later is used to compiler for C code to hardware SD card booth file. SVM will be use as object classification for detected object. Besides, all the final data of performance is analyzed with frames per second (FPS). Preliminary Result will be obtaining and as a reference for following works.

1.5 Expected Outcome

The expected outcome for this project is implement of FPGA with HOG algorithm using SDSoC to detect object. FPGA SDSOC Xilinx is used for object detect. The object will be capture automatically when it detected the object. The rate for the frame per second of the image that capture for this project is expected to proceed up to 30 frame per second. All the images that captured by camera will be stored in local drive storage. At last, the inference time of object detect will be classified according to the design.

1.6 Thesis structure

This dissertation contains five chapters:

Chapter 1 discusses more on the background, problem statement, objectives, scope of this project study and expected outcome. It gives an overview for the study. Chapter 2 explains the literature reviews about the computer vision, object detection, HOG, classifier SVM, FPGA SDSOC Xilinx and Xilinx Zedboard. Chapter 3 will cover the methodology and technique that will be implemented in this project. The approach for software implementation of Visual Studio 2017 software and Xilinx software and hardware implementation of Xilinx Zedboard are presented in this chapter. In chapter 4, the outcome of this project is discussed and presented on how the system performance. This section will likewise discuss the result acquired in a detailed manner. Chapter 5 presents the conclusion and future research. On the same time, the preference and the shortcoming of this project also discussed. This project can be improved in the future to make the object detection in FPGA more useful and functioning.

CHAPTER 2

BACKGROUND STUDY

2.1 Introduction

This project required to do a lot of researches and finding for the facts and theory about the background for each section. This is because with this finding and facts, this project can be proceeding more smoothly and successful. This chapter explains in detail about the review for the related previous research paper and journals of computer vision, object detection, HOG, FPGA and SDSoC. Based on the idea methods and techniques that been used in those previous researches, the best solution was selected and applied to this project as the methodology.

2.2 Overview

Although computer technology that related to computer vision technology and image processing have only exploded recently, it helps to detect object with several classes can classified it with a known class, such as cars, traffic signs, people or face in an image or video. [1] Today, many different interesting and useful detection algorithms or applications are proposed and implement according to desire application by different researchers or companies to achieve accurate and real time pedestrian detection. Human detection is an integral part of any video surveillance system with numerous applications in numerous computer vision fields. For example, automotive sector of robotics, Advanced driver-assistance systems (ADAS) developed and unmanned ground vehicles (UGV). [1], [3], [5]

2.3 Feature descriptor

Numerous innovative feature descriptors have been present in recent decades, Feature descriptor use in computer vision for the visual features description of the content in image or video. [5] They describe elementary characteristics such as, the color, texture, shape or the motion, among others. [6] In 2001, GIST is the first scene recognition and a typically computed global image descriptor for scene classification purposes over the entire image shown in figure 2.1 is proposed by A. Oliva. [7]

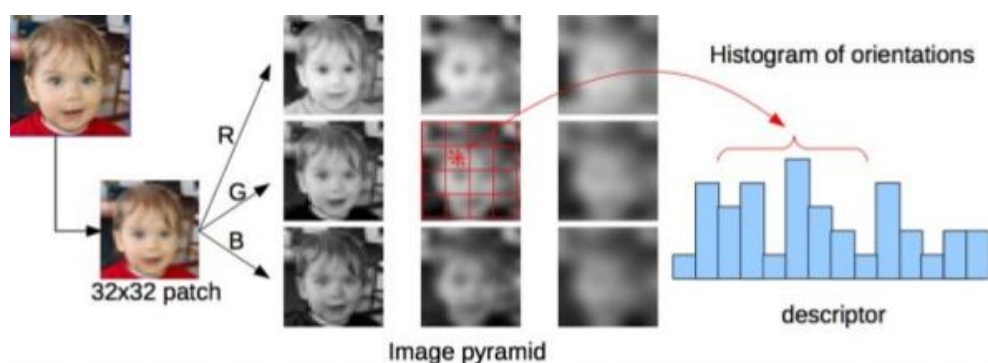


Figure 2.1: The pipeline of GIST feature descriptor [7]