ANALYSIS OF ELECTRICAL CHARACTERISTICS IN STRAINED SI/SIGE N-CHANNEL MOSFET DEVICE

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Thank you to all my families, supervisor and my friends for me to finish this thesis.

ABSTRACT

As scaling down MOSFET devices degraded device performance in term of leakage current and short channel effect. To overcome the problem, some significant changes in device structure and material such as Silicon Germanium (SiGe) was needed for continued transistor miniaturization and equivalent performance improvements. In this project, the performances of strained Si/SiGe n-channel MOSFET device was investigated. Simulation of this device fabrication is being performed by using ATHENA module. Meanwhile the simulation of electrical characteristics is being implemented by using ATLAS module from Semiconductor TCAD tools. Semiconductor TCAD tools are computer programs which allow for the creation, fabrication, and simulation of semiconductor devices. For this device, the results showed that the drive current (Ion), leakage current (Ioff), threshold voltage (Vth) and subthreshold swing (SS) were 631.43μA/μm, 68.54pA/μm, 0.5326V and 84.41mV/dec respectively. Most of the results obtained were within the range and met the requirement of low power (LP) technology for the year 2015 as predicted by International Technology Roadmap Semiconductor (ITRS) 2013. As a conclusion, the design of n-channel Si/SiGe MOSFET device has successfully been created to obtain the low power consumption value

ABSTRAK

Pengecilan peranti MOSFET menjejaskan prestasi peranti dari segi efek saluran pendek dan kebocoran arus. Bagi mengatasi masalah ini, beberapa perubahan yang ketara dalam struktur peranti dan bahan seperti Silikon Germanium (SiGe) diperlukan untuk pengecilan transistor berterusan dan peningkatan prestasi setaraf. Simulasi fabrikasi peranti ini dilaksanakan dengan menggunakan modul ATHENA. Manakala simulasi ciri-ciri elektrik dilaksanakan dengan menggunakan modul ATLAS dari Semikonduktor TCAD. Semikonduktor TCAD adalah program komputer yang membolehkan penciptaan, fabrikasi, dan simulasi peranti semikonduktor. Bagi peranti ini, keputusan menunjukkan bahawa arus pacu (Ion), arus bocor (Ioff), voltan ambang (Vth) dan 'subthreshold swing' (SS) ialah 631.43μA/μm, 68.54pA/μm, 0.5326V and 84.41mV/dec masing-masing. Kebanyakan keputusan adalah didalam julat yang dibenarkan dan memenuhi keperluan yang telah ditetapkan oleh teknologi kuasa rendah (LP) untuk tahun 2015 yang telah ditetapkan oleh 'International Technology Roadmap Semiconductor' (ITRS) 2013. Sebagai kesimpulan, rekabentuk peranti salur-n Si/SiGE MOSFET telah berjaya direka untuk mendapatkan nilai penggunaan kuasa yang rendah

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LIST OF SYMBOLS AND ABBREVIATIONS

V_{TH}	:	Voltage Threshold
I_{ON}	:	Current On State
I_{OFF}	:	Current Off State
SS	:	Subthreshold Slope
DIBL	:	Drain Induced Barrier Leakage
ITRS	:	International Technology Roadmap Semiconductor
SCE	;	Short Channel Effect
SiGe	:	Silicon Germanium

CHAPTER 1

INTRODUCTION

1.1 Background

The transistor MOSFET (Metal Oxide Semiconductor Field Effect Transistor) is a field-effect transistor (FET) with an insulated gate where the voltage determines the conductivity of the device. It is used for switching or amplifying signals. The ability to change conductivity with the amount of applied voltage can be used for amplifying or switching electronic signals. MOSFETs are now even more common than BJTs (bipolar junction transistors) in digital and analog circuits. In this manner, the MOSFET has essentially unending impedance and this makes MOSFET valuable for power amplifiers.

Semiconductor industry has relied on the advance of smaller and faster MOSFET to provide ever better digital electronics products. The main reason to create the transistors become small is increasingly packaging devices in a chip area. This results in a chip with the same features in a smaller area or chips with more features in the

same area. The transistor shrinking to dimensions below 100 nm makes it possible to place hundreds of millions of transistors on a single chip [1]. It is supported by many research nowadays was focusing to obtain a higher speed, low power consumptions and low cost devices.

The purpose for this project is to do a performance analysis of single gate N-Channel MOSFET by strained the silicon. In reducing the short channel effects that occur during the downscaling process of the MOSFET [2]. The project is aimed to design nanoscale of N-Channel MOSFET device using TCAD in generating the current-voltage (I-V) Characteristic, structure and the value of threshold voltage. Therefore, the performance analysis of single gate N-Channel strained with 19 nm channel length is studied and developed using the Silvaco TCAD simulation software.

1.2 Objectives of this project

The objectives of this research are:

i) To design 19nm single gate (SG) N-Channel MOSFET by using ATHENA module in Silvaco TCAD tool.

ii) To analyze the electrical characteristics of strained single gate (SG) N-Channel MOSFET by using Silvaco ATLAS module.

1.3 Problem Statement

Previous, the technology of MOSFET introducing a downscaling of the gate length method to create a better performance of devices. This device is continually scaled down, obeying Moore's Law. Moore's law states that transistors of feature size are scaled down every 18 months at a rate of about 0.7 [3]. The physical gate length is estimated to be approximately 30 percent for each generation [4]. However, due to several physical limitations associated with the device miniaturization, it has become

more difficult. [2]. Therefore, a lot of attention has recently been focused on the technology of improving mobility by applying strain on PMOS channels. By offering 19 nm channel length, the gate leakage current will be affected. To address this problem, some improvement and changes in device structure and material are needed to deliver higher power, faster speed and lower power consumption [2][5].

1.4 Scope of Project

The limitation of this study include the device structure and material that contribute to the design and development of strained silicon single gate N-Channel MOSFET by nanometer scale dimension. Simulation of N-Channel MOSFET device The fabrication is carried out using the ATHENA module while simulating the electrical characteristics of the 19 nm N-Channel MOSFET gate using the ATLAS module where both are using SILVACO TCAD tools. The result that shows in the ATHENA and ATLAS will be refer to ITRS 2013 and the result will be compared the other different thickness of Germanium. The strained silicon device have their potential for achieving higher channel mobility and device current enhancement [2]. In this research, the performance analysis of strained single gateN-Channel MOSFET will carry out to meet the objectives of study.

1.5 Report Structure

This thesis overall has five chapters which are diving into the main chapter such as introduction, literature review, methodology, result and discussion and the last chapter is conclusion and recommendation.

The first chapter explains an introduction, purpose, and scope of this project. The overall overview of the project also will be discussed in this chapter. The second

chapter contains about literature review where some theories and related researchers from other institute is presented.

In chapter three, the simulation by using SILVACO TCAD is carried out. This simulation process will elaborate more on methodology by displaying the method and the implementation for solve a problem during design and develop the MOSFET device structure, material, and their characteristic.

Next, the expected result of the electrical characteristic and performance analysis will elaborate more in chapter four. Finally, in chapter five will specify the conclusion regarding of whole research and recommendation for improvement in future.

CHAPTER 2

LITERATURE REVIEW

This chapter will explain an introduction to MOSFET theories and some of related researches done. Over the 10 years before, MOSFETs have shown remarkable performance improvements by incorporating strained silicon (Si) technology. Due to this achievement, emphasis will be given regarding to the strained silicon technology in N-Channel MOSFET from various research.

2.1 Introduction to MOSFET

The transistor MOSFET (Metal Oxide Semiconductor Field Effect Transistor) is a semiconductor device widely used in electronic devices to switch and amplify electronic signals. The MOSFET is a core of integrated circuit and due to these very small sizes it can be designed and manufactured in a single chip. The MOSFET is a four-terminal device with terminals of source (S), gate (G), drain (D) and body (B).

The MOSFET's body is often connected to the source terminal, making it a three-terminal device such as a field effect transistor [6]. The MOSFET is the most widely used transistor and can be used in both analog and digital circuits. Figure 2.1 illustrates MOSFET's basic structure.

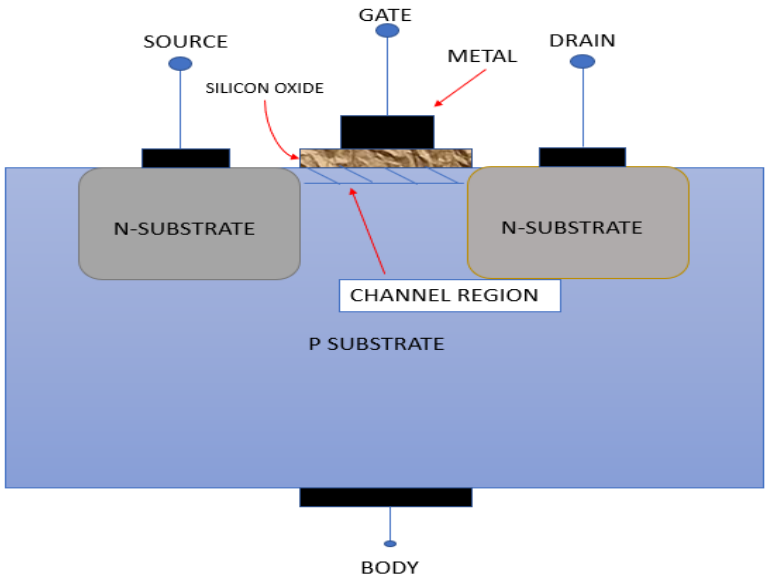

Figure 2.1 Basic structure of MOSFET

The working of a MOSFET depends upon the MOS capacitor. The MOS capacitor is the main part of MOSFET. The semiconductor surface at the below oxide layer which is located between source and drain terminals. It can be inverted from p-type to n-type by applying positive or negative gate voltages. There are three forms when the gate voltage is varied. These three forms are accumulation, depletion, and inversion conditions.

Accumulation occurs typically when a low negative voltage is applied to the gate. Therefore, the negative charge on the gate attracts holes from the substrate to the oxide-semiconductor interface. Next, depletion occurs when a low positive voltage is applied to the gate and results in some positive charge on the gate. The positive charge

on the gate pushes the mobile holes into the substrate, thereby depleting the semiconductor of the mobile carriers and leaving a negative charge in the space-charge region, which is due to the ionized acceptor ions.

The voltage separating the accumulation and depletion regimes is referred as the flat-band voltage. An inversion occurs when a higher positive potential exceeding critical threshold voltage (V_{TH}) is applied to the gate, thus attracting more positive charge of the gate. The holes are repelled further and a small number of free electrons in the body is attracted to the region beneath the gate. In addition to the depletion layer charges, a negatively charged inversion layer forms at the oxide-semiconductor interface. There are commonly three types of n-channel transistor modes, which are cutoff, linear (triode), and saturation modes.

2.2 The Short Channel Effect (SCE)

Starting from the introduction of Intel 4004 microprocessor that appeared in 1971, the number of MOSFETs integrated in the integrated circuit has increased, thus more highly functional device will be built. Unfortunately, when MOSFET head-shrinker below 45nm of logic gate length, it already at its physical limit. Beyond this length, the performance of MOSFET diminish extraordinarily [7]. MOSFET device is considered for facing the SCE when there is some communion of electrical charge between drain, gate and source. The ability of gate in controlling the electron flow become fewer. This happens because the channel length is the same order of magnitude as the source and drain junction depletion layer width. Therefore, the gate is unable to completely shut down the channel in off-mode operation. This result the leakage current increase between the drain and source.

The SCE resulted in the limitation of the electron drift characteristic in the channel and the modification of the threshold voltage due to the shortening channel length. In N-Channel MOSFET technology, the channel leakage current is defined as the current flowing from the drain to the supply voltage V_{DD}, gate, source and bulk ground. It is also known as Off State Current. The phenomenon happens due to diffusion current, which increase as the decreasing feature size. Subsequently, if the drive current increases due to lower the threshold voltage, the leakage current also increase.

Besides, there are others parameter that indirectly contribute to the increment of leakage current such as V_{TH} roll-off and drain induced barrier lowering (DIBL). Drain Induced Barrier Lowering (DIBL) effect is increasingly prominent, due to significant field penetration from drain to source. Since channel length (L) is reduced and the voltage across drain to source (V_{DS}) is increased, the drain depletion region moves closer to source depletion, resulting in field penetration. Because of this field penetration, the potential barrier at the source is lowered, resulting in increased source injection of electrons over the reduced channel barrier, resulting in shifted threshold voltage [8]. The Figure 2.2 shows the type of SCE that can lead to leakage current. The L1 reversed bias p-n junction leakage and L2 is weak inversion current. Meanwhile, the L3 in this figure is gate leakage and L4 is gate current due to hot carrier injection. The L5 is gate induce drain leakage and L6 channel punch through current.