MULTI INPUT ZVS CONVERTER FOR RENEWABLE ENERGY

WONG JIAN LOONG

BACHELOR OF ELECTRICAL ENGINEERING WITH HONOURS
UNIVERSITI TEKNIKAL MALAYSIA MELAKA

2019

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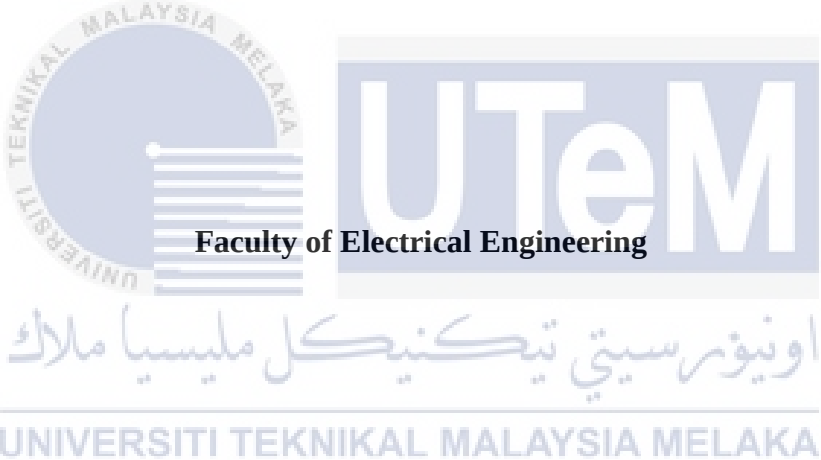
A report submitted
in partial fulfillment of the requirements for the degree of
Bachelor of Electrical Engineering with Honours



Faculty of Electrical Engineering

UNIVERSITI TEKNIKAL MALAYSIA MELAKA

2019

DECLARATION

I declare that this thesisentitled “MULTI INPUT ZVS CONVERTER FOR RENEWABLE ENERGYis the result of my own research except as cited in the references. The thesis has not been accepted for any degree and is not concurrently submitted in candidature of any other degree.

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Signature : .....

Supervisor Name : .....

Date : .....

DEDICATIONS

To my beloved mother and father

ACKNOWLEDGEMENTS

I was conducted many researches from online journals, articles and internet sources in order to get information about my project title to improve my understanding about the title in order to design and analyse the product. Besides, the researches also provide some information to me in order to write and prepare this report which present all the information about the product which include how to design, analyse and comparison about what components will be suitable for the product and what methods will be suitable to analyse and design the product. .Moreover, I'm also very thankful to my supervisor PROFESOR MADYA DR KASRUL BIN ABDUL KARIM for his guidance , advices and motivation. He gives some ideas and information to me when I face some problems such as simulation problems. He also put full attention to check my progress works and my report. Without his support and interest, this project would not have been same as presented here.

ABSTRACT

This report discussed about the design and the simulation of a multi input ZVS phase shift full bridge DC to DC converter to overcome the problem that face by renewable energy by using MATLAB/ SIMULINK software. The first problem that need to solve is the unstable and overload output voltage produce by renewable energy that cause load disturbance. So, to solve this problem, firstly phase shift full bridge DC to DC converter have designed to overcome it by using phase shift modulation of the pulse signal of the lagging leg switches respect to leading leg switches. The second is apply ZVS technic to solve the switching losses due to PSM of the pulse signal of the switches to regulate the output voltage. The third is develop a close loop phase shift full bridge DC to DC converter by using PI controller to overcome the fluctuate of the input voltage from the renewable energy that cause load disturbance. The full bridge phase shift ZVS DC to DC converter will choose because it can handle high power and high voltage. The high frequency operation for the use of MOSFET switches also allow the system operate in high frequency in order to reduce the conduction loss hence improve system efficiency. The three objectives have been achieved by using MATLAB/ SIMULINK software which the first objective where design a single phase phase shift full bridge DC to DC converter which can regulate the output voltage by PSM of the pulse signal of the switches when load disturbance occur. Second, the ZVS technic have been carry out to apply in this converter to improve the system efficiency during PSM of the pulse signal of the MOSFET switches and third a controller have been apply to regulate the output voltage automatically by undergo PSM at the pulse signal of the switches when there is fluactuate of the input voltage from the renewable energy.

ABSTRAK

Laporan ini dibincangkan mengenai reka bentuk dan simulasi input pelbagai ZVS fasa peralihan jambatan penuh DC ke DC converter untuk mengatasi masalah yang dihadapi oleh tenaga boleh diperbaharui dengan menggunakan perisian MATLAB / SIMULINK. Masalah pertama yang perlu diselesaikan adalah voltan keluaran yang tidak stabil dan dihasilkan oleh tenaga boleh diperbaharui yang menyebabkan gangguan beban. Jadi, untuk menyelesaikan masalah ini, peralihan fasa pertama jambatan penuh DC ke DC converter telah direka untuk mengatasinya dengan menggunakan modulasi peralihan fasa isyarat denyut suis kaki ketinggalan berkenaan dengan suis kaki terkemuka. Yang kedua adalah menggunakan teknik ZVS untuk menyelesaikan kerugian beralih disebabkan oleh PSM isyarat denyut suis untuk mengatur voltan keluaran. Yang ketiga adalah mengembangkan fasa gelung jarak pergeseran jambatan penuh DC ke DC converter dengan menggunakan pengawal PI untuk mengatasi turun naik voltan input dari energi terbarukan yang menyebabkan gangguan beban. Fasa fasa jambatan penuh ZVS DC ke DC converter akan dipilih kerana ia boleh mengendalikan kuasa tinggi dan voltan tinggi. Operasi frekuensi tinggi untuk penggunaan suis MOSFET juga membolehkan sistem beroperasi dalam frekuensi tinggi untuk mengurangkan kehilangan konduksi dan seterusnya meningkatkan kecekapan sistem. Tiga objektif telah dicapai dengan menggunakan perisian MATLAB / SIMULINK yang objektif pertama di mana mereka bentuk fasa fasa tunggal beralih sepenuhnya jambatan DC ke DC converter yang dapat mengawal voltan output oleh PSM dari isyarat nadi suis apabila gangguan beban berlaku. Kedua, teknik ZVS telah dilaksanakan untuk digunakan dalam penukar ini untuk meningkatkan kecekapan sistem semasa PSM isyarat denyut suis MOSFET dan ketiga pengawal telah digunakan untuk mengawal voltan keluaran secara automatik dengan menjalani PSM pada isyarat nadi suis apabila terdapat voltan masukan dari tenaga yang boleh diperbaharui.

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LIST OF SYMBOLS AND ABBREVIATIONS

D	-	Duty Cycle
PSM	-	Phase Shift Modulation
PWM	-	Pulse width Modulation
DC	-	Direct Curent
AC	-	Alternating Current
V	-	Voltage
	-	
	-	

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CHAPTER 1

INTRODUCTION

1.1 Project Overview

The title of this project is multi input zero voltage switching converter for renewable energy. Nowadays, the world have changed to use renewable energy as the alternative source for the electrical appliances. There are few types of renewable energy that use as the alternative source such as solar energy, wind energy, biomass energy and also fuel cell. By using these renewable energy as the alternative source for the electrical appliances, there allow to save the cost of electrical bill but sometimes there will faced some problems such as unstable output voltage produce due to the weather conditions. For example, for solar system, the voltage accumulated depends on the sunlight. If the sunlight is unstable the voltage accumulate will be unstable and load disturbance will occur. So it is not suitable to supply for the electrical appliances and sometimes will cause the load burn.

To overcome this problem, a converter is designed to regulate the output voltage from the renewable energy source before supply to the load. There are various types of converters such as DC to AC converter (inverter), AC to DC converter and DC to DC converter (chopper). For this project, a DC to DC converter use because the voltage supply from renewable energy is DC. There are two types of DC to DC converter which are isolated and non-isolated DC to DC converter. The three main types of non-isolated DC to DC converter are buck converter, boost converter and buck-boost converter. These three types of converters have limitation which buck converter only can step down the input voltage, boost converter only can step up the input voltage and for buck-boost converter it can either step up or step down the input voltage but the output voltage produce is always in negative. For isolated DC to DC converter, such as fly back and forward converter, there can step up or step down the input voltage by using the transformer and use transformer to

store energy compare to non-isolated DC to DC converter that use inductor to store energy. The output voltage produce by isolated converter is in positive and the phase shift of the pulse signal of the switches of the converter also can apply to step down the input voltage when overload occur.

So, for this project, an isolated DC to DC converter which is a phase shifted full bridge DC to DC converter will be use. The DC input voltage must be convert to AC before the transformer going to step up or step down the input voltage to a specific value. Then it will convert to DC back before supply to the load. The construction of the circuit of the converter will be discuss in the literature review at chapter 2. Inside the converter it consist of transformer to step up or step down the DC source input voltage which use to supply single phase load. Not only that, the converter consists of switches which use for switching mode and what types of switches and transformer use will be discuss in the literature review later. Below figure 1.1 shows the basic topology of phase shift full bridge DC to DC converter.

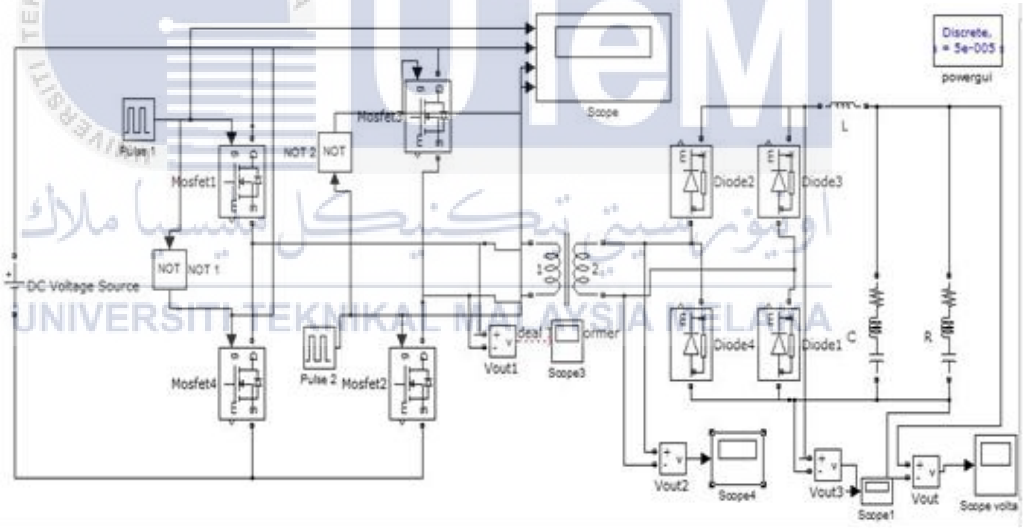


Figure 1.1: the basic topology of phase shift full bridge DC to DC converter

Besides, the second problem which faced when using renewable energy as alternative source is sometimes switching and conduction loss will occur during convert and regulate the output voltage by undergo pulse width modulation (PWM) and phase shift modulation (PSM) for the pulse signal at the switches of the DC to DC converter [1].

To overcome this problem, there is need to apply zero voltage switching (ZVS) which state at the title of this project. The zero voltage switching phase shifted full bridge DC to DC converter is apply to overcome this problem. Zero voltage switching phase shifted full bridge DC to DC converter mostly use in high power and voltage applications. This converter able to handle high power and voltage with low switching and conduction loss [1]. The phase shift feature of the control signal allow ZVS and it able to eliminate the switching loss during FET device transition and this can increase the system efficiency also. ZVS on the phase-shifted PWM control signal can also minimize the parasitic effect so that the conduction loss will be reduced because the converter operate at high switching frequency.

Phase shifted PWM full bridge converter consists of two parts. The first part consists of the DC to AC H bridge converter and the high frequency transformer, and the second part is the AC to DC part. For the first part, the input DC voltage from the renewable energy will be convert to AC by using the DC AC H bridge before going to step up or step down to a desire output voltage that need for the load. The phase shift application of the converter is use to regulate the desire output voltage when there is load disturbance occur due to unstable input voltage which phase shift the pulse signal of the lagging leg switch S2 respect to leading leg switch S1 as shown in figure 1.1. After the AC voltage have been step up to a desire output voltage need for the load and the AC voltage will convert back to DC by using the second part which is AC to DC part.

Besides, to improve the input voltage and power in order to produce enough output voltage and power to supply for the load, a multi input from different sources or same sources of renewable energy can be apply at the input. For multi input, it is easier to achieve the desire output voltage and power need compare to single input. This is because more voltage and power store at the input for multi input.

1.2 Motivation

Nowadays, renewable energy such as solar energy, biomass, wind energy and fuel cell are popular in the world and many place such as residential and industries had applied to reduce the use of electrical energy from govournment to safe the

electrical bills. Not only that, renewable energy also environment friendly which conserve the environment by saving the use of energies. However, there are some problems that faced when use renewable energy to generate electricity which is the unstable output voltage produce due to unstable input voltage. Hence, this is the point that motivated to carry out this project to design a converter to regulate the input voltage from renewable energy in order to achieve the desire output voltage.

Besides, if the output voltage is regulated by using phase shift modulation of the pulse signal of the switches of the converter, the efficiency of the system will be decrease. So, this also motivated to undergo this project to carry out to apply zero voltage switching technic (ZVS) to the switches of the converter in order to improve the system efficiency.

1.3 Problem Statements

The purpose that construct a multi input ZVS converter for renewable energy is to overcome the following problems.

Firstly, the voltage accumulate from the renewable energy is unstable and the voltage is not suitable to supply for the load. This is because the voltage accumulate for the renewable energy such as solar panel use is depends on the weather condition. If the weather condition is change, the voltage accumulated will be unstable and this will cause the output voltage that supply to the load will be unstable or load disturbance will occur.

The second problem is the conduction and switching loss occur in the converter during convert and regulate the output voltage from the source of renewable energy by undergo pulse width modulation (PWM) or phase shift modulation(PSM) for the pulse signal of the switches due to unstable input voltage from the renewable energy. Sometimes there is unstable or overload voltage accumulate at the source of renewable energy during bad weather conditions.

These unstable output voltage from the source of renewable energy will not regulate by the converter because the input voltage and the ratio for the transformer

have been set and fix. For example the input voltage have been set to 24 V and the ratio is 1:10 so the output regulate voltage will be 240. So if there is unstable input voltage, the converter cannot be control and the PWM or PSM for the pulse signal of the switches is need to solve this problem. During PWM or PSM for the pulse of the switches, the conduction loss and switching loss will occur, so ZVS for the pulse signal of the switches after PWM modulation is use to solve this problem.

1.4 Objectives

i) To overcome the problem of unstable output voltage produce from the renewable energy, a ZVS full bridge phase shift DC to DC converter is designed to overcome this problem by undergo PSM or PWM on the pulse signal of the switches.

ii) To overcome the problem of switching and conduction loss on the switches when undergo PSM or PWM on the pulse signal of the switches. A ZVS operation for the phase shifted full bridge DC to DC converter is apply to overcome the problem of switching and conduction loss in the MOSFET switches of the converter due to PSM of the pulse signal of the switches to regulated the input voltage.

iii) To design a controller to auto regulate the pulse signals of the switches to achieve the desire output voltage need when the input voltage is fluctuated. The controller will responsible to determine the amount of phase shift that need for the pulse signal of the switches in order to reach the desire output voltage need to supply to the load by varies input voltage.

1.5 Scope

In this report, a phase shift full bridge ZVS DC to DC converter is design only for single phase load by using MATLAB/ SIMULINK software. The load that suitable for this converter is small DC motor such as DC water pump that use to pump water. Not only that, to undergo ZVS for this converter, it has the limit of input

voltage range in order to produce the reference output voltage. The range of input voltage from 350 V DC to 400V DC in order to produce the reference output voltage of 150 V DC . ,If the input voltage is out of the range, the ZVS operation to reduce the switching losses due to PSM of the pulse signal of the switches unable to carry out. The output voltage also unable to maintain at 150V reference voltage. To overcome the problem of fluctuated of the input voltage, the PI controller is use.

CHAPTER 2

LITERATURE REVIEW

2.1 Basic Operation Of The ZVS Phase Shifted Full Bridge DC To DC Converter

The purpose to develop a ZVS phase shifted full bridge DC to DC converter is to overcome the switching loss and conduction loss during FET devices transition when there is undergo PSM or PWM on the control signal of the switches when there is unstable output voltage produce from the source of renewable energy. As Oladimeji [1,14] points out that the phase shifted PWM full bridge converter consists of two states which the first stage is DC- AC bridge converter which consists of four gate switches and a transformer. At this stage, the input DC source from the renewable energy will direct flow to the H bridge and convert to AC before flow to the transformer to step up or step down the voltage to a desire value that need for the load. The transformer use must be high frequency transformer. The second stage is the AC- DC part which consist of several diodes and to converts the output AC voltage from the transformer to DC voltage and supply to the load.

Generally, there are many ways to regulate the unstable output voltage before it supply to the load. For example, adjust the winding ratio of the transformer is the first way. As Nor Zaihar Yahaya [1] points out that pulse width modulation for the pulse signal of the switches is more easier. Moreover, from [2], state that phase shift modulation (PSM) also can apply to the pulse signal of the switches to regulate the output voltage which phase shift of the pulse signal of the lagging leg switches respect to the pulse signal of the leading leg switches.

In [1], FET devices are the backbone of the converter and contain non- linear characteristic which having parasitic parameters effect more pronounce at high frequency. For this characteristics, it helps give the system operate at high efficiency.

Moreover, in [1], for high power application, mostly full bridge converter will be use compare to half bridge because full bridge converter able to own its high power handling capacity due to the number of FET switches. Not only that, full bridge converter that consists of four FET switches improve the smoothness and efficiency of the system.

However, due to the pulse width modulation or phase shift modulation on the pulse signal of the switches to regulate the output voltage before supply to the load due to the unstable input voltage will directly effect the efficiency of the system due to switching and conduction loss and so decrease system efficiency. In [1,15], during undergo pulse width modulation or phase shift modulation on the pulse signal of each switches, the conventional full bridge converter operation turn the diagonal pair switches at a dead time. From this, hard switching occur and cause high switching losses [1]. By the way there is a dead time where all the four switches turn into off state for a period of time. By this, the load current will be freewheels through the rectifier diodes at the AC to DC site of the converter and cause the energy stored in the leakage inductance which located at the primary site of the transformer [1]. This phenomena give some ringing correspond with FET switches junction capacitance [1]. By eliminate high power switching loss, the phase shifted PWM pulse signal of the FET switches will allow ZVS to carry out on the FET switches during turn on.

2.2 Comparison Of Topology Of The ZVS Phase Shifted Full Bridge DC To DC Converter

In this section, the comparison of the switches use at the DC to AC H bridge and the type of transformer use as the isolated transformer will be discussed.

2.2.1 The Comparison Of the Topology Of The ZVS Phase Shifted Full Bridge DC To DC Converter With Different Types Of Switches

In [1], ZVS can be carry out by placing a snubber capacitor across each FET switches and a leakage inductor insert in series with the transformer and the parallel inductor is the magnetizing inductor of the transformer. However, in [2], Praveen state that the snubber capacitance have probability to become the internal drain to

source capacitor of the MOSFET. So, the connection make the circuit of the converter very simple. The connection of the inductor in series with the transformer will loss the ZVS capability at light load condition. The inductor in parallel connection will loss ZVS under short circuit. So, the loss of ZVS of the ZVS phase shift full bridge DC to DC converter will result in the size of heat sink need to increased , the reverse recovery current of the body diodes will reduced the reliability, and the high differentiate of the current of the snubber discharging current respect to time will result higher EMI.

In [2,4,5,17], to overcome the problem as state, an IGBT full bridge circuit developed as an alternative full bridge converter topology. This topology control by bidirectional switches that employed at each leg of the full bridge to achieve ZVS of the main switches. For this topology that use ICBT switches, it is suitable for lower power application which is lower than 3kW [2].This topology is very attractive for telecommunication application such as rectifier for central power plants. This is because even for all operating conditions either open or short circuit, this topology will provide ZVS for all the switches. In various of circuit analysis, this design of this type of converter not given in detail.

However, in [1], the MOSFET was choose as the switches of the converter. This is because for MOSFET, although it can handle low power capability but also can up to 3kW and operate in high frequency. Due to this two characteristics of MOSFET switches, the topology of the ZVS phase shift full bridge PWM DC to DC converter with MOSFET switches will be more suitable for high power and high voltage applications for this project which the load is up to 3 kW. The high frequency operation will minimise the parasitic effect and conduction loss. Hence, MOSFET switch choose as the switches for the AC to DC H bridge.

2.2.2 The Comparison Of The Topology Of The ZVS Phase Shifted Full Bridge DC To DC Converter With Different Types Of Transformer

For the phase shift full bridge DC to DC converter, there are various types of transformer that can be use such as ideal transformer, linear transformer and centre tapped transformer. Mostly, the types of transformers that apply in this converter are

ideal transformer and linear transformer. In [1,3,16], an ideal transformer have been choose to apply in the design a ZVS phase shifted full bridge DC to DC converter. Usually, there is no advantages, and disadvantages between the apply of linear or ideal transformer in the design of the converter. The only different between these two transformer are the setting of the ratio of the primary winding and secondary winding depends of the input voltage of the converter and the output voltage need and also the topology of the converter will be different. The setting of the ratio of the primary and secondary windings of ideal and linear transformer are different. The model of ideal and linear transformer have shown figure below.

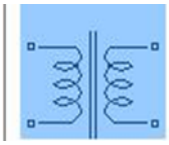


Figure 2.1: Ideal transformer

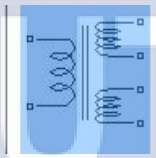


Figure 2.2: Linear transformer

For ideal transformer, it consist of two windings which are primary and secondary winding. The equation that describe this transformer is V1= N *V2 and I2= N* I1. Where V1 and I1 stand for primary voltage and primary current respectively, V2 and I2 stand for secondary voltage and secondary current respectively and N is the ratio of the secondary to primary turn. So, when an ideal transformer apply in the converter, the ratio N need to tuned in order to get the desire output voltage base on the input voltage.

For linear transformer, it consists of one primary winding and two secondary windings. There are some different on the setting of the ratio of the windings for linear transformer. As long as the linear transformer consists of two windings on the secondary side, so if the ratio selected is one to one, it means that the secondary output voltage will be two times the input voltage. This is because the one to one ratio represent that the primary winding to the first winding of the secondary

side and also one to one ratio to the second winding of the secondary side. The total ratio is one to two.

Between there is also have different of the topology of the converters that use ideal transformer and linear transformer. For the use of ideal transformer, there are 4 diodes that need to apply in the AC to DC side of the converter at which convert the step up AC voltage to DC before supply to the load. This is because for ideal transformer, there is only one output winding and contain terminals which are positive and negative terminal. So, in order to convert the AC step up output voltage to DC, the AC to DC circuit need two diodes for the positive cycle at the positive terminal and two diodes for the negative cycle at the negative terminal. For linear transformer, as long as it consists of two winding at the output terminal which contain two positive and two negative terminals. For this features, there is only two diodes need at the AC to DC side. This is because the two positive terminals is connect to one diode to produce positive cycle while the two negative terminals will connect to one diode to produce negative cycle. So, an ideal transformer will choose as the isolated transformer although it make the circuit more complex which need 4 diodes to connect at the AC to DC bridge but it is more simple to set the parameters such as windings ratio and this make the calculation for the windings ratio that need for the converter to undergo ZVS more simple. The topology of the ZVS phase shifted full bridge DC to DC converter with linear and ideal transformer have shown in figure below.

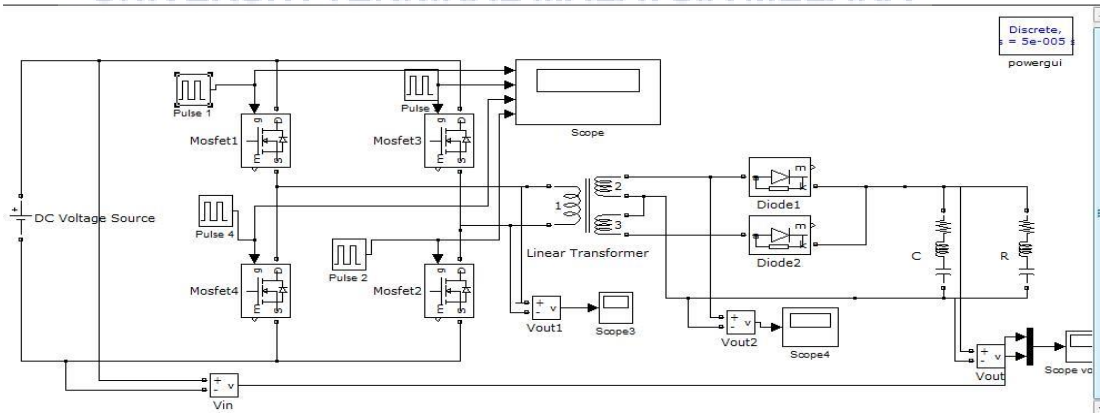


Figure 2.3: Topology of the ZVS phase shifted full bridge Dc to Dc converter with Linear Transformer

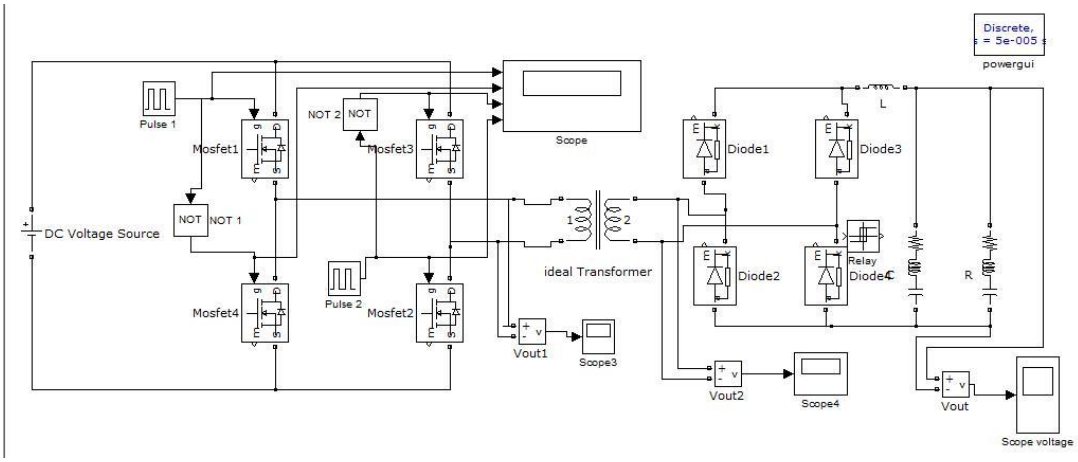


Figure 2.4: Topology of the ZVS phase shifted full bridge DC to DC converter with ideal transformer

2.3 Steady-state Analysis Of Phase Shift Full Bridge ZVS DC-DC Converter

The topology of the full bridge DC-DC converter as shown as figure 2.4 above consists of one lagging leg and one leading leg. For leading leg, the pair of switches are S1 and S4 and for lagging leg, the pair of switches are S2 and S3 [1, 3]. To regulate the output voltage, the phase shift modulation of the signal pulse of switches at the lagging leg will adjusted and the switches at the leading leg will stay [1]. From this the phase shift of the pulse signals of switches S2 and S3 respect with the pulse signals of switches S1 and S4 allow to control the output voltage depends on how much phase shift and how much pulse width remains after undergo phase shift. The more it shift, the duty cycle will be decrease more and the output voltage remain will be less. The relationship in [3], due to this phase shift modulation of the signal pulse of the switches allow switching for the MOSFET switches with ZVS by using the junction capacitance and transformer leakage inductance energy. Below figure 2.5 shows that the PWM gating switching control signal to the H bridge inverter lagging leg that undergo phase shift with respect to the switches at the leading leg [1,3].

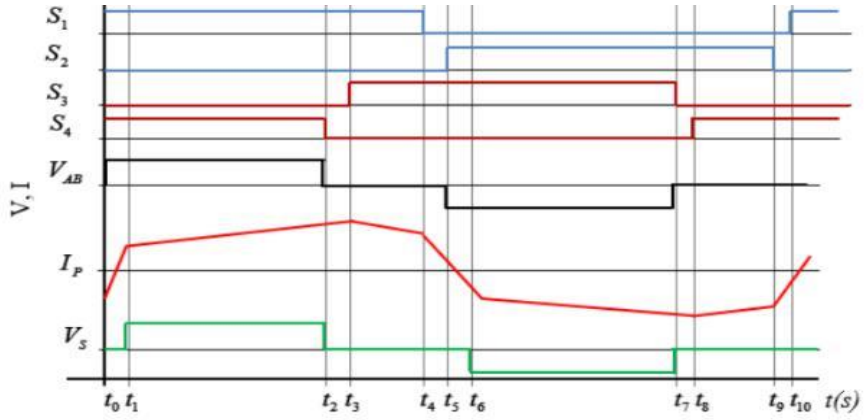


Figure 2.5:Basic waveform of phase shift full bridge ZVS DC-DC converter

From figure 2.5 above, it shows that the switches S2 and S3 at the lagging leg will turn on complimentary with 50 percent duty cycle minus the short dead time [1, 3]. Know, the parameters that need to determine to analyse the phase shift full bridge ZVS DC to DC converter will be discussed [3]. Firstly, the output voltage produce by the converter, V0 of the phase shift full bridge ZVS DC to DC converter will be analyse by using the formula(1).

$$V0 = Vin\ (Ns/Np)\ Deff \qquad (2\text{-}1)$$

From the formula above Vin is the input voltage for the converter, Ns is the number of turn of the secondary side of the isolated transformer, Np is the number of turn of the primary side of the isolated transformer, and Deff is the secondary side duty cycle. For the duty cycle, the duty cycle that located at the secondary side of the converter will be lower than the duty cycle that located at the primary side. This phenomena is due to the rising and falling edge of the primary current when the MOSFET switches of the converter undergo ZVS transition as shown in figure 2.5 [3,6]. Since the current does not change instantaneously when flow through the leakage inductance that located at the primary side of the isolated transformer, the duty cycle that located at the secondary side of the isolated transformer will decrease and less effective because of the rising and falling edge of the primary current. So, the primary duty cycle, D will be equal to Deff plus delta D, where delta D is the duty cycle loss due to the rising and falling edge of the primary current. So, from formula (1), the Deff is the effective duty cycle of transformer secondary voltage.

Next, the leakage inductance energy, EL also need to analyse. The leakage inductance energy must be equal or more than the total capacitive energy of the MOSFETs devices' snubber capacitance in order to achieve ZVS operation. The switches S1 and S4 at the leading leg that undergo zero voltage switching will depends on the leakage inductance energy and also the total inductive energy which allow ZVS transition operation is as (2-1)

EL = ELK=1/2 LlkI2 (2-2)

Where EL and ELK are the leakage inductance energy and the total inductive energy respectively. Lk is the value of the leakage inductance and I2 is the primary current of the converter.

For the switches at the lagging leg which are S2 and S3 the transformer magnetizing inductance energy, ELM , leakage inductance energy, ELK, and the reflect output inductance energy , ELo will be use to determined the requirement for ZVS operation [7]. So, the total energy that require for ZVS operation is given by:

$$E_{L-B} = \frac{1}{2} L_M I_{M(pk)} + \frac{1}{2} L_{lk} I_2^2 + \frac{1}{2} L_o \left(\frac{N_p}{N_s} \right)^2 \left(I_{Lo(\max)} \frac{N_s}{N_p} \right)^2 \quad (2\text{-}3)$$

Where LM and IM are magnetizing inductance and magnetizing current respectively.

Moreover, the minimum dead time of the td for the MOSFET switches also need to analyse to complete the zero voltage switching transition. This minimum dead time is require to allow the resonance of MOSFET switches switching transition in each pair of leg. The charging and discharging of the MOSFET switches' snubber capacitance is control by the dead time which also depends on the resonant circuit parameters. The formula that use to analyse the resonant frequency to allow zero voltage switching operation for all switches is given by:

fr =1/(2pi)(Llk Ct)1/2 (2-4)

Where Ct = 2Coss(tr) + CTX.

The minimum dead time of the switches that require for zero voltage switching operation is given by :

$$t_d \geq \frac{\pi}{2}\sqrt{L_{lk}(2C_{oss(tr)} + C_{Tx})} \quad (2\text{-}5)$$

Where Coss(tr) is the MOSFET switches energy that in the nonlinear drain to source output capacitance which is snubber capacitance and CTX is the transformer capacitance.

From [3], the switches at lagging leg will be more effective to undergo zero voltage switching operation compare to the switches at leading leg. This is because of the lagging leg have sufficient energy from leakage inductance energy and also the output inductor for switching as shown as the formula (3). While the switches at leading leg only depends on the transformer leakage inductance energy.

Lastly, from [3,7], it also consist of the minimum load current which allow for zero voltage switching operation. That means, it has a range of the load current that allow for zero voltage switching for the converter and zero voltage switching operation will not available when the load current is reduce to a certain level by undergo phase shift for the pulse signal of the switches.

The critical current which is the minimum load current that require for zero voltage switching operation is given by:

$$I_{crit}^{\ 2} = \frac{2}{L_{lk}}\frac{1}{2}(2C_{oss(er)} + C_{Tx})V_{in}^{\ 2} \quad (2\text{-}6)$$

Lets assume the energy store in the drain to source output capacitance of the MOSFET switches is linear and the critical current is known and the require leakage inductance can be calculate as :

$$L_{lk} = \frac{C_t V_{in}^{\ 2}}{I_{crit}^{\ 2}} \qquad (2\text{-}7)$$

Above are the steps that require to undergo steady state analysis of phase shift full bridge DC-DC converter from [3]. From [1], there are some different ways and steps to undergo the steady state analysis and the step will be discuss below.

In [1], to analyse the converter, there have some different and more detail compare to [3]. The first step is to analyse the number of primary turn of the high frequency isolated transformer. The number of primary turn of the transformer is given by:

$$N_p = \frac{V_{in(\min)} D}{2B_{\max}(G)A_c(cm^2)f_s(\mathrm{Hz})} X10^8 \qquad (2\text{-}8)$$

Where Vin(min) is the minimum input voltage to the converter normally is the nominal input voltage, D is the maximum duty cycle of the converter. From [1] , there is some losses produce by the isolated transformer and it need to reduce. To reduce these losses, the magnetic flux of the magnetic core of the isolated transformer and the cross area must be determine . So, these two parameters will be determined in order to set the transformer's primary turns by using formula (1) above. Normally, to reduce the losses, the maximum flux density of the magnetic core of the transformer will set at 0.2 T (2000G) and the cross section area use AC will set to 1.5 centimetre square. The material of the magnetic core will be ferrite material which with low saturation flux density that suitable for the maximum magnetic flux of the 0.2 T.

Next, the maximum secondary voltage of the converter will be set in order to meet the require output voltage of the converter. The secondary voltage of the converter must be satisfied the condition given by:

$$V_{\text{sec}} \geq \frac{V_o}{D_{\max}} \qquad (2\text{-}9)$$

Where Vo is the output voltage requirement and Dmax is the maximum duty cycle. That means, for a phase shift full bridge ZVS DC –DC converter, it is a must to set a range of output voltage that needed in order to determined the maximum duty cycle that need when undergo phase shift of the pulse signal of the MOSFETS switches. For a desire output voltage need, the secondary voltage must be set in order to satisfy (2). This is because the voltage drop across the circuits elements such as the capacitance at the load side that use to reduce output voltage ripple and the output inductance at the secondary side of the transformer [1, 8].

Moreover, the number of turn of the secondary side of the isoalated transformer can be determined by:

$$N_s = N_p \frac{V_{\text{sec}}}{V_{in(\min)}} \qquad (2\text{-}10)$$

Where the Np primary turn of the transformer, Vsec of the transformer and the Vin(min) of the converter have been known.

Next, the voltage across the output inductor that use to filter the ripple voltage will also determine by (nVin – Vo) in order for the converter to achieve zero voltage switching. Where n is the ratio of turn of the isolated transformer The output filter inductance also can be determined by :

$$L_o = \frac{(nV_{in} - V_o)D_{eff}}{\Delta I_L f_s} \qquad (2\text{-}11)$$

Where delta IL is the ripple current and need to be assume normally assume more smaller will be suitable, for example 1.5A. The fs is the switching frequency and also need to be assume. For switching frequency, normally will set higher in order to improve the system efficiency, for example 100kHz. In [1], if the output inductor current ripple is 20percent of the output load current, the output filter inductor will be 1.605 mH.

Besides, the output filter capacitor at the load side will be determined also in order achieve zero voltage switching frequency of the converter to improve the system efficiency. To determine the requirement value of the output filter capacitor, there is the same way that use to determine the value of the output filter inductor and the only different is for output filter capacitor it need to assume the output voltage ripple. The output voltage ripple is assume and same as output current ripple will be a less value, for example 1V. From [1], the output voltage ripple that suitable in order to achieve system efficiency is also 1V which is 0.25 percent of the output voltage requirement. The formula that use to determine the output filter capacitor is given by:

$$\Delta V_c = \frac{V_o(1-D_{eff})}{16 f_s^{\,2} C L_o f_s} \qquad (2\text{-}12)$$

Where the switching frequency, output filter inductor and the output ripple voltage have been known and the output filter capacitor can be determined.

Finally, this is the same parameter as [3] that have been analyse for the phase shift full bridge ZVS DC to DC converter in order to achieve zero voltage switching operation which is resonant frequency fr. The formula use is same which is given by:

$$f_r = \frac{1}{2\pi\sqrt{L_{lk} C_r}} \qquad (2\text{-}13)$$

In [1] , the transition of the voltage across the drain source require the minimum frequency at least one quadrant of resonant period (Tr/4). That means td must be greater than Tr/4. From [1], the minimum value of td is 200ns, so the value

of the leakage inductance also can calculate by given formula below then only calculate fr.

$$L_{lk} = 4t_d^{\,2} / \pi^2 C_r \qquad (2\text{-}14)$$

2.4 The Zero Voltage Switching Operation Of The Phase Shift Full Bridge ZVS DC – DC Converter

From [1], the zero voltage switching operation of the phase shift full bridge DC to DC converter have been discussed by follow each of the period interval of the PWM phase shift full bridge converter waveform from the figure 2.5 above.

The waveform presented the operating waveform of the gating control signal of the pulse signal of the MOSFET switches and also the waveform of the steady state transformer primary and secondary. Besides, the different transition mode of the power circuit for a complete switching period from t0 to t10 also briefly explained as follows. The number of switch will be different for the following explanation because the use of new diagram of the topology of the converter. The topology is same as previous figure 2.4 and the different is just the number label for the MOSFET switches.

Firstly, the period from t0 to t1 which call duty cycle loss period will discussed. During this period, The switch S1 and S4 will be in on state which is positive cycle. At this mode with ZVS the switch S1 will turned on following end of mode t10. At this interval, the transformer secondary voltage Vs will remains zero. Once the primary current Ip turn from negative direction to positive direction, the reflected output inductor current nILO will reach since the primary current rise. This can be reach at t1.

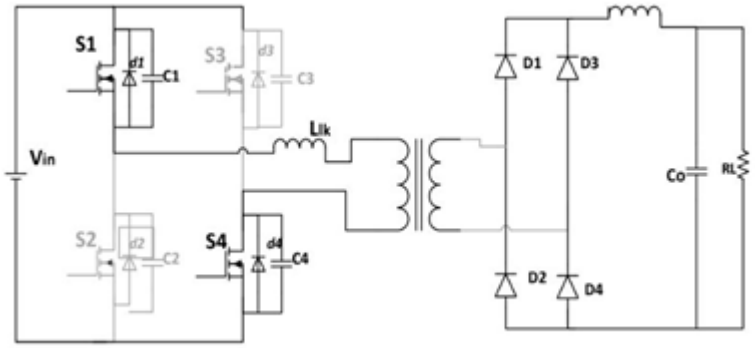


Figure 2.6: the converter in the interval t0 to t1

Next, at interval t1 to t2, in this interval, its called power delivery mode. During t1, the transformer secondary voltage equal to nVin since if the ratio of the transformer set to 1:1. For the secondary AC to DC side, the rectifier diode D1 and D4 will be in forward biased. So, a positive cycle of output voltage will produce. The converter will transfer power from source to load at this interval. From t1 to t2, the effective phase shift duty cycle will be start. So at this interval, the primary side duty cycle will be different with secondary side duty cycle since the rising and falling edge of the primary current that have been discussed previously. The output filter allow the current across it to rise and the primary current Ip will then equal to the reflected output inductor current nI_{LO}.

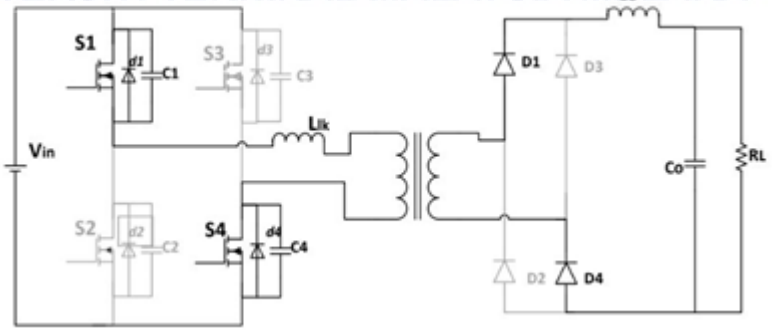


Figure 2.7: The converter in the interval t1 to t2

Next, at interval t2 to t3, this interval called zero voltage switching mode for switch S3. At t2, the switch S4 will be turn off. And the snubber capacitance at the switch S4 will be charged by the primary current Ip , while the snubber capacitance of switch S3 will be discharged from Vin to zero voltage. This cause the body diode

d3 start to conduct to achieve zero voltage switching for switch S3. For this phenomena in this interval, the switching losses and conduction losses when tune the output voltage requirement by phase shift of the gate signal pulse of the switches will be eliminated. Moreover, the transformer secondary voltage will become zero and the primary current reduced and free wheel through diode D1 and D4 at the AC to DC bridge rectifier at the secondary side of the converter.

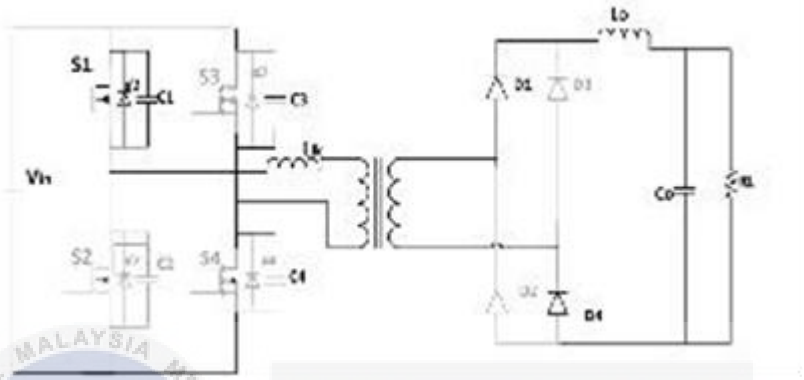


Figure 2.8: The converter in the interval t2 to t3

Next, at interval t3 to t4, at this interval, its called freewheeling mode of the converter. At t3, due to ZVS and the switch S3 is turned on, the primary current will freewheel through switch S1 and S3 and the transformer secondary voltage will still remains zero. Since the primary current decrease to a certain level and the transformer secondary voltage become zero, the output inductor voltage will discharged by the load at this interval.

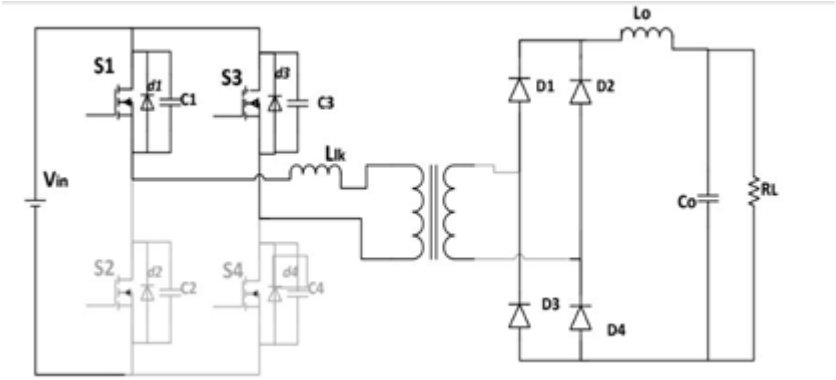


Figure 2.9: The converter in the interval t3 to t4

Next, for t4 to t5, at this interval , the switch S2 will undergo zero voltage switching. At t4, the switch S1 will be turned off and the snubber capacitor of switch S1 will be charge by the primary current Ip. While the snubber capacitance of switch

S2 will be discharge and the voltage will be discharge from Vin to zero also. At this interval, the body diode, d2 will start to conduct to achieve zero voltage switching for the switch S2 and the secondary voltage will still remains zero at this interval.

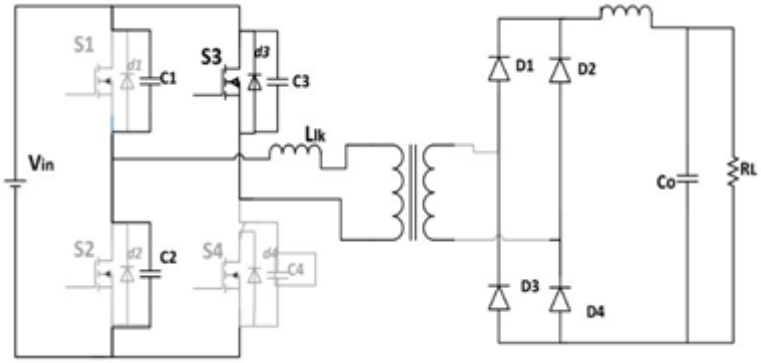


Figure 2.10: The converter in the interval t4 to t5

Next, from t5 to t6, at this interval, it's the negative cycle turn which S2 and S3 will be turn on. The duty cycle loss also will be occur at this interval. After end of t4, the switch S2 will be turned on with ZVS. In this mode, since the primary current reverse its direction to negative direction, the secondary voltage will change from zero to negative secondary voltage, Vs. The primary current start to rise to reach the reflected output inductor current nILo at t6. The primary current will rise to a certain level with Vin/ Llk as the Vin discharge the leakage inductance and cause no power delivered to the output.

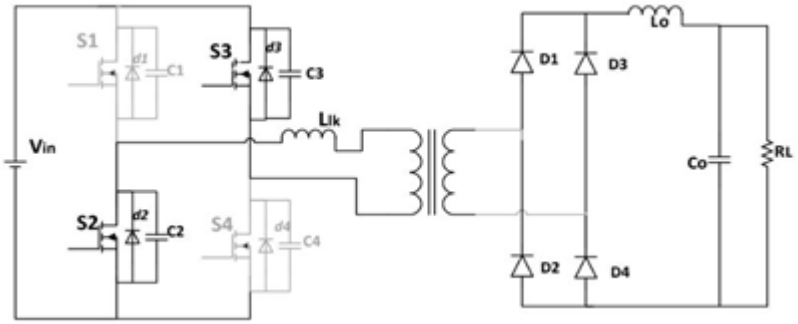


Figure 2.11: The converter in the interval t5 to t6

Next, from t6 to t7, its called the power delivering mode for negative cycle of the converter. At t6, the transformer secondary voltage Vs equal to nVin. Now, for negative cycle, the rectifier diode D2 and D3 at the AC to DC bridge of the secondary side of the converter will in forward biased. The diode D2 and D3 will

conducted to charge the output conductor. At this interval, the effective phase shift duty cycle start again. The primary current Ip is in negative direction and equal to reflected output inductor current nI_{LO}.

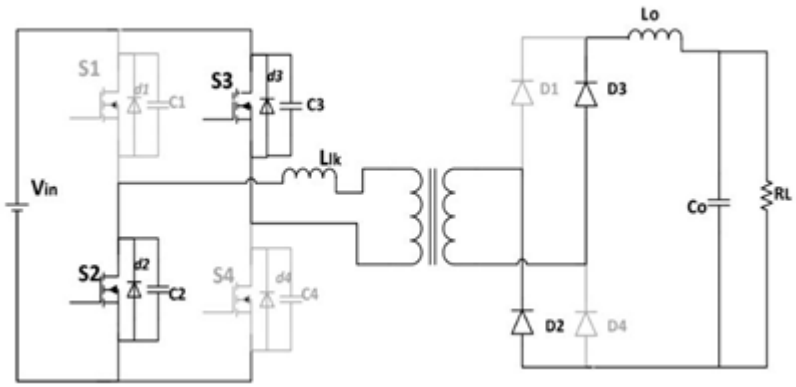


Figure 2.12: The converter in the interval t6 to t7

For interval t7 to t8, at this interval, the switch S4 will undergo ZVS operation. During t7, the snubber capacitance at switch S4 will be discharge and the snubber capacitance at switch S3 will be charge. Since the voltage completely discharge from Vin to zero for snubber capacitor of switch S4, the the body diode d4 will start to conduct to achieve zero voltage switching operation for switch S4. The transformer secondary voltage will drop to zero and the current free wheel through the secondary AC to DC rectifier diodes D2 and D3.

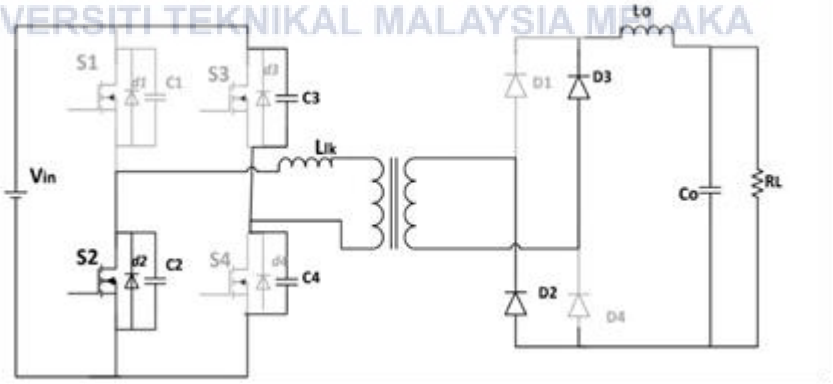


Figure 2.13: The converter in the interval t7 to t8

Next, for interval t8 to t9, the current will in freewheeling mode. Since there is ZVS operation, the switch S4 will turn on at t8 and the current will freewheel through switch S2 and switch S4. At this interval, Since the secondary voltage is zero, and the output inductor voltage will discharge by the load.

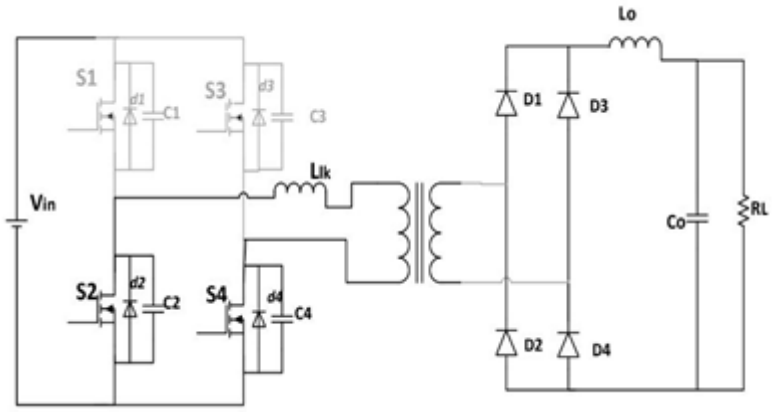


Figure 2.14: The converter in the interval t8 to t9

Lastly, at the interval of t9 to t10, the switch S1 will undergo zero voltage switching operation. As usual, at t9, the snubber capacitor of switch S2 will be charges and the snubber capacitor of switch S1 will be discharge from Vin to zero. The body diode d1 will be conduct since the snubber capacitor od switch S1 is discharged and undergo zero voltage switching operation. So, the switching loss and conduction loss of the MOSFET switches during undergo phase shift of the signal pulse will be eliminated. Since the secondary voltage still remains zero at this interval, the current will freewheel through the diode D2 and D3 at the AC to DC rectifier at the secondary side of the converter.

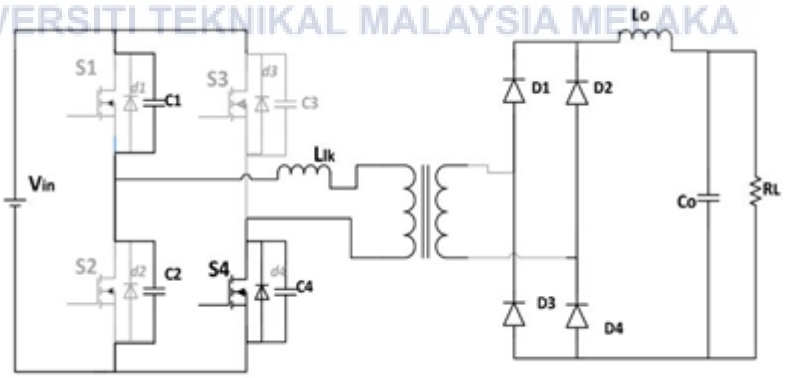


Figure 2.15 The converter in the interval t9 to t10

As a conclusion, this is the process on how the zero voltage switching operate in a phase shift full bridge DC to DC converter. The parameter that need to apply and analyse in order to achieve zero voltage switching operation of the converter need to determines as discusses previously and the step to determine the parameters in order

to design a phase shift full bridge ZVS DC to Dc converter will be discussed in detail in Chapter 3 which is methodology.

2.5 Develop Multi Input For The ZVS Phase Shift Full Bridge DC To DC Converter

For a multi input ZVS phase shift full bridge DC to DC converter, it has more voltage and power store at the input compare to single input. This is because for multi input it consists of different sources of renewable energy or more same sources of renewable energy connect together at the input, so the voltage and power accumulate at the input will be higher [1]. For example, the different type of renewable energies such as fuel cell, wind energy, solar energy, and biomass can be combine together and connect in series at the input of the converter as shown as figure 2.16 below.

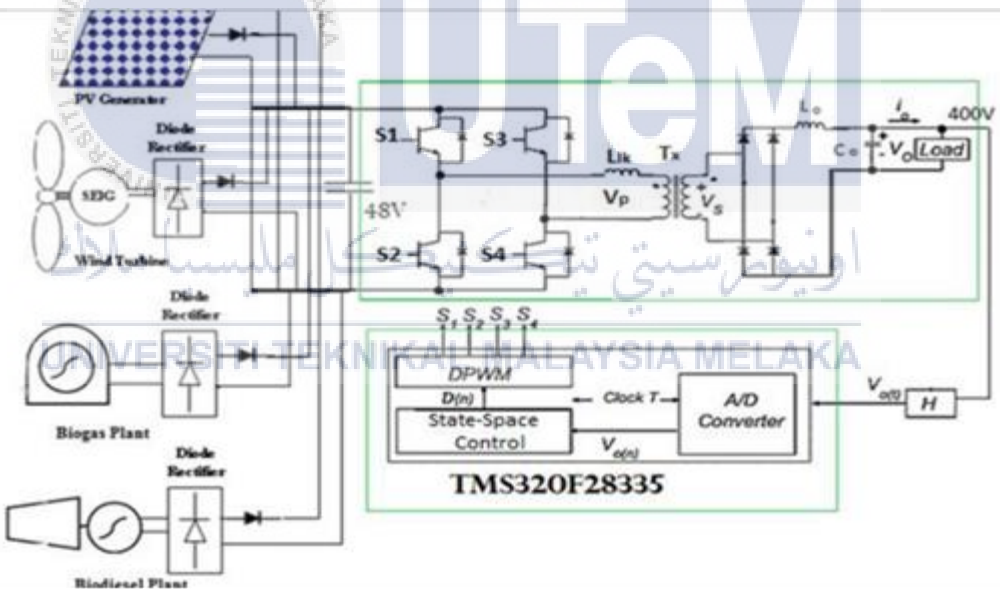


Figure 2.16: The different type of renewable energies such as fuel cell, wind energy, solar energy, and biomass that combine together and connect in parallel at the input of the converter

For multi input, the different type of renewable energy connect in series and each of the sources will connect with a diode and connect at the input of the converter [1].

2.6 Design Of A Close Loop ZVS Phase Shift Full Bridge DC To DC Converter

A close loop ZVS phase shift full bridge DC to Dc converter is connect a controller to regulate the output voltage of the converter automatically. Mostly, a state space controller as shown as figure 2.16 above or a PI controller will choose as the controller.

From figure 2.16, the output voltage is feedback and compare with the desire output voltage need and if there is different for the output voltage produce with the desire output voltage, the controller will base on the signal of the comparison of the output voltage produce with the desire output voltage and control the phase shift of the pulse signal of the MOSFET switches to regulated the output voltage to a desire value.

The design of state space controller will be more complex compare to the design of PI controller. For PI controller, the topology of the close loop ZVS phase shift full bridge DC to DC converter show as figure 2.17 below [10].

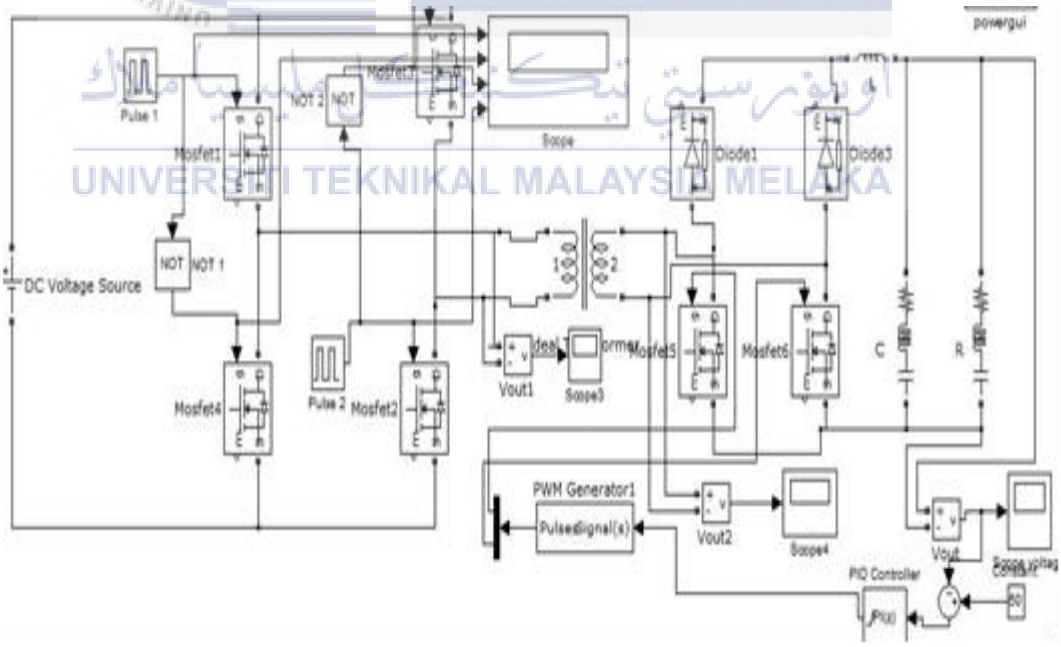


Figure 2.17: the topology of the close loop ZVS phase shift full bridge DC to DC converter with PI controller

From figure 2.17 above, output voltage is feedback and compare with the desire output voltage need and if there is different for the output voltage produce

with the desire output voltage, the PI controller will base on the signal of the comparison of the output voltage produce with the desire output voltage and control the phase shift of the pulse signal of the MOSFET switches to regulated the output voltage to a desire value. The different for PI controller and state space controller is for PI controller, pulse generator need to connect after the PI controller that use to generate the pulse signal that need to control the phase shift of the pulse signal of the MOSFET switches in order to achieve the desire output voltage [10].

CHAPTER 3

METHODOLOGY

3.1 Introduction

In this chapter, the flows that carry out to achieve the objectives of this project will be discussed.

3.2 The Design Of A Phase Shift Full Bridge DC To DC Converter To Regulate The Output Voltage By Undergo Phase Shift Modulation For The Pulse Signal Of The Switches

The model of the phase shift full bridge DC to DC converter have been simulate by using MATLAB/SIMULINK as shown as figure 3.1 below which combine every renewable energy source such as wind, solar and biomass into 1 input DC source.

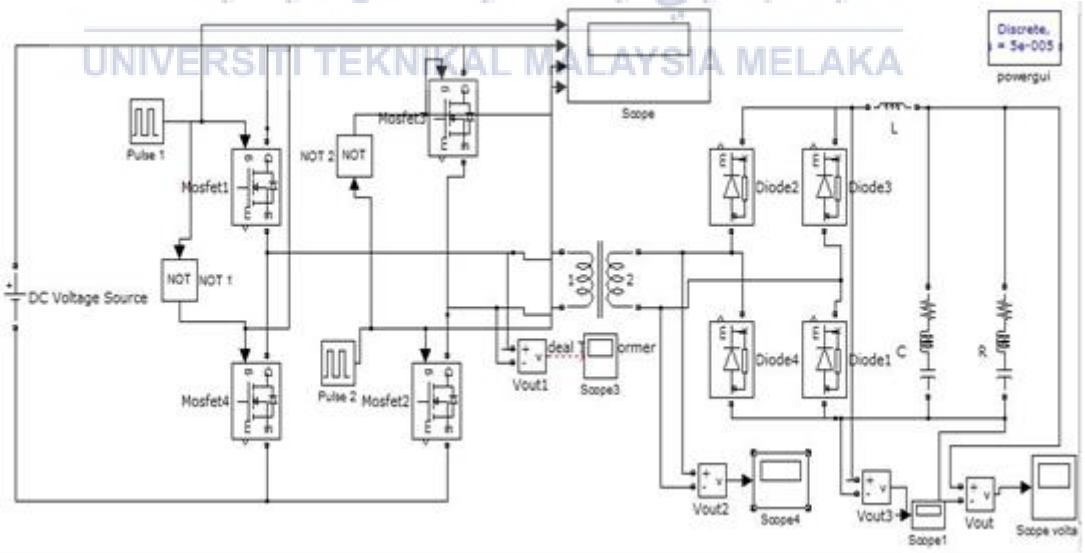


Figure 3.1: The simulation model of the phase shift full bridge DC to Dc converter

To simulate this model, firstly, choose a DC voltage source from the Simulink library. The DC voltage source was choose because this converter is applied to stable or varied the output voltage form the input voltage from the renewable energy such as solar energy.

Next, to simulate the H bridge at the primary side of the converter, four MOSFET switches have been choose from the Simulink library. The H bridge at the primary side of the converter is used to converts the DC input voltage from the input DC voltage source before going to step up the input voltage to a desire value to supply for the load. MOSFET switches was choose because it can handle high power capability and can operate at high frequency switching during switching and this can improve system efficiency.

After all the four MOSFET switches have been choose, connected to the DC voltage source as shown as figure 3.1 above. Next, the pulse was selected from Simulink library and connected to MOSFET 1 and MOSFET 2, one pulse located at the leading leg switch S1 and another located at lagging leg switch S2.

Next, the NOT gate was choose from the Simulink library. One NOT gate will be connected to the switch switch S4 which inverse the signal pulse from the switch S1. Similary, the another NOT gate will connect be connected to switch S3 which inverse the pulse signal from switch S2. Form here, the MOSFET switch S1 and S2 will produce positive cycle of AC voltage through the H bridge and MOSFET switch S3 and S4 will produce negative cycle of the AC voltage. The pulse signal of the pulse was set as figure 3.2 below.

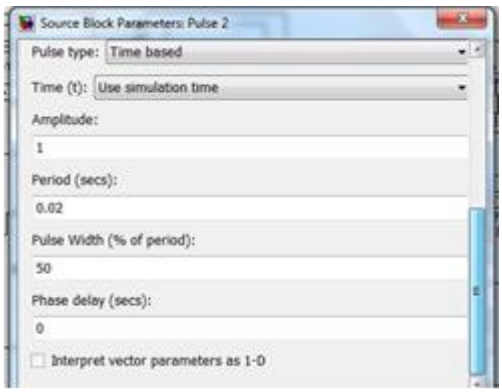


Figure 3.2: The parameter that set for the pulse signal of the MOSFET switches

The period was calculated from 1/50 where the frequency is set for 50 HZ. The phase delay set to zero for both leading and lagging leg switches and the pulse width will set to 50 % of the period.

After that the primary H bridge that connected with the DC voltage source will connected to the isolated transformer. To connect the isolated transformer, an ideal transformer was choose from the Simulink library. After the ideal transformer was connected to the H bridge, where positive terminal connected to the positive end of the H bridge and negative terminal connected to the negative end of the H bridge. After the transformer was connected, the parameters of the transformer have been set as shown as figure 3.3 below.

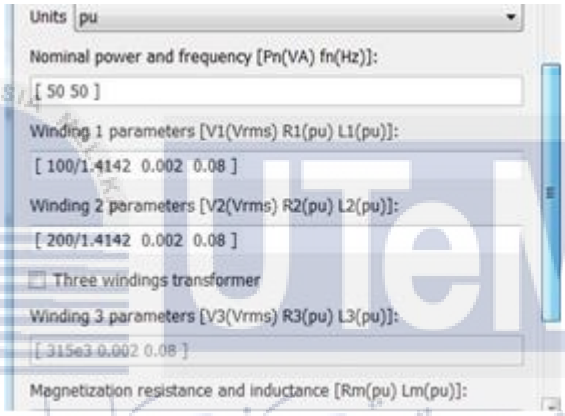


Figure 3.3: The parameter that set for the ideal transformer

The nominal power of the transformer will set to 50 VA and the frequency was set to 50Hz. For the winding parameters, it can set to 100/1.4142 for winding 1 and 200/1.4142 for winding 2 to produce 1 to 2 ratio. The divided 1.4142 is to convert the voltage to rms value. That's means the full load output voltage produce is 200 V DC.

The magnetizing resistance and inductance was set to 500 pu respectively.

Next, the secondary side of the ideal transformer will connect to the AC to DC bridge and the AC to DC bridge was connected to the output filter inductor, output filter capacitor and the load. The output filter inductor and the output filter capacitor are used to filter the output ripple voltage .

The AC to DC bridge at the secondary side of the converter have connected by four normal basic diodes that can found in Simulink library. The AC to DC rectifier of the converter is used to converted the AC output voltage to DC voltage after step up by the transformer and supply to the load.

The output filter capacitor value and the output filter inductor was set as figure 3.4 and figure 3.5 which are 190 micro Farad and 0.0001 H in order to achieve low ripple output voltage.

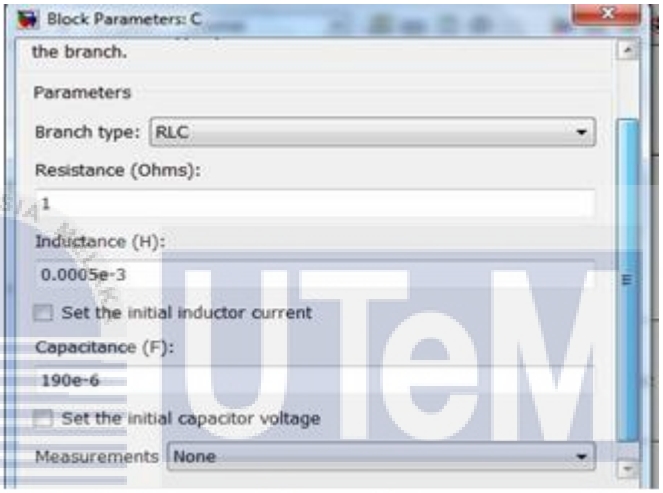


Figure 3.4: The parameter that set for the output filter capacitor value

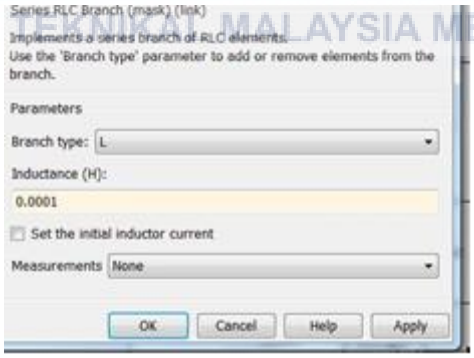
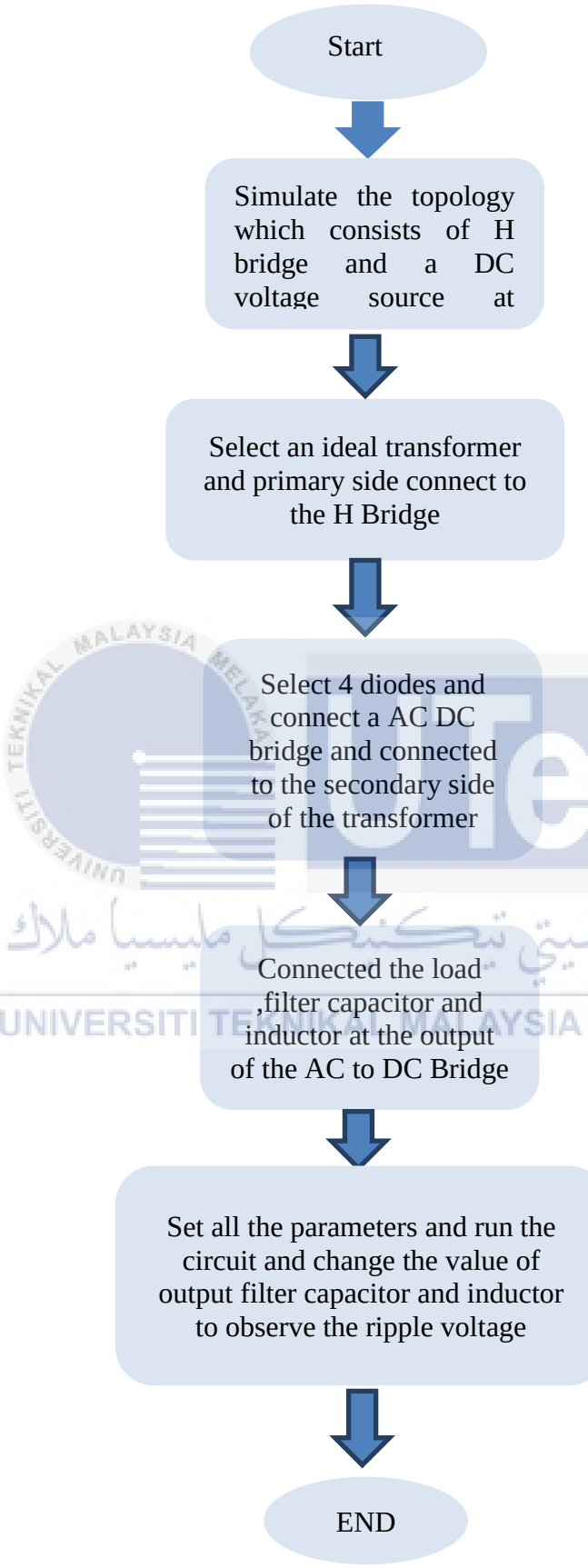


Figure 3.5: The parameter that set for the output filter inductor value

Next, the phase shift of the signal pulse of the lagging leg switches S2 and S3 was adjusted by set the phase delay at the pulse block respect to leading leg switches S1 and S4 and analysed the change of the output voltage. The primary voltage at the primary side of the isolated transformer after the DC to AC H bridge, secondary voltage from the secondary side of the transformer before the Ac to DC bridge,

secondary voltage after the AC to DC bridge and output voltage after the filter capacitor and inductor was show at the scope voltage after undergo phase shift. The output voltage have been analysed after undergo phase shift after undergo phase shift by changing the D to 0.85 and 0.75. The output voltage satisfy the condition Vo = Vin(Ns/Np)D , the converter operated in right way and achieved objective 1 which is same phenomena when overload occur at the input, the output voltage can be regulate by phase shift to maintain the desire output voltage.

Finally, test the output voltage and by change the output filter inductor and output filter capacitor value have been carried out. The flow chart below have summarized the steps to design a phase shift full bridge DC to Dc converter to regulate the output voltage by undergo phase shift modulation for the pulse signal of the MOSFETS switches.



3.3 Design A Simulink Model Of Phase Shift Full Bridge ZVS DC To DC Converter

In this report, a design of a 150V DC output voltage phase shift full bridge ZVS DC-DC converter with the input voltage range between 350 V DC to 400 V DC with the reference input voltage of 350 V have been done.

According to the method from [1] and [3], that have been discuss in previous chapter 2, there is some error when the simulation run when all the parameters that have been calculated base on the range that need to design have been set in the simulation. So, a new method from [11] have been develop to design the phase shift full bridge ZVS DC-DC converter and this is the different method to evaluate whether the full bridge phase shift DC-DC converter will undergo ZVS when the pulse signal of the MOSFETS at the lagging leg undergo phase shift respect to the pulse signal of the MOSFETS at the leading leg . The steps of design have show below.

Firstly, the simulation of the phase shift full bridge ZVS DC-DC converter have simulated in Simulink as show as figure 3.6 below.

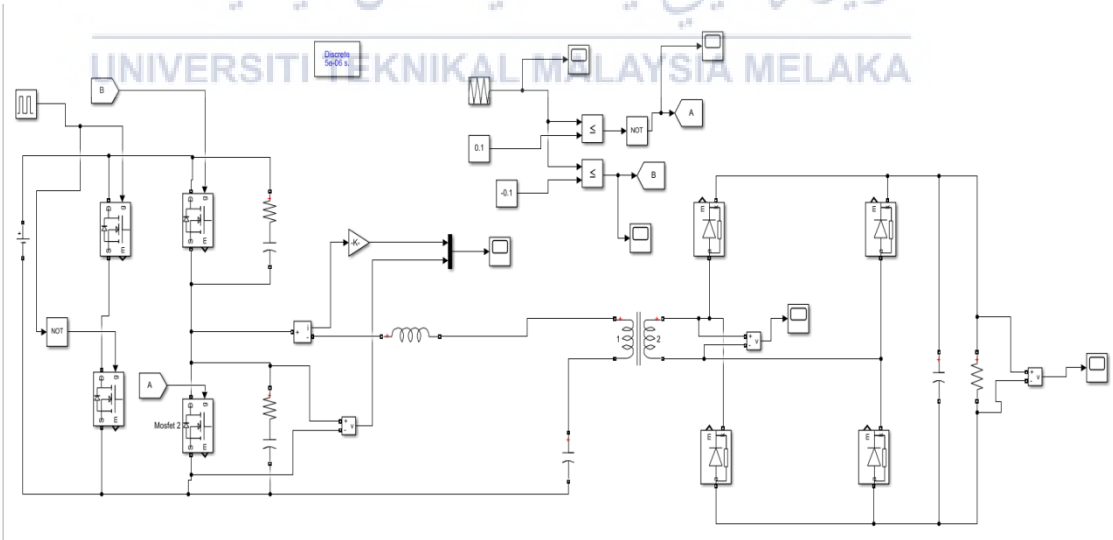
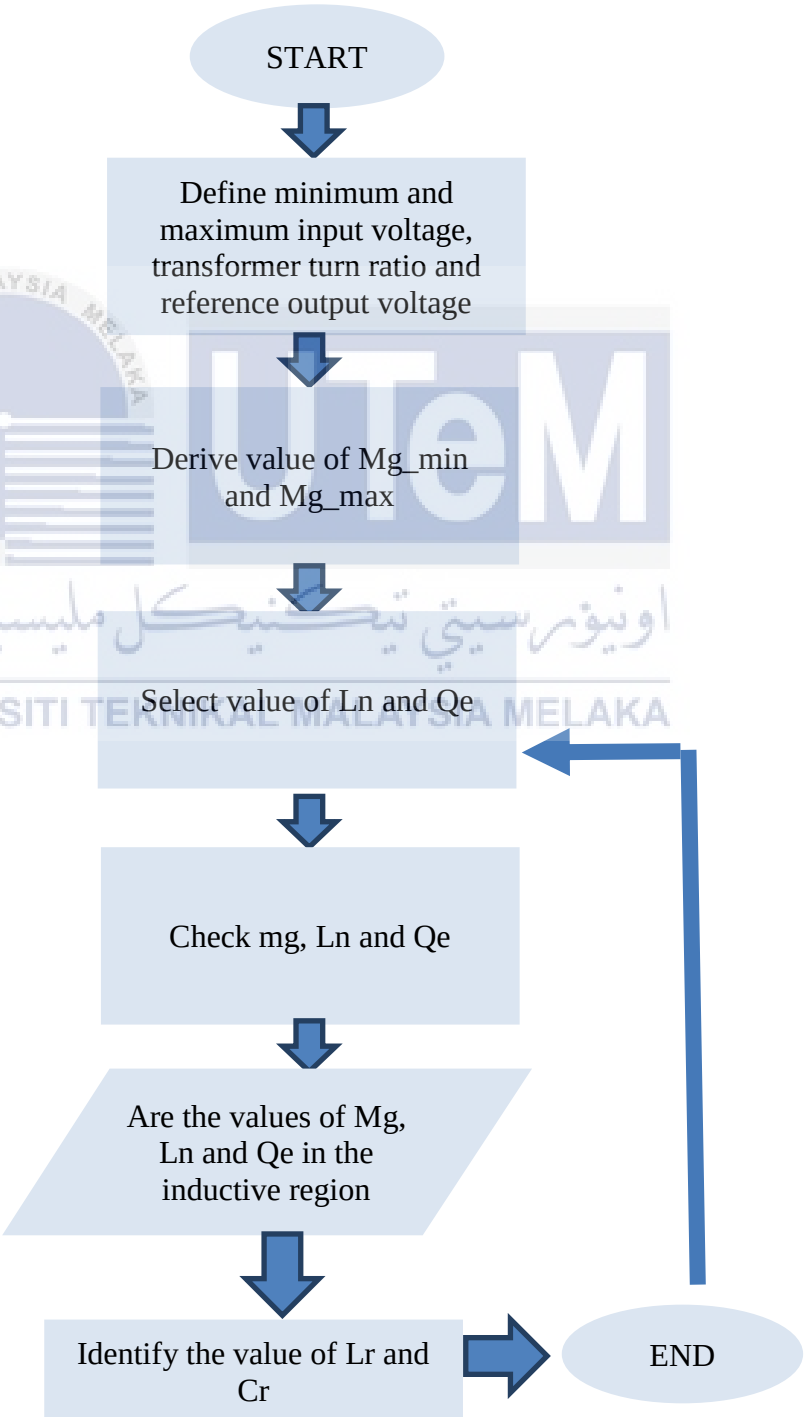


Figure 3.6: The simulation of the ZVS phase shift full bridge DC-DC converter in Simulink

After the simulation done, set the transformer ratio N2/N1 to 7/3 which is step down the designed reference input voltage of 350 V to 150 V reference output

voltage. Next, the value of the inductor and the capacitor in the resonant tank which located at the primary side of the transformer have been designed in order to reduce the switching loss of the MOSFETS switches by ZVS via resonance phenomena during the phase shift of the pulse signals of the MOSFETS at the lagging leg respect to the pulse signals at the leading legs in order to maintain the output voltage of 150 V when the input voltage varies from 350 V to 400 V . The steps to design the inductor and capacitor value have been show as the flow chart below.



The Mg_min and Mg_max have been determine by the formula as show as figure 3.7 below. After the two value have been determine, The Ln and Qe value can be determine from the graph as show as figure 3.7 and figure 3.8 below. After get all the values, the conditions that state as the flow chart above have been checked and the value of the resonant inductor and capacitor have been found by using the graph of figure 3.9. By follow the steps, the value of the resonant inductor and capacitor that need to set in order to occur ZVS via resonance effect is one micro henry and 27.3 nano farad which have been found. This is because the smaller the size of the resonance inductor and capacitor, the period that require to charge is fast in order to discharge the snubber capacitor at the MOSFET switch to undergo ZVS during the cut off period when phase shift occur.

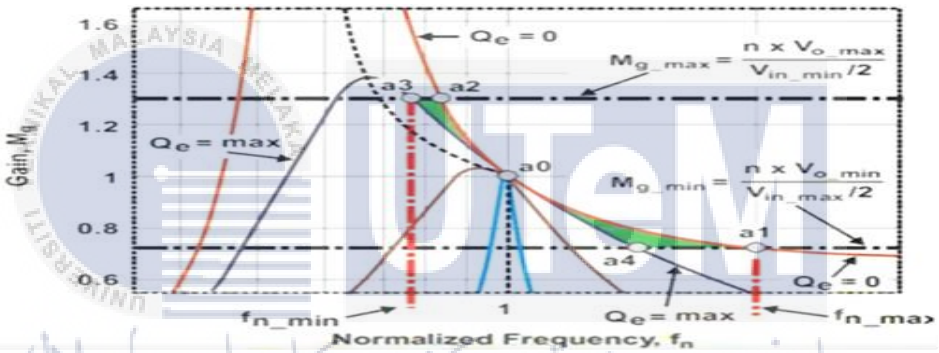


Figure 3.7:The graph of Mg versus Qe

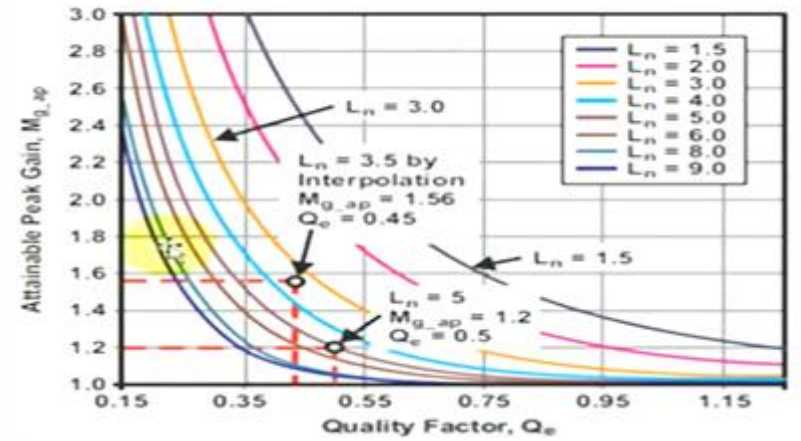


Figure 3.8: The graph of Mg versus Qe to determine Ln

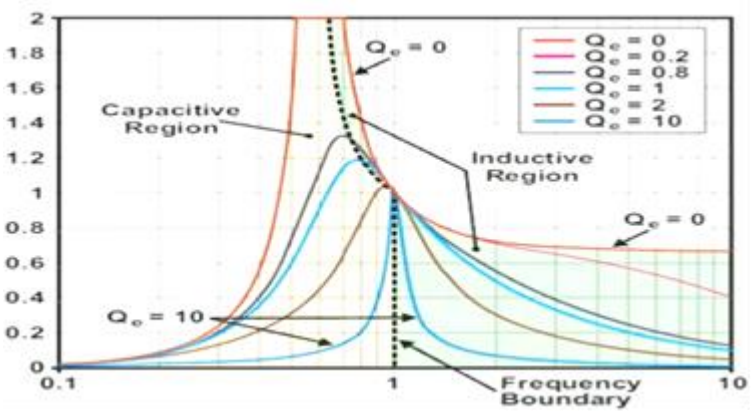


Figure 3.9: The graph of capacitive and inductive region to check the value of resonant inductor and capacitor value base on the Qe, Ln and Mg value

Lastly, the triangular wave have been set by using repeating sequence as show as figure 3.10 below which use to compare the constant and the varies input voltage in order to produce the desire duty cycle for MOSFETS at the lagging leg in order to produce the pulse signal and undergo phase shift of the signal respect to the pulse signal of the MOSFETS at the leading leg to produce the desire output voltage . The area that cross between the input voltage MOSFET 2 and the output current graph will determine whether the ZVS occur to maintain the efficiency of the converter when phase shift of the pulse signal of the MOSFETS at the lagging leg respect the lagging leg of the converter for the input voltage varies from 350V to 400 V. The results have been analysed and discussed in chapter 4.

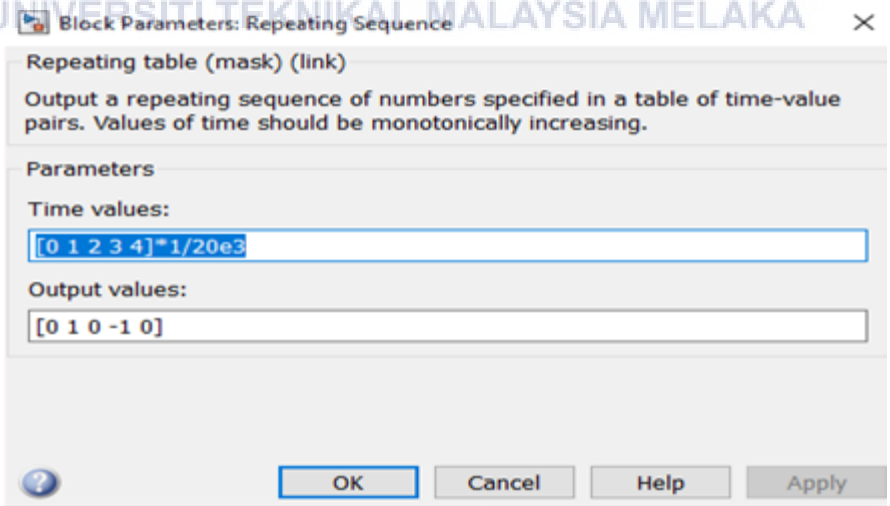


Figure 3.10:The setting for the repeating sequence

3.4 The Design Of The Close Loop Full Bridge Phase Shift DC-DC Converter

In this report, the close loop full bridge phase shift DC-DC converter have been designed to overcome the problem of fluctuated of input voltage. The simulation of the close loop full bridge phase shift DC-DC converter has show as figure 3.11 below [12].

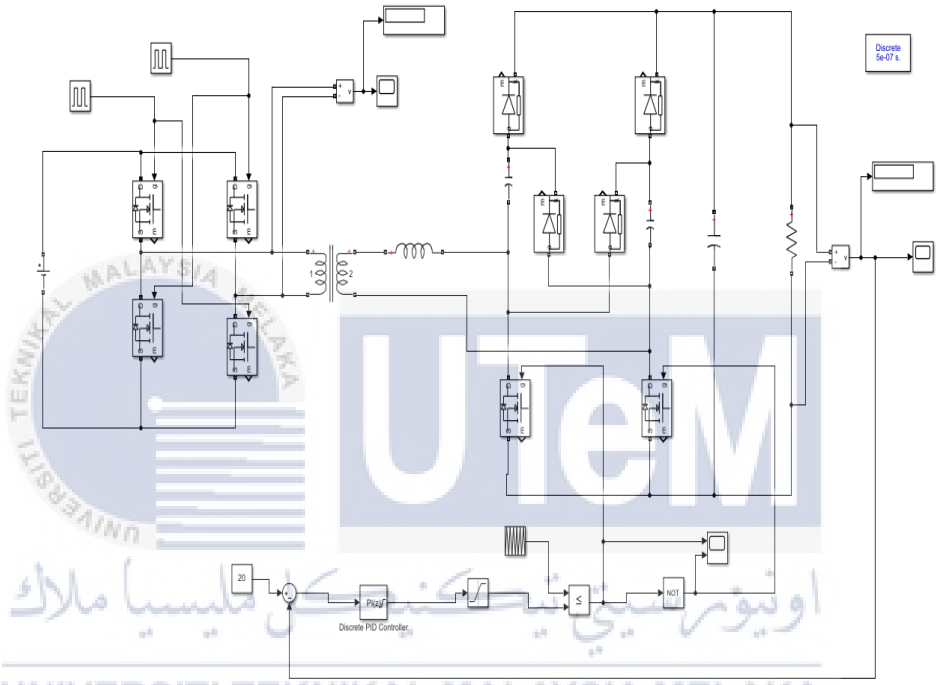


Figure 3.11: Close Loop Full Bridge Phase Shift DC-DC Converter In Simulink

The range of the input voltage that have been designed are 45 V to 60V, which 60 V is the reference input voltage and a reference output voltage of 20V. The design of this converter is to step down the input voltage . For this design, the PI controller will able to regulate the output voltage with 20V of reference voltage when the input voltage fluctuated from 60 V to 45 V. The setting of the PI controller, upper and lower limit of the saturation and the sample time as show as Table 3.1 below.

Table 3.1: Parameters of the PI controller

Proportional gain (Kp)	8000000
Integral gain (Ki)	3000000000
Saturation limits	[0.8 -0.7]
Sample time	5e-07

The results that shows the close loop full bridge phase shift DC-DC converter that regulate the output voltage with the reference voltage of 20V when the input voltage fluctuated from 60V to 45V have been analysed and discussed in chapter 4.

CHAPTER 4

RESULTS AND DISCUSSIONS

4.1 The Relationship Of The Output Voltage Of The Converter With Phase Shift Modulation Of The Pulse Signal Of The MOSFET Switches

The objective 1 for this project have been achieved and the results achieved as shown below.

The primary voltage at the primary side of the isolated transformer after the DC to AC H bridge, secondary voltage from the secondary side of the transformer before the Ac to DC bridge, secondary voltage after the AC to DC bridge and output voltage after the filter capacitor and inductor have been analysed .To undergo this, the phase delay of the pulse block of the MOSFET switched at the lagging leg which are S2 and S3 have set.

The duty cycle that have been varied to test the different of output voltage of the converter are 1, which is full phase, 0.85 , 0.75. The input voltage will set as 100 V and the transformer ratio is set to 1:2 ratio. To set the time delay at the pulse block of the MOSFET switches according to the duty cycles that need to set, just use the duty cycle times the period of the pulse which is 0.02. The period of the pulse get from 1 per frequency where the frequency set to 50 HZ. After the product of the duty cycles and the period of the pulse, the answer will minus by the period 0.02 and the delay time of the signal pulse of the switches at the lagging leg will be determined. The results have shown below.

4.1.1 The Results For The Designed Full Bridge DC-Dc Converter

The Results of Primary Voltage Produce After The DC to AC H Bridge, Secondary Voltage From The Secondary Side Of The Transformer Before The Ac

To DC Bridge, Secondary Voltage After The AC to DC Bridge But Before Output Filter Capacitor And Inductor And Output Voltage After The Filter Capacitor And Inductor When Undergo Phase Shift Modulation Of The Pulse Signal Of The MOSFET Switches At Lagging Leg have been discussed.

Below are the results and discussions on the relationships of the primary voltage produce after the DC to AC H bridge, secondary voltage from the secondary side of the transformer before the Ac to DC bridge, secondary voltage after the AC to DC bridge and output voltage after the filter capacitor and inductor when undergo phase shift which change the duty cycle D from 1, 0.85 , and 0.75.

4.1.2 Duty Cycle 1, Phase Delay 0 Second

Figure 4.1: : the waveform of the primary voltage after the DC to AC H bridge produce for full phase

From the figure 4.1 above, there is no phase shift between the signal pulse of the switches at the lagging leg and the switches at the leading leg. So, the complete waveform of the AC input voltage of 100 V will be produce with full pulse width. From here, the output voltage can be determined by Vout = VinD(Ns/Np), where D is the duty cycle equal to 1 for full phase and the transformer ratio will be 1:2 and the output voltage produce for full phase is 200V DC as shown as figure 4.2 below after the input voltage step up by the transformer and filter by the AC to DC rectifier at the secondary side of the transformer which after the filter capacitor and inductor.

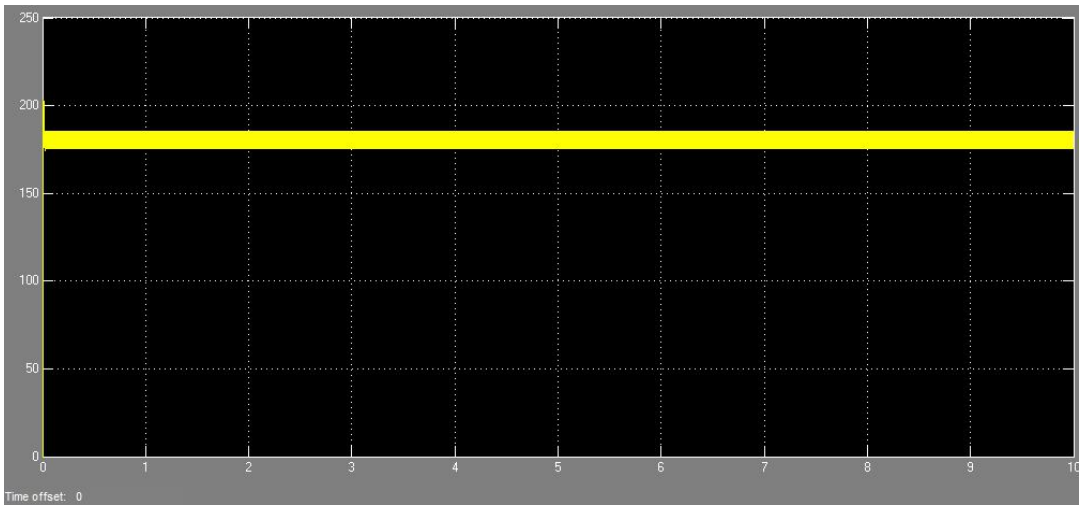


Figure 4.2: The output voltage produce after the filter capacitor and inductor by the converter under full phase operation

The simulation results shows that it is not accurate 200 V and is below approximate 180 to 190 volt. This is because the voltage drop occur across the circuit elements such as output filter inductor and capacitor that use to reduce the ripple output voltage. To overcome this problem, the transformer windings' ratio need to set higher in order to achieve the accurate output voltage. The process to change the step up 200V DC output voltage with less ripple will be discuss and show as figure 4.3 and 4.4 below.

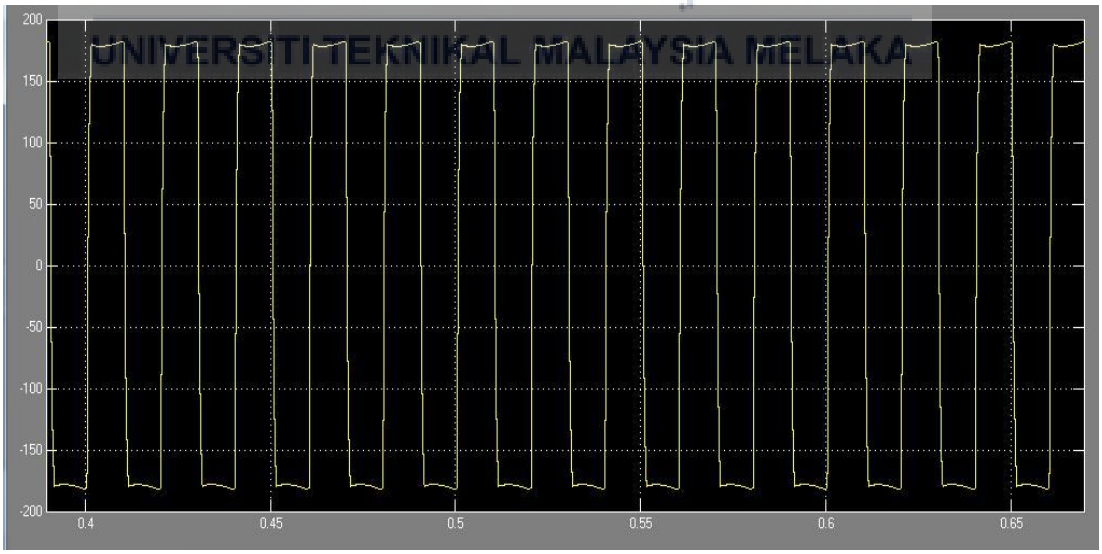


Figure 4.3: The output voltage produce at the secondary transformer before the AC to DC bridge

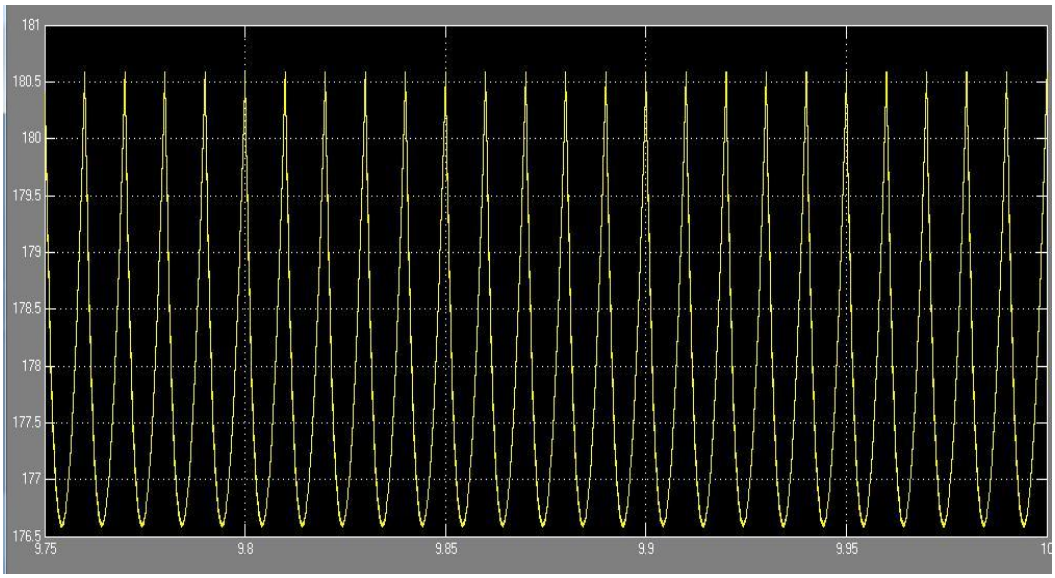


Figure 4.4: Output DC voltage produce after the AC DC bridge and before the output ripple capacitor and inductor

4.1.3 Duty Cycle 0.85, Phase Delay 0.003 Second

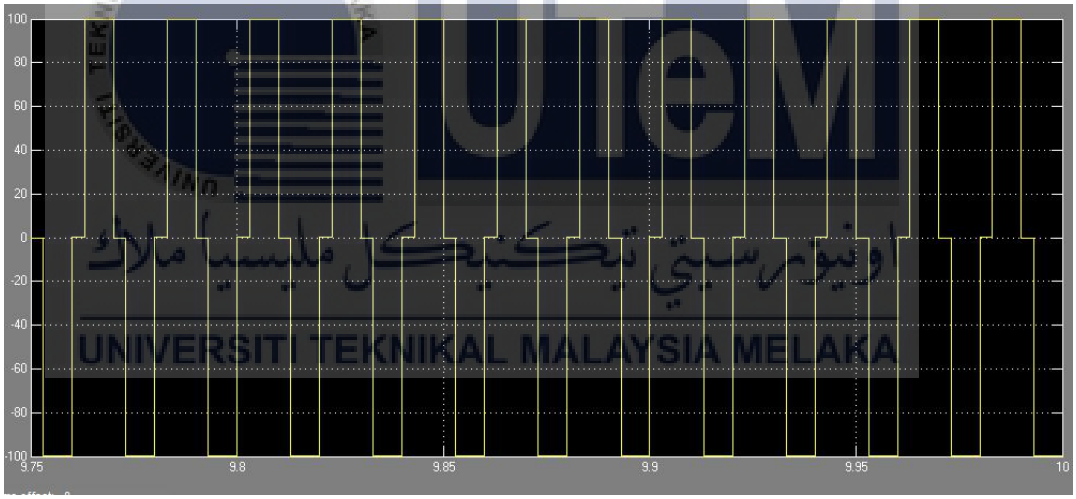


Figure 4.5: The waveform of the primary voltage after the DC to AC H bridge

From figure 4.5 above, since there is phase shift of the pulse signal between lagging leg and leading leg switches, the pulse width of the AC primary voltage waveform will be decrease which the switches on time will be decrease. So, from here, the average DC output voltage produce will be reduce which can be calculate by the formula and the output voltage will be 170 V DC as shown as figure 4.6 below.

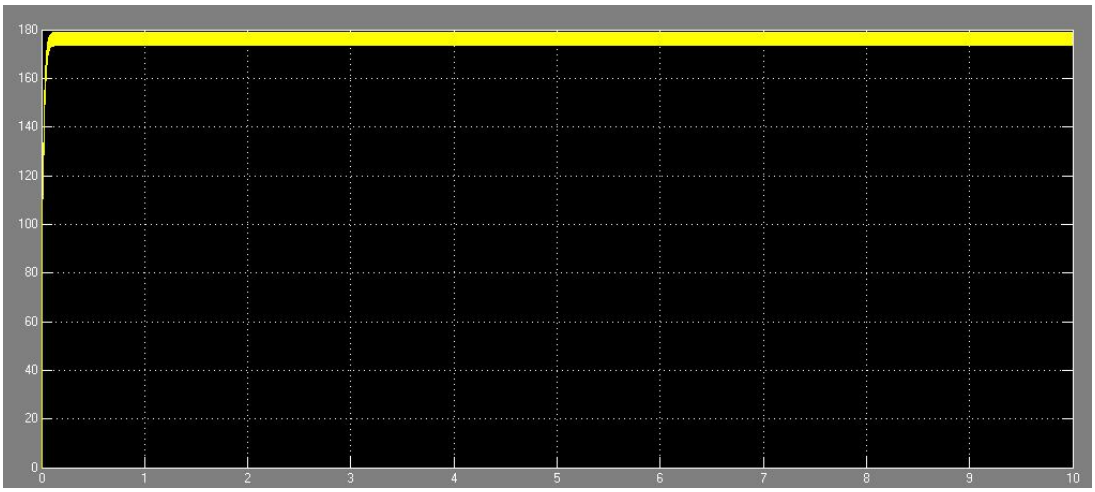


Figure 4.6: The output voltage produce after the filter capacitor and inductor by the converter

The process to change the step up 170V DC output voltage with less ripple will be discuss and show as figure 4.7 and 4.8 below.

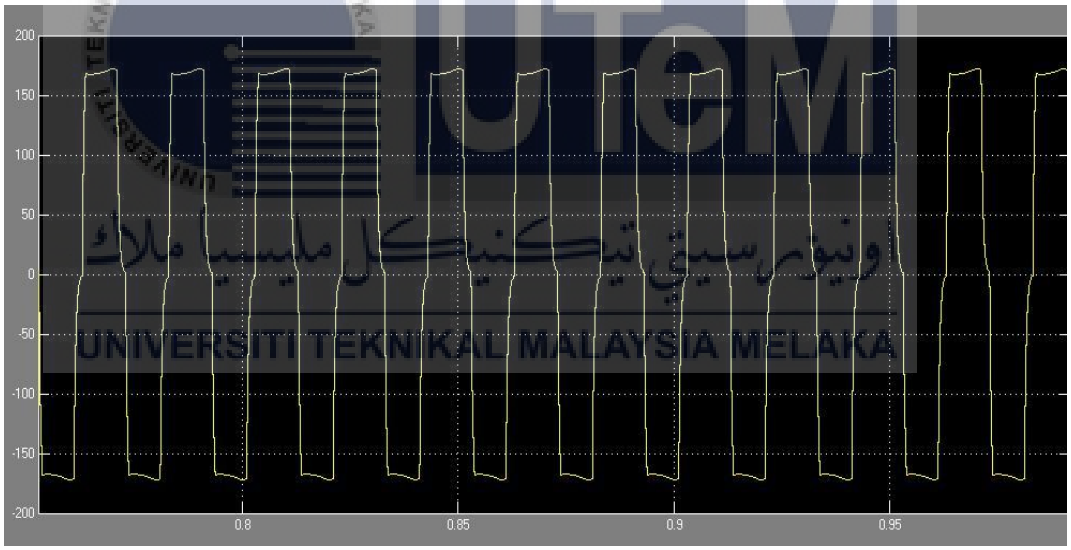


Figure 4.7 : The output voltage produce at the secondary transformer before the AC to DC bridge

Figure 4.7 above shows that the AC step up voltage produce and the voltage will convert back to DC 170V to supply to the load. Figure 4.8 below shows the output 170V DC voltage produce before the output capacitor and inductor filter which contain more ripple than the DC output voltage produce after the output filter capacitor and inductor as shown as figure 4.6 above.

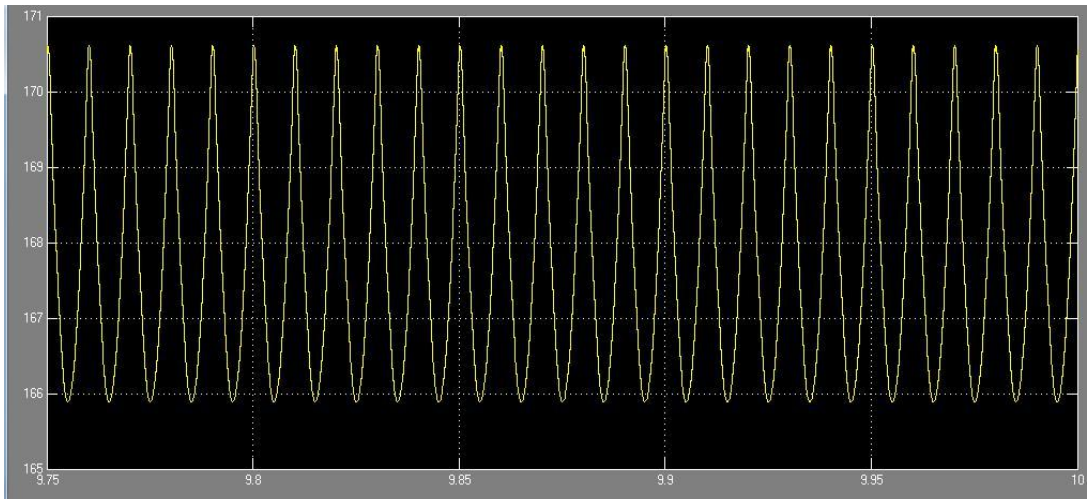


Figure 4.8: Output DC voltage produce after the AC DC bridge and before the output ripple capacitor and inductor

4.1.4 Duty Cycle 0.75, Phase Delay 0.005 seconds

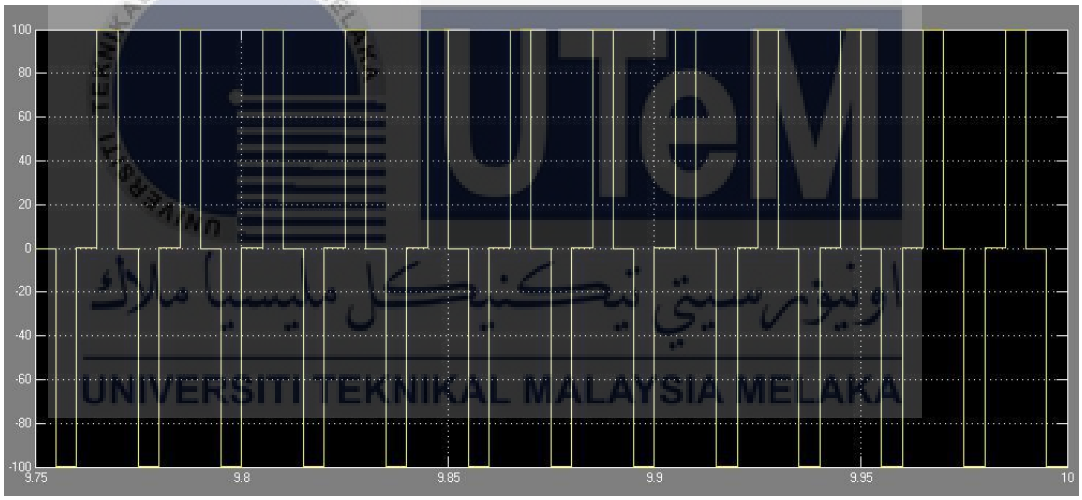


Figure 4.9: the waveform of the primary voltage after the DC to AC H bridge produce

From figure 4.9 above, since there is phase shift of the pulse signal between lagging leg and leading leg switches, the pulse width of the AC primary voltage waveform will be decrease which the switches on time will be decrease. So, from here, the average DC output voltage produce will be reduce which can be calculate by the formula and the output voltage will be 150 V DC as show as figure 4.10 below.

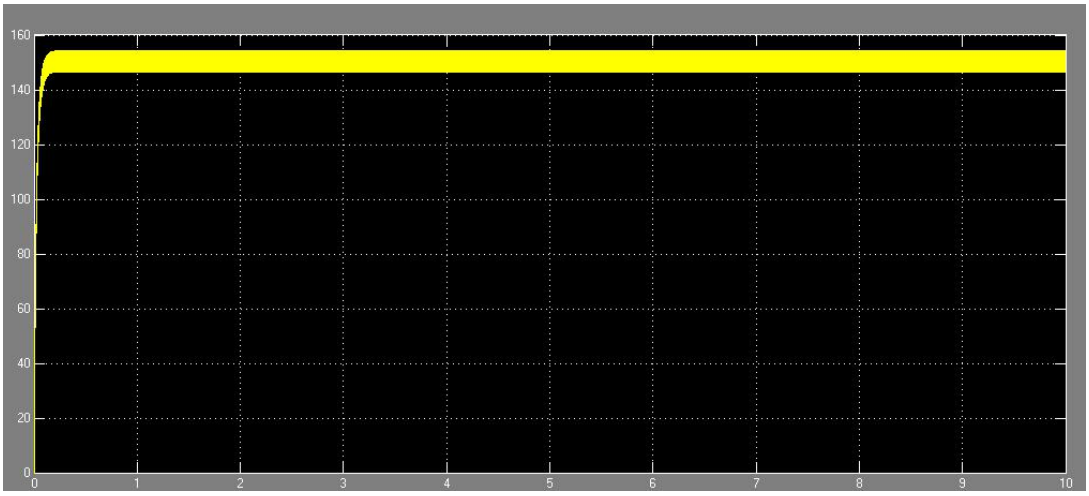


Figure 4.10: The output voltage produce after the filter capacitor and inductor by the converter

The process to change the step up 150V DC output voltage with less ripple will be discuss and show as figure 4.11 and 4.12 below.

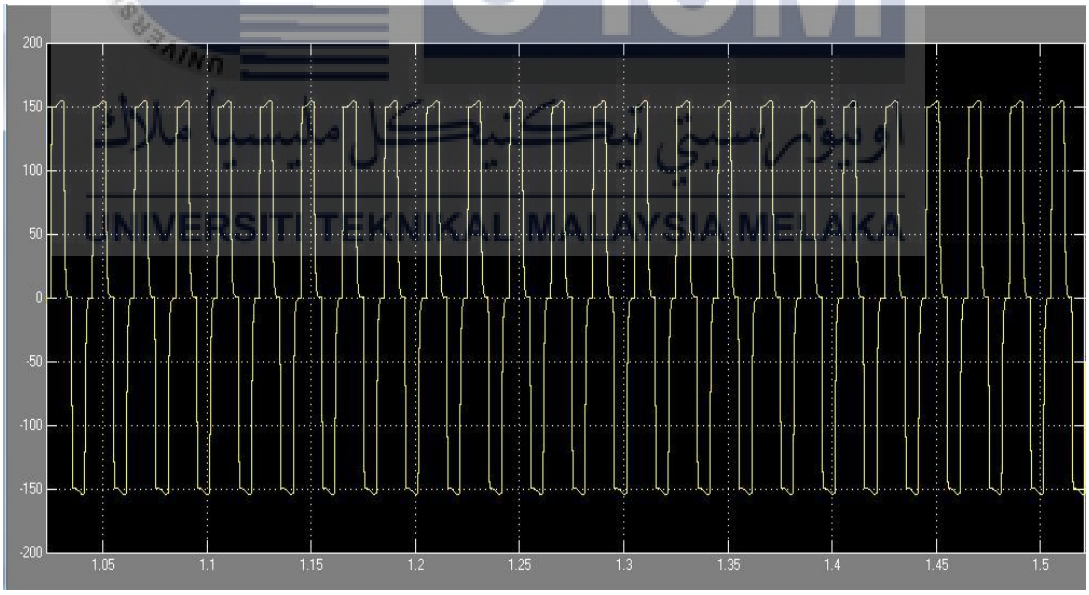


Figure 4.11: The output voltage produce at the secondary transformer before the AC to DC bridge

Figure 4.11 above shows that the AC step up voltage produce and the voltage will convert back to DC 150V to supply to the load. Figure 4.12 below shows the output 150V DC voltage produce before the output capacitor and inductor filter

which contain more ripple than the DC output voltage produce after the output filter capacitor and inductor as shown as figure 4.10 above.

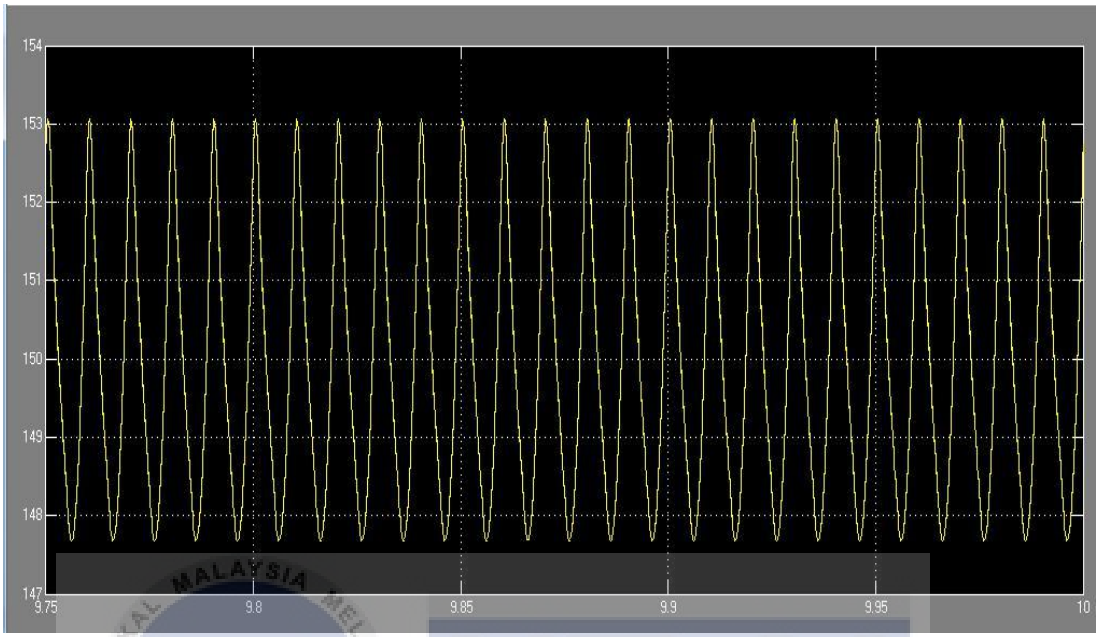


Figure 4.12: Output DC voltage produce after the AC DC bridge and before the output ripple capacitor and inductor

4.2 The Relationship Of the Value Of Output Filter Capacitor And Inductor With The Output Voltage Ripple

In this section , the , duty cycle equal to 1 and zero phase shift condition will be use to test the change of the output voltage ripple for the output voltage after the filter inductor and capacitor by the change of the value of the value of output filter inductor and capacitor. Below shows the results that the higher the value of output filter inductor and capacitor, the lower the output voltage ripple for the DC output voltage.

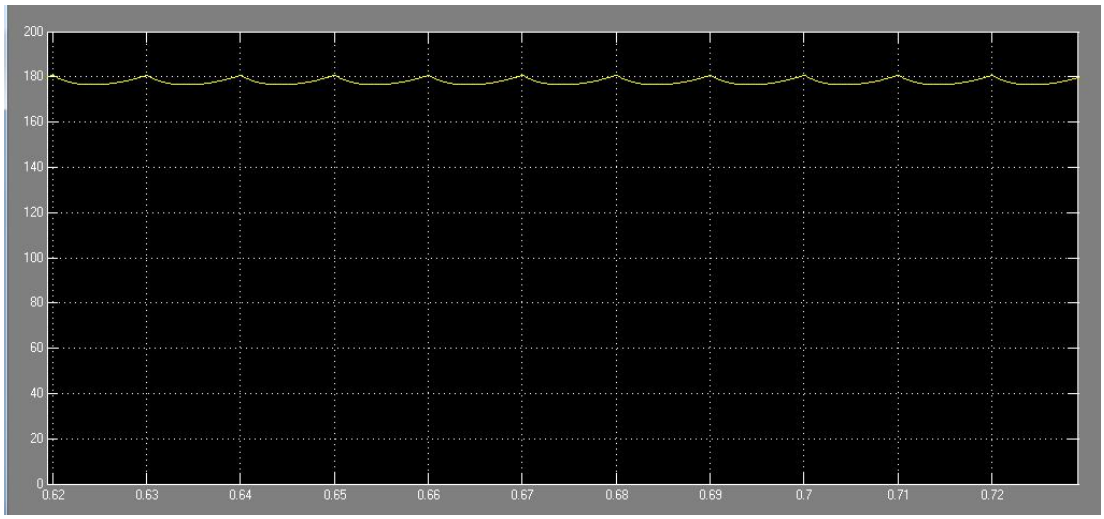


Figure 4.13: The output voltage ripple produce for the value of output filter capacitor and inductor are Lo = 0.0001 H, C=180 micro farad

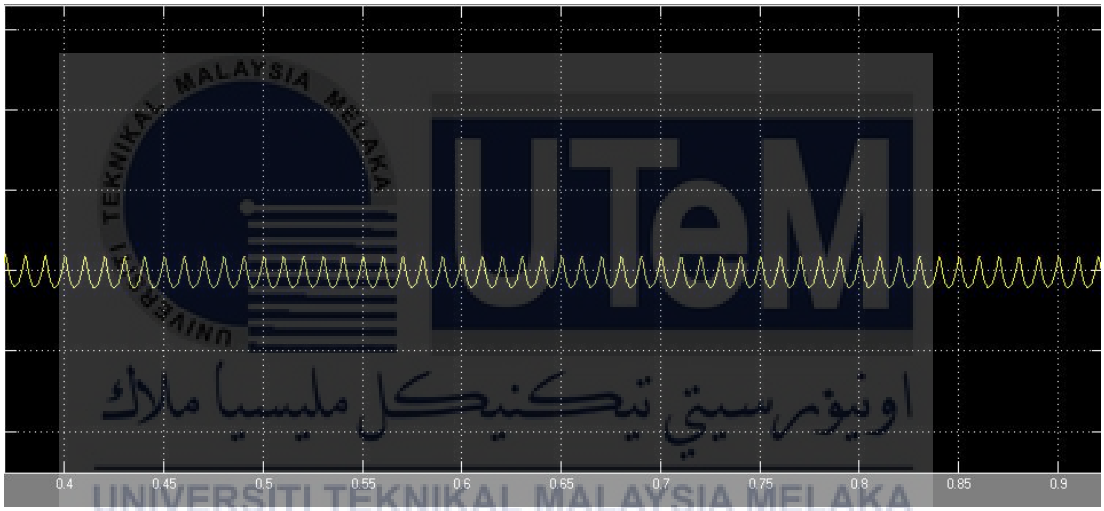


Figure 4.14: The output voltage ripple produce for the value of output filter capacitor and inductor are Lo = 1 H, C=200 micro farad

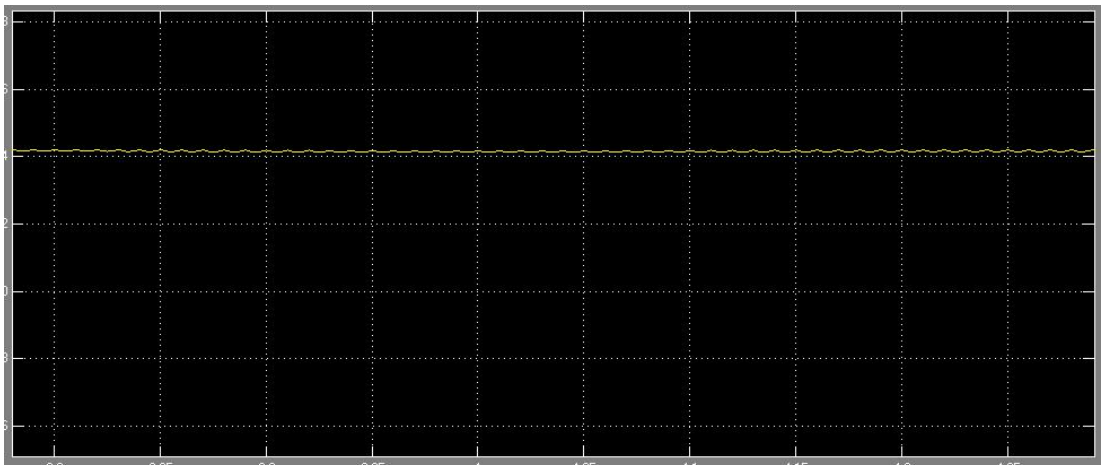


Figure 4.15: The output voltage ripple produce for the value of output filter capacitor and inductor are Lo = 10 H, C=300 micro farad

As a conclusion, the more the pulse signal at the lagging leg shift, the lower the output voltage produce. From here, the output voltage can be varied from 200 volt at full phase to 170V and 150 V. So by this theory, it can apply to solve problem 1 which stable the output voltage when overload of the input voltage from the renewable energy occur. Moreover, the higher the value of the output filter inductor and capacitor will reduce the ripple of the output voltage . however the value can,t set very high because it will increase the voltage drop across it and cause losses of the the output voltages. So the suitable value of the output filter capacitor and inductor are 0.0001H and 180 micro farad which will produce less losses of the output voltage plus less ripple also.

4.3 Design Of ZVS Phase Shift Full Bridge DC-DC Converter

In this section, the results of the designed ZVS phase shift full bridge DC-DC converter have been discussed. The results have show that the zero voltage switching has occur by resonance phenomena in order to reduce the switching and conduction loss during pulse width modulation (PWM) of the pulse signals of the MOSFET switches to regulate the output. The simulation of the converter have show as figure 4.16 below.

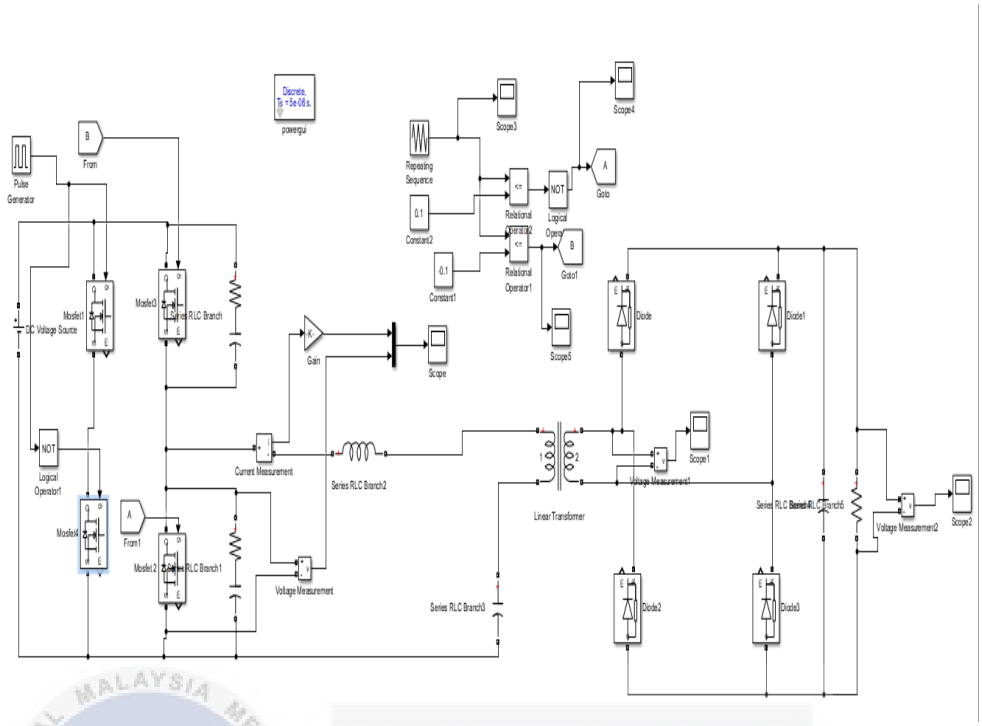


Figure 4.16: The simulation of the ZVS full bridge phase shift DC-DC converter

To design the full bridge phase shift DC-DC converter that able to undergo ZVS, only the lagging leg of the converter which are MOSFET 3 and MOSFET 2 that need to evaluate as show as the above simulation in figure 4.16 from the original full bridge phase shift DC-DC converter as show as figure 4.17 below. This is because only the MOSFET switches at the lagging leg will undergo pulse width modulation (PWM) of the pulse signal of the switches by undergo phase shift of the pulse signals respect to the pulse signals of the MOSFET switches at the leading leg which are MOSFET 1 and MOSFET 4 in order to regulate the output voltage.

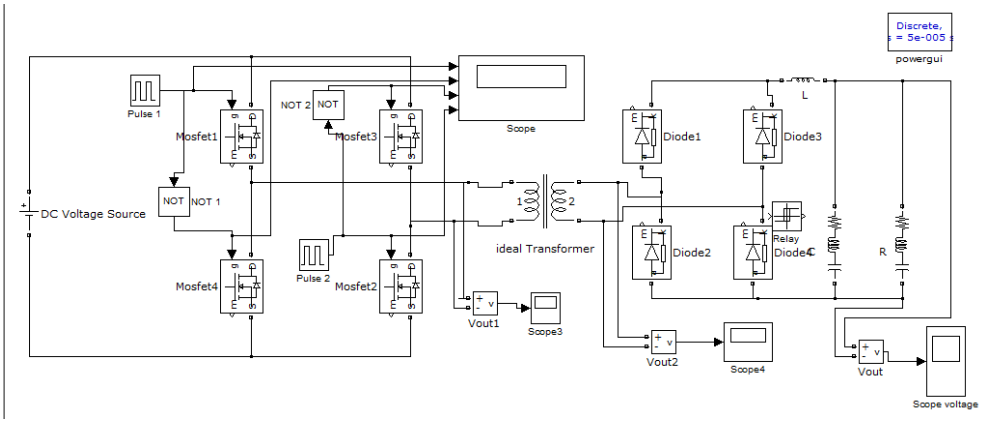


Figure 4.17: The original full bridge phase shift DC-DC converter

MOSFET 3 produce negative cycle which pair with MOSFET 4 at the leading leg while MOSFET 2 produce the positive cycle which pair with MOSFET 1 at the leading leg. The repeating sequence have been set to produce triangular wave that compare different input voltages with the constant to produce the desire duty cycle for MOSFET 2 and MOSFET 3 which from the formula Vo = Vin (N2/N1)D in order to produce the pulse signal and undergo phase shift of the signal respect to the pulse signal at the leading leg to produce the desire output voltage . The value of the resonant inductance and the capacitance have been set in order to achieve ZVS. The triangular wave that set and the signal after compare the input voltages with the constant and triangular wave have show in figure 4.18 and figure 4.19 below.

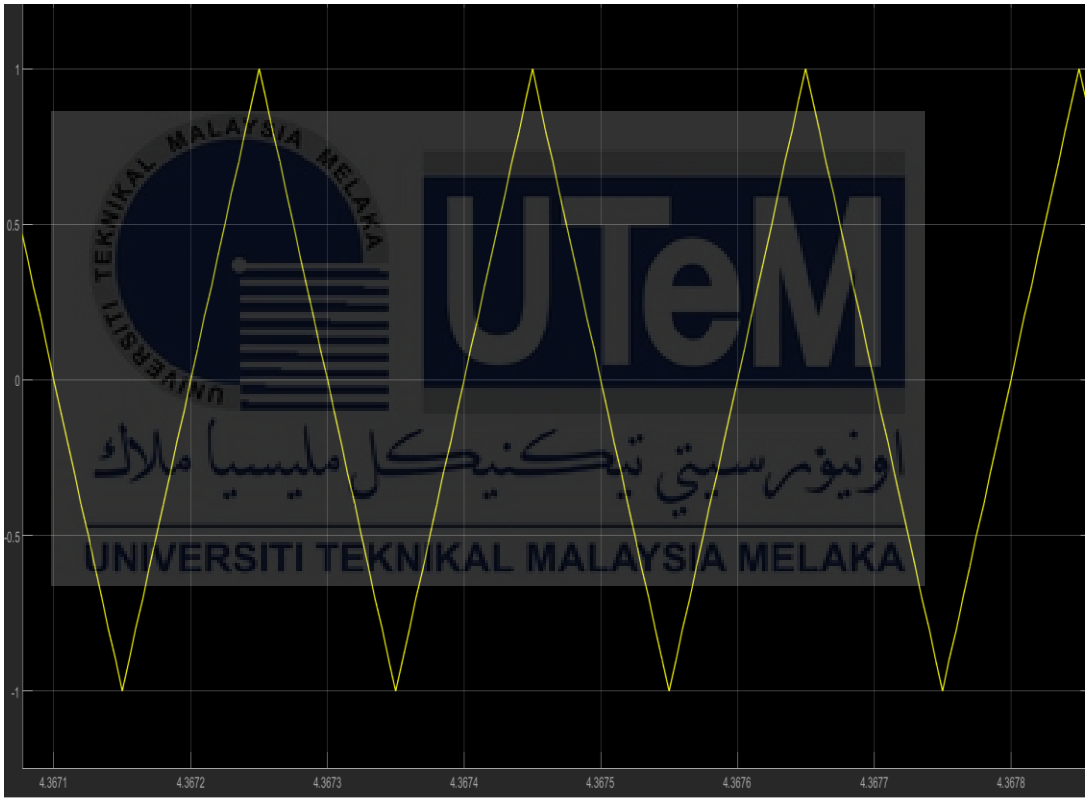


Figure 4.18: The triangular wave that have set

4.3.1 The results of Resonance Phenomena That Occur For The Full Bridge Phase Shift DC-DC Converter

Results below show that ZVS occur via resonance phenomena when the input voltage to the converter varies from minimum input voltage of 350 V DC to

maximum input voltage of 400 V DC to maintain the reference output voltage of 150V DC.

The below results shows that the resonant tank that design for the full bridge phase shift DC-DC converter have function well to allow ZVS occur during pulse width modulation of the signal pulses of the MOSFETS. During the positive cycle, the MOSFET 2 at the lagging leg at the simulation will undergo phase shift respect to the MOSFET 1 at the leading leg to regulate the output voltage when the input voltage varies from reference voltage of 350 V DC to 390 V DC. During switching loss due to the disconnected of MOSFET 2 when undergo phase shift, conduction loss will occur and the input voltage become zero. The inductance and capacitance at the resonant tank will discharge the snubber capacitor and inductor in MOSFET 3 as show in the simulation and charge MOSFET 2, ZVS will occur at MOSFET 3 at this moment which current free wheel through MOSFET 1 and MOSFET 3.

Lets refer to the results below for the input voltage of 360 V. From figure 4.20 the graph of the input voltage and the output current from MOSFET 2 which the graph in blue colour is the input voltage and the graph in yellow colour is the output current, shows the resonance phenomena that allow ZVS cause some delay for the output current to decrease to minimum when MOSFET 2 disconnect and increase to maximum when the MOSFET 2 reconnect. This is because the place of the inductor in the resonant tank that cause the output current lag behind the input voltage. The output current decrease to negative value during the disconnection of MOSFET 2 and increase slowly when MOSFET reconnect. These cause the area crossing under the graph of input voltage and the output current become lower and the efficiency is maintain by ZVS during phase shift of the pulse signals of the MOSFETS. By theoretical, the smaller the area crossing under the graph of input voltage and output current, the higher the efficiency of the converter. The results below shows the same condition when the input voltage varies to 370 V, 380 V and 390 V which the area crossing under the input voltage graph and the output current is maintain at the small area which prove that ZVS occur to maintain the efficiency of the converter by reducing the switching losses when phase shift of the pulse signals of the MOSFETS switch carry out to maintain the desire output voltage of 150 V.

4.3.2 Input voltage of 360 V DC , D= 0.97

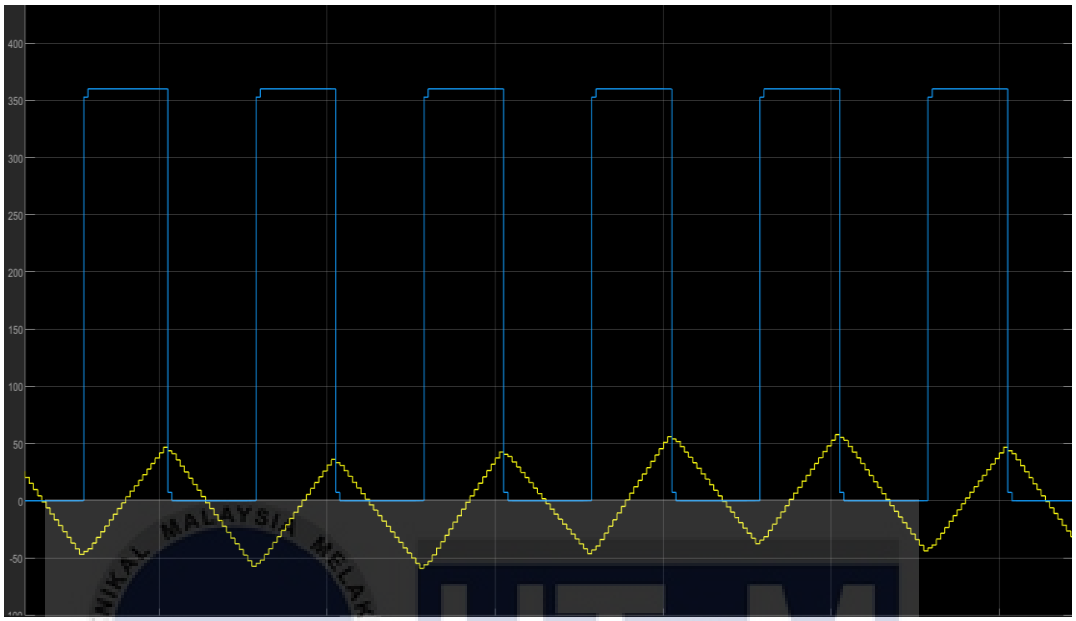


Figure 4.19: The graph of the input voltage and the output current which the graph in blue colour is the input voltage and the graph in yellow colour is the output current

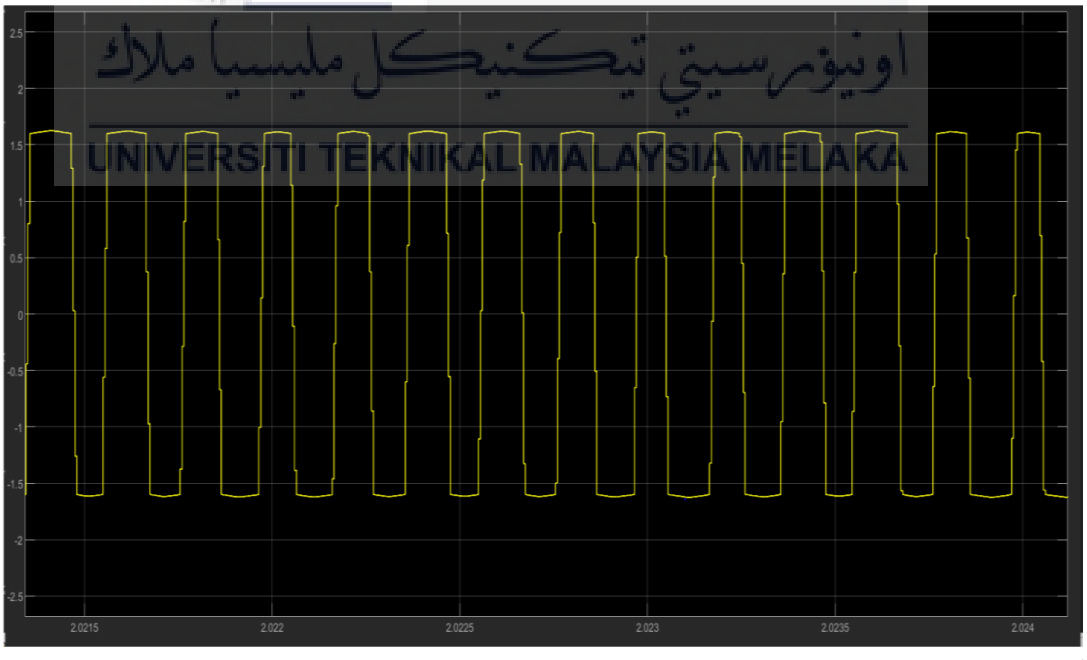


Figure 4.20: The Desire output voltage

4.3.3 Input voltage of 370 V DC, D= 0.95

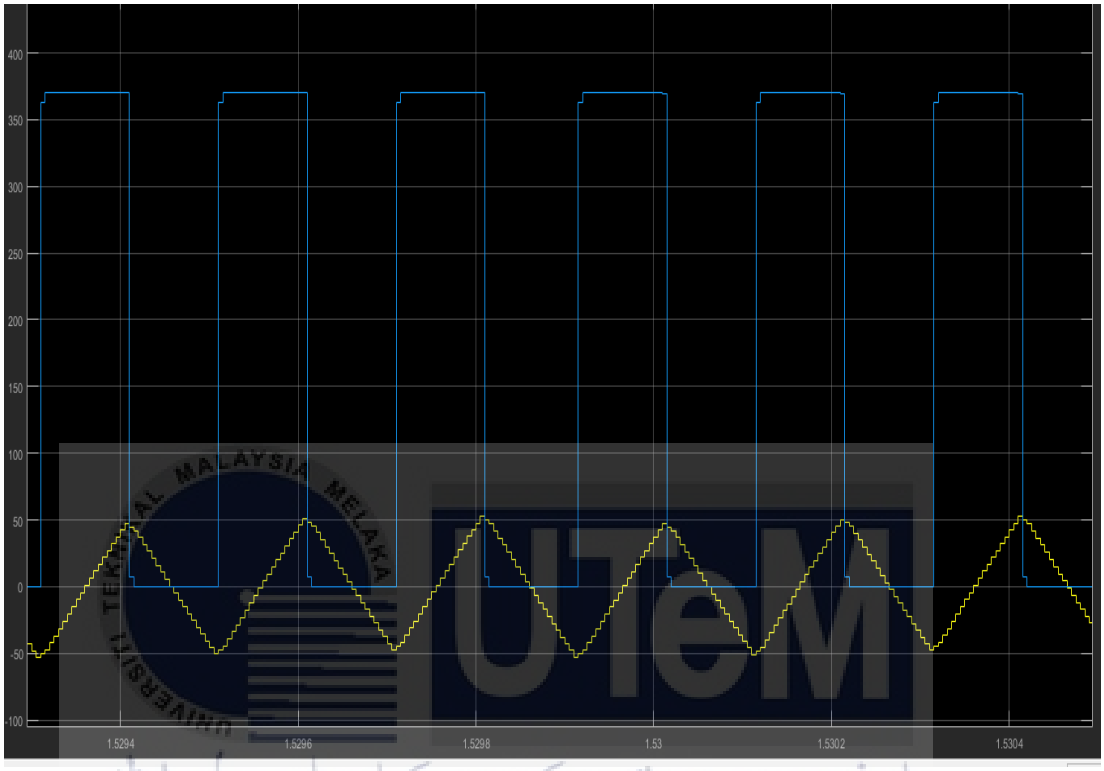


Figure 4.21: The graph of the input voltage and the output current which the graph in blue colour is the input voltage and the graph in yellow colour is the output current

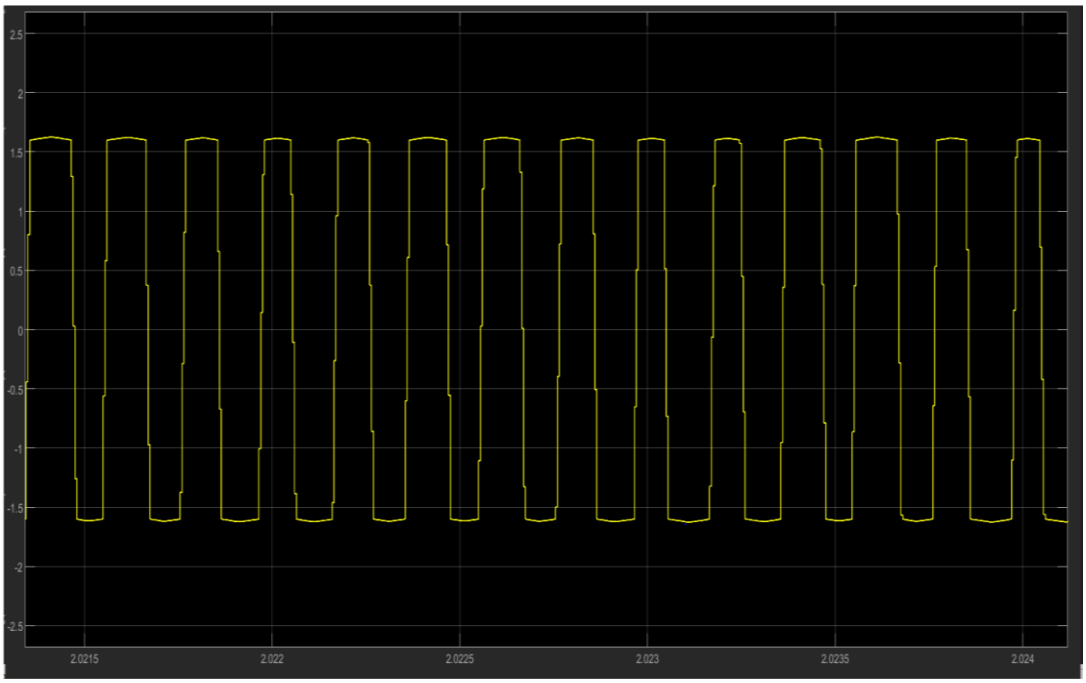


Figure 4.22: The Desire output voltage

4.3.4 Input voltage of 380 V, D= 0.92

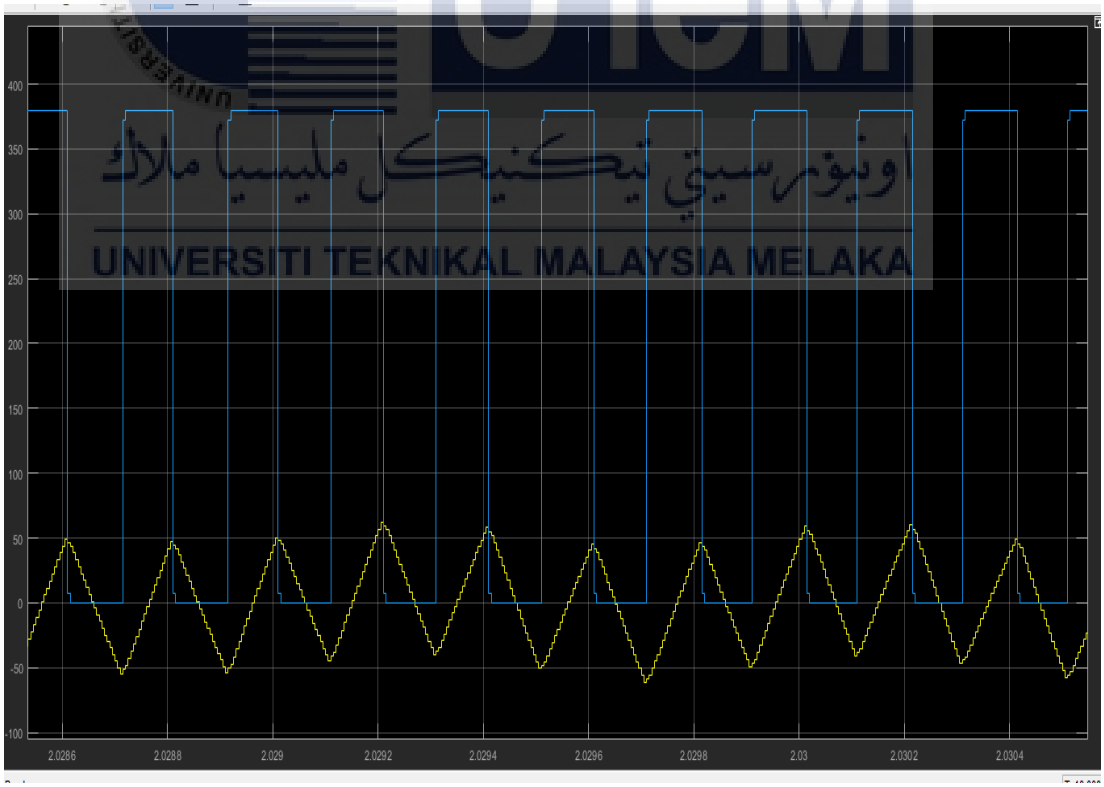


Figure 4.23: The graph of the input voltage and the output current which the graph in blue colour is the input voltage and the graph in yellow colour is the output current

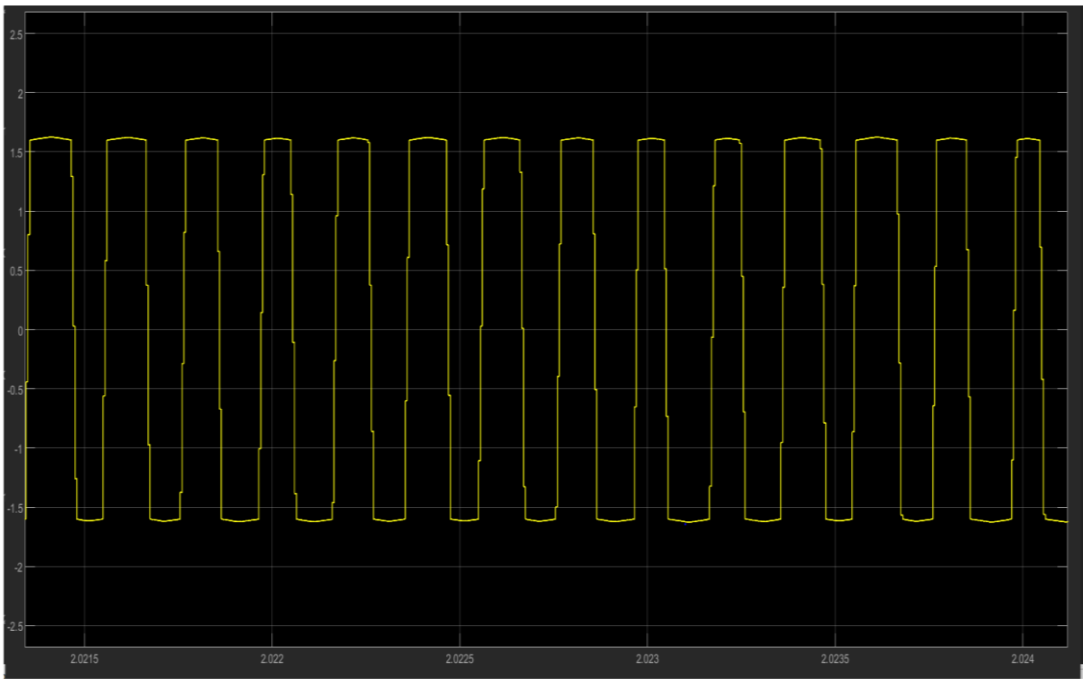


Figure 4.24: The Desire output voltage

4.3.5 Input voltage of 390 V , D= 0.89

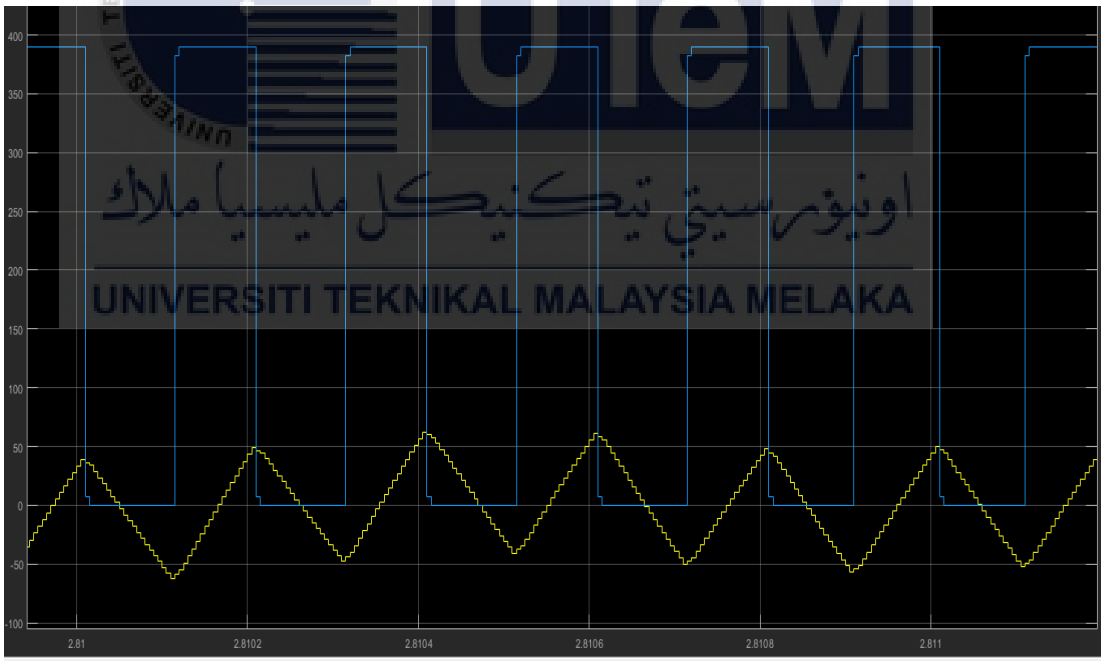


Figure 4.25: The graph of the input voltage and the output current which the graph in blue colour is the input voltage and the graph in yellow colour is the output current

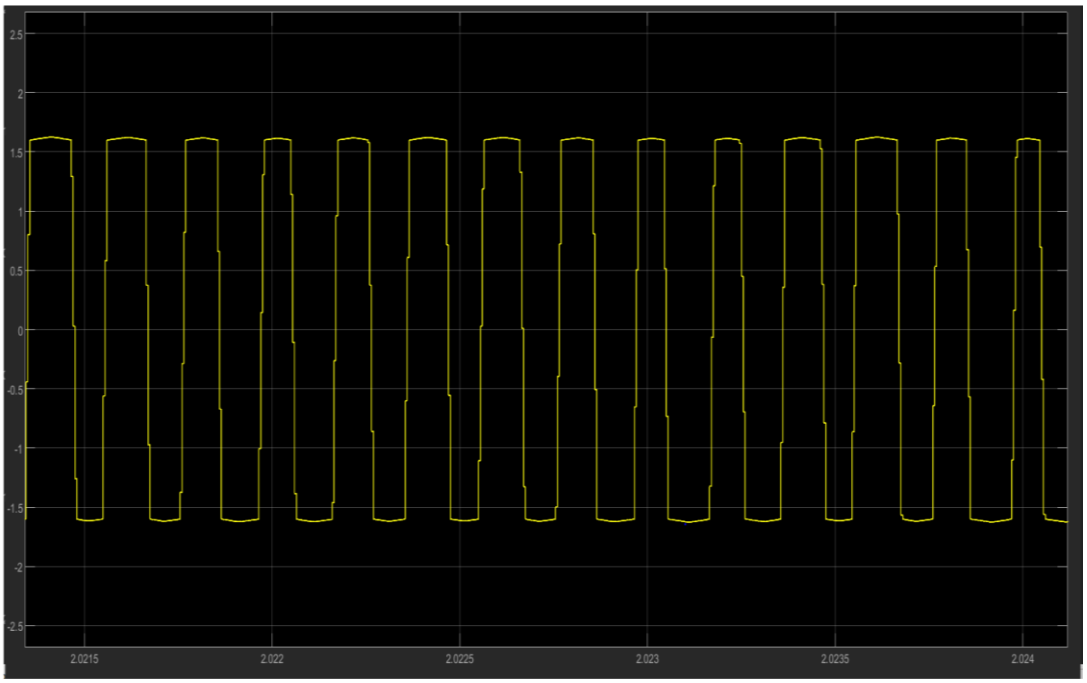


Figure 4.26: The Desire output voltage

4.4 Design Of Close Loop Phase Shift Full Bridge DC-DC Converter

In this section, the close loop phase shift full bridge DC-DC converter have been develop in order to control the output voltage maintain the desire value when there is fluctuate of the input voltage. The purpose to develop this close loop phase shift full bridge DC-Dc converter is to boost the output voltage to the desire value needed when the input voltage is fluctuated . The simulation of close loop phase Shift full bridge DC-DC converter show as figure 4.27 below.

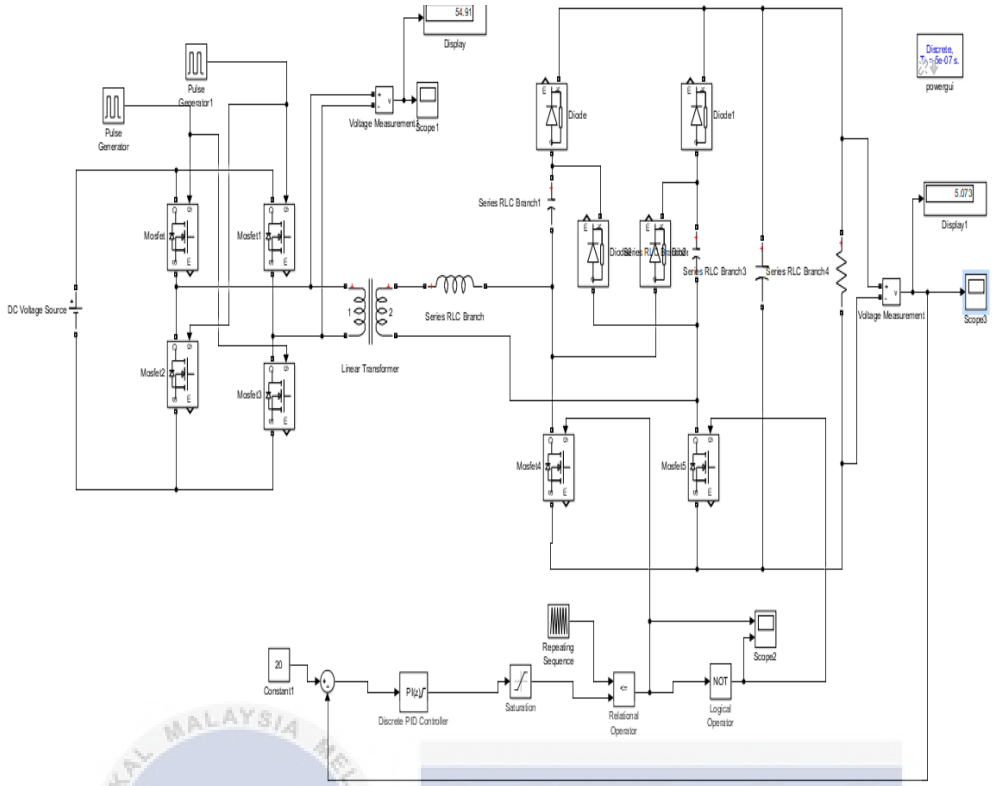


Figure 4.27: Simulation of close loop full bridge phase shift DC-DC converter

The reference output voltage that set for this converter is 20 V and the reference input voltage is 60 which is design to step down the input voltage. If the input voltage is fluctuated, in order to maintain the reference output voltage, the close loop control which consists of PI controller is used. For the close loop part as show in figure 4.27, The output voltage will feed back to compare with the reference output voltage. After the output voltage have compared with the desire output voltage, if there is different from the reference output voltage, the error signal will given to the PI controller and compare with the reference triangular wave form that have been set at the repeating sequence by using the relational operator and generate the waveform as show in figure 4.28 to control the MOSFETS at the secondary side of the converter which located at the AC to DC side to regulate and boost the output voltage to the reference value.

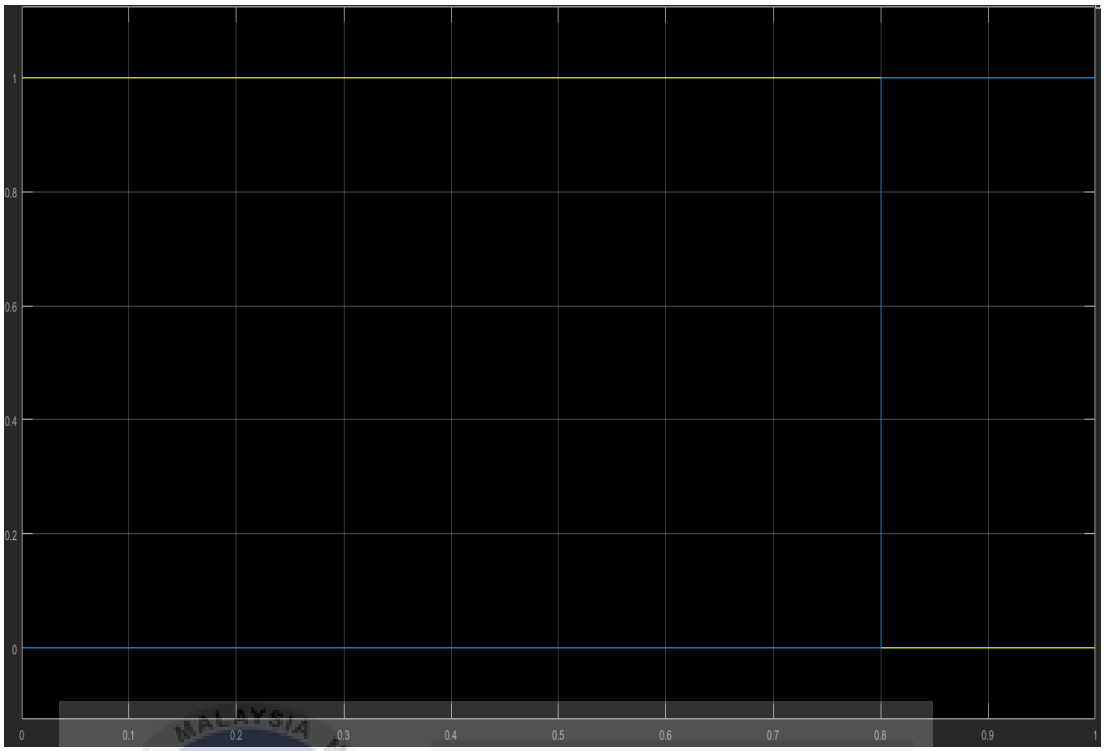


Figure 4.28: Waveform generated to control the MOSFETS at the secondary side of the converter

The function of the saturation is used to set the lower and upper limit which the PI controller able to function to regulated the voltage level to the reference value. Which the upper limit is the minimum voltage level that fluctuated and the lower limit is the maximum voltage level that fluctuated. For this close loop phase shift full bridge DC-DC converter, the input voltage range that have been designed is 45 V to 60V which 60 V is the reference input voltage and 20 V reference output voltage. If the input voltage fluctuated from 59V to 45V , the PI controller able to boost and regulate the reference output voltage of 20 V. The parameters of the PI controller have been set as table 4.1 below.

Table 4.1: The parameters of the PI controllers

Proportional gain (Kp)	8000000
Integral gain (Ki)	5000000000
Saturation limits	[0.98-0.7]
Sample time	5e-07

The value of the proportional gain must be always greater than the integral gain. Below show the results when the input voltage change from 60 V to 45V . The results shows that the output voltage that corrected is not exactly 20 V as same as the

reference voltage that have been set which have around plus minus 5 V. This is because the core losses of the transformer and diode losses of the converter.

4.4.1 Input voltage of 55V

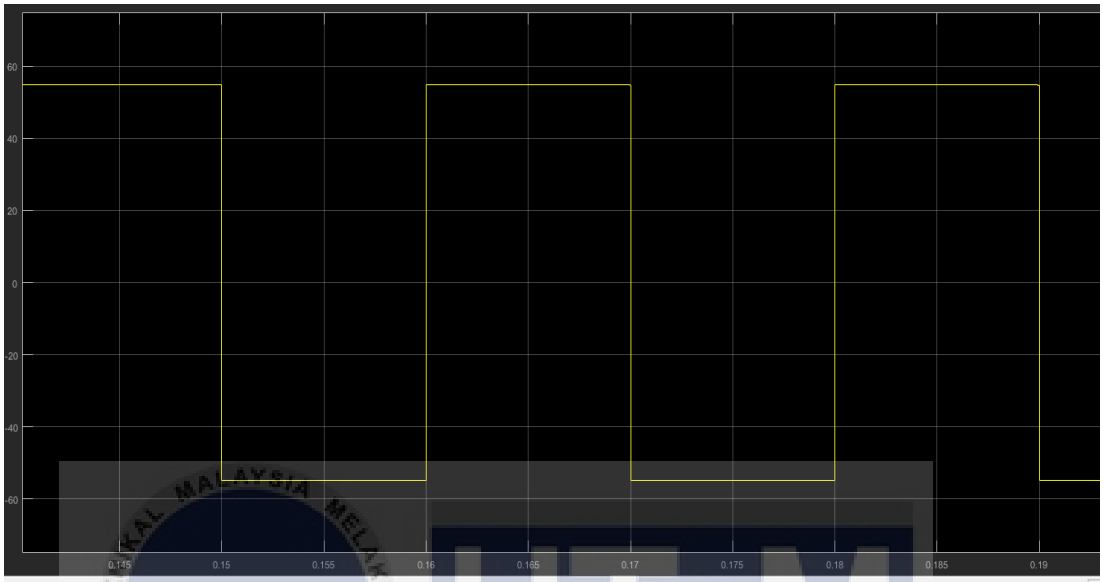


Figure 4.29: The input voltage after the DC to AC converter at the primary side

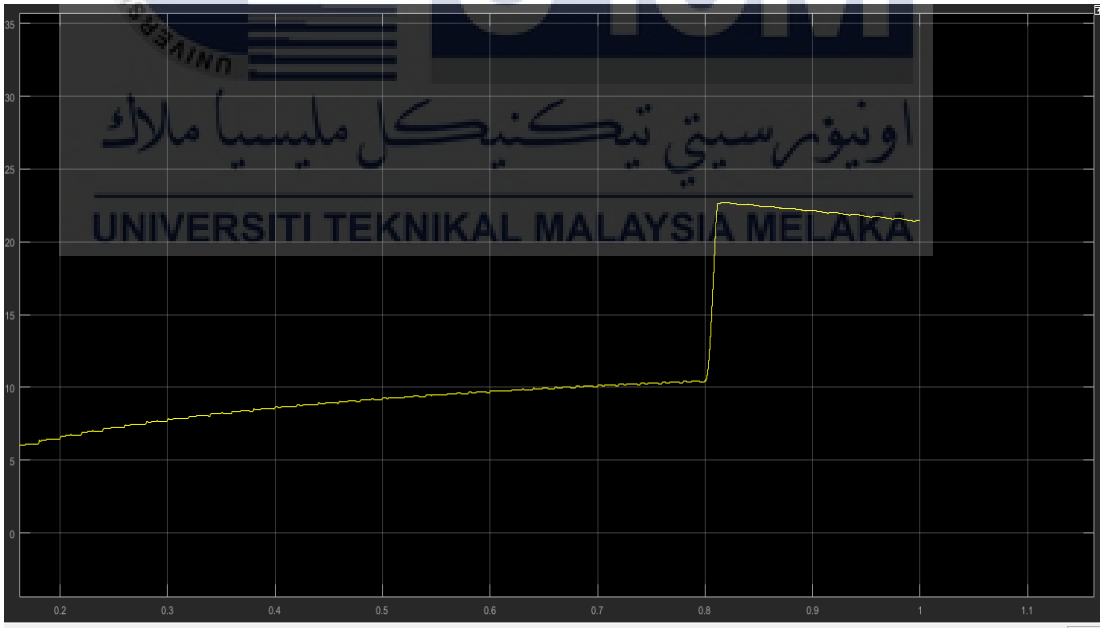


Figure 4.30: Graph that show the process that the PI controller to regulate the output voltage to the reference value

4.4.2 Input Voltage of 50 V

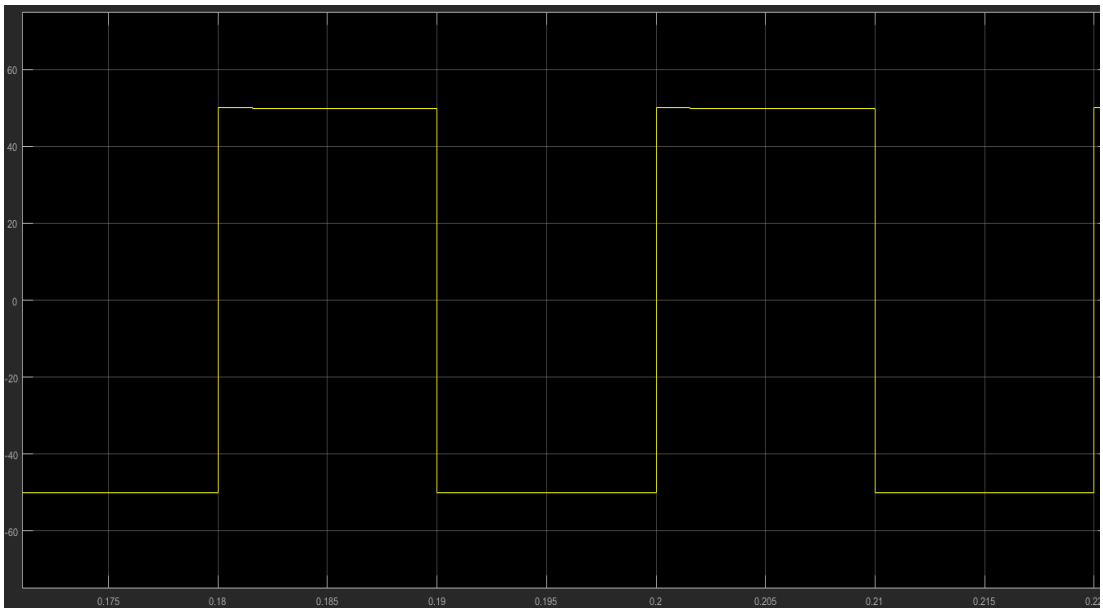


Figure 4.31: The input voltage after the DC to AC converter at the primary side

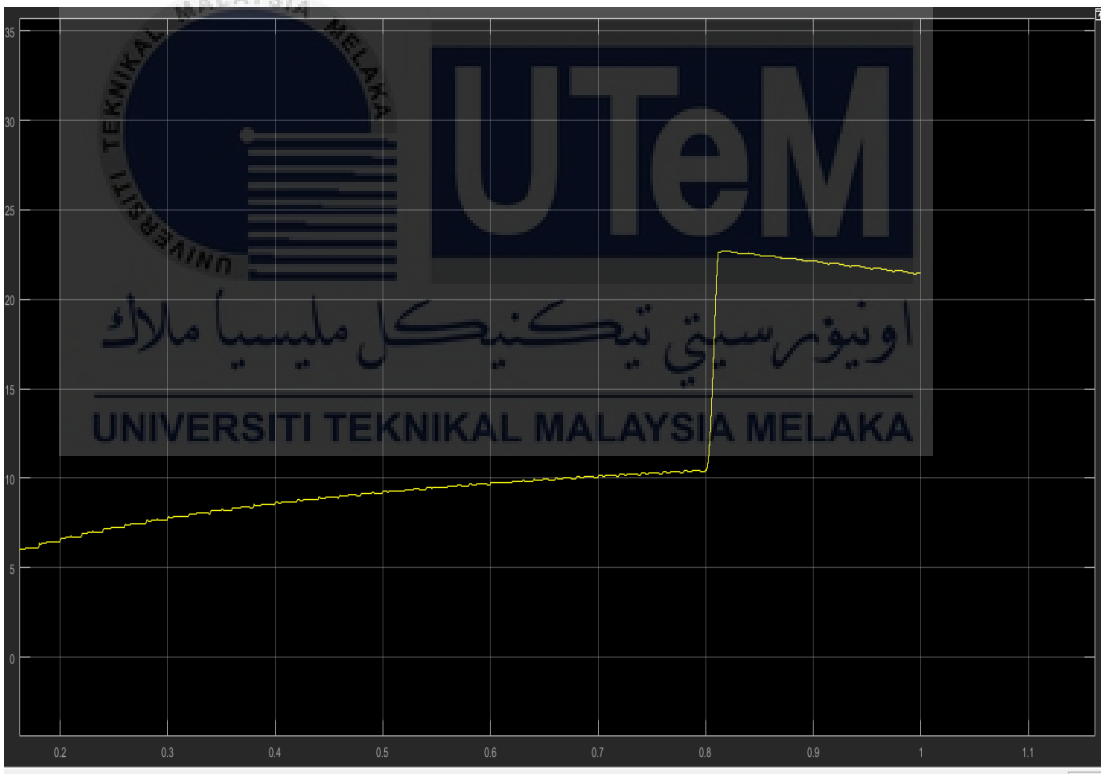


Figure 4.32: Graph that show the process that the PI controller to regulate the output voltage to the reference value

4.4.3 Input Voltage of 45V

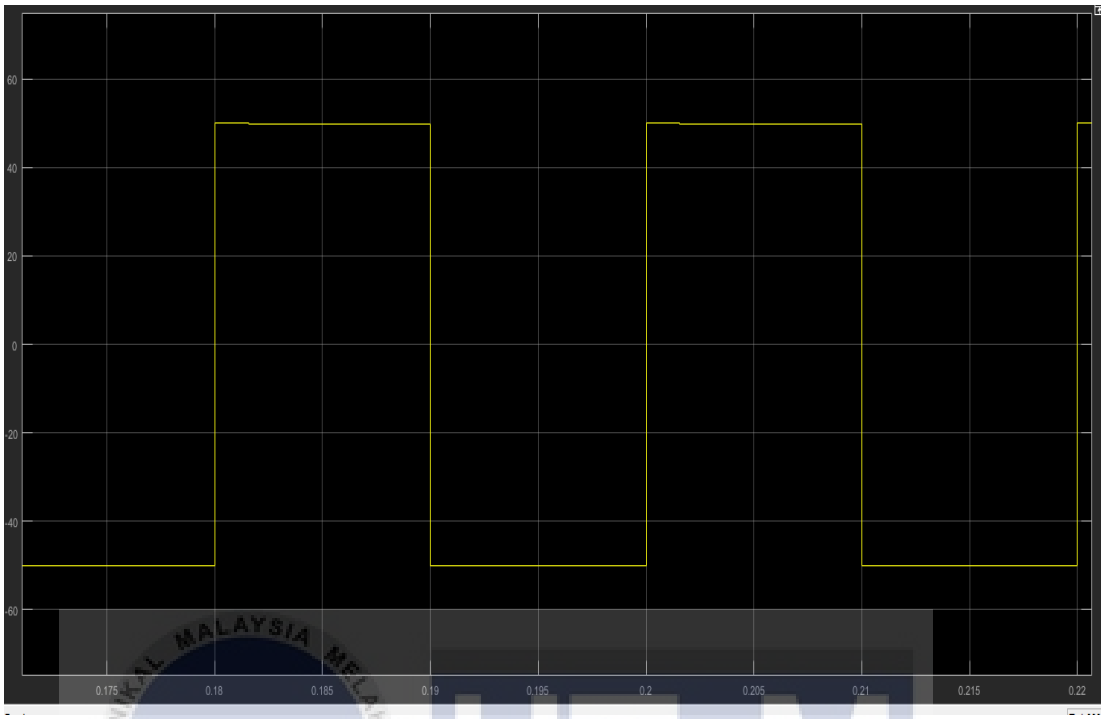


Figure 4.33: The input voltage after the DC to AC converter at the primary side

Figure 4.34: Graph that show the process that the PI controller to regulate the output voltage to the reference value

CHAPTER 5

CONCLUSION AND RECOMMENDATIONS

5.1 Conclusion

As a conclusion, the three objectives that present in this report have achieve which the first is use the theory of phase shift modulation of the pulse signal of the switches to reduce the output voltage to a desire value when the overload of the input voltage is occur. This have been done by maintain the input voltage for the phase shift full bridge DC to DC converter for 100 V DC and set the transformer ratio to 1:2. Next undergo phase shift for the pulse signal of the MOSFETS by set the phase delay to 0.85 and 0.75 to step down the output voltage to 170 V DC and 150 V DC. From this results, it shows that if overload from the input voltage from renewable energy occur, the phase shift of the pulse signal of the MOSFETs can applied to maintain the reference output voltage. From PSM, there is a conduction and switching loss occur at the MOSFET switches due to this hard switching [1,3]. So, for objective 2, a ZVS full bridge phase shift ZVS DC to DC converter have been designed to improve the system efficiency and eliminate the conduction and switching losses of the MOSFET switches during phase shift modulation to regulate the output voltage. The iterative method from [1,3] have been discussed to analyse and design a phase shift full bridge ZVS DC to DC converter by analyse and determine the circuits parameters that have been discuss previously in the literature review. The method from [1,3] have been try to simulate in MATLAB/ SIMULINK but have been failed. So, the other method have been use which evaluate the efficiency of the converter through the area overlap between the output voltage and the output current from the MOSFETS after undergo PSM. From the results, it shows that the area that overlap between the output current and voltage from MOSFETS will maintain the same although the input voltage varied and PSM carried to maintain the reference output voltage. Lastly, the a close loop phase shift full bridge ZVS DC to DC converter with PI controller have been designed in order to regulate

the output voltage automatically when fluctuated of the input voltage from renewable energy occur .

This chapter contains a brief summary of the entire work, including methods, results and major conclusions /recommendations arising from the work. This chapter can be written in a single section or in separately numbered sections. Weaknesses, shortcomings and strengths of the project are presented. Recommendations for future work may also be included together with contributions of project. Any potential of commercialization or practical application must also be included.

5.2 Future Works

For MATLAB/ SIMULINK software, there is some weakness in for the design of phase shift full bridge ZVS DC-DC converter. For MATLAB/ SIMULINK, the ZVS operation that carry out to maintain the efficiency of the converter when PSM occur to regulated the output voltage is evaluate through the area that overlap between the output voltage and current from the MOSFETS after PSM carry out. When the area that overlap between the output voltage and the current of the converter is maintain at small area when the input voltage varied and PSM is carry out to regulate the output voltage to reference output voltage, that means ZVS has carry out and the efficiency of the converter have maintain. This is less accurate because for MATLAB/ SIMULINK unable to read the output power and input power from the converter to evaluate the efficiency of the converter after undergo PSM to regulate the output voltage. Even from [1,3] shows that MATLAB/SIMULINK can get the input and output power, but fail when simulated the circuit in MATLAB/ SIMULINK maybe lack of information. For future recommendation, hope that other students can continue this project by using the PSIM software to design a full bridge phase shift ZVS DC to DC converter which PSIM software able to evaluate the input and output power from the converter after PSM carry out to regulate the output voltage.

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APPENDICES

APPENDIX A : GANTT CHART FOR FYP 1 and FYP 2