OPTIMIZATION OF 16NM DOUBLE GATE FINFET DEVICE FOR REDUCED VARIABILITY AND ENHANCED PERFORMANCE

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UNIVERSITI TEKNIKAL MALAYSIA MELAKA

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OPTIMIZATION OF 16NM DOUBLE GATE FINFET DEVICE FOR REDUCED VARIABILITY AND ENHANCED PERFORMANCE

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This report is submitted in partial fulfilment of the requirements for the degree of Bachelor of Electronic Engineering with Honours

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APPROVAL

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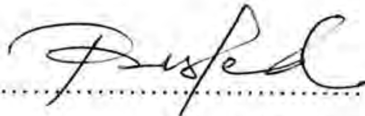
Signature : 

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DEDICATION

For my beloved parents, family, lectures, friends and whom going through up and down with me during this journey. Thank you for everything.

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ABSTRACT

The evolution of electronic technology is directly proportional with the evolution of the semiconductor industry. According to Gordon Moore, he predicted that the number of transistors in integrated circuit would double every two years. Therefore, this observation can be proved by shrinking the transistor size to obtain high drive current due to the denser transistor per chip. However, the continuous miniaturization process leads to some drawbacks when it enters the nanometer scale. As this research worked on 16nm size in gate length, there were a few approaches to solve the short channel effect (SCE). Throughout the project, the process simulation of the transistor was performed by using a ATHENA module in Silvaco TCAD. Meanwhile, the electrical characterization of the device was implemented by using ATLAS module. In this research, the transistor was designed by employing double gate (DG) FinFET structure. Then, it was tested with three different materials such as Titanium Oxide (TiO_2), Hafnium Oxide (HfO_2) and Silicon Nitride (Si_3N_4) as gate dielectric. From the analysis, the Titanium Oxide produced the best results for threshold voltage (V_{TH}), drive current (I_{ON}), leakage current (I_{OFF}) and sub-threshold swing (SS). Then, the transistor was optimized by statistical method, 2k-factorial to get the optimum response. The effect of process parameter variation was reduced by this technique. After optimization process, the values of V_{TH}, I_{ON}, I_{OFF} and SS is 0.241V, 1589.3µA/µm, 15.82pA/µm and 97.43mV/dec respectively. All the final results are well within the International Technology Roadmap Semiconductor (ITRS) 2013 for high performance (HP) Multi Gate (MG) technology for the year 2015. Therefore, the optimization of 16nm DG FinFET with different material dielectric using 2k-factorial was successfully achieved.

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ABSTRAK

Evolusi teknologi elektronik meningkat seiring dengan evolusi industri semikonduktor. Menurut *Gordon Moore*, beliau meramalkan bahawa jumlah transistor dalam litar bersepadu akan bertambah dua kali ganda setiap dua tahun. Oleh itu, pemerhatian ini dapat dibuktikan dengan mengecilkan saiz transistor untuk mendapatkan arus pemacu yang tinggi disebabkan oleh bilangan transistor per cip yang lebih padat. Walau bagaimanapun, proses pengecilan yang berterusan menyebabkan beberapa kelemahan apabila ia memasuki skala nanometer. Oleh kerana kajian ini dilakukan pada saiz 16nm, terdapat beberapa pendekatan untuk menyelesaikan masalah kesan saluran pendek (SCE). Sepanjang projek ini dijalankan, proses simulasi bagi transistor dilakukan dengan menggunakan modul ATHENA dalam Silvaco TCAD. Sementara, pencirian elektrik bagi peranti dilaksanakan dengan menggunakan modul ATLAS. Dalam kajian ini, transistor direka bentuk dengan menggunakan struktur dua get (DG) FinFET. Kemudian, ia diuji dengan tiga jenis bahan yang berbeza seperti Titanium Oksida (TiO_2), Hafnium Oksida (HfO_2) dan Silikon Nitrida (Si_3N_4) sebagai dielektrik get. Dari analisis, Titanium Oksida menghasilkan keputusan yang paling baik bagi voltan ambang (V_{TH}), arus pemacu (I_{ON}), arus bocor (I_{OFF}) dan ayunan ambang (SS). Kemudian, transistor dioptimumkan dengan kaedah statistik, *2k-factorial* untuk mendapatkan tindak balas yang optimum. Kesan variasi parameter proses dikurangkan dengan teknik ini. Selepas proses pengoptimuman, nilai bagi V_{TH}, I_{ON}, I_{OFF} dan SS adalah 0.241V, 1589.3μA/μm, 15.82pA/μm dan 97.43mV/dec masing-masing. Semua keputusan akhir adalah dalam linkungan Hala Tuju Teknologi Antarabangsa bagi Semikonduktor (ITRS) 2013 untuk teknologi tinggi (HP) Get Pelbagai (MG) bagi tahun 2015. Oleh itu, pengoptimuman 16nm DG FinFET dengan bahan dielektrik yang berbeza menggunkan *2k- factorial* berjaya dicapai.

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LIST OF SYMBOLS AND ABBREVIATIONS

ANOVA	:	Analysis of Variance
CMOS	:	Complementary Metal Oxide Semiconductor
DIBL	:	Drain induced barrier lowering
FD SOI MOSFET		Fully Depleted Silicon On Insulator Metal Oxide Semiconductor Field Effect Transistor
FinFET	:	Fin Field Effect Transistor
HfO_2	:	Hafnium oxide
IC	:	Integrated Circuit
I_{OFF}	:	Leakage current
I_{ON}	:	Drive current
ITRS	:	International Technology Roadmap Semiconductor
L_g	:	Gate length
μm	:	Micrometer
MOSFET	:	Metal Oxide Semiconductor Field Effect Transistor
nm	:	Nanometer
NMOS	:	N-type MOSFET
PD SIO MOSFET	:	Partially depleted silicon on insulator Metal Oxide Semiconductor Field Effect Transistor
PMOS	:	P-type MOSFET
SCE	:	Short channel effect

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SiO_2	:	Silicon dioxide
Si_3N_4	:	Silicon Nitride
SOI	:	Silicon on insulator
SS	:	Sub threshold swing
TCAD	:	Technology Computer Aided Design
TiO_2	:	Titanium Oxide
V_{TH}	:	Threshold voltage

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CHAPTER 1

INTRODUCTION

The simulation project about optimization of 16nm Double Gate FinFET device by using Silvaco TCAD. Basically, the earliest part of report will give the introduction and elaborate more on project background. Besides, it also contains a problem statement, objective and scope of the study.

1.1. Background

Nowadays, almost electronic devices have their own integrated circuit (IC). Practically, this makes the device become smarter and sophisticated. IC is semiconductor wafer that has millions of tiny transistors, capacitors and resistors which fabricated altogether on it. There are many advantages of using IC as part of the technology. For instance, the small size of IC makes it lighter in weight and less power required. Besides, IC is high reliability since there is no soldering connection and easy

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replacement in case of failure chip. Therefore, the advancement of the technology is in line with the human desire which require superior performance of device in term of low power consumption, speed, quality and absolutely low price.

The IC can be function as an amplifier, oscillators, timer, counter, computer memory or microprocessor. The numerous application of IC is found in a wide range of electronic devices such as television, smartphone, computer, graphic card, RAM, microwave, camera and also aero plane, space craft and military equipment's. In short, the presence of IC really give high impact and revolutionized the electronic industry since their invention. Historically, the development of the modern electronic device began since 1925 where it depends on the first solid state transistor. It is also known as metal-oxide-semiconductor field effect transistor or MOSFET. Certainly, the transistor is the real backbone or the workhorse of the blooming of the electronic industry.

The transistor plays the vital role such an amplifier and switch. For an amplifier, the transistor can amplify the current from the input and produced larger current at the output. Next, the transistor also operates as an electronic switch by being completely on or completely off where it has stated 'On' and 'Off' or '1' and '0'. The one and zero or binary code is used for encoding data in computing and telecommunication. Hence, the transistor is very crucial in the development of the computer and any digital device. Simultaneously, this influence the engineers to keep minimize the size of transistor to provide the best achievement of IC. Between 1970 and 2011, the gate length of MOSFET shrank from 10um to 28nm. Subsequently, the number of transistors increases tremendously from 200 to over 1 000 000 per square millimeter in the IC.

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For more than a few decades, the miniaturization of MOSFET is following the Moore's Law. Moore' law is the observation that the number or transistor in a dense integrated circuit double approximately every two years [1]. Then, absolutely the density of transistors in IC can be increased. This will make a higher transistor drive current that can faster switching speed and lowering the production cost [2]. As addition, Intel began releasing FinFET CPU technology in 2012 with its 22nm Ivy Bridge processor. The law then is used to update the International Technology Roadmap for Semiconductor (ITRS).

Recently, Intel had announced their product, Intel's "Knight's Corner" Xeon Phi supercomputer component processor contain an astonishing 7 billion transistors. This ultimate record has defeated another processor such as Kirin 970 from Huawei's, Apple A10 Fusion designed by Apple Inc. and Snapdragon 835 Qualcomm's best chipset. The number of transistors per chip are 5.5 billion, 3.3 billion and 3 billion respectively. To emphasize the development of the integrated circuit, the coming fifth generation wireless broadband, 5G, also contribute in this field. 5G is latest evolution of wireless revolution mobile communication network. Its offer the consumers for having higher data transfer speed, ten times faster than 4G technology which it take less than a second. Besides, 5G also offer shorter delays and increased connectivity among consumers and devices. Eventually, this phenomenon also contribute to the Internet of Thing (IoT) and the Fourth Industrial Revolution (IR 4.0). Hence, this prove that the presence of transistor really affecting the world entirely.

Another important development in the evaluation of the MOSFET is the gate dielectric of the transistor. Earlier, silicon oxide (SiO_2) was used as gate dielectric. Nevertheless, the leakage current annoyed the electrical characteristics. So, SiO_2 was

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replaced with the high-k dielectric material. Moreover, the high-k material allows increased gate capacitance without the increase leakage effect. There were three different materials tested in this project such as hafnium oxide (HfO_2), titanium oxide (TiO_2) and silicon nitride (Si_3N_4). All the experiments were conduct accordingly. Then, the best high-k material were measured based on the performance of double gate FinFET such as the threshold voltage, current drive, current leakage and sub threshold slope. Generally, the threshold voltage is always become the leading electrical characteristic as it determine the functionality of the device.

So, in this research, the study was focused on the new structure of transistor, double gate FinFET (DG FinFET) to replace the bulk MOSFET [3]. The FinFET is a type of non-planar or 3D transistor where the conducting channel rise above the level of insulator. Eventually, the phenomenon create a thin silicon structure shape like a fin, called a gate electrode. The fin shaped electrode allows double gates to operate on single transistor. The bonus of this design are definitely can double up the current drives and have better control short channel effect. To compare, the bulk transistor which equivalent to the planar transistor, the planar design was built on silicon on insulator (SOI) substrate. As conclusion, DG FinFET is an improvement form of fully depleted SOI device with extremely narrow buried oxide.

Overall, the project investigate the design and optimize the 16 nm DG FinFET using Silvaco TCAD. The software is very convenient for the researcher to test the feasibility feature of the transistor in a short time. The simulation of the device was performed by using ATHENA module while the electrical characterization of the device was implemented by using ATLAS module. This advanced nanotechnology was optimized by analyzing the process parameter variance in order to reduce the

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variability and enhance the performance. The technique to identify the process parameter whose variability would impact the most on the device characteristic was realized through a process using Design of Experiment (DOE). Thus, 2k-factorial statistical method was chosen in determining the best factor to be improved.

1.2. Problem Statement

The smaller the size of the transistor, the capacitance will reduce, eventually increasing the operating speed. Besides, the transistor also capable to enlarge the memory capacity and packing density. Since the invention of the first calculation machine, miniaturization has been a constant challenge to increase the speed and the complexity in the microelectronic industry. As the MOSFET transistor approaching the nanotechnology regime, there is also the presence of unwanted side effects. When the channel of MOSFET becomes the same order of magnitude as the depletion layer width of source and drain, the transistor achievement diminished. Eventually, the performance of the device also degrades such as high power dissipation.

The process downscaling of the MOSFET has led to some drawbacks of Short Channel Effects (SCE) like drain induced barrier lowering (DIBL), surface scattering, velocity saturation, impact ionization and hot carrier injection. The statistical fluctuation causes variations in electrical device parameters which also known as process variation. It will irritate the parameters such reduce the threshold voltage control, increase the sub threshold slope and leakage current exponentially. The reduced threshold voltage causes the sub threshold leakage current to increase dramatically and make the device difficult to turn off. In order to tackle the arisen problem, the FinFET is the best solution to perform. The replacement structure of the

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transistor from planar to non-planar double gate FinFET is undeniable will produce better gate control and suppression on the short channel effects.

1.3. Objective of Study

The main goal of the project is to study the characteristic of DG FinFET and compare with the MOSFET. Specifically, the objectives of the study are:

(i) To design 16nm DG FinFET device using ATHENA module

(ii) To analyze electrical characteristic of 16nm DG FinFET using ATLAS module

(iii) To optimize the process parameter variance in 16nm DG-FinFET device for reduce variability and enhanced performance.

1.4. Scope of Study

The research project is based on simulation and programming development. This project is to optimize the process parameter in 16nm Double Gate FinFET using 2k-factorial method in the Minitab Statistical Software. The design of 16nm DG FinFET will follow International Technology Roadmap of Semiconductor (ITRS) 2013 for the year 2017. The fabrication of 16nm DG FinFET will be designed by ATHENA module, whereas the electrical characteristic will be analyzed by ATLAS module. The electrical characteristics that will be determined are drive current (I_{ON}), leakage current (I_{OFF}), threshold voltage (V_{TH}) and Sub threshold Swing (SS).

1.5. Report Structure

The thesis contains five chapters which include the introduction, literature review, methodology, result and conclusion. Chapter 1 is an introduction of the final year

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