DESIGN AND OPTIMIZATION OF A BILAYER GRAPHENE ON 22 NM PMOS DEVICE

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UNIVERSITI TEKNIKAL MALAYSIA MELAKA

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DESIGN AND OPTIMIZATION OF A BILAYER GRAPHENE ON 22 NM PMOS DEVICE

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This report is submitted in partial fulfillment of the requirements for the degree of Bachelor of Electronic Engineering with Honors

Faculty of Electronic and Computer Engineering
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DEDICATION

To my beloved parents, brothers and sister, thank you for your endless love and support, without them, I would be aimless. To my lecturers and friends, guidance and knowledge were shared and discuss together till a sleepless night. Thank You.

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ABSTRACT

A bilayer grapheme on 22 nm PMOS device was optimized and analyzed to obtain the optimum value of performance parameters. The device consists of Titanium dioxide (TiO_2) as a high permittivity (high-k) and Tungsten silicide (WSi_x) as a metal gate. The ATHENA and ATLAS modules from the Silvaco software were utilized to simulate the virtual device fabrication process and to verify the electrical properties of the device respectively. Taguchi L9 orthogonal array method was then employed to improve the device process parameters for the optimum threshold voltage (V_{TH}) and lowest leakage current (I_{LEAK}) in-line with International Technology Roadmap for Semiconductor (ITRS) specification which are -0.289 V ± 12.7% (V_{TH}) and 100 nA/µm (I_{LEAK}).The result from the signal-to noise ratio (SNR) of nominal-the-better (NTB) for V_{TH} and smaller-the-better (STB) for I_{LEAK} are then analysed by the percentage that affects the process parameters. The results in the simulation shows that halo tilting angle and S/D implantation are the most dominant factor and adjustment factor in affecting the V_{TH} and I_{LEAK} respectively. The optimized results show an outstanding device performance with V_{TH} of -0.2893V which is 0.0261% closer to the ITRS 2012 target and I_{LEAK} is 0.0389 nA/µm which is far lower than the prediction.

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ABSTRAK

Dua lapisan grapheme pada peranti PMOS 22 nm dioptimumkan dan dianalisis untuk mendapatkan nilai parameter yang optimum. Modul ATHENA dan ATLAS dari perisian Silvaco digunakan untuk mensimulasikan proses fabrikasi peranti maya dan untuk mengesahkan sifat-sifat elektrik peranti. Kaedah orthogonal Taguchi L9 kemudiannya digunakan untuk memperbaik proses parameter peranti untuk voltan ambang yang optimum (V_{TH}) dan kebocoran arus yang rendah (I_{LEAK}) sejajar dengan spesifikasi PelanTindakanTeknologi Antarabangsa untuk Semikonduktor (ITRS) iaitu -0.289 V (V_{TH}) dan 100 nA/µm (I_{LEAK}). Hasil dari nisbah isyarat-ke-bunyi (SNR) nominal-lebih-baik (NTB) untuk V_{TH} dan kecil-lebih-baik (STB) untuk I_{LEAK} kemudian dianalisis oleh peratusan yang mempengaruhi parameter proses. Keputusan dalam simulasi menunjukkan bahawa sudut condong halo dan implantasi S/D adalah faktor yang paling dominan dan factor penyelarasan yang mempengaruhi V_{TH} dan I_{LEAK} masing-masing. Hasil yang dioptimumkan menunjukkan prestasi peranti yang bagus dengan nilai V_{TH} -0.2893 V yang mana 0.0261% lebih dekat dengan target ITRS 2012 dan I_{LEAK} adalah 0.03898 nA/µm yang jauh lebih rendah daripada ramalan.

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LIST OF SYMBOLS AND ABBREVIATIONS

V_{TH}	:	Threshold voltage
I_{LEAK}	:	Leakage current
High-k	:	High permittivity
ITRS	:	International Technology Roadmap for Semiconductor
TiO_2	:	Titanium dioxide
WSi_x	:	Tungsten silicide
MOSFET	:	Metal-oxide-semiconductor field-effect transistor
CMOS	:	Complementary metal-oxide-semiconductor
SiO_2	:	Silicon dioxide
Poly-Si	:	Polycrystalline silicon
S	:	Source
G	:	Gate
D	:	Drain
B	:	Body
V_{GS}	:	Gate-source voltage
I_{DS}	:	Drain-source current
V_{DS}	:	Drain-source current

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V_P	:	Pinch-off voltage
I_{DSS}	:	Saturated current
HfO_2	:	Hafnium dioxide
ZrO_2	:	Zirconium dioxide
Al_2O_3	:	Aluminium dioxide
BF_2	:	Boron Difluorite
BPSG	:	Borophosphosilicate glass
PMD	:	Pre-metal dielectric
SNR	:	Signal-to-Noise Ratio
NTB	:	Nominal-the-Best
ANOVA	:	Analysis of Variance

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CHAPTER 1

INTRODUCTION

1.1 Introduction

In this chapter, an introduction of a bilayer graphene PMOS device, including the background of this project are discussed. Next, the problem statement which leads to the idea of this project is discussed. The objectives, scope of project and report structure are also discussed in this chapter.

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1.2 Background

The rule of scaling was presented by Gordon E. Moore in his fundamental paper distributed in 1965 which recommended that the transistor thickness on the chip should double every two years [1]. This innovation has been prompted by the International Technology Roadmap for Semiconductors (ITRS) for a successful device scaling in the accompanying 15 years [2]. The evaluation of complementary metal-oxide-semiconductor (CMOS) technologies requires a low power for fast growing mobile applications that can provide low standby power, enhanced performance, and active power without a high cost.

One of the most technologies that are designed for a low power application to meet the above requirement is a high-k / metal gate [3]. The researcher designed new innovation technology utilizing high permittivity (high-k) materials as the gate dielectric material which is being combined with metal gates. This creation just supplanted the conventional silicon dioxide (SiO_2) and polycrystalline silicon (poly-Si) gate structure design respectively [4]. The carrier mobility also degrades due to remote coulomb scattering and variations in material parameter, although the high-k / metal-gate technology significantly reduces the gate leakage current and offer better electrostatic integrity over gate oxide [5].

Recently, graphene a 2-D carbon-based material, has draw interest among researcher. In 2004, groups from Manchester University (Manchester, U.K.) and from Georgia Institute of Technology (Atlanta, GA, USA) distributed two pioneering papers on the development of graphene and the event of the field impact in their samples. Moreover, high carrier mobility has been discovered in graphene [6].

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1.3 Problem Statement

The downscaled CMOS structure gives a considerable measure of difficulties to researchers as the smaller measurements will prompt the inefficiency of the device to function. One of the fundamental challenges in creating a nanoscale transistor is to control its threshold voltage (V_{TH}) since V_{TH} mismatch will influence the entire system of the device and worst scenario, the device will not be functioning [7].

A bilayer graphene was then presented together with the employment of pairing high-k / metal gate as the top gate of the transistor to produce the bandgap, modulates the drain current and limits the carrier mobility through the channel [2]. The enhancement in downscaling of the device structure is considered in order to obtain a smaller dimensional device with the best threshold voltage (V_{TH}) by optimizing the process parameter variability using Taguchi method [4].

1.4 Objectives

The objectives of this research are:

i. To design and simulate a bilayer graphene on high-k / metal gate on 22 nm PMOS device by using Silvaco.
ii. To analyze and optimize the electrical characteristics of device by using Taguchi L9 orthogonal array method.

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1.5 Scope of Work

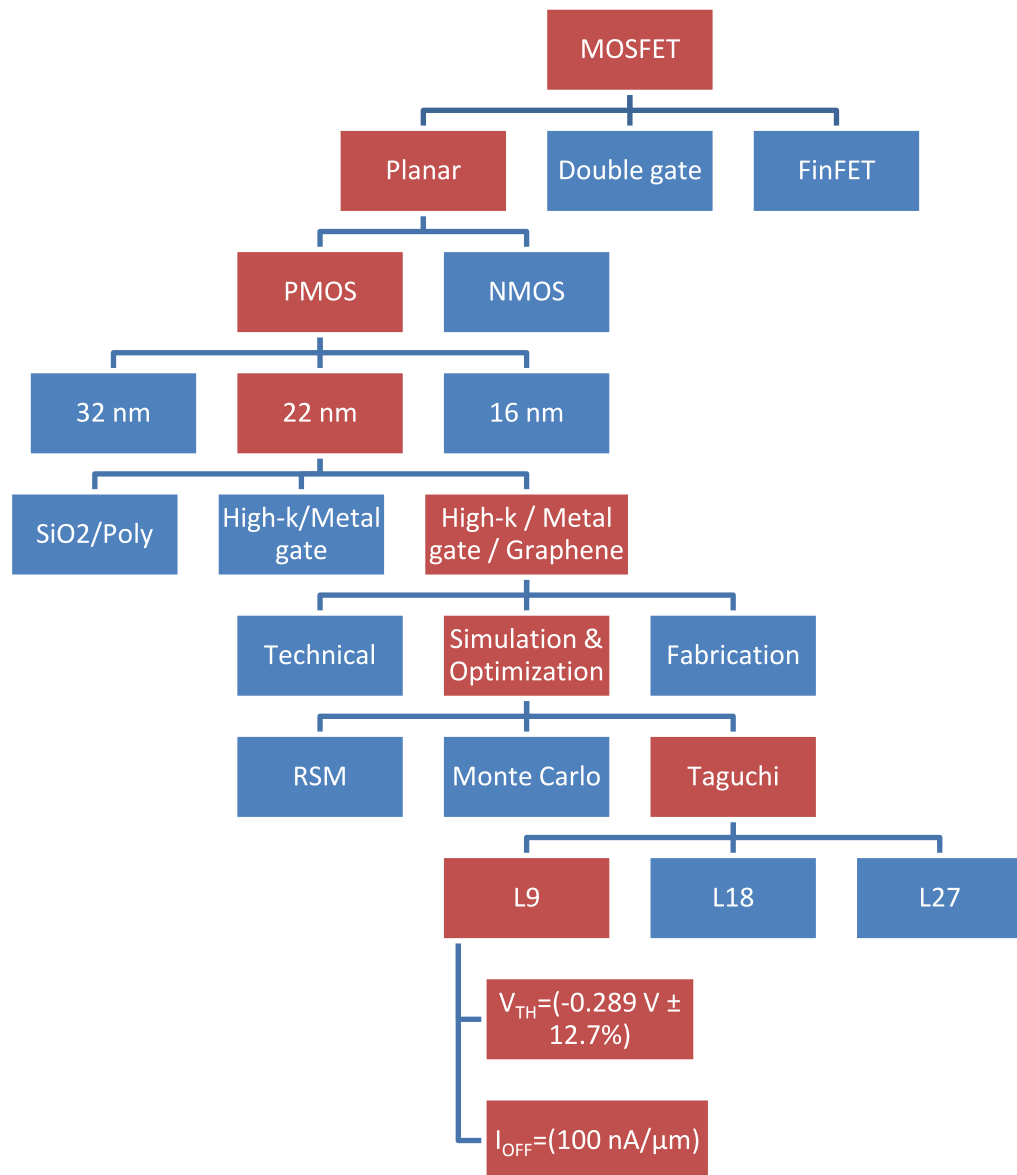

Figure 1.1: Scope of work flowchart

Figure 1.1shows the flowchart of this project scope. For the software that will be use to complete this project are Silvaco software. The Silvaco ATHENA will use to design the device while the Silvaco ATLAS is for the electrical properties. In EXCEL, Taguchi method is applied for statistical analysis to search a good combination to produce a device with better performance. Next, the existing device structures are the high-k Titanium dioxide (TiO_2) and Tungsten silicide (WSi_x) metal

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gate. For the addition, graphene will be added to this project to be tested. No equipment will be needed in this project because this project only covers for simulation. Lastly the size of the prototype is 22 nm PMOS device.

1.6 Report Structure

This report focuses on designing and simulates a bilayer graphene on high-k/metal gate on 22 nm PMOS device by using Silvaco. This report is divided into five major chapters which are introduction, literature review, methodology, results and discussions also, conclusion and future work. Chapter 1 discusses about the background of the project, problem statement, objectives, scope of project and the report structure. Chapter 2 discusses about the literature review which includes the introduction, and other studies that relates to this project which are MOSFET fundamental, Moore's Law, high-k / metal gate, graphene properties and summary of papers from previous study. Chapter 3 discusses about the methodology used to fulfill the objectives and the scope of project. In this chapter, experimental setup, software requirement, flowchart which illustrates the project progress from the beginning through the end of the project and summary will be discussed. Chapter 4 discusses about the results obtained and discussion from the design project. In this chapter, the result from the virtual transistor fabrication steps, the device electrical properties and the process parameter chosen from the orthogonal Taguchi L9 method are discussed. Chapter 5 discusses about the conclusion that can be conclude from the results and the future work for this project.

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CHAPTER 2

BACKGROUND STUDY

2.1 Introduction

Chapter 2 of this project report provided the introduction to the metal-oxide-semiconductor field-effect transistor (MOSFET) device and the Moore's Law which is the rule of transistor scaling. Furthermore, this chapter has a review of the materials that are used to design the PMOS device. There are several advantages of the materials properties are reviewed in this chapter. Besides that, this chapter reviews the studies of previous paper that are related to this project.

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2.2 MOSFET Fundamental

A semiconductor device which is broadly utilized for switching and amplifying electronic signals in the electronic devices is known as MOSFET transistor. MOSFET is a core of integrated circuit due of these small sizes and it can be designed and fabricated on a single chip. There are four terminals in MOSFET device which are source (S), gate (G), drain (D) and body (B) terminals. However, the body of the MOSFET is usually combined to the source terminal making it a three terminal device like field effect transistor. By far, MOSFET is the most widely transistor and can be used in both analog and digital circuits [8].

2.2.1 Transistor Electrical Characteristic

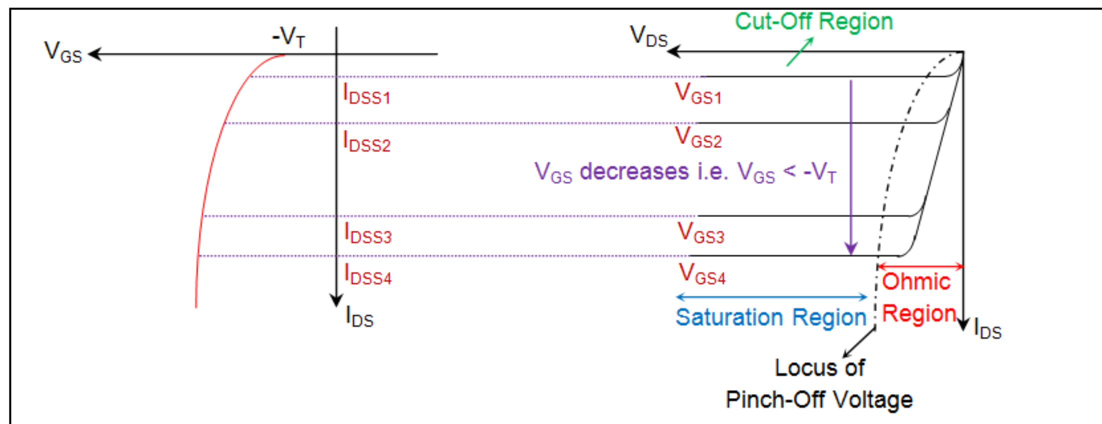

Figure 2.1: Electrical Characteristic Curve

Figure 2.1show the I_D remains zero (cut-off state) until gate-source voltage (V_{GS}) becomes equal to $-V_{TH}$ [9]. This is due to connect the drain terminal and the source terminal of the device to form a channel. From the graph, it can be seen that the increment of drain-source current (I_{DS}) in inverse direction, which signifying the increase of device current that will flow from source to drain, and the decrease in the

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value of drain-source current (V_{DS}). This shows that the device is operating in its ohmic region where the current through the device increases as the voltage applied increases.

However, when the V_{DS} become equal to negative pinch-off voltage, – (V_P), the device will enter into saturation mode which a saturated current (I_{DSS}) flows through the device by the value of V_{GS}. As the V_{GS} becomes more negative, the value of saturation current flows through the device will increase [9].

2.3 Scaling MOSFET

Hot-electron effects extremely constrained the progress of MOSFET innovation, especially CMOS technology. From the earliest, the essential idea of integrated-circuit technology has been to utilize advanced lithographic and process techniques to make ever smaller devices and to expand the chip-level integration.In 1963, CMOS circuits were stated with the guarantee of irrelevant standby power dissipation. Thus, when the theory of MOSFET scaling was distributed, the possibility of MOSFET circuits with low standby power dissipation, that is both easy to make and scaleable, appeared to be very feasible. The expected drain current equation for the scaled MOSFET is as shown in equation 2.1 [10].

$$I_d(scaled) = \frac{\mu_{eff}\varepsilon_{ox}}{t_{ox}/\mathrm{K}}\left(\frac{W/\mathrm{K}}{L/\mathrm{K}}\right)\left(\frac{V_g - V_t - V_d/2}{\mathrm{K}}\right)(V_d/\mathrm{K}) = \frac{I_d(reference)}{\mathrm{K}} \quad \textbf{(2.1)}$$

I_d (reference) - the drain current of the reference MOSFET

I_d (scaled) - the drain current of the scaled MOSFET

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