OPTIMIZATION OF GRAPHENE FIELD-EFFECT TRANSISTOR (GFET) DEVICE USING TAGUCHI-BASED GRA

MUHAMMAD ARIFF AFFIAN BIN CHE LAH

UNIVERSITI TEKNIKAL MALAYSIA MELAKA

OPTIMIZATION OF GRAPHENE FIELD-EFFECT TRANSISTOR (GFET) USING TAGUCHI-BASED GRA

MUHAMMAD ARIFF AFFIAN BIN CHE LAH

This report is submitted in partial fulfilment of the requirements for the degree of Bachelor of Electronic Engineering with Honours

Faculty of Electronic and Computer Engineering
Universiti Teknikal Malaysia Melaka

2018

UNIVERSITI TEKNIKAL MALAYSIA MELAKA
FAKULTI KEJUTERAAN ELEKTRONIK DAN KEJURUTERAAN KOMPUTER

BORANG PENGESAHAN STATUS LAPORAN
PROJEK SARJANA MUDA II

Tajuk Projek : OPTIMIZATION OF GRAPHENE FIELD-EFFECT TRANSISTOR (GFET) USING TAGUCHI-BASED GRA

Sesi Pengajian : 2017/2018

Saya MUHAMMAD ARIFF AFFIAN BIN CHE LAH mengaku membenarkan laporan Projek Sarjana Muda ini disimpan di Perpustakaan dengan syarat-syarat kegunaan seperti berikut:

1. Laporan adalah hakmilik Universiti Teknikal Malaysia Melaka.
2. Perpustakaan dibenarkan membuat salinan untuk tujuan pengajian sahaja.
3. Perpustakaan dibenarkan membuat salinan laporan ini sebagai bahan pertukaran antara institusi pengajian tinggi.
4. Sila tandakan (✓):

☐ **SULIT***	(Mengandungi maklumat yang berdarjah keselamatan atau kepentingan Malaysia seperti yang termaktub di dalam AKTA RAHSIA RASMI 1972)
☐ **TERHAD***	(Mengandungi maklumat terhad yang telah ditentukan oleh organisasi/badan di mana penyelidikan dijalankan.)
☐ **TIDAK TERHAD**	

Disahkan oleh:

(TANDATANGAN PENULIS) (COP DAN TANDATANGAN PENYELIA)

Alamat Tetap: Lot 1923, Jalan sentosa, Kg air tawar, 22200 Kg raja, Terengganu

Tarikh : 25 Mei 2018 Tarikh : 25 Mei 2018

*CATATAN: Jika laporan ini SULIT atau TERHAD, sila lampirkan surat daripada pihak berkuasa/organisasi berkenaan dengan menyatakan sekali tempoh laporan ini perlu dikelaskan sebagai SULIT atau TERHAD.

DECLARATION

I declare that this report entitled "Optimization of Graphene Field-Effect Transistor (GFET) using Taguchi-based GRA" is the result of my own work except for quotes as cited in the references.

Signature : .....

Author : MUHAMMAD ARIFF AFFIAN BIN CHE LAH

Date : .....

APPROVAL

I hereby declare that I have read this thesis and in my opinion this thesis is sufficient in terms of scope and quality for the award of Bachelor of Electronic Engineering with Honours.

Signature	:	……
Supervisor Name	:	DR FAUZIYAH BINTI SALEHUDDIN ……
Date	:	……

DEDICATION

To my beloved family members,

To my supportive supervisor,

And to my friends.

ABSTRACT

The aim of this research is to optimize the process parameters variations of graphene field-effect transistor (GFET) device using Taguchi-based grey relational analysis (GRA). The process of the device was initially stimulated using ATHENA module of Silvaco TCAD meanwhile the electrical characterization was carried out using an ATLAS module of Silvaco TCAD. The electrical characteristics that being calculated were threshold voltage (V_{th}), drive current (I_{on}), leakage current (I_{off}), current state ratio (I_{on}/I_{off}) and sub-threshold slope (SS). The L_9 orthogonal array (OA) method, signal-to-noise ratio (SNR) and analysis of variance (ANOVA) were used to analyze the effect the process parameters. The process parameters that were used are halo implant energy, halo implant dose, source/drain (S/D) implant energy and S/D implant dose with noise factors which were halo implant tilt angle and S/D implant tilt angle. All the experimental values are converted to grey relational grade (GRG) and the level of process parameter with the highest GRG are selected as the most optimal level. The values of I_{on}, I_{off}, I_{on}/I_{off} and V_{th} after optimization approaches were 612.21μA/μm, 0.69nA/μm, 1.04E6 and 0.548V respectively. Most of the results obtained were within the range and met the requirement of low power (LP) technology for the year 2015 as predicted by International Technology Roadmap Semiconductor (ITRS) 2013. As a conclusion, the design of GFET has successfully been created and through the Taguchi-based GRA, the optimal solution for the robust design of the devices has successfully been achieved.

ABSTRAK

Tujuan kajian ini adalah untuk mengoptimumkan variasi parameter terhadap peranti graphene transistor (GFET) menggunakan kaedah analisis hubungan Grey (GRA) berasaskan Taguchi. Proses bagi peranti disimulasikan dengan menggunakan modul ATHENA Silvaco TCAD sementara pencirian eletrikal dijalankan menggunakan modul ATLAS Silvaco TCAD. Ciri-ciri eletrikal yang telah dikira adalah voltan ambang (*Vth*), arus pacu (I_{on}), arus bocor (I_{off}), nisbah arus (I_{on}/I_{off}) dan *sub-threshold slope* (*SS*). Kaedah L_9 *orthogonal array* (OA), nisbah isyarat-kepada-bunyi (SNR) dan variasi analisis (ANOVA) telah digunakan untuk menganalisis kesan kepada parameter proses. Parameter proses yang telah digunakan adalah *halo implant energy*, *halo implant dose, source/drain (S/D*) *implant energy* dan *S/D implant dose* dengan faktor bunyi adalah *halo implant tilt angle* dan *S/D implant tilt angle*. Semua nilai eksperimen ditukar kepada *grey relational grade* (GRG) dan paras parameter proses dengan GRG tertinggi dipilih sebagai tahap paling optimum. Nilai bagi I_{on}, I_{off}, I_{on}/I_{off} dan V_{th} selepas dioptimumkan adalah 612.21μA/μm, 0.69nA/μm, 1.04E6 dan 0.548V masing-masing. Kebanyakan keputusan adalah didalam julat yang dibenarkan dan memenuhi keperluan yang telah ditetapkan oleh teknologi kuasa rendah (LP) untuk tahun 2015 yang telah ditetapkan oleh *International Technology Roadmap Semiconductor* (ITRS) 2013. Sebagai kesimpulan, reka bentuk GFET telah berjaya direka dan melalui kaedah GRA berasaskan Taguchi, penyelesaian optimum untuk reka bentuk yang teguh bagi peranti telah berjaya dicapai

ACKNOWLEDGEMENTS

In the name of Allah, the Most Gracious and the Most Merciful, all praises and thanks to Allah S.W.T as I have successfully finished this final year project. Firstly, I would like to express my thanks and appreciation to my supervisor, Dr. Fauziyah binti Salehuddin, who had been very helpful and supportive as she always help me in finishing my thesis. Her willingness to educate me in this project had been such a great help.

Apart from that, my deepest appreciation to my family members especially my parents, Che Lah bin Latif and Normah binti Hamid, other lecturers and friends for their supports and encouragements that led to my achievement. Last but not least, many thanks to all who directly or indirectly assisted me upon the accomplishment of this project.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

LIST OF SYMBOLS AND ABBREVIATIONS

CMOS	:	Complementary metal oxide semiconductor
MOSFET	:	Metal oxide semiconductor field-effect transistor
OLED	:	Organic light-emitting diode
R&D	:	Research and development
GFET	:	Graphene field-effect transistor
GRA	:	Grey relational analysis
LP	:	Low power
ITRS	:	International Technology Roadmap of Semiconductor
Bi-FET	:	Bilayer field-effect transistor
$S_I O_2$	:	Silicon dioxide
TCAD	:	Technology computer aided design
Bi-GFET	:	Bilayer graphene field effect transistor
DNA	:	Deoxyribonucleic acid
ITO	:	Indium tin oxide
V_0	:	Neutrality point
SNM	:	Special nuclear material

S_IC	:	Silicon carbide
GNRFET	:	Graphene Nano ribbon field-effect transistor
ULSI	:	Ultra large scale integration
2D	:	Two dimensional
EDA	:	Exploratory data analysis
1D	:	One dimensional
3D	;	Three dimensional
DC	:	Direct current
AC	;	Alternating current
V_{TH}	:	Threshold voltage
I_{ON}	:	Drive current
I_{OFF}	:	Leakage current
I_{ON}/I_{OFF}	:	Current state ratio
I_D	:	Drain current
V_G	:	Gate voltage
HfO_2	:	Hafnium dioxide
WSi_2	:	Tungsten silicide
Si_3N_4	:	Silicon nitride
BPSG	:	Boron phosphor silicate glass
PMD	:	Pre-metal dielectric
OA	:	Orthogonal analysis
S/N	:	Signal to noise ratio
ANOVA	:	Analysis of variance

SSQ	:	Sum of squares
DF	:	Degree of freedom
GRC	:	Grey relational coefficient
GRG	:	Grey relational grade
SS	:	Sub-threshold slope
MSSQ	:	Mean sum of squares
IC	:	Integrated circuit
S/D	:	Source/Drain
ANN	:	Analysis neural network

CHAPTER 1

INTRODUCTION

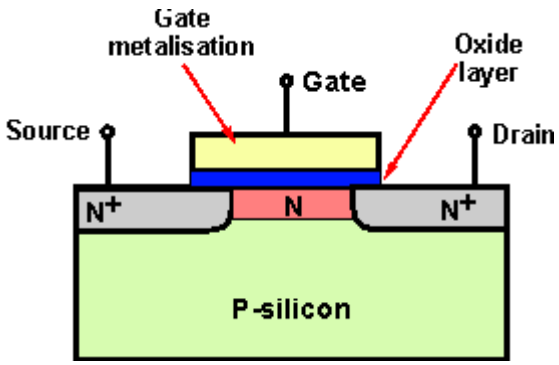
1.1 Background

Moore's law is predicated on shrinking the critical features of the planar process which is the smaller these features, the more the bits that can be packed into the given area. The most critical feature size is the physical gate length as shrinking it not only makes transistor smaller, it makes it faster. Simply, Moore's law postulates that the level of chip complexity that can be manufactured for minimal cost is an exponential function that doubles in a period of time [1]. Where Ct = Component count in a period t, Ct-1 = Component count in the prior period.

$$Ct = 2 \cdot Ct - 1 \tag{1.1}$$

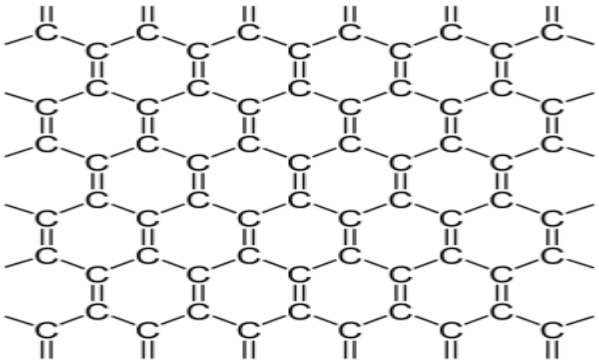
The amazing advancements to date in Complementary Metal Oxide Semiconductor (CMOS) technology have come primarily from scaling which is

reducing the critical dimensions of the transistors. This has been accomplished by advances in photolithography, innovations in the fabrication processes, and the use of new materials. One important approach is to increase the electron and hole mobility [1]. CMOS is the technology that constructed integrated circuits that also used in microprocessor and microcontroller. Typical design style with CMOS uses complementary and symmetrical pairs of p-type and n-type metal oxide semiconductor field effect transistors (MOSFETs) for logic functions [2]. CMOS transistors have inherent parasitic structures, such as diodes, resistors, and the capacitors, whereas the whole circuit may have inductor properties in the signal lines [3].



1.1: N-type semiconductor design

Graphene is allotrope of carbon in the form of a two-dimensional, atomic-scale, hexagonal lattice in which one atom forms each vertex [12]. Bilayer graphene is a material consisting of two layers of graphene which can be made by exfoliation from graphite [11]. It has zero band-gap and can behave like semiconductor. The energy dispersion of graphene is conical and has large modification in the carrier density [4].



1.2: Graphene structure

The application has widely increased nationwide. It is therefore expected to be applied to various electronic devices, such as transistors, interconnects, transparent electrodes, sensors, and new-principle devices [5]. Graphene is mostly being develop in room-temperature high resolution semiconductor radiation spectrometer because it has a negligible intrinsic capacitance [6]. The interest in graphene has mobilized both academic and industry realms making it an ideal candidate for the design of modern nano-scale transistors, chemical and biosensors, flexible and organic light-emitting diodes (OLEDs) displays, solar and fuels [7].

Robust design methods or commonly Taguchi method that created by Genichi Taguchi, is to increase the quality of goods mostly in engineering. This method will function in solving the multiple parameter optimization with less of experiments [8]. Robust engineering is an engineering optimization strategy ideally used for the development of the new technologies in the areas of product and process design. It represents the application of Taguchi Methods at the start of R&D or advanced product. It also concentrates on identifying the ideal functions for a specific technology. Then, it concentrates on selectively choosing the best nominal values of the design parameters that optimize performance reliability at lowest cost [9].