DESIGN AND OPTIMIZATION OF 22 NM NMOS DEVICE HIGH-K/METAL GATE WITH BI-LAYER OF GRAPHENE

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UNIVERSITI TEKNIKAL MALAYSIA MELAKA

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DESIGN AND OPTIMIZATION OF 22 NM NMOS DEVICE HIGH- K/METAL GATE WITH BI-LAYER OF GRAPHENE

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This report is submitted in partial fulfillment of the requirements for the degree of Bachelor of Electronic Engineering with Honours

Faculty of Electronic and Computer Engineering
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DEDICATION

Special dedicate to my family, supervisor and all my fellow friends in helping me to accomplish this report.

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ABSTRACT

This project is based on simulation and program development of NMOS device performance by adding a bi-layer of graphene by using Silvaco software. This project exhibits general structure of the simulation for the 22 nm NMOS device after simulated by ATHENA and ATLAS module. ATHENA is the Silvaco process simulator used for device fabrication tool while ATLAS simulation module performs the device simulator procedures for electrical characteristics. These two simulator are combined with Taguchi Method in order to optimize the process parameter. Silicon Dioxide is replaced with high-k material which is Titanium Dioxide and replaced polysilicon with metal gate which is tungsten silicide. As transistor is reduce in size, the thickness also decreased to increase the gate capacitance. As the thickness of high-k metal gate material scale to 22 nm, the leakage current will increase drastically due to channel tunneling which lead to high power consumption and lower device reliability. Therefore, replacing the traditional gate material with high-k metal gate allows gate capacitance to increase without any correlation with leakage effects.

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ABSTRAK

Projek ini adalah berdasarkan kepada simulasi dan pembangunan prestasi peranti NMOS dengan menambah satu lapisan graphene dengan menggunakan sistem perisian Silvaco. Projek ini mempamerkan struktur umum untuk 22 nm peranti NMOS selepas disimulasi menggunakan modul ATHENA dan ATLAS. ATHENA ialah simulator proses Silvaco yang digunakan untuk alat fabrikasi peranti sementara modul ATLAS sebagai prosedur simulator peranti untuk ciri-ciri elektrik. Kedua-dua simulator ini akan digabungkan dengan Kaedah Taguchi untuk mendapatkan parameter proses yang optimum. Silikon Dioksida digantikan dengan bahan High-k iaitu Titanium Dioksida manakala poli-silikon digantikan dengan get logam iaitu silisida tungsten. Oleh kerana saiz transistor dikurangkan, ketebalan juga berkurang untuk meningkatkan kapasitansi get. Ketebalan get logam high-k dikurangkan hingga 22 nm akan menyebabkan arus kebocoran meningkat secara drastik lalu mengakibatkan terowong saluran yang membawa kepada penggunaan kuasa yang tinggi dan kebolehpercayaan peranti yang lebih rendah. Oleh itu, menggantikan get tradisional dengan get logam high-k membolehkan kapasitansi pintu meningkat tanpa sebarang korelasi dengan kesan kebocoran arus.

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LIST OF SYMBOLS AND ABBREVIATIONS

SiO_2	:	Silicon Dioxide
TiO_2	:	Titanium Dioxide
WSiX	:	Tungsten Silicide
FET	:	Field Effect Transistor
Si	:	Silicon
MOSFET	:	Metal-oxide semiconductor field effect transistor
EOT	:	Electrical Oxide Thickness
V_{TH}	:	Threshold voltage
I_{off}	:	Leak current
ITRS	:	International Technology Roadmap for Semiconductor
V_{GS}	:	Gate source voltage
V_G	:	Gate voltage
LPCVD	:	low pressure chemical vapor deposition process
BPSG	:	Borophosphosilicate Glass
PMD	:	pre-metal dielectric
CF	:	Control Factor

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NF	:	Noise Factor
High-k	:	High dielectric constant k
EOT	:	Electrical Oxide Thickness
SOS	:	Silicon-on-Sapphire
OA	:	Orthogonal Array
S/D	:	Source/Drain

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CHAPTER 1

INTRODUCTION

This chapter presents a short introduction about the project. First, the background of the project is explained and is followed by the problem statement of project, the objectives of the project. Based on the problem statement and the objective of the project, the scope or limitation of the project is identified. Finally, the organization of the report is clarified.

1.1 Background of study

This research execution is based on simulation and program development of NMOS device performance and reliability related phenomena by adding a bi-layer of graphene by using TCAD Silvaco software. In this project, we replaced Silicon Dioxide (SiO_2) with high-k materials which is Titanium Dioxide (TiO_2) and replaced polysilicon with metal gate which is tungsten silicide (WSi_X). The reduction of the

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size of the dimensions of MOSFETs, is known as scaling. Scaling gate dielectric thickness of the device can lead to leakage current. Shifting a high-k material can help solving most of the problems such as decreasing gate leakage current and require an increased capacitance gate dielectric to control short channel effects. The expected results of this study are all objectives of this project which is to design and simulate a bi-layer graphene on high-k / metal gate on 22 nm NMOS device using SILVACO software is achieved in order to produce high reliable NMOS in small size.

Graphene could be a thin layer of pure carbon atoms that are bonded together in a very hexangular honeycomb lattice. It is the thinnest material better-known, however, it's passing robust, light-weight and versatile. It conducts heat better than diamond and will conduct electricity better than silver. This unique combination of properties makes graphene an ideal platform for flexible electronics [1].

A typical silicon technology is approaching its basic material and physical limits with continuous scaling, there's a growing push to seem for brand spanking new platform to design circuits or device for nanoelectronic applications. One in all the foremost necessary properties of graphene could be a robust electric field result that ends up in an electrostatically tunable carrier density within the vary of $n < 10^{14}$ cm. Commonly with high carrier mobility for both electrons and holes (as high as 10^4 cm^2/Vs at room temperature), this attracts a lot of attention to graphene as a possible material for a future high-speed field effect transistor (FET) [2].

Silicon dioxide (SiO_2) has been used because of the gate dielectric material over decades, and therefore the current device scaling trend needs the film thickness. In this case, the tunneling current can increase exponentially resulting in increased power dissipation. The increase in power dissipation would be a critical problem

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because of the thermal management issues in submicron device structures. Moreover, the use of thin oxide films is not reliable [3]. To overcome this problem many new high-k dielectric materials have been recently introduced as a replacement for SiO_2 gate dielectric film. Many metal oxides (Al_2O_3, ZrO_2, HfO_2, TiO_2, etc.) and ferroelectric materials are being reviewed and investigated as competitors to replace SiO_2. However, the combination of polysilicon (poly-Si) and high-k gate material is still relevant and can still be used in NMOS transistors [3].

The reduction of the dimensions of the scale of MOSFETs is usually called scaling. Scaling gate dielectric thickness of the device will result in discharge current (leakage current). High-k dielectrics are employed in semiconductor manufacturing processes that typically accustomed replace a silicon oxide gate insulator or another dielectric layer of a tool. The term high-k dielectrics refer to a fabric with a high dielectric constant k (as compared to silicon oxide). Shifting a high-k material will facilitate resolution most of the issues resembling decreasing gate leakage current and need an increased capacitance gate dielectric to regulate short channel effects. Smaller transistors need an increased capacitance gate dielectric to regulate short channel effects. Therefore, this device is introduced due to control the problems.

In this modern era, graphene has become a promising radiance in the horizon of fabrication technology, due to some of its distinctive electronic properties like zero band gap, high saturation velocity, higher electrical conductivity and mobility. Graphene could be an ideal use in the future because of electrons transfer at high speed. It also has an extraordinary thermal, optical and mechanical properties such as high thermal conductivity, optical transparency, flexibility and thinness. Graphene based devices requested to be thought as a potential selection for post Si based fabrication technology.

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1.2 Problem Statement

In trend of world competition, modern semiconductor industries have adjusted their production method to be a lot of economic and competitive. Regarding from that, a lot of advanced technologies got to scale down the MOSFET into nanometer. Since MOSFET are often scaled right down to a smaller dimension which produce higher performance, at the same time gate length and oxide thickness also reduce. Scaling is that the distinctive property of MOSET because it allows to decrease the size in nanoscale region. Scaling permits the reduction in dimension in all aspect but scaling cannot go on forever. There is limit of scaling beyond that the device does incorporate unexpected result [4]. As the thickness scales of reduced, leak currents because of tunneling increase drastically, resulting in high power consumption and reduce device reliability. Therefore, substitute SiO_2 with a high-k material allows increased in gate capacitance. Shifting a high-k material facilitate determination most of the issues such as decreasing gate leakage current and require an increased capacitance gate dielectric to control short channel effects. Smaller transistors require an increased capacitance gate dielectric to control short channel effects. Therefore, this device is introduced due to overcome the problems.

1.3 Objectives

i. To design and simulate a bi-layer graphene on high-k / metal gate on 22 nm NMOS device using SILVACO
ii. To analyze and optimization the electrical characteristics of device by using Taguchi L9 orthogonal array method

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1.4 Scope of Project

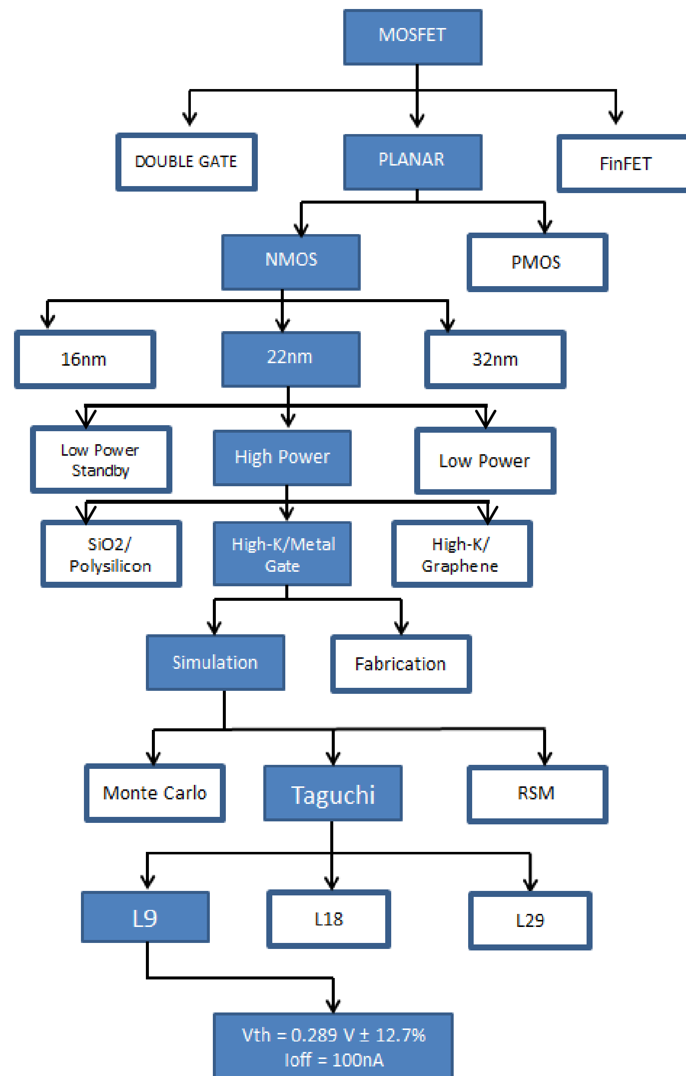

Figure 1.1: Scope of the project

This analysis execution relies on simulation and program development and downscaling a 22 nm of planar NMOS device performance and dependability related phenomena by adding a bi-layer graphene by using TCAD Silvaco software. The electrical characteristics of this device are analyzed by using the L9 experimental array of Taguchi method. Athena is the Silvaco process simulator used for device fabrication whereas ATLAS simulation module performs the device simulator procedures for electrical characteristics. These two simulators can be combined with

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