DESIGN AND DEVELOPMENT OF SYSTEM ON CHIP FOR SMART SIGN LANGUAGE TRANSLATOR GLOVE

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UNIVERSITI TEKNIKAL MALAYSIA MELAKA

DESIGN AND DEVELOPMENT OF SYSTEM ON CHIP FOR SMART SIGN LANGUAGE TRANSLATOR GLOVE

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This report is submitted in partial fulfilment of the requirements for the degree of Bachelor of Electronic Engineering with Honours

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DEDICATION

This thesis is dedicated to my family and Lee Chi Kee.

ABSTRACT

Typical sign language translator glove utilize general purpose microcontroller or microprocessor module which is higher in power consumption due to unused General Purpose Input Output (GPIO) and other functional blocks. Thus, a System-on-Chip (SoC) is designed using Intel 8051 Intellectual Property (IP) core as a substitution for the conventional microcontroller module to achieve higher integration while reduce the power consumption. In this work, a sign language translator glove for speech impaired community has been developed as the application. Trend of changes in sensors are used as the input of the system through the Inter-Integrate Circuit (I2C). The manipulated data will be transmitted though UART bus protocol to a Bluetooth Low Energy (BLE) module. The data is received by an Android smartphone for comparing with the database that are stored on Firebase Cloud Database and it will produces the corresponding output of the gesture through the speaker and display. Validation, simulation, verification and synthesis of the proposed design are implemented using Synopsys tools in SilTerra 180nm process technology to produce the final layout (GDSII) that is fabrication-ready. Zedboard SoC Development Board is utilized to simulate the system to validate the functionality of the work. Power optimizing techniques such as clock gating are implemented in order to further reduce

the power consumption of the developed system. Effectiveness of techniques used will be evaluated from the aspect of power consumption, delay and layout size. By reducing the power consumption of the IoT devices, this could greatly prolong the battery lifespan of the application which directly increase the possibility of the application to be commercialize as there are no such device on the market currently.

ABSTRAK

Sarung tangan penterjemah bahasa isyarat biasa menggunakan modul mikropengawal atau modul mikropemproses yang lebih tinggi dalam penggunaan kuasa akibat daripada elemen yang tidak digunakan. Oleh itu, System-on-Chip (SoC) direka menggunakan Intel 8051 harta intelek (IP) sebagai penggantian modul mikrokontroller konvensional untuk mencapai integrasi yang lebih tinggi sambil mengurangkan penggunaan kuasa. Dalam karya ini, sarung tangan penterjemah bahasa isyarat untuk komuniti kurang upaya telah dibangunkan sebagai aplikasi. Trend perubahan dalam sensor digunakan sebagai input sistem melalui Inter-Integrated Circuit (I2C). Data yang dimanipulasi akan dihantar walaupun protokol bas UART ke modul Bluetooth Low Energy (BLE). Data diterima oleh telefon pintar Android untuk membandingkan dengan pangkalan data yang disimpan di Firebase dan ia akan menghasilkan maksud isyarat tangan tersebut dengan pembesar suara dan paparan. Simulasi, pengesahan dan sintesis reka bentuk yang dicadangkan dilaksanakan dengan menggunakan alat-alat Synopsys dalam teknologi proses SilTerra 180nm untuk menghasilkan susunan akhir (GDSII) yang siap sedia untuk difabrikasi. Zedboard digunakan untuk mensimulasikan sistem untuk mengesahkan kefungsian sistem tersebut. Teknik pengoptimuman kuasa seperti “clock gating”

dilaksanakan untuk mengurangkan lagi penggunaan kuasa sistem yang dibangunkan. Keberkesanan teknik yang digunakan dinilai dari aspek penggunaan kuasa, kelewatan dan saiz litar bersepadu. Dengan mengurangkan penggunaan kuasa, ini dapat memanjangkan jangka hayat bateri aplikasi yang secara langsung meningkatkan kebolehpasaran produk tersebut kerana tidak ada peranti sedemikian di pasaran hari ini.

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LIST OF SYMBOLS AND ABBREVIATIONS

ASL	:	American Sign Language
IC	:	Integrated Circuit
IoT	:	Internet of Things
DC	:	Design Compiler
ICC	:	Integrated Circuit Compiler
VCS	:	Verification Compiler Simulator
SoC	:	System on Chip
ASIC	:	Application Specific Integrated Circuit
IP	:	Intellectual Property
RAM	:	Random Access Memory
UART	:	Universal Asynchronous Receiver Transmitter
I2C	:	Inter-Integrated Circuit
BLE	:	Bluetooth Low Energy
FPGA	:	Field Programmable Gate Array

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CHAPTER 1

INTRODUCTION

This chapter includes project background, problem statement, objectives, scope of project and chapter organization.

1.1 Project Background

It is predicted that there will be 50 Billion Internet of Things (IoT) devices by the year of 2020. As a results, power consumption of these devices must be minimized in order to cope with the energy generation trend worldwide. In this work, a smart sign language translator glove for speech impaired community has been developed as our application. The movement of hand during sign language will be modelled by finite state machine. Trend of changes in sensors which include flex sensors and gyroscope will be used as the input of the system. Generally, a sign language translator utilize conventional general purpose microcontroller and this type of control unit has a

number of disadvantages such as relatively high power consumption and larger in layout size. Thus, a System on Chip (SoC) design with Application-Specific Integrated Circuit (ASIC) is proposed to substitute conventional microcontroller technology which used in our application. Power optimizing techniques such as clock gating will be tested and implemented in order to further reduce the power consumption of the developed system. Effectiveness of technique used will be evaluated from the aspect of power consumption, time delay and layout size. By reducing the power consumption of the IoT devices, this could greatly prolonged the battery's lifespan of the application. Validation, simulation, verification and synthesis of the proposed design will be implemented using Synopsys tool in SilTerra 180nm process technology node.

1.2 Problem Statement

According to the prediction of Cisco Internet Business Solution Group (IBSG) that in the year of 2020, there would be a total number of 50 billion IoT devices connected worldwide. Assuming the power consumption of one device consume 1W of power and total of 50 billion of devices will consume a total of 50 GW. Moreover, Moore's law states that integrated circuit technology will doubled the number of transistors that could be embedded on a single chip every two years. Thus, future integrated circuit will consume higher power consumption as more number of transistors on a single IC.

Due to the fact that most of the IoT devices required high mobility, the size of power storage must be as compact as possible. Technically speaking, miniature size battery will limit the energy storage which will results in the needs of routinely replacing the power source. To cope with this hiccup, there is drastically demand of low power

consumption. System on Chip (SoC) is able to supersede general purpose microcontroller unit disadvantage in term of power consumption and layout size. In order to design and optimize a low energy consumption application based system, techniques such as clock gating needed to be verified and implemented if all the criteria ranging from power consumption to layout size are met in designing of the system.

1.3 Objective

In this work, there are four objectives that need to be achieved at the end of my research;

1. To identify the design parameters for sign language translator.

2. To design the embedded system using Verilog language for both Field Programmable Logic Array (FPGA) and Application Specific Integrated Circuit (ASIC) application.

3. To synthesize the proposed system into application-specific integrated circuit (ASIC) final layout file that is fabrication-ready.

4. To analyze the performance of the developed system in term of power consumption, timing delay and layout size compared to conventional general purpose microcontroller.