DESIGN AND OPTIMIZATION OF 22NM PMOS DEVICE WITH A BI-LAYER OXIDE

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This report is submitted in partial fulfilment of the requirements for the degree of Bachelor of Electronic Engineering with Honours

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ABSTRACT

Moore's prediction about his law has created a major roadblock for the metal-oxide-semiconductor-field-effect-transistor (MOSFET) to have high performance. Therefore, a comprehensive study of 22 nm PMOS device with a bi-layer oxide has been presented in this project. The objectives are to design and simulate a bi-layer oxide on high-k / metal gate on 22 nm PMOS device by using Silvaco software and to analyse and optimize the electrical characteristics of device by using Taguchi L9 orthogonal array method. A 22 nm PMOS device with a bi-layer oxide was designed using a Silvaco software in ATHENA module while the electrical characteristics are determined by ATLAS overlay. The results of threshold voltage ($V_{th)}$ and leakage current (I_{off}) are -0.289 V ± 12.7% and 100 nA/μm respectively must be well within the International Technology Roadmap Semiconductor (ITRS) 2012 value. Taguchi's Signal-to-Noise-Ratio (SNR) of nominal-the-best (NTB), the source/drain (S/D) implantation dose has been identified to be a dominant factor while compensation implant is an adjustable parameter for the device for V_{th}. While, by using the SNR of smaller-the-better (STB) determined the best process parameters combination for I_{off}.

ABSTRAK

Ramalan Moore mengenai undang-undangnya telah mewujudkan pelbagai masalah utama untuk logam-oksida-semikonduktor-medan-kesan-transistor (MOSFET) untuk mempunyai prestasi tinggi. Oleh itu, satu kajian terhadap peranti PMOS 22 nm dengan dual lapisan bi-oksida telah dibentangkan dalam projek ini. Objektif projek adalah merekabentuk dan mensimulasikan oksida dual lapisan pada k tinggi / get logam pada peranti PMOS 22 nm dengan menggunakan Silvaco dan mengoptimumkan ciri-ciri elektrik dengan menggunakan kaedah Taguchi L9 ortogonal. Peranti PMOS 22 nm direka menggunakan perisian Silvaco dalam modul ATHENA manakala ciri-ciri elektrik ditentukan oleh modul ATLAS. Keputusan simulasi untuk voltan ambang (V_{th}) dan kebocoran arus (I_{off}) mestilah berada dalam lingkungan nilai Pelan Tindakan Teknologi Semikonduktor Antarabangsa (ITRS) 2012 iaitu -0.289 V ± 12.7% dan 100 nA/μm. Dengan menggunakan nominal-yang-terbaik (NTB) daripada nisbah isyarat-kepada-bunyi (SNR), dos implantasi sumber/longkang (S/D) sebagai faktor yang dominan manakala dos implan pampasan sebagai laras parameter untuk peranti untuk V_{th} manakala I_{off} menggunakan kaedah kecil-lebih-baik (STB).

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LIST OF SYMBOLS AND ABBREVIATIONS

ANOVA	:	Analysis of variance
CMOS	:	Complementary metal-oxide-semiconductor
DF	:	Degree of Freedom
DIBL	:	Drain-induced-barrier lowering
FET	:	Field-effect-transistor
Hf	:	Hafnium
IC	:	Integrated circuit
I_{off}	:	Leakage current
ITRS	:	International Technology Roadmap Semiconductor
JFET	:	Junction field-effect-transistor
k	:	permittivity
MOSFET	:	Metal Oxide Semiconductor Field Effect Transistor
NTB	:	Nominal-the-Best
O_2	:	Oxide
PMOS	:	P-type MOSFET
PSG	:	Phosphosilicate Glass
SCE	:	Short-channel-effect
SNR	:	Signal-to-Noise

TiO_2	:	Titanium Dioxide
V_{gs}	:	Gate-source voltage
V_{th}	:	Threshold voltage
WSi_x	:	Tungsten Silicide
Zr	:	Zirconium

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CHAPTER 1

INTRODUCTION

1.1 Background

In 1974, the chairman emeritus of Intel, Gordon Moore has a long-term prediction under his Moore's Law. He stated that the number of transistors per square inch integrated in a chip will approximately double for every 24 months [1]. Moore's law is an observation and projection of his prediction in a semiconductor industry. For several decades, his prediction proved accurate and semiconductor industry has been using it as a guideline for research development. Therefore, in order to follow Moore's Law, researcher community are working towards getting higher integration densities at faster switching time and reduced power consumption at lower cost. Downscaling the MOSFET not only yields higher integration density but also a higher transistor

drive current for faster switching speed and lowering production cost. However, further downscaling the size of transistor has its drawbacks. It will increase short channel effects (SCE), drain induced barrier lowering (DIBL), and hot carrier effect will lead to current leakage and high power consumption [2].

1.2 About MOSFET

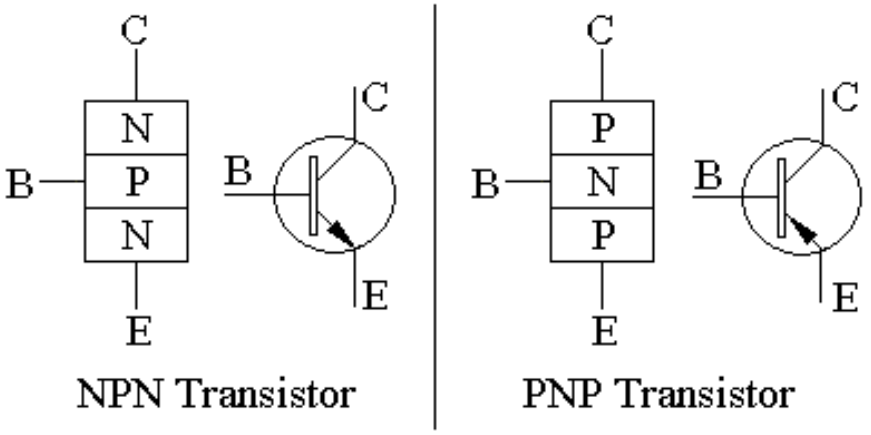

Figure 1.1 : Basic Construction of N-channel and P-channel MOSFET

Figure 1.1 [3] shows the basic construction of n-channel and p-channel MOSFET. MOSFET is a device that works electronically and digitally for amplifying and switching electronic signals. It has four terminals which include gate (G), drain (D), source (S) and body (B) in which the current that flows between the source and drain are controlled by the gate voltage. The body (B) of the device is frequently connected to the source terminal making it a three terminals device like field effect transistor. Furthermore, the device is usually fabricated under controlled oxidation of silicon. It has the insulated gate whose voltage determines the conductivity of the device. The gate is also a place for movement of current in and out of device through source and drain. The difference between MOS and FET are MOS part relates to the structure of

the transistor such as Positive-Negative-Positive (PNP) types or Negative-Positive-Negative (NPN) types while field-effect-transistor (FET) part relates on how the device operates. Figure 1.1 shows the basic construction of an N-channel and P-channel MOSFET.

The basic principle of FET was first patented by Julius Edgar Lilienfeld in 1925. The main advantage of MOSFET over any other device are it has higher input impedance and can withstand high speed operation compared to JFETs. MOSFET is the most common transistor so far and can be used in analog and digital circuits. There operates in two modes which are enhancement mode and depletion mode.

1.2.1 Enhancement Mode

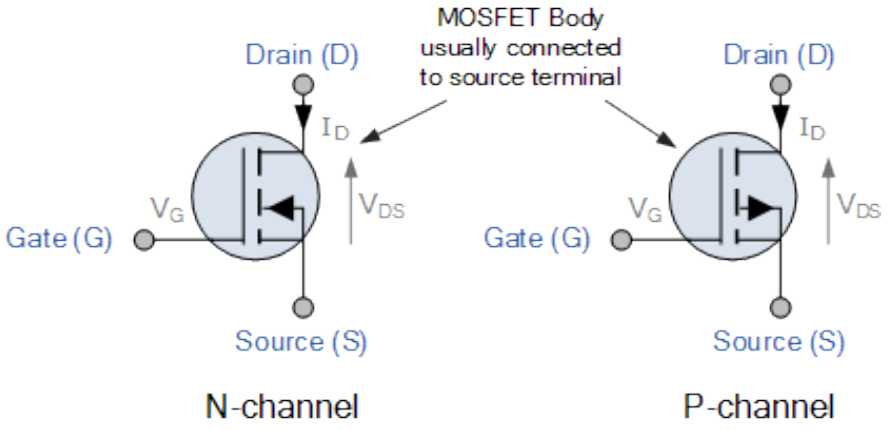

Figure 1.2 : N-channel and P-channel of enhancement mode of transistor

Figure 1.2 [3] shows the N-channel and P-channel of enhancement type of a transistor. Gate-source voltage V_{gs} is required to switched 'ON' the device and are off at zero V_{gs}. The enhancement mode MOSFET is equivalent to a 'Normally Open' switch. In n-type MOSFET, this device can be powered up by pulling the gate voltage higher than source voltage. While in p-type MOSFET, this device can be powered up by pulling the gate voltage lower than source voltage.

1.2.2 Depletion Mode

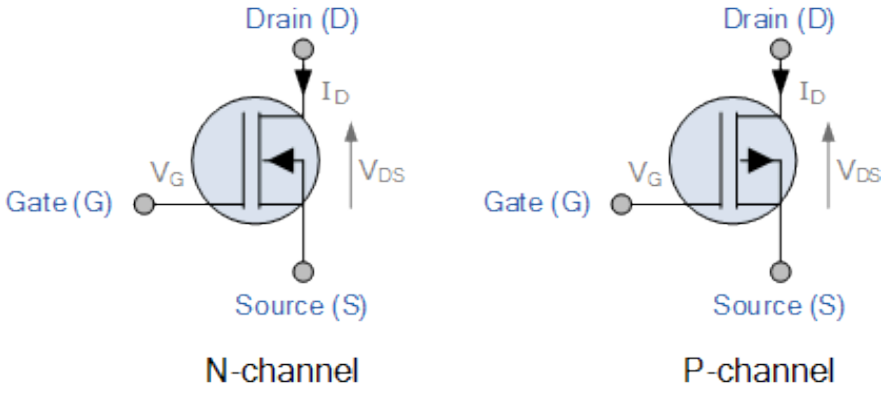

Figure 1.3 : N-channel and P-channel of depletion mode of transistor

Figure 1.3 [3] shows the N-channel and P-channel of depletion mode of a transistor. Gate-source voltage V_{gs} is required to switched 'OFF' the device. The device is usually 'ON' at gate-source voltage. Besides, this device is usually applied as load resistors in logic circuits. The depletion mode MOSFET is equivalent to a 'Normally Closed' switch. In n-type depletion -load devices, it might have -3 V threshold voltage, so it could be turned off by pulling the -3 V. While in p-type, the polarity is reversed.

1.3 Problem Statement

MOSFET devices need to have good performance with low cost and low power dissipation. Therefore, the most effective way to enhance performance and reduce cost is to scale the gate length [2]. The reduction of the size of MOSFET is commonly referred to downscaling. Scaling the thickness of the gate dielectric has long been recognized as one of the keys to improve the performance of devices. However, reducing the gate length of the transistor has a lot of challenges to research community. It has led to many major roadblocks. Some of them are SCE, DIBL and hot carrier effect which in turn led to the innovation of high-k / metal gate devices [3].

This is because the gate act as a door to the transistor where the charges built up and goes in the transistor. When gate thickness decrease, the leakage current increases. Due to the drawbacks, high-k / metal gate is introduced at the gate of the transistor to reduce leakage current.

To overcome this problem, many new high-k / metal gate dielectric materials have been recently introduced as a bi- layer oxide on the gate of the transistor. K stands for dielectric constant which shows how much charge a material can hold. In semiconductor industry, performing an actual fabrication is extremely expensive and time consuming. Therefore, the simulation technique is being one of the smartest way and favorable for researcher to get the design before setting up an actual fabrication design. This kind of research also can act as a guideline for industries before they fabricate to save cost and time.

1.4 Objectives

The main objective in this project is to add high-k / metal gate with a bi-layer oxide on 22 nm PMOS device. The sub- objectives are stated below:

i) To design and simulate a bi-layer oxide on high-k / metal gate on 22 nm PMOS device by using SILVACO software.

ii) To analyze and optimize the electrical characteristics of device by using Taguchi L9 orthogonal array method.