ANALYSE THE PERFORMANCE OF SOI MOSFET DEVICE WITH DIFFERENT GATE SPACER MATERIALS

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I hereby declare that I have read this thesis and in my opinion this thesis is sufficient in terms of scope and quality for the award of Bachelor of Electronic Engineering with Honours.

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DEDICATION

This thesis is dedicated to my beloved parents; Manin Bin Ahmad and Zaridah Binti Shuib, and siblings whom never failed to support and encourage me to do my best.

ABSTRACT

Along with the Industrial Revolution 4.0, there has been a great demand for continual miniaturization of the Bulk-Si MOSFET device as it improves the integrated circuit (IC) in both cost per production and performance. However, scaling down MOSFET degrades the performance of the device through increasing leakage current and short channel effect (SCE). Therefore, Silicon-On-Insulator (SOI) technology has been introduced to mitigate the SCE problems. This project is executed by using Silvaco TCAD software to simulate both fabrication process and electrical characteristics for the structure of SOI MOSFET that has been designed by following the International Technology Roadmap of Semiconductor (ITRS) 2013. Furthermore, this project facilitates the improvement of performance of 19nm SOI MOSFET using high-k material as the gate spacer. Through this project, the design of 19nm SOI MOSFET with BOX layer thickness of 30nm and titanium oxide (TiO2) as the gate spacer yields the highest drive current (Ion) of 548.78μA/μm and the lowest leakage current (Ioff) of 113.475pA/μm at the threshold voltage of 0.533V compared to other high-k materials as gate spacer and Bulk-Si MOSFET device.

ABSTRAK

Seiring dengan Revolusi Perindustrian 4.0, terdapat permintaan yang sangat tinggi bagi pengecilan peranti *Bulk-Si* MOSFET yang berterusan kerana ia menambahbaik litar bersepadu (IC) dari aspek kos setiap pengeluaran dan prestasi. Walau bagaimanapun, pengecilan MOSFET merendahkan prestasi peranti melalui peningkatan kebocoran arus dan kesan saluran pendek (SCE). Oleh itu, teknologi *Silicon-on-Insulator* (SOI) telah diperkenalkan untuk mengurangkan masalah SCE. Projek ini dilaksanakan dengan menggunakan perisian Silvaco TCAD untuk mensimulasikan proses fabrikasi dan ciri-ciri elektrik bagi struktur SOI MOSFET yang telah direka dengan merujuk Hala Tuju Teknologi Antarabangsa bagi Semikonduktor (ITRS) 2013. Tambahan pula, projek ini membantu peningkatan prestasi 19nm SOI MOSFET dengan menggunakan bahan *high-k* sebagai *gate spacer*. Melalui projek ini, reka bentuk 19nm SOI MOSFET dengan ketebalan lapisan BOX sebanyak 30nm dan titanium dioksida (TiO_2) sebagai *gate spacer* telah menghasilkan arus pemacu (Ion) yang tinggi iaitu 548.78μA/μm dan arus bocor (Ioff) yang rendah sebanyak 113.475pA/μm pada voltan ambang 0.533V berbanding dengan bahan *high-k* yang lain sebagai *gate spacer* dan peranti *Bulk-Si* MOSFET.

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LIST OF SYMBOLS AND ABBREVIATIONS

Al_2O_3	:	Aluminium oxide
BOX	:	Buried oxide
BPSG	:	Boron Phosphor Silicate Glass
CMOS	:	Complementary Metal Oxide Semiconductor
CVD	:	Chemical Vapor Deposition
D	:	Drain
HfO_2	:	Hafnium oxide
IC	:	Integrated circuit
I_D	:	Drain current
I_{on}	:	Drive current
I_{off}	:	Leakage current
ITRS	:	International Technology Roadmap of Semiconductor
k	:	Dielectric constant
L_G	:	Gate length
MOSFET	:	Metal Oxide Semiconductor Field Effect Transistor
PECVD	:	Plasma Enhanced Chemical vapor deposition

S	:	Source
Si_3N_4	:	Silicate nitride
SiO_2	:	Silicon dioxide
SOI	:	Silicon–on-Insulator
SS	:	Subtreshold swing
STI	:	Shallow trench isolation
TiO_2	:	Titanium oxide
V_{DS}	:	Drain-to-source voltage
V_G	:	Gate voltage
V_{GS}	:	Gate-to-source Voltage
V_{th}	:	Threshold voltage
ZrO_2	:	Zirconium oxide

CHAPTER 1

INTRODUCTION

This chapter presents the brief introductory of project background which contains objectives, problem statement, scope and the significances of this project..

1.1 Background

As technology keeps evolving, people become more dependent on electronic and digitalized devices. It is not that long ago when the embedded system and computer system in Industrial Revolution 3.0 are broadly used. Now, in the era of Industrial Revolution 4.0 and Internet-of-Things (IoT), the needs of fast and improved communications, electronic devices and systems continue to increase. Manufacturing industries demand the high speed machines, systems, managements and production while people wish to have the best electronic services and products. Thus, with the

increasing requests, evolution of transistor plays a dominant role in getting everything to the desired point [1].

Metal Oxide Semiconductor Field Effect Transistor (MOSFET) which is a type of transistor is one of the vital elements in the integrated circuit (IC). It could amplify electronic signals and act like a switch whenever it is in the conduction mode. Meanwhile, an IC or also known as a chip or microchip is an electronic device or microprocessor which thousands or millions of its functional blocks such as transistors, capacitors and resistors are all fabricated on a same piece of silicon wafer [2]. Such its functions, ICs are widely used in modern electronic devices, for instance, computers, smartphones, digital watches, calculators, robots and machines. The MOSFET is the most preferable type of transistors to be used in ICs due to its special characteristics. The MOSFET is small in size and space-saving which makes it easily fabricated on the IC, higher commutation speed, reliable to be used in digital circuits as well as consumes low power to operate thus dissipates less power loss to the surroundings.

Along with the passing years, industry has scaled down the dimension of MOSFET based on Moore's Law. As shown in Figure 1.1, the technology node becomes smaller; from microscale to nanoscale as entering the 21st century. Thus, semiconductor companies are competing to abide this prediction by reducing the gate dimension and the length of effective channel. Miniaturizing the dimension of MOSFET allows numbers of transistor to be integrated on a chip. As proofs, in year 2014, the best Intel processor available contains 1.7 billion transistors while in year 2016, Intel's has well-E CPUs contained 2.6 billion transistors and the high-end Xeon server chips are reported to have more than two billion transistors [3].

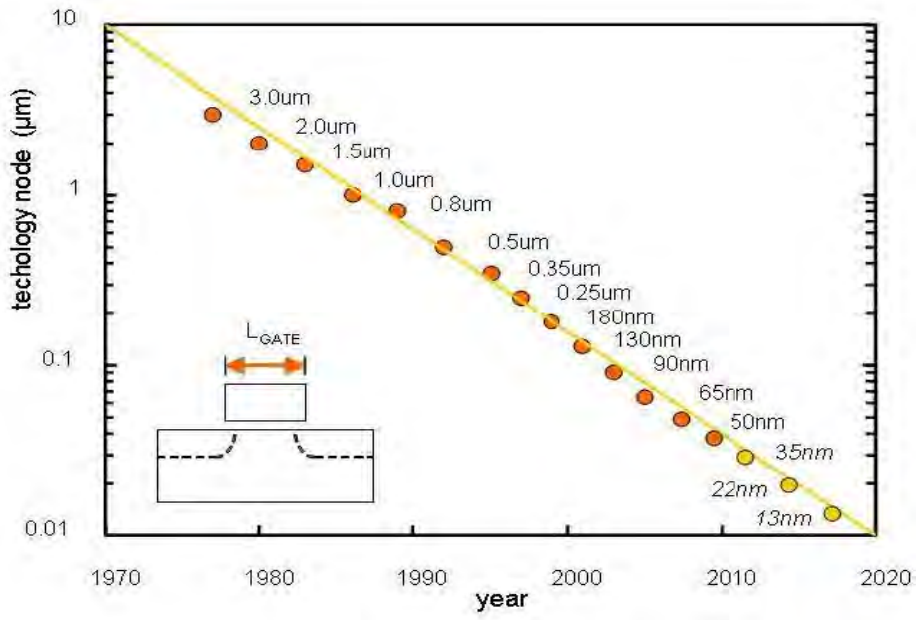

Figure 1.1: The prediction in technology node follows Moore's Law [4]

Besides, transistor scaling technology gives benefits in reducing the cost per production per single IC, increase the speed and performance, better stability of the operation and less power dissipation of the device. Raspberry Pi boards recently cost only for $5 (around RM 20.40 in Malaysia) and people got a recipe for robotics everywhere to develop small inventions through Internet of Things (IoT). Furthermore, scaling down both in price and size has led to some excellent home applications. People now can invent robot vacuum cleaners to perform human tasks at home while smartphones helps as virtual assistants and as a hub for other simpler robotic appliances.

Unfortunately, there are several challenges arise as the device becomes smaller such as performance degradation and short channel effects (SCEs) which make it difficult to continue reducing the device's size follows the conventional law [5]. When down scaling MOSFET, it is hard to maintain a nominal threshold voltage (V_{th}) as well as reduce the leakage current (I_{off}) and subthreshold swing (SS) to