Faculty of Electrical Engineering

A VOLTAGE BASED SPWM TECHNIQUE ON A NEW APPROACH FOR MULTILEVEL INVERTER

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Degree of Bachelor of Electrical Engineering (Control, Instrumentation and Automation)

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DECLARATION

I declare that this report entitle "A Voltage Based SPWM Technique on a New Approach for Multilevel Inverter" is the result of my own research except as cited in the references. The report has not been accepted for any degree and is not concurrently submitted in candidature of any other degree.

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Supervisor's Name: DR. AZRITA BINTI ALIAS

Date : .....

DEDICATION

To my beloved parents,

for their enduring love, motivation and support

ACKNOWLEDGEMENT

I wish to express my deepest appreciation to various people for their contribution in completing this project. A special gratitue I would like to give to Dr. Azrita bt. Alias, my research supervisor, for her contribution in stimulating ideas and assisting the research. Also, her critiques, support, encouragement and patient guidance throughout this project.

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Finally, I wish to thank my parents for their love, support, encouragement and patience throughout my study.

ABSTRACT

Inverters are power electronic converters converting the several levels of direct current (DC) voltages into alternating current (AC) voltages required for loads. Multilevel inverters are the inverters with voltage level three or more. Recently, industries have begun to demand higher power equipment. Therefore, multilevel inverters started to gain popularity among industries since they are able to deal with higher voltage levels. There are few advantages of multilevel inverter: it produces nearly sinusoidal waveform, decreases the harmonic distortion, thus decreases the losses, can deal with high power ratings equipment, and needs a smaller filter to smooth the graph. Besides that, the system's complexity is also reduced and it became lighter and cheaper. This paper aims to investigate on SPWM switching strategy of 5- level cascaded hybrid multilevel inverter (CHMI) needed to develop a new sinusoidal pulse width modulating (SPWM) switching strategy for CHMI. This paper also aims to investigate on output voltage total harmonic distortion of conventional inverter and five- level inverter. In this paper, there will be a new switching strategy for a 5- level CHMI. The model of a 5-level CHMI will be simulated using MATLAB Simulink. The output of the simulation will be analysed.

ABSTRAK

Inverter adalah penukar kuasa elektrik yang menukarkan arus terus (DC) ke arus ulang-alik (AC) yang diperlukan untuk beban elektrik. Inverter Voltan Bertingkat adalah inverter dengan tiga atau lebih tingkat voltan keluaran. Baru-baru ini, industri telah mula memerlukan peralatan kuasa yang lebih tinggi. Oleh itu, Inverter Voltan Bertingkat mula mendapat populariti di kalangan industri kerana mereka mampu menangani voltan yang lebih tinggi. Terdapat beberapa kelebihan Inverter Voltan Bertingkat iaitu ia menghasilkan bentuk voltan keluaran berbentuk sinusoidal, mengurangkan harmonik, sekali gus mengurangkan kehilangan tenaga, boleh berurusan dengan peralatan berkuasa tinggi, dan memerlukan penapis yang lebih kecil untuk melicinkan bentuk voltan keluaran. Selain itu, kerumitan sistem juga dikurangkan dan ia menjadi lebih ringan dan lebih murah. Kertas kerja ini bertujuan untuk mengkaji strategi pensuisan SPWM untuk Inverter Voltan Bertingkat Lima. Kertas ini juga bertujuan untuk menganalisi voltan output, jumlah harmonik inverter konvensional dan tahap lima inverter. Dalam kertas ini, akan ada satu strategi pensuisan baru untuk tahap 5- CHMI. Model 5-tahap CHMI akan disimulasikan menggunakan MATLAB Simulink. Output simulasi akan dianalisis.

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LIST OF TERMINOLOGIES

AC	-	Alternating current
DC	-	Direct Current
PWM	-	Pulse width modulation
SPWM	-	Sinusoidal pulse width modulation
CHMI	-	Cascaded H- bridge multilevel inverter
VSI	-	Voltage source inverter
CSI	-	Current source inverter
MVSI	-	Multilevel voltage source inverter
THD	-	Total harmonic distortion
SDLC	-	System Development Life Cycle
PH Disposition	-	In phase
PO Disposition	-	In phase above zero, opposite phase below zero
APO Disposition	-	Alternatively in opposite phase

CHAPTER 1

INTRODUCTION

1.1 Project Background

The renewable energy resources are gaining industries more attention, since the shortage of fossil fuels and greenhouse effect crisis are worrying nowadays[1]. The demand for renewable energy sources such as solar, wind and hydro energy is one of the reasons of the fast development in power converters research. In most of the renewable resources power systems, an inverter system is needed for renewable energy conversion from DC (renewable resources) to AC for commercial use.

Inverters are power electronic converters that convert DC to AC. The inverters can be categorized into voltage source inverter (VSI) and current source inverter (CSI). In renewable resources systems, VSI is more suitable compared to CSI[2]. This is due to a VSI is fed by a fixed DC voltage and its components needed is lesser than of a CSI. Besides that, the output of a CSI has higher harmonics. A power system with a higher harmonics has the tendency to create additional switching losses. Therefore, to eliminate the harmonics, additional filters must be added at the input and the output sides.

There are conventional inverters and multilevel inverters. The conventional inverter output voltage waveform is the bipolar square wave with two levels of voltage which are the input voltage, V_{DC} and $-V_{DC}$. The multilevel inverter's output voltage waveform is a staircase-liked waveform with higher than two output voltage levels.

The most common way to control the output voltage of multilevel voltage source inverter (MVSI) is to implement sinusoidal pulse-width modulation (SPWM) switching strategies. The SPWM control is operating based on the concept of comparison of a modulating signal with triangular carrier waveforms.

Although the complexity of the SPWM switching circuits of multilevel inverter is higher than of conventional inverter, but there are many advantages of using MVSI for electric power system. It produces lower output harmonic compared to conventional inverters. Besides, it also puts less stress on the switching devices thus reduces switching losses.

1.2 Motivation

There are many pros of using multilevel inverters. The most important advantage is that multilevel inverters can reduce output total harmonic distortion (THD) which leads to switching losses reducing. The higher the number of output voltage levels, the smaller the THD. The power supplied can be used to perform other useful task.

Besides, the multilevel inverter can produce high output voltages with low harmonics. The arrangement of the power switches in the topology accumulates these multiple dc sources in order to achieve higher voltage at the output.

The comparison between conventional and multilevel inverter is shown in Table 1.1 below. The main difference that distinct multilevel inverter from conventional inverter is that it produces output with lower total harmonic distortion. This will lead to lower switching stresses in the inverter circuit and thus lower switching losses. Besides, output voltage of multilevel inverter is higher since the output voltage of it is equal to the summation of each H- Bridge cell's output voltage. Multilevel inverters have more than two output voltage levels while conventional inverters have two voltage levels. For multilevel inverters, they need lower switching frequency compared to the conventional inverters to produce the desired output waveform. Therefore, the switching losses are lower than that of the conventional inverter. The power supply can be used to perform other useful task.

Since there are many advantages of multilevel inverters, a topology of multilevel inverter will be simulated and analysed in this paper.

Table 1.1: Comparisons between conventional inverters and multilevel inverters

Comparison	Conventional inverter	Multilevel inverter
THD	Higher	Lower
Switching stress	Higher switching stresses	Reduced switching stresses
Output Voltage	Higher	Lower
Voltage levels	Two levels	Higher than two levels
Switching frequency	Needs higher switching frequency thus it has high switching losses	Needs lower switching frequency thus it has lower switching losses

1.3 Problem Statement

As the renewable energy resources are gaining people's concern nowadays, sunlight is treated as one of the important resources to generate electricity. Inverters are needed to convert sunlight which is direct current (DC) to alternating current (AC) which can be connected to power grid for domestic use. As the trend requiring higher power output and less total harmonic distortion, inverters are not able to cope with the requirement. Therefore, multilevel inverters are needed. The higher the level of multilevel inverters, the better the performance of the inverters since it produces nearly sinusoidal waveform [3]. However, the existing switching strategies for inverters can be a burdensome since it is quite complicated. Therefore, the proposed work shall include the new switching strategy which has a lower complexity compared to the existing switching strategies.

1.4 Objective

There are four objectives in this paper.

First, this project aims to investigate on types of inverter and to simulate it using MATLAB Simulink.

Second, the objective of this project is to simplify the switching strategy for multilevel inverter.

Third, this project aims to implement a voltage based SPWM technique for 5- Level Cascaded H- Bridge Multilevel Inverter.

Fourth, this project aims to analyse the multilevel inverter performance in terms of total harmonic distortion (THD) and the power factor.

1.5 Scope

The scopes of this project are:

1. This project will focus on the single phase 5- level cascaded H- bridge multilevel voltage source inverter.

2. The input DC voltage for the inverter is 60V; the peak voltage of the output sine waveform is 120V before adding filtering circuit.

3. A voltage based SPWM technique is implemented using modified PID controller.

4. This project will analyse the total harmonic distortion and power factor at the end.

CHAPTER 2

LITERATURE REVIEW

2.1 Introduction

Inverters are power electronic converters that convert direct current (DC) source into alternating current (AC) output. Since trend of industrials nowadays require higher output power, thus multilevel inverters are introduced. There are several types of multilevel inverters which are implemented by several techniques.

In this chapter, types of multilevel inverters and Pulse Width Modulation (PWM) techniques will be discussed.

2.2 Topologies of Multilevel Inverter

There are three common topologies of multilevel inverter which are:

i. Cascaded H- Bridge
ii. Flying Capacitors
iii. Diode- clamped

Thongprasri (2011) had tabulated the numbers of components needed by different types of multilevel inverters as in Table 2.1 below. Cascaded H-bridge inverter is the topology that requires least number of components.

Table 2.1: Components of Single Phase Multilevel Inverters[4]

Types of multilevel inverter	No. of switches	No. of diodes	No. of capacitors
Cascaded H- bridge	8	-	-
Flying capacitors	8	-	10
Diode- clamped	8	12	4

2.2.1 Cascaded H- Bridge

Cascaded H- Bridge Multilevel Inverter is popular topologies among all multilevel and multi- pulse inverters. This is due to the structures of H- bridges in a multilevel inverter are identical and it enables the H- bridge to be modularized, manufactured and packaged easily [5]. Low switching frequency and the ability to be modularized are the advantages of cascaded H-bridge inverter. There are some cons when using Cascaded H- Bridge topology too. When the output voltage level increases, the switches and dc sources have to be increased, which leads to increasing cost and weight of the circuit[6]. The levels of output voltages can be increased by two levels by cascading an H- bridge module to the existing one. The number of output voltage levels can be calculated using the formula, 2m+1; where m is the number of cells as shown in Figure 2.1. The idea of this inverter is connecting H-bridge inverters serially to get a sinusoidal output voltage. The output voltage can be calculated by summing the voltage produced by each H- Bridge. It needs fewer components compared to diode-clamped and flying capacitors type multilevel inverters.

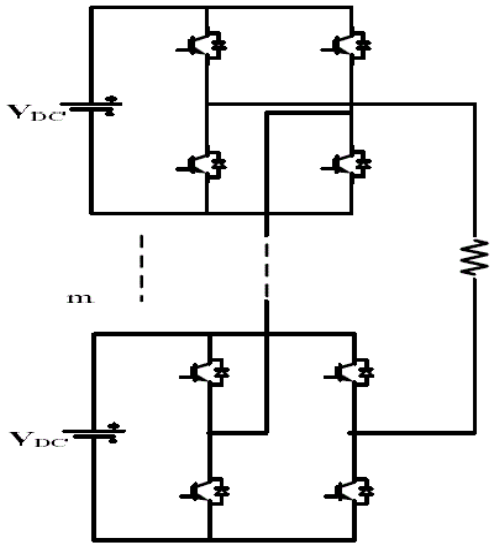

Figure 2.1: Cascaded H- Bridge Inverter Topology

2.2.2 Diode- Clamped

The Diode- Clamped Multilevel Inverter topology was proposed in 1981. This topology as shown in Figure 2.2 is also known as neutral point inverters and it is designed for low frequency applications [7]. The number of components needed in this topology depends on the number of output voltage levels desired. (n-1) voltage source, 2(n-1) switching device and [(n-1) (n-2)] diodes are needed for n level inverter; given n is the number of output voltage levels as stated by Varsha and Shraddha (2013). This inverter's idea is by using diodes, it limits bus voltage to reach the require steps in the output [8]. The advantage of using diode- clamped topology is that all phases using the common bus for its application in three phases. The disadvantage of using this topology is the difficulty faced in real power flow. This is due to the imbalanced capacitors and it made this topology less popular in industries.

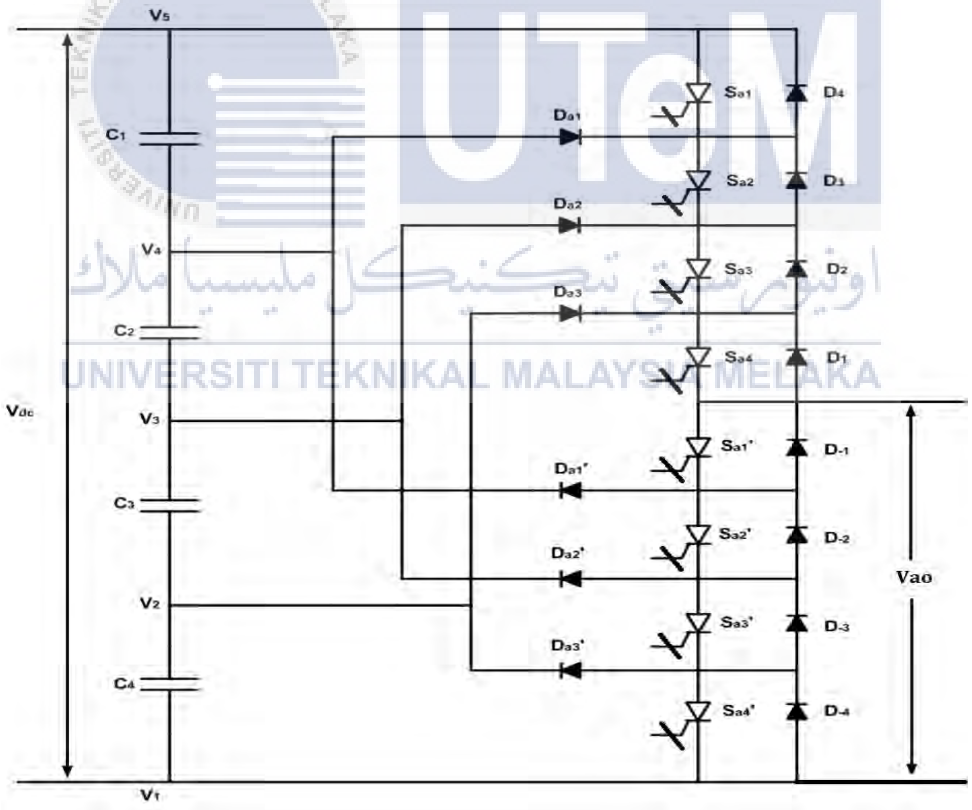

Figure 2.2: Diode- Clamped 5- Level Inverter Topology[7]

2.2.3 Flying Capacitors Clamped Multilevel Inverter

Flying Capacitors Clamped was proposed by Maynard and Foch in 1992 [9]. As stated by Ahmed (2014), the topologies of Flying Capacitors Clamped and Diode Clamped Multilevel Inverter are almost the same except that capacitors are used in Flying Capacitors Clamped topology and diodes are used in Diode Clamped topology. This topology needs the largest number of capacitors compared to Cascaded H- Bridge and Diode Clamped topologies to limit the output voltage to a certain level. Practically, this topology can produces only six levels output voltage although theoretically it can gives infinite levels. The arrangement of capacitors, switches and diodes is shown in Figure 2.3.

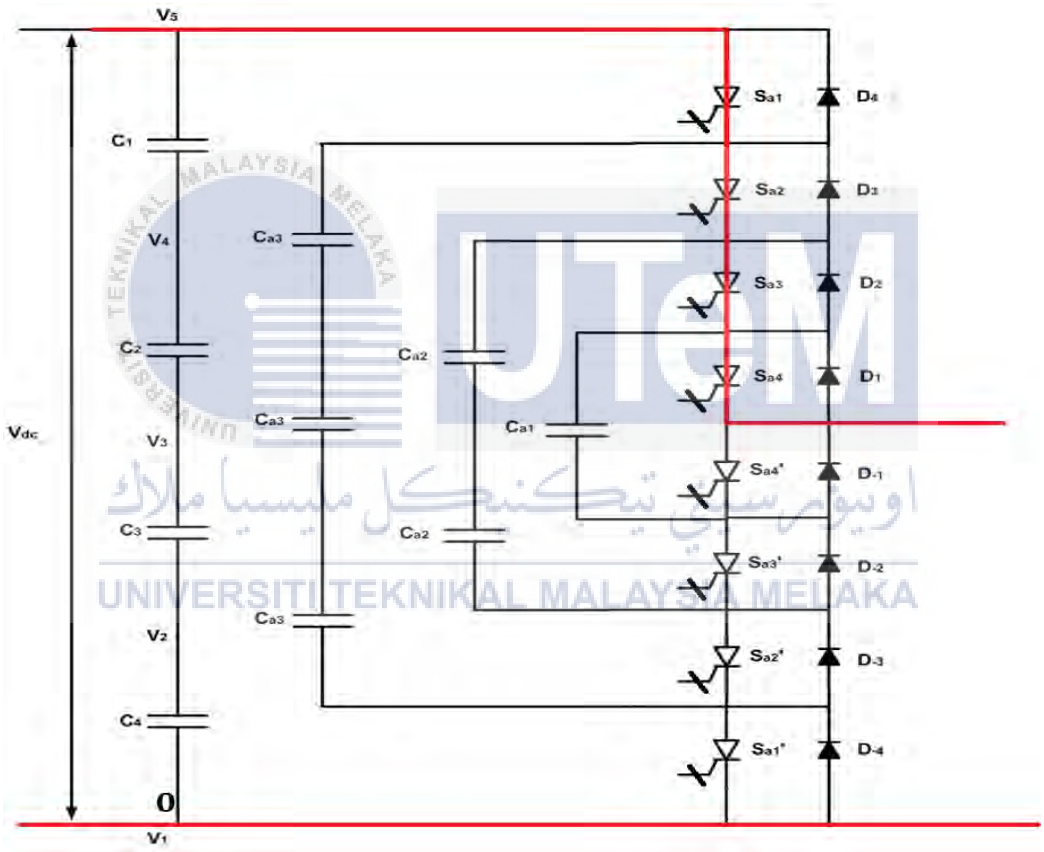

Figure 2.3: Flying Capacitors Clamped 5- Level Inverter Topology

2.3 Sinusoidal Pulse width modulation (SPWM)

Sinusoidal pulse width modulation (SPWM) is a switching method that gives alternating output voltage and current waveforms in an inverter circuit. It uses switching pulse to turn on and off the switches to perform this function. SPWM method is used to reduce the total distortion (THD). To generate the SPWM signal, two signals are compared,

a lower frequency modulating sine-wave signal and the higher frequency carrier triangular signal. A simple voltage based inverter is shown in Figure 2.4.

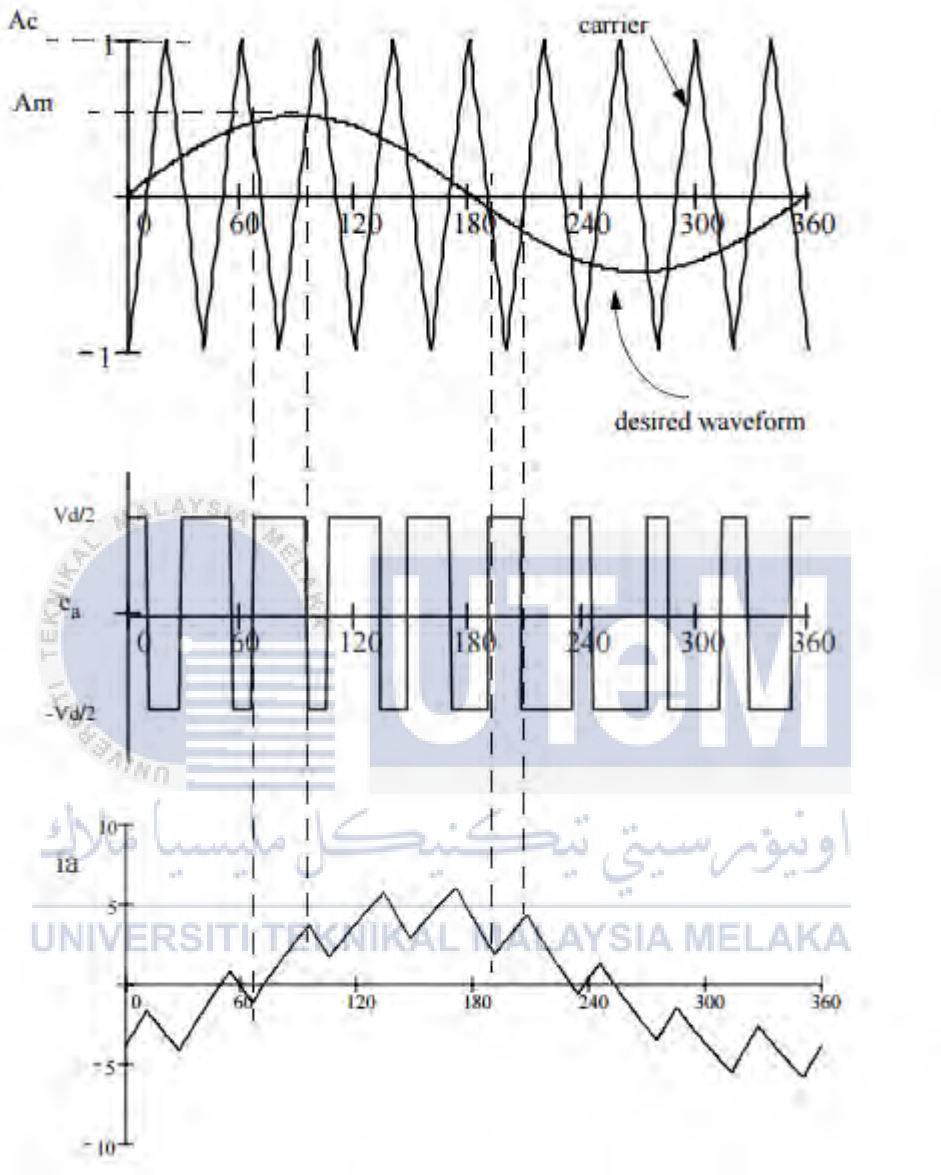

Figure 2.4: Principle of PWM

2.3.1 Sinusoidal Pulse Width Modulation for Multilevel Inverter

The difference between two level SPWM and SPWM for multilevel inverter is the number of carriers used. According to Aspalli and Wamanrao (2009), for 'm' level inverter, 'm-1' carriers are used [6]; m represents the number of output voltage level. In the most common implementation, comparison between the modulating signal and carrier signal is

used to generate the desired output voltage. In certain condition, the switch will be switched ON or OFF depending on whether positive or negative dc bus voltage is applied at the output. In phase disposition where the carriers are shifted vertically as shown in Figure 2.5, all four carriers are at the same frequency, phase and amplitude. The comparison between the reference signal and the four carrier signals is performed.

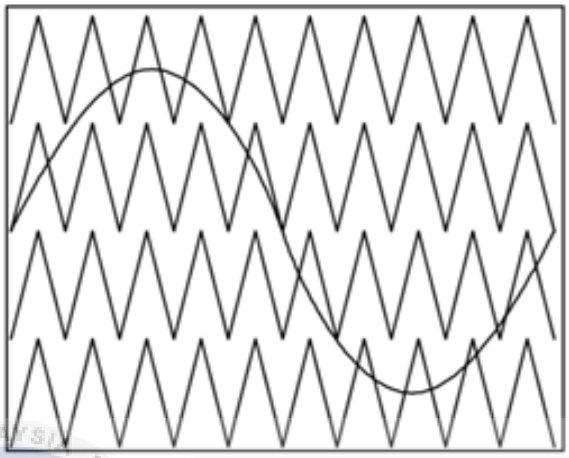

Figure 2.5: Carriers which are shifted vertically [6].

2.4 PID Controller

PID controller is a controller that get output value by reading a sensor, then control the output actuator to produce desired output by computing proportional, integral, and derivative responses. Figure 2.6 shows the position of a PID controller in a control system; while Figure 2.7 shows the block diagrams inside a PID controller.

In PID controller, there are three main components which are Proportional (P), Integral (I) and Derivative (D). The P component in PID controller multiply the error signal by the Proportional gain (K_p), I component is the sum of all the instantaneous error signal and D component functions as a future- predicting component. D component does the control action by calculating the future measured value and projecting the current measured value. However, D component will affect the output where it will cause noises. Therefore, the Derivative gain (K_D) must not be too large.

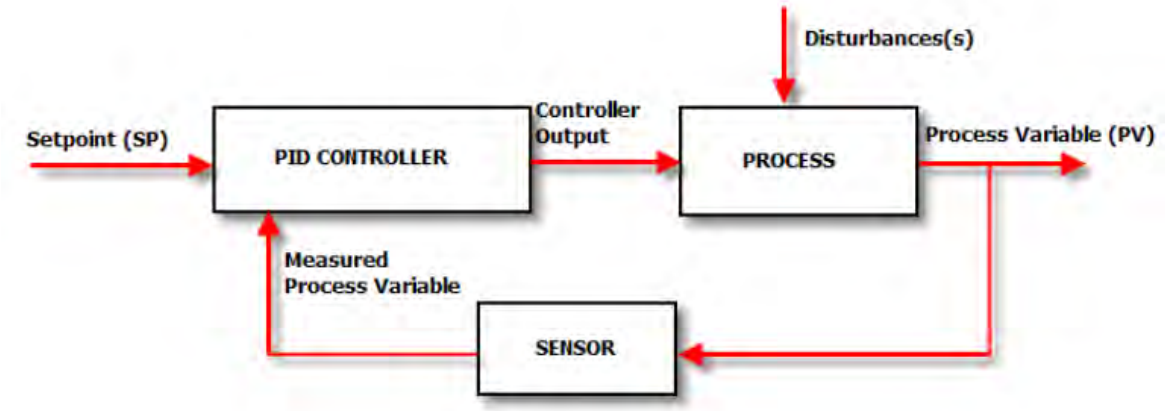

Figure 2.6: A PID controller in a control system

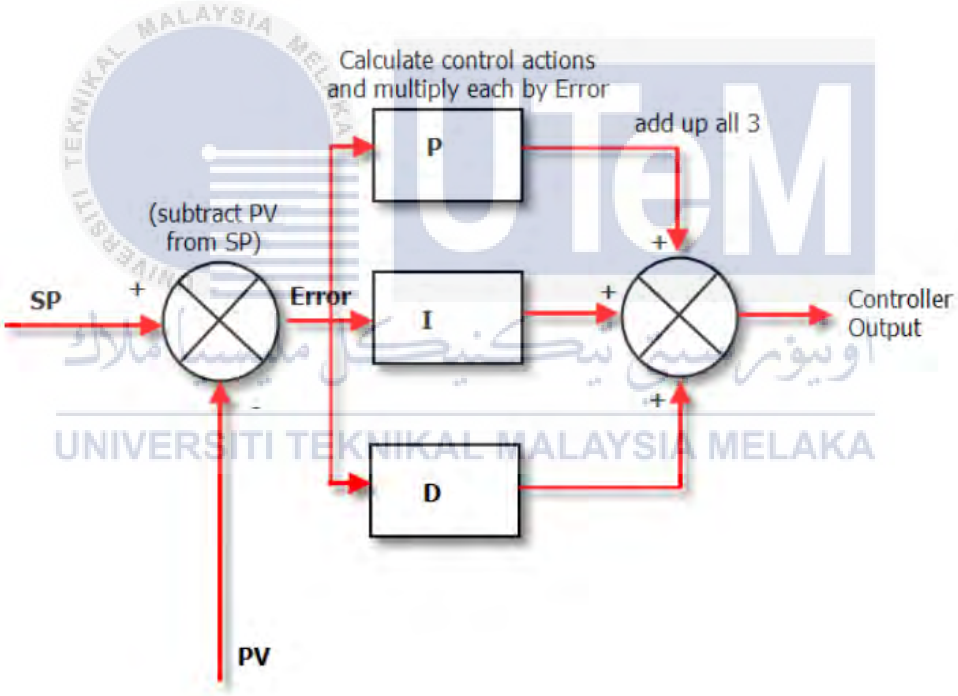

Figure 2.7: Components of PID Controller

2.5 Summary

There are three topologies of multilevel inverter which are cascaded H- Bridge, diode- clamped and flying capacitors are discussed in this chapter. From few aspects, it can be concluded that the most proper topology is H- Bridge cascaded topology. Referring to

Table 2.1, this topology requires least number of components for the same number of output voltage levels. Furthermore, in the industry application, this topology is the most suitable topology since it is in modular form. Troubleshooting works will be easier if any fault occurred in the circuit. Sinusoidal Pulse Width Modulation (SPWM) method is chosen in this project since it can reduce switching losses.

In a conclusion, SPWM has been implemented to control signals for the IGBTs in the H-bridge cascaded multilevel inverter circuits in this project.

CHAPTER 3

METHODOLOGY

3.1 Introduction

Details explanation of methodology of this project will be discussed under this chapter. In the first section, procedures of this project are discussed. In the second section, the principle of operation of SPWM signals is discussed.

The results of this project is has been obtained based on the methodology discussed. The project mainly focuses on analysing the total harmonic distortion (THD) and output voltage of a multilevel inverter topology. Therefore, simulation using MATLAB will be conducted to complete the analysis part.

This project started by researching on the related information such as types of multilevel inverter and control signal for multilevel inverter. Then, the harmonics behaviour was analysed by using MATLAB.

3.2 General Procedures for this Project

Methodologies generated from journals are used to achieve the objectives of this project. The methodology of System Development Life Cycle (SDLC), generally three major steps, which are planning, implementing and analysis, is one of the methods in this project.

As shown in Figure 3.1, the project starts with the planning phase. Second, all the related data are collected and analysed. Then, a system or a procedure will be designed followed by implementation of the system. The planning phase includes data collection and software specifications. All the data are collected through related journals and articles. The analysis phase includes analyse the performance of multilevel inverter and identify the

improvement need to be done. The design phase includes designing the topology and switching to meet the specifications. Implementation phase includes implement the project and testing the project. After implementing the project, analysis on the system performance is done again. If the performance of the system meets the requirement, the system can proceed to maintenance and support phase. If the performance of the system does not meet the requirement, the system needs to undergo planning phase again.

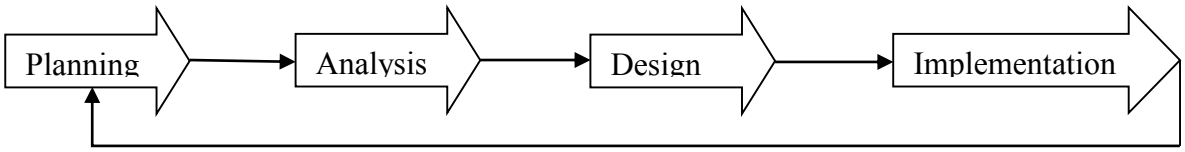

Figure 3.1: The SDLC

3.3 Project in Brief

According to Figure 3.2, the project can be summarized by four steps. First, SPWM which is used as the triggering pulses for the IGBTs is designed for the five- level CHMI. Second, SPWM is implemented into five- level CHMI inverter using MATLAB Simulink. Third, the output voltage and current are obtained through MATLAB Simulink. Finally, harmonics of the output voltage will be analysed.

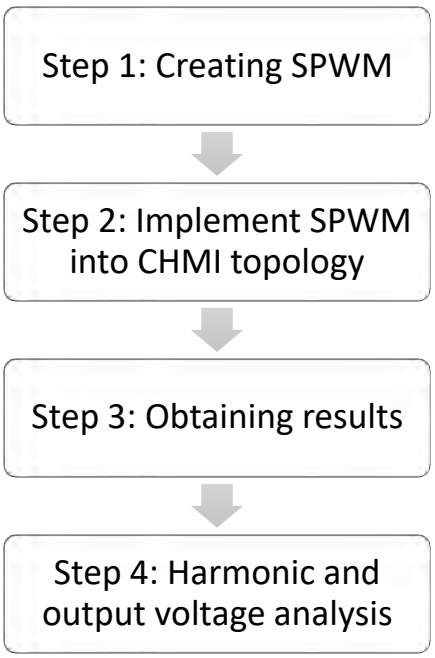

Figure 3.2: Project Summary

3.4 Design specification of Sinusoidal Pulse Width Modulation (SPWM)

The SPWM in this project was designed using the following specification:

i. The switching frequency of the SPWM signal is 20 kHz;
ii. The frequency of reference signal is 50Hz.

3.5 Sinusoidal Pulse Width Modulation (SPWM)

The switches in the multilevel inverter will either be switched ON or OFF to control the flow of power in the multilevel converter. Phase shifting technique is used in SPWM to reduce the harmonics.

Vertically shifted SPWM scheme comes with three variant: [6]

i. In phase carriers signals (PH disposition)
ii. In phase carries above the zero, but in opposite phase with those below zero (PO disposition)
iii. Alternatively in opposite phase carriers (APO disposition)

The scheme used in this project is PH disposition as shown in Figure 3.3. The scheme that produces least harmonic is the PH disposition scheme since it puts harmonic energy directly into a common mode carrier component. For five- level multilevel inverter, four carriers (V_{c1}

– V_{c4}) signals are needed. It divides the whole modulating voltage into four regions as shown in Figure 3.3. For five level multilevel inverter as shown in Figure 3.3, the region are a = 1, 0,-1, -2. Region a=1 signals are used to control switch S7 and complementary signals are used to control S8, region a = 0 signals are used to control switch S5 and complementary signals are used to control S6. While signal from region a = -1 are used to control switch S3 and complementary signals are used to control S4, signals from region a = -2 are uses to control switch S1 and complementary signals are used to control switch S2. The gate pulses produced as the result from the comparison between the reference signal and four carrier signals are presented in Figure 3.4 and 3.5. Figure 3.4 shows the gate pulses for S1, S2, S3 and S4 while Figure 3.5 shows the gate pulses for S5, S6, S7 and S8.

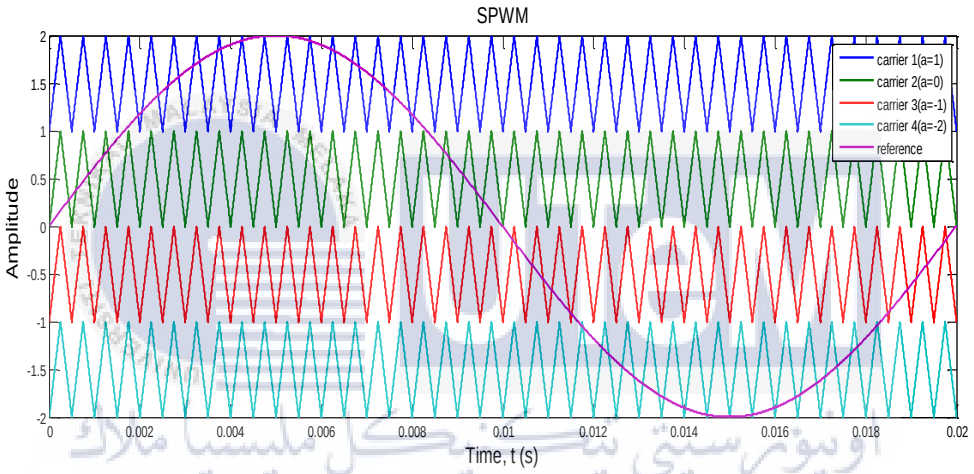

Figure 3.3: SPWM for 5 level multilevel inverter for one cycle

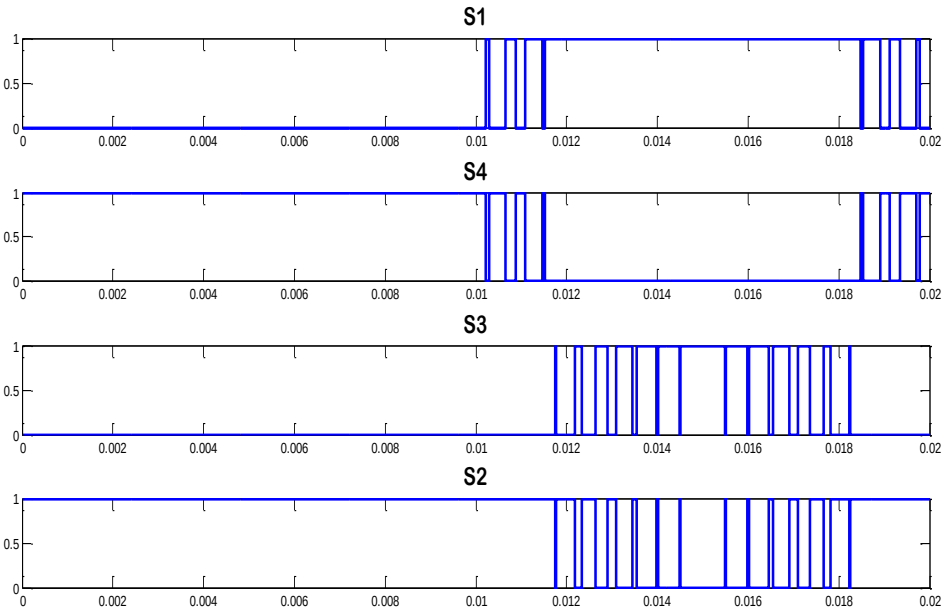

Figure 3.4: Gate signals for triggering five- level CHMI S1, S2, S3 and S4

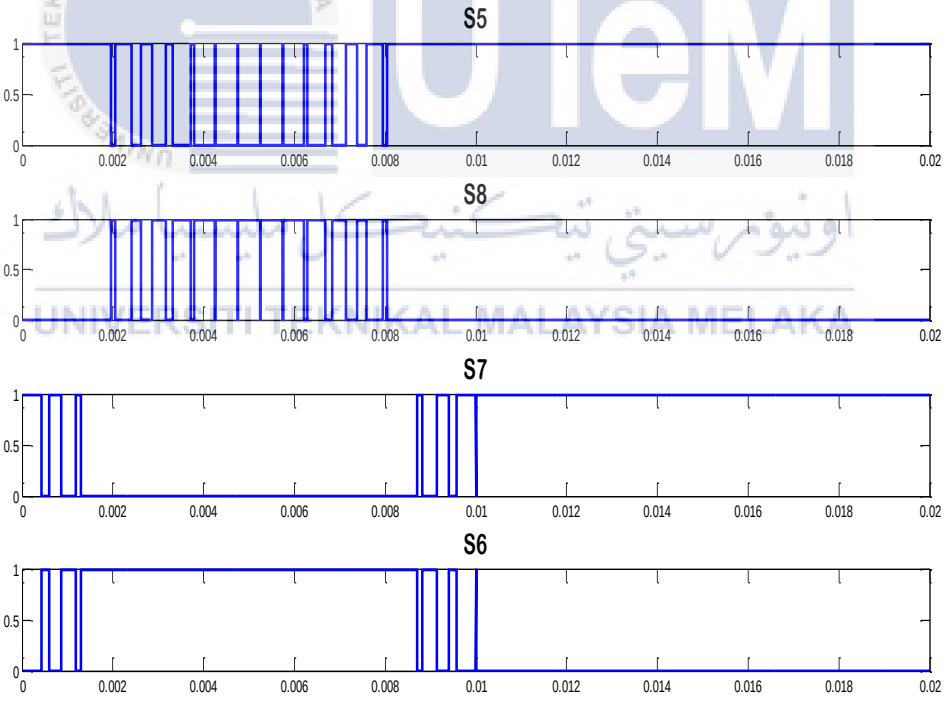

Figure 3.5: Gate signals for triggering 5- level CHMI S5, S6, S7 and S8

3.6 Principle of Operation of Cascaded H-bridge Multilevel Inverter (CHMI)

Figure 3.6 shows a five level cascaded H-bridge multilevel inverter. The converter consists of two H-bridge cells in series, which are connected to two voltage sources. The output waveform shows the sum of both the H- Bridge cells output. Assuming the first cell output voltage as V_1; second cell output voltage as V_2, the multilevel inverter output voltage is the summation of V_1 and V_2 which can be summarized by the equation below:

$$V_o = V_1 + V_2 \tag{3.1}$$

There are five level of output voltage which is V_1, V_2, V_3, $-V_2$ and $-V_3$ where V_1=0V, V_2=60V and V_3=120V. The relation of switching states for each switches and the output voltage is shown in Table 3.1. The output voltage for the first H- Bridge, V_1 is $+V_{DC}$ when S_1 and S_4 are closed or $-V_{DC}$ when S_2 and S_3 are closed. Then the output voltage of second H- Bridge, V_2 is $+V_{DC}$ when S_5 and S_8 are closed or $-V_{DC}$ when S_6 and S_7 are closed. Since the H- Bridge is connected in series, therefore the inverter output voltage is equal to the summation of V_1 and V_2.

Figure 3.7 shows the Simulink model for five- level CHMI. As shown in the figure, there are two H- Bridges which are being cascaded. The structure of first H- Bridge is shown in Figure 3.8 while the structure of the second H- Bridge is shown in Figure 3.9.

Table 3.1: The switching states of five- level CHMI multilevel inverter.

Output Voltage, V (V)	**S1**	**S2**	**S3**	**S4**	**S5**	**S6**	**S7**	**S8**
V_1	0	0	0	0	0	0	0	0
V_2	1	0	0	1	0	0	0	0
V_3	1	0	0	1	1	0	0	1
$-V_2$	0	1	1	0	0	0	0	0
$-V_3$	0	1	1	0	0	1	1	0

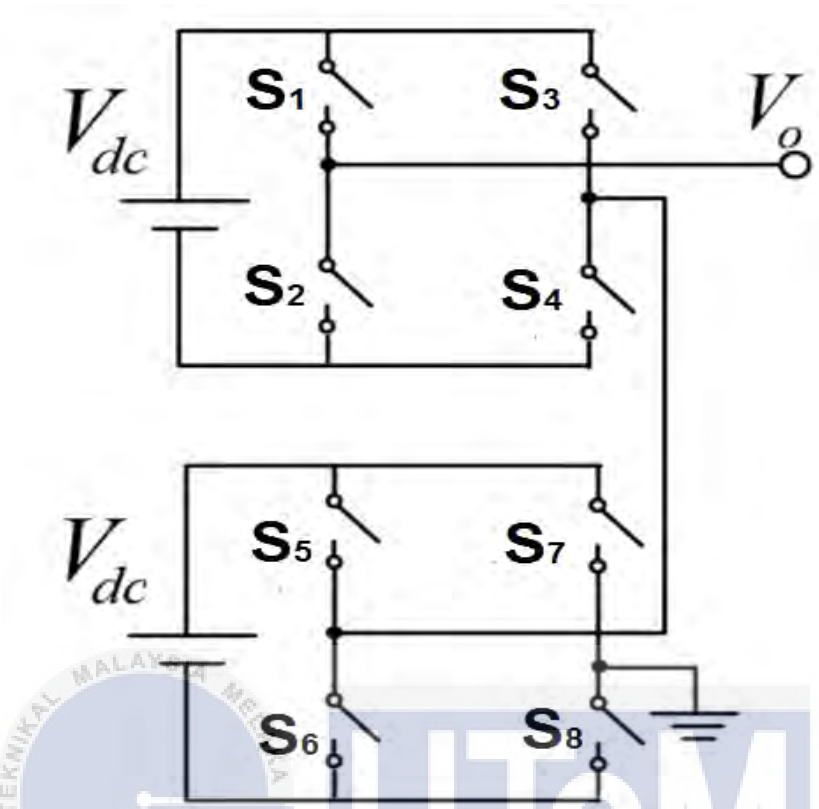

Figure 3.6: Five level cascaded H-bridge multilevel inverter.

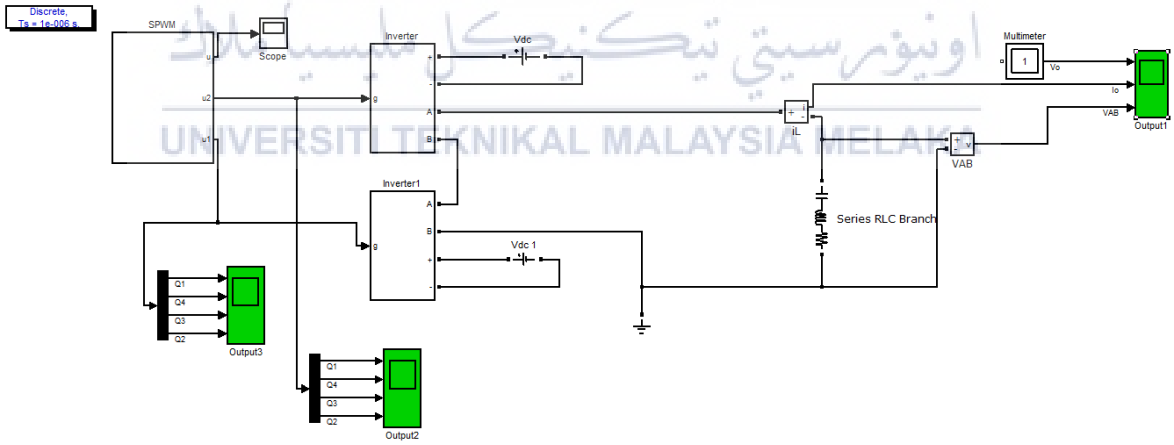

Figure 3.7: Simulink model for five- level CHMI

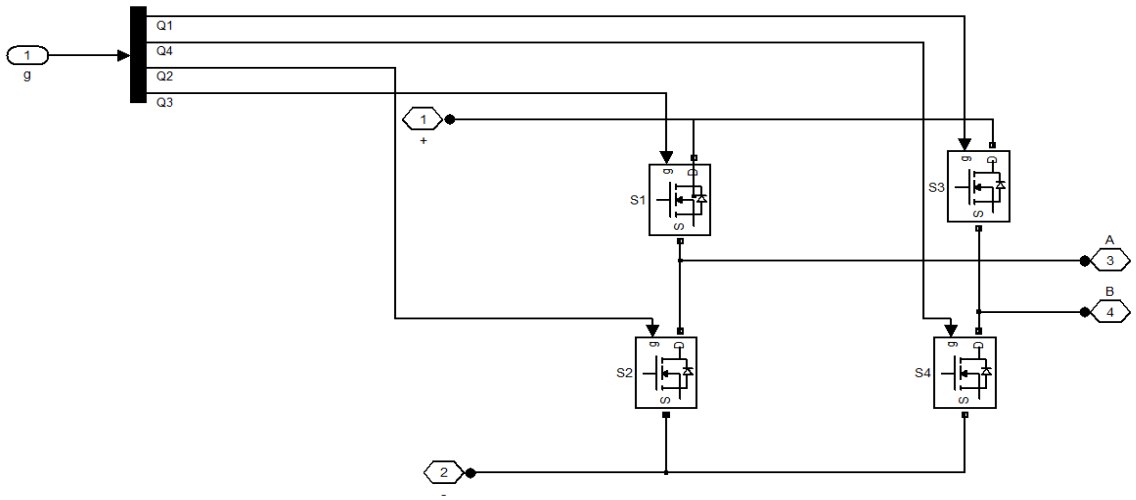

Figure 3.8: First H- Bridge circuit for five- level CHMI

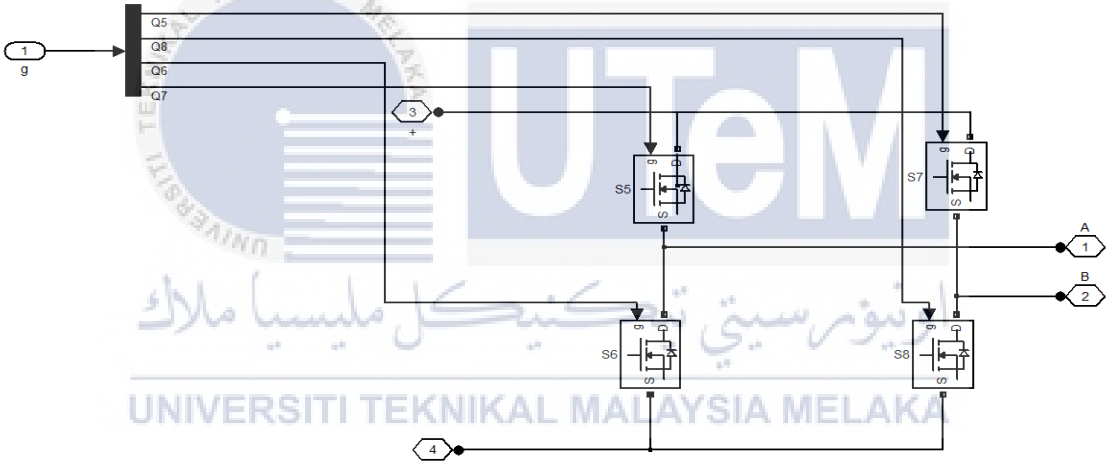

Figure 3.9: Second H- Bridge circuit for five- level CHMI

3.7 The Proposed Switching Strategy for 5- Level CHMI

A new switching scheme for a 5- level CHMI will be proposed. Unlike the other schemes, only one triangular carrier signal is used for a 5- level CHMI in this scheme. The proposed switching strategy is implemented on a Five- Level CHMI as shown in Figure 3.8, 3.9 and 3.11. The output voltage of each module is connected in series, the output voltage of the CHMI is equal to the sum of output voltage of each module. The number of output voltage levels, N can be calculated using the formula:

$$N= 2M+1 \quad (3.2)$$

where M is equal to the number of cells. The proposed switching strategy is based on the SPWM switching technique. This switching strategy compares a reference sinusoidal signal with a single triangular carrier signal as shown in Figure 3.10. The reference signal is vertically shifted by -1V, +1V and 2V. The reference signal frequency, f_m is 50 Hz; while the carrier signal, f_c is 20 kHz. The amplitude of reference signal, A_m can be calculated by using the formula:

$$A_m = 4M_a A_c \quad (3.3)$$

Equations (3.2) and (3.3) define the ratio of number of output voltage levels, N to the number of cells, M and the modulation. The switching pattern for the five- level CHMI is shown in Figure 3.12.

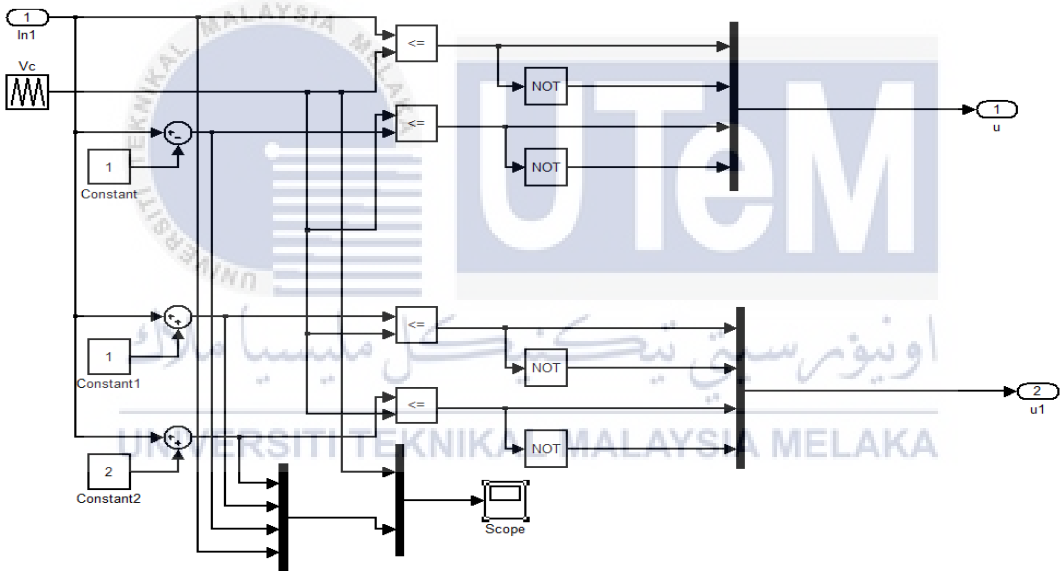

Figure 3.10: The MATLAB Simulink circuit for the new switching scheme

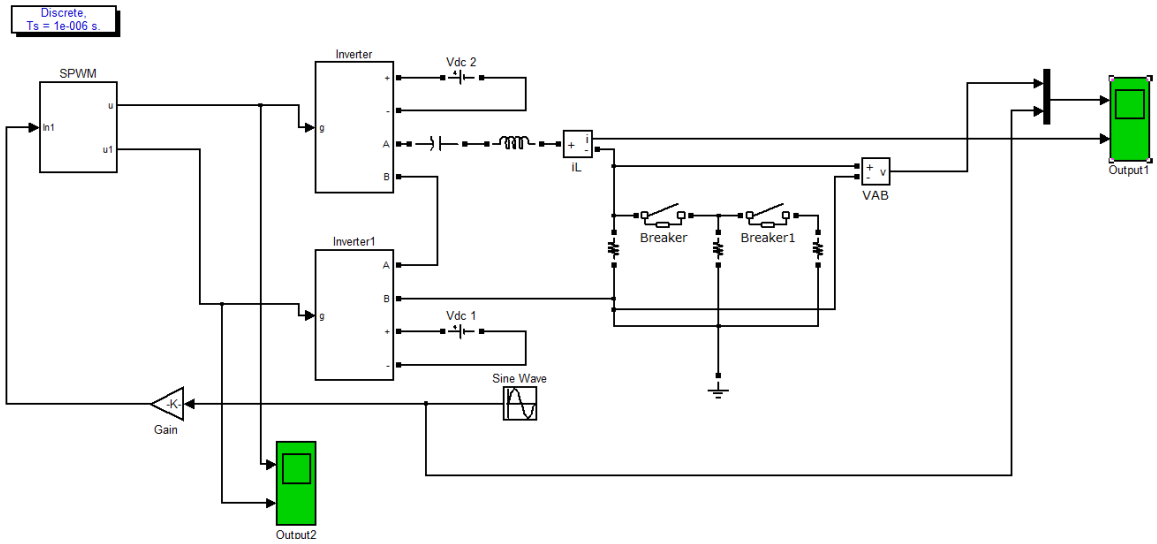

Figure 3.11: The Five- Level CHMI circuit in MATLAB Simulink

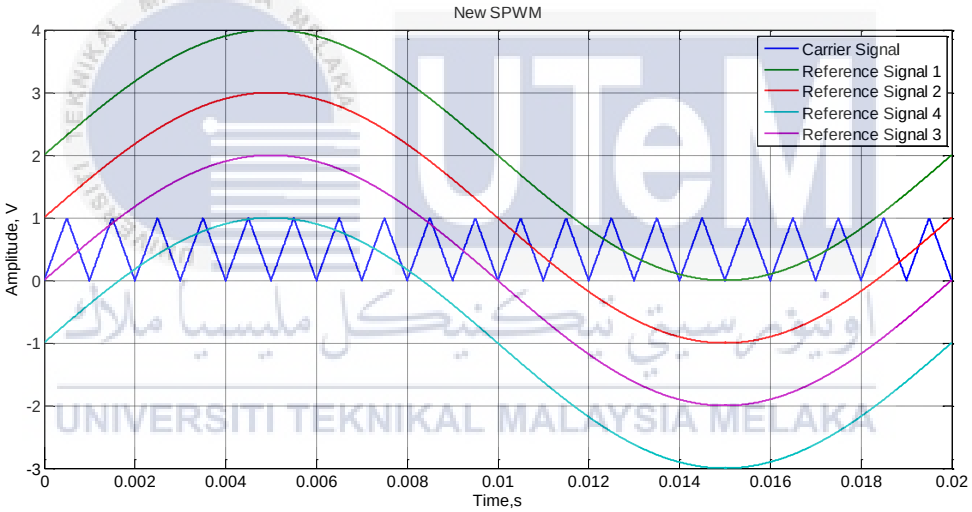

Figure 3.12: The modified sinusoidal reference signals and a single triangular carrier signal.

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3.8 Closed Loop Five- Level Cascaded H- Bridge Multilevel Inverter (CHMI)

Closed-loop control system is a control system where the quantity of the output being measured has no effect on the input of the control process. It uses open loop system as its forward path and one or more feedback loops between the output quantity and reference input. It corrects the output of the system according to the error signal with the aid of controller.

One of the most common controller is PID controller. PID controller is a controller that get output value by reading a sensor, then control the output actuator to produce desired output by computing proportional, integral, and derivative responses. However, there are limitations of PID controller due to its fixed structure and there are only three tuning parameters. Besides, the derivative gain, K_D of conventional PID controller may saturate the system. Therefore, modified PID controller is used in this 5- level CHMI switching pulse to improve the performance of the inverter. The main function of modified PID Controller in this system is to regulate the switching to obtain a desired output voltage. The output voltage can be affected by changes in load. Switching pulses play an important roles in output voltage. When the load is changed, it can be clearly seen that the output voltage will be affected.

A modified PID controller had also been proposed and was tested for the 5- Level CHMI using the new switching strategy. Figure 3.13, 3.14 and 3.15 show the block diagram of the modified PID controller in the system. Figure 3.16 shows the position of the controller in the system. The proportional gain (K_P), derivative gain (K_D) and T_d is tuned by using root locus technique. K_P used in this controller is set as 1600 where it has been found that the system is stable when K_P is between 0 and 2434. K_D is set to around ten times of T_d which is 0.002. The value of T_d is set to 0.00003 where $\frac{-1}{T_D}$ the location of the zero is, the zero must be far to the left in s- plane since the effect of the zero on the system can be ignored.

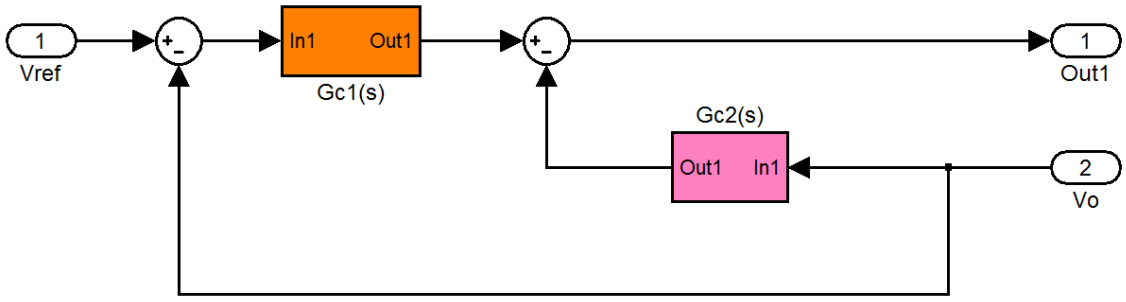

Figure 3.13: Block diagram of the modified PID controller

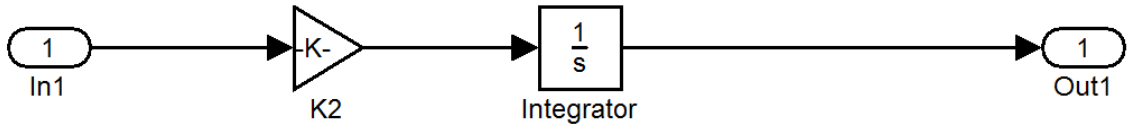

Figure 3.14: The proportional integral compensator, $G_{c1}(s)$ block diagram

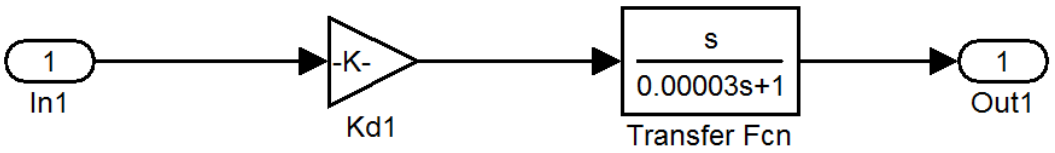

Figure 3.15: The derivative compensator, $G_{c2}(s)$ block diagram

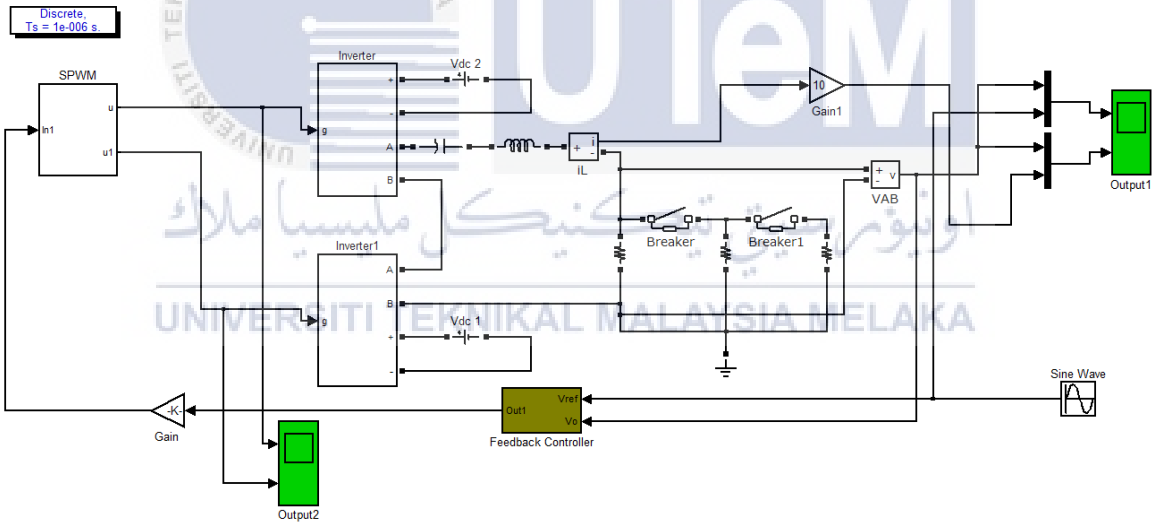

Figure 3.16: 5- Level CHMI with modified PID controller

CHAPTER 4

RESULTS

4.1 Introduction

In conventional SPWM method of modulation for five- level CHMI four carriers and one reference sinusoidal signal are used. Arrangements of these carriers are using the scheme PH disposition (all carriers are in phase). Figure 4.1 shows how the conventional SPWM switching signals are produced by comparing four carrier triangular signals and one reference sinusoidal signal.

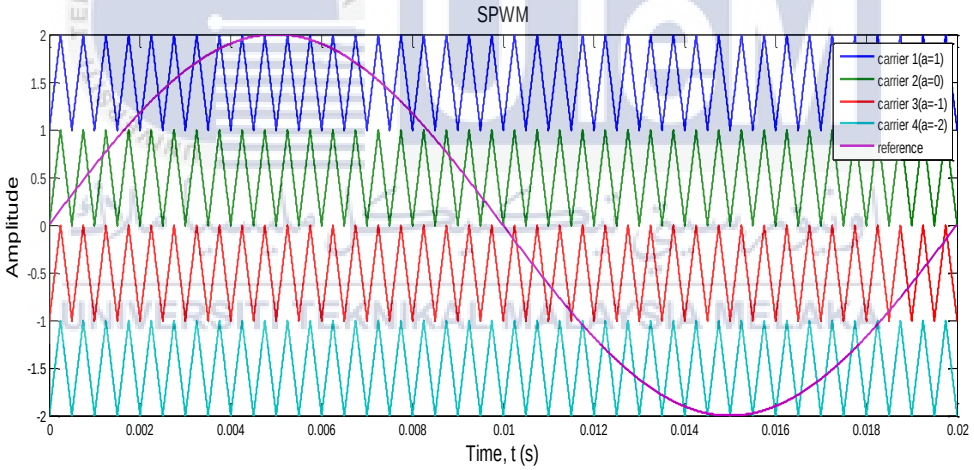

Figure 4.1: SPWM for 5 level multilevel inverter (one cycle)

In the newly proposed switching strategy for five- level CHMI, only one triangular carrier, V_c and one sinusoidal reference, V_r signals are used. The original reference signal, V_{r1} is shifted positively by two units along y- axis to form V_{r2}; shifted positively by a unit along y- axis to form V_{r3}; and shifted negatively by a unit along y- axis to form V_{r4}. Figure 4.2 shows how the SPWM switching signals are produced by comparing one triangular carrier signal and one sinusoidal reference signal. The reference signals can be represented as below:

$$V_{r_2} = V_{r_1} + 2 \quad (4.1)$$

$$V_{r_3} = V_{r_1} + 1 \quad (4.2)$$

$$V_{r_4} = V_{r_1} - 1 \quad (4.3)$$

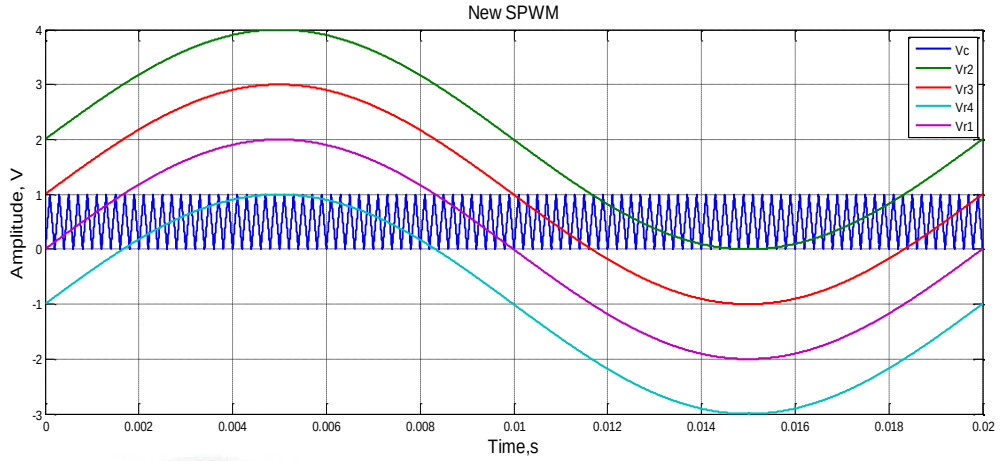

Figure 4.2: The new switching strategy for five- level CHMI (one cycle)

4.2 Simulation Results

Simulation provides accurate description of the real hardware output and it will be done before constructing the hardware. In real world implementation, human error is common and one of the way to reduce the bad impact is by performing software simulation. One of the positive impact of using software simulation is the cost required to build the hardware prototype will be reduced.

In this section, both the schemes will be simulated using MATLAB Simulink. This simulation process is done to validate the proposed switching strategy of the five- level cascaded H- Bridge multilevel inverter.

There are three main parts in simulation results which are simulations of: Two- Level Inverter, Five- Level Inverter and Five Level Inverter using the newly proposed switching strategy.

4.2.1 Two- Level Inverter

A two-level inverter produces two output voltage levels. The input DC voltage, V_{dc} is equal to 60V. The inverter produces 60V and -60V as the output voltages. The advantage of the inverter is the complexity of the circuitry is low. But, usually the inverter is not used due to output of it is difficult to be smoothen as AC output.

4.2.1.1 Two- Level Inverter without Low Pass RL Filter

Figure 4.3 shows the output voltage for Two- Level Inverter. As shown in Figure 4.3, it can be seen that there are two output voltage levels which are 60V and -60V. Figure 4.4 shows the load current where the maximum current is 6A and minimum current is -6A. To make the waveform more to sinusoidal waveform, low pass RL filter is used.

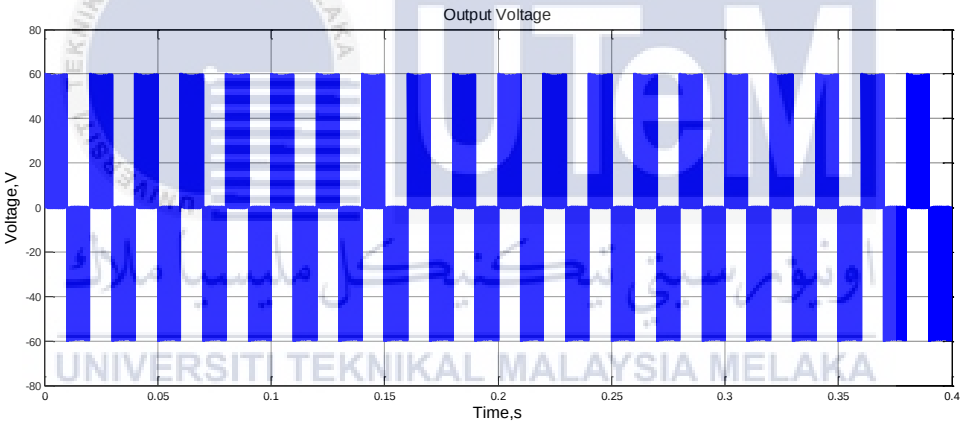

Figure 4.3: The output voltage for conventional inverter

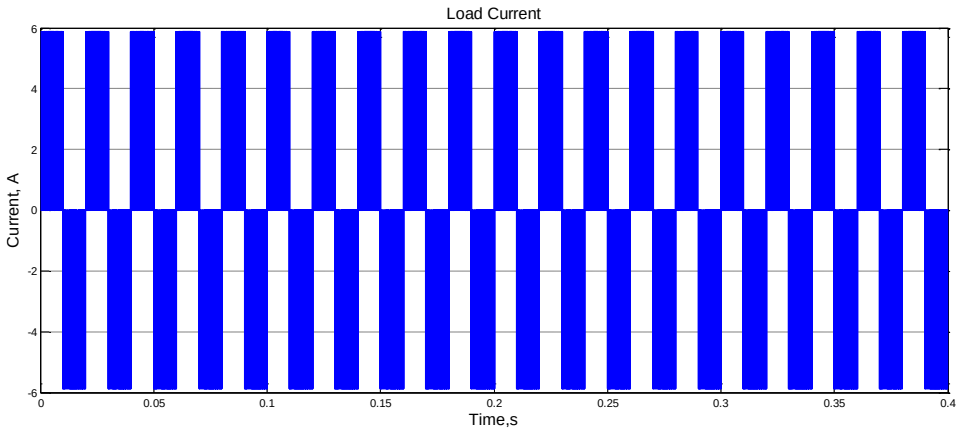

Figure 4.4: The load current for conventional inverter

4.2.1.2 Two- Level Inverter with Low Pass RL Filter

With the aid of the filter, the high frequency signals can be filtered and a more sinusoidal waveform will be obtained. An inductor, L=3000μH is added in series with DC input and the load is added in parallel with DC input. The output voltage waveform of the inverter when modulation index, M=0.8 is shown in Figure 4.5. The maximum output voltage when M=0.8 is 47V. Figure 4.6 shows the total harmonic distortion of it is 7.51%. The output voltage waveform of the inverter when modulation index, M=1.0 is shown in Figure 4.7. The maximum output voltage is 60V when M=0.8. Figure 4.8 shows the total harmonic distortion of it is 7.28%. From the results, we can deduced a relationship between modulation index, output voltage and total harmonic distortion. It can concluded that the reduction of M leads to decrease of output voltage and increase of THD.

Figure 4.9 shows the output voltage and load current versus simulation time. It can be observed that the output voltage and load current is nearly in phase. Power factor can be defined as the ratio of real power to the apparent power of a system. It can also be calculated using the formula below:

$$Power\ factor, PF = \cos \Theta; \tag{4.4}$$

where Θ is the phase difference between voltage and current. It can be clearly seen that the output voltage is nearly in phase with the load current. Therefore, it is assumed that Θ=0˚. PF= cos 0˚=1 which means unity power factor. Unity power factor is what industries longed for since a load with a lower power factor draws larger current than a load with a high power factor. The higher currents increase the energy lost and reduce the efficiency of a system.

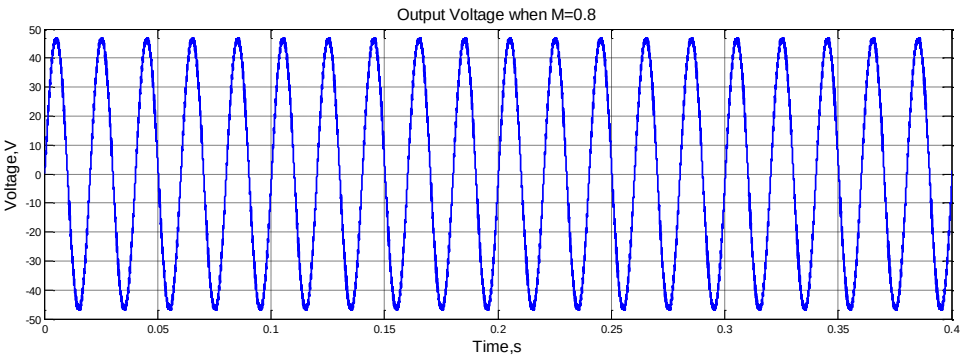

Figure 4.5: The output voltage of Two- Level inverter when M=0.8

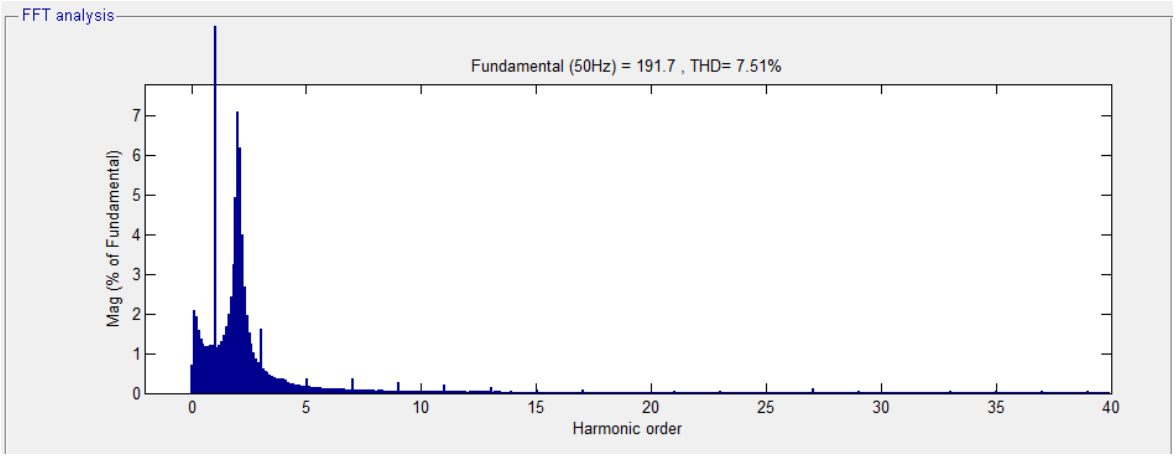

Figure 4.6: The total harmonic distortion of Two- Level inverter when M=0.8

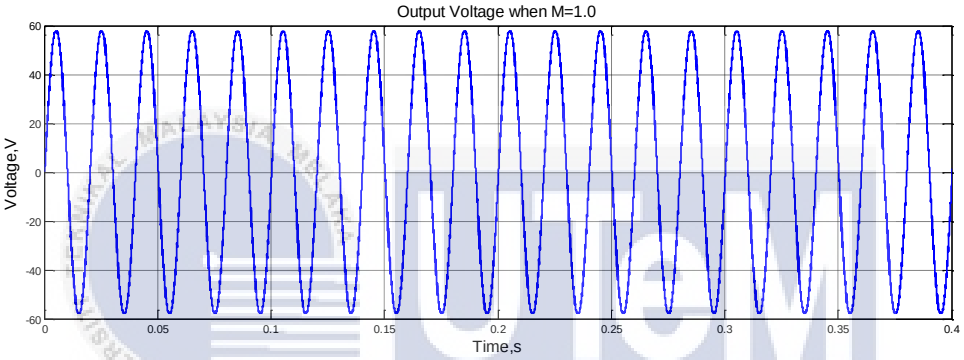

Figure 4.7: Output Voltage of Two- Level inverter when M=1.0

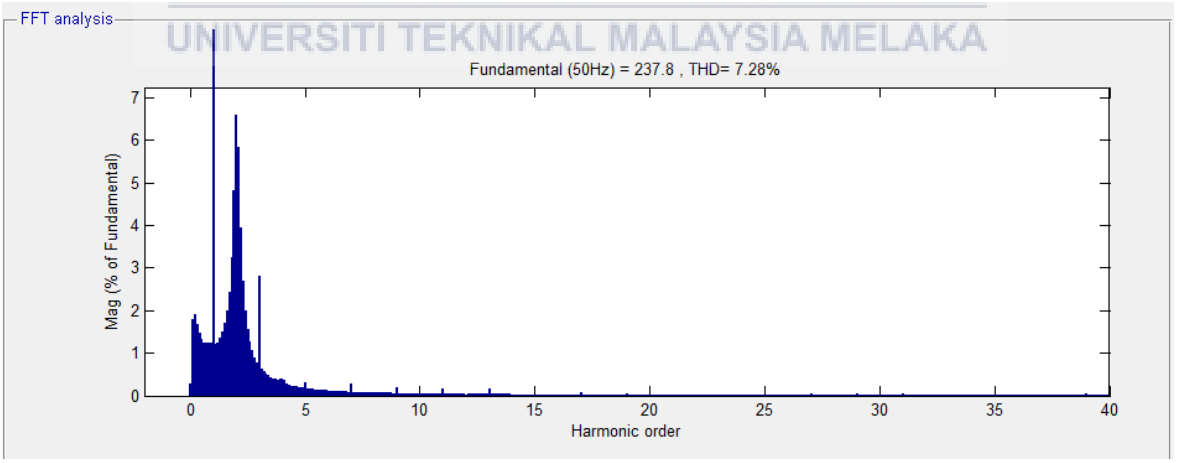

Figure 4.8: The total harmonic distortion of Two- Level inverter when M=1.0

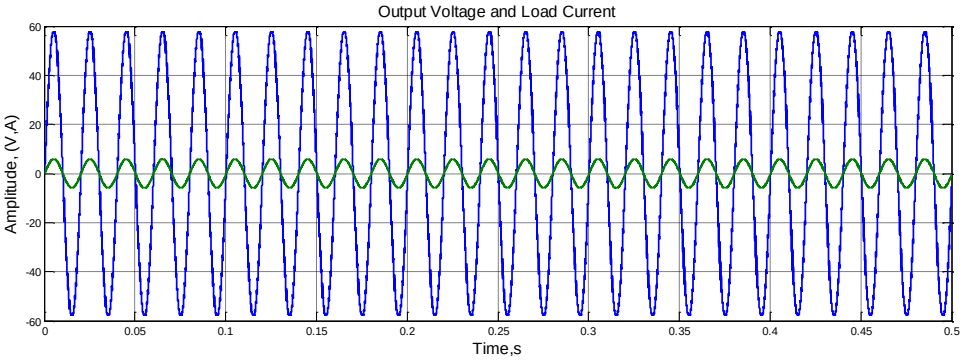

Figure 4.9: The output voltage and load current of Two- Level inverter

4.2.2 Five- Level Cascaded H- Bridge Multilevel Inverter (CHMI)

The topology used is Cascaded H- Bridge Multilevel Inverter (CHMI). The resulting SPWM switching is shown in Figure 4.11 and 4.12. In 5- level CHMI, two cascaded cells with eight switches were used, therefore eight signals were needed to trigger the switches. By referring to Figure 3.6 in chapter 3, switches S1 and S2 should operate at the same time for the first half of the cycle while S3 and S4 should operate in the next half at the same operation time. For the second cell of CHMI, the same method of triggering was used.

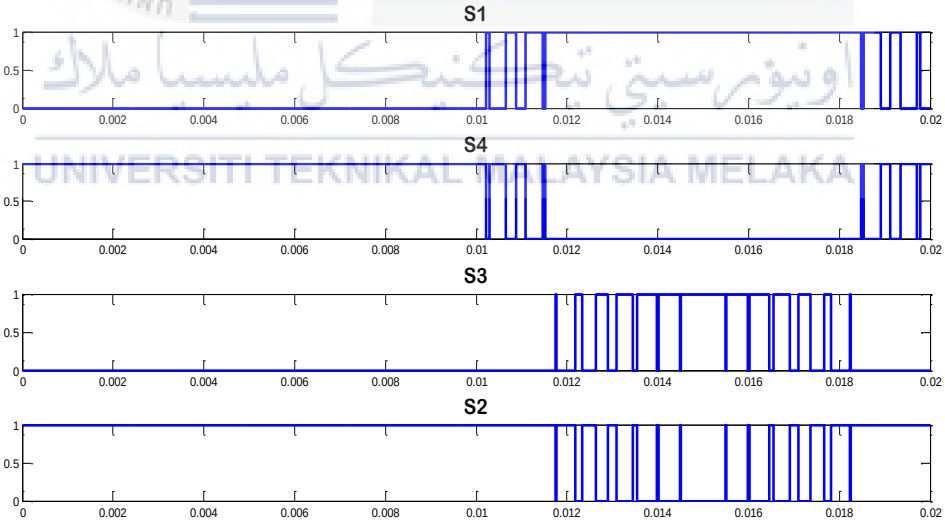

Figure 4.10: SPWM for 5- Level CHMI S1-S4

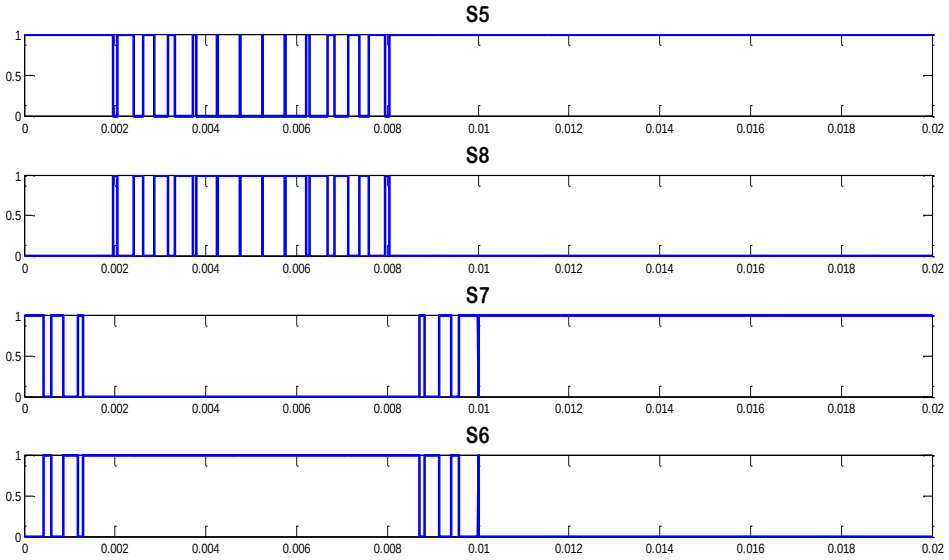

Figure 4.11: SPWM for 5- Level CHMI S5-S8

4.2.2.1 Five- Level CHMI without Low Pass RL Filter

Figure 4.13 shows the output voltage for five- level Cascaded H- Bridge Multilevel Inverter. As shown in Figure 4.13, it can be seen that there are five output voltage levels which are V_1, V_2, V_3, $-V_2$ and $-V_3$; where V_1= 0V, V_2= 60V, and V_3= 120V. To make the waveform more to sinusoidal waveform, low pass RL filter is used. Figure 4.14 shows the load current of the 5- level CHMI before low pass RL filter is used.

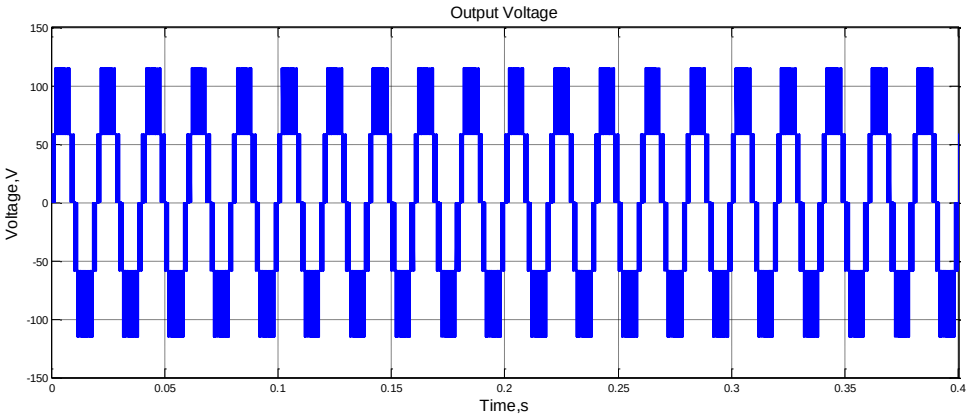

Figure 4.12: Output Voltage for 5- level CHMI

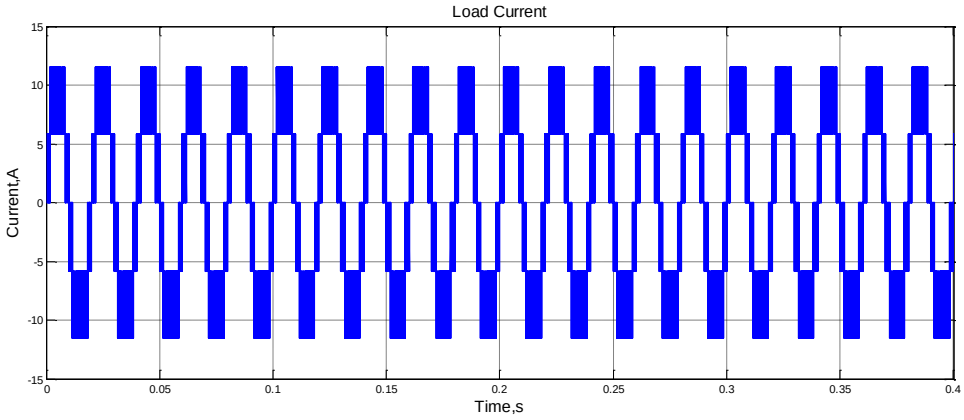

Figure 4.13: The load current for 5- Level CHMI

4.2.2.2 Five- Level CHMI with Low Pass RL Filter

With the aid of the filter, the high frequency signals can be filtered and a more sinusoidal waveform will be obtained. An inductor, L=3000μH is added in series with DC input and the load is added in parallel with DC input. The output voltage shows maximum value of 80V when modulation index, M=0.8. The output voltage is shown in Figure 4.14. Figure 4.15 shows the total harmonic distortion (THD) when M=0.8 is equal to 0.99%. The output voltage shows maximum value of 115V when modulation index, M=1.0 as shown in Figure 4.15. Figure 4.16 shows the THD when M=1.0 is equal to 0.99%. As the relationship deduced from Two- Level Inverter, the reduction in modulation index, M can lead to decrease in output voltage and increase in THD.

Figure 4.17 shows the output voltage and load current versus time, it shows that the output voltage and load current are nearly in- phase. Thus, the power factor of the inverter is nearly 1 (unity power factor).

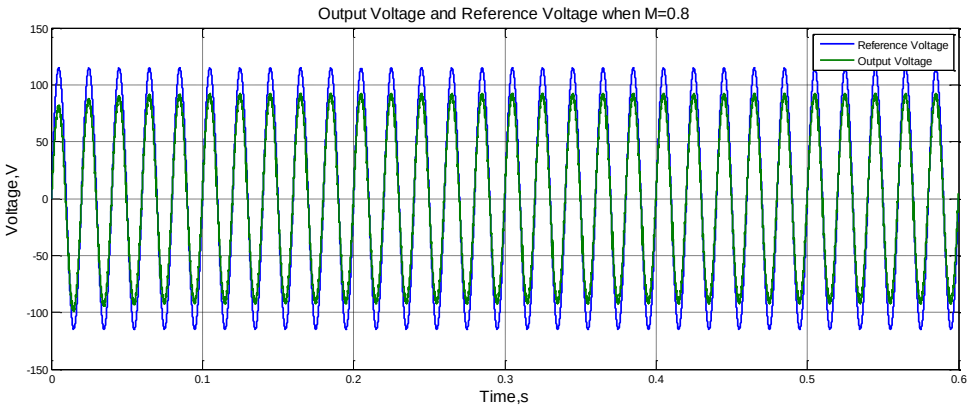

Figure 4.14: Output Voltage for 5- level CHMI when M=0.8

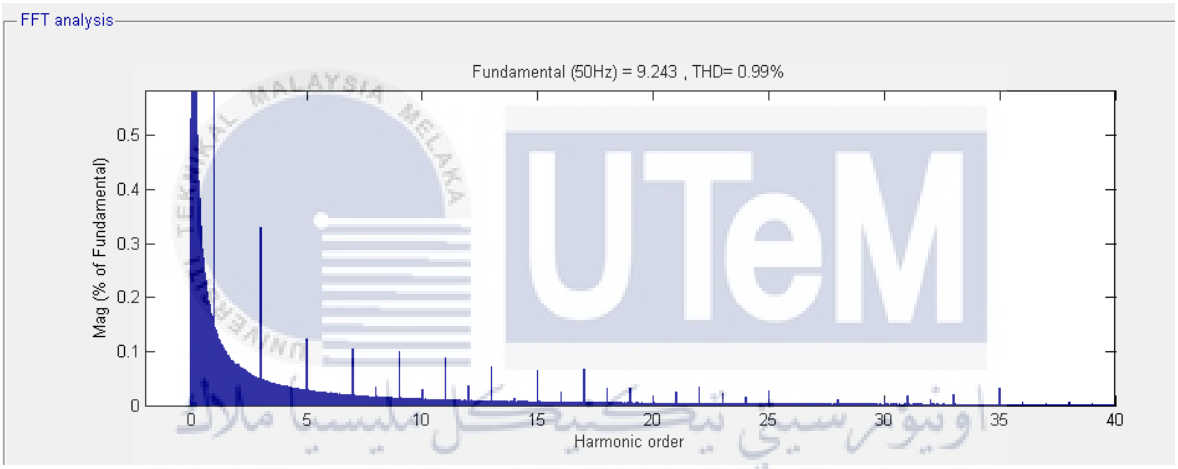

Figure 4.15: The total harmonic distortion when M=0.8

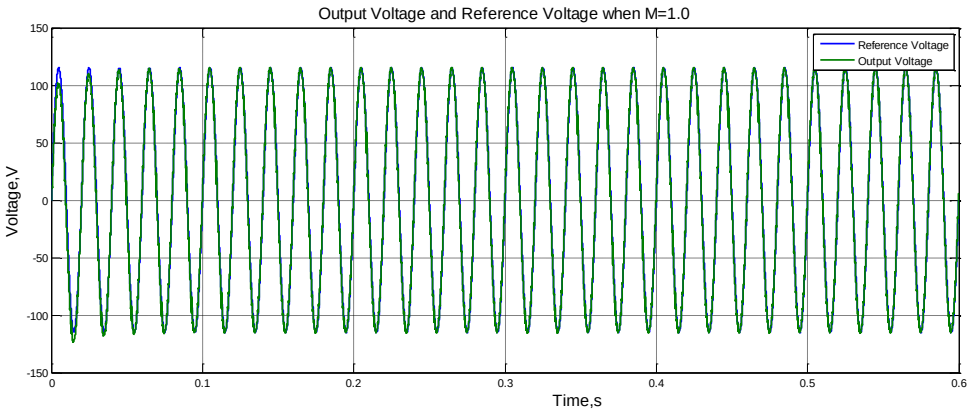

Figure 4.16: Output voltage of Five- Level CHMI when M=1.0

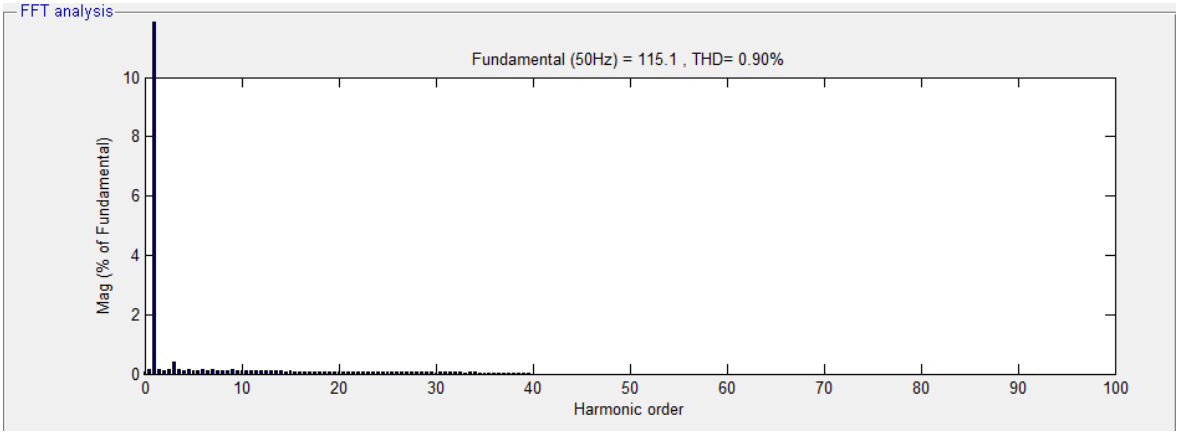

Figure 4.17: The total harmonic distortion when M=1.0

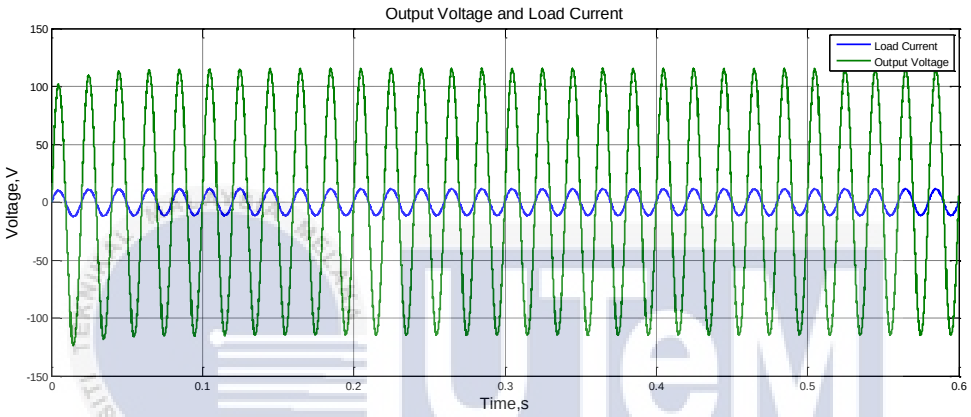

Figure 4.18: The output voltage and load current for Five- Level CHMI

The THD of Two- Level Inverter is 7.28%; while THD of Five- Level Inverter is 0.90% which is 6.38% lesser than of Two- Level Inverter. Therefore, the new switching strategy is designed based on Five- level CHMI.

4.2.3 Five- Level CHMI Using Newly Proposed Switching Strategy

The resulting SPWM switching is shown in Figure 4.19 and 4.20. The gating signals produced are the same as those produced by using the scheme PH disposition. The positive side of this scheme is it can produce the same gating signals using lesser carrier signal. It uses only one sinusoidal reference and one triangular carrier signal.

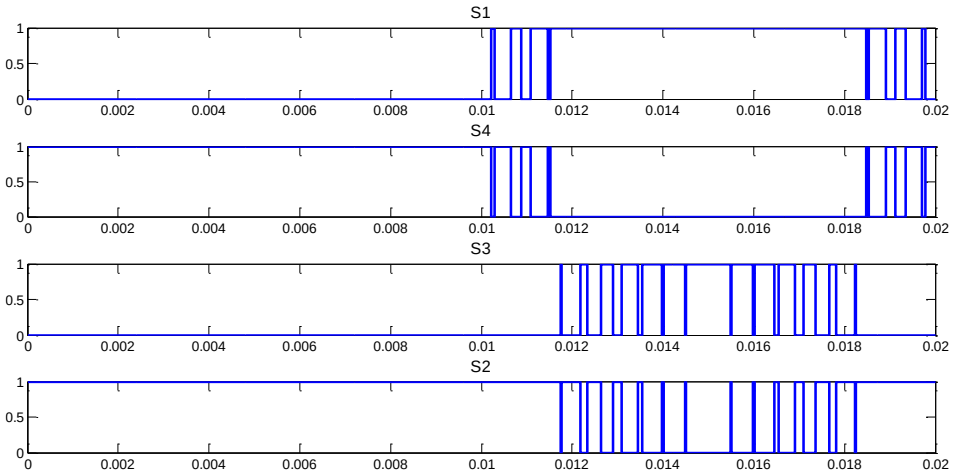

Figure 4.19: The gate signals for S1-S4

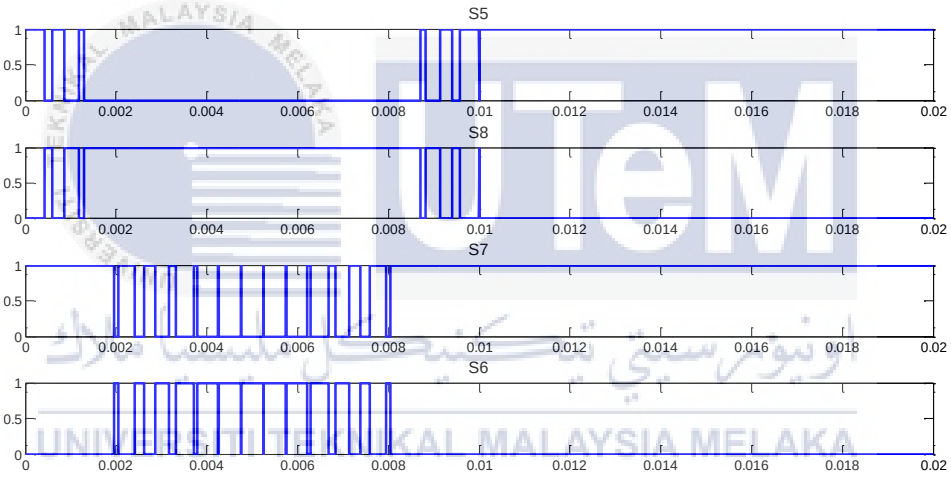

Figure 4.20: The gate signals for S5-S8

Figure 4.21 shows the output voltage for five- level CHMI using the proposed switching strategy where modulation index, M=0.8. As shown in Figure 4.21, it can be seen that the maximum output voltage is 80V. The total harmonic distortion (THD) of five- level CHMI is 0.98% when M=0.8 as shown in Figure 4.22. Figure 4.23 shows the output voltage for five- level CHMI using the proposed switching strategy where modulation index, M=1.0. As shown in Figure 4.23, it can be seen that the maximum output voltage is 115V. The total harmonic distortion (THD) of five- level CHMI is 0.72% when M=1.0 as shown in Figure 4.24. The theories stated that the highest output voltage, V_o should be the sum of the input voltage, V_{in} of each cell. V_{in} of each cell is 60V, thus the peak output voltage should be 120V.

This is due to the when the switches are turned ON and OFF, its intrinsic parasitic capacitance stores energy and dissipates it as heat during each switching transition. This situation often called as switching losses.

Figure 4.25 shows the output voltage and load current which is almost in phase. Power factor of it is nearly 1 which means unity power factor.

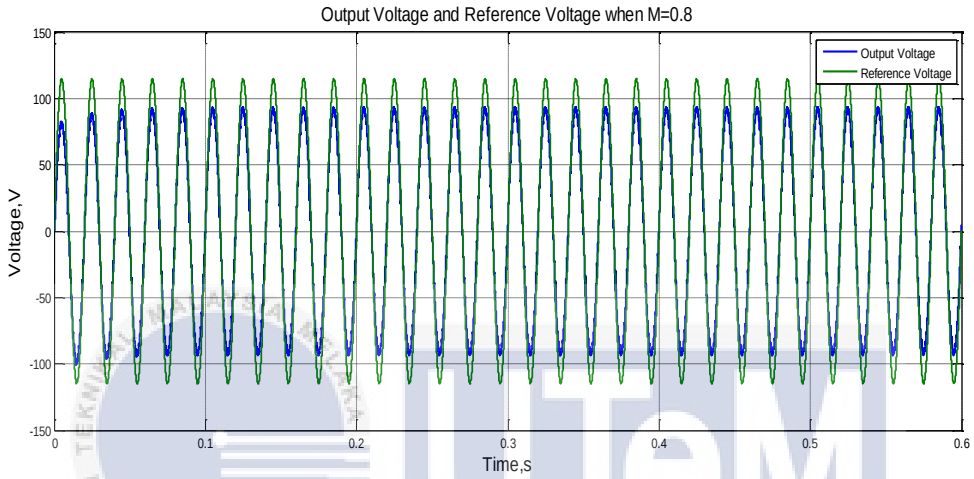

Figure 4.21: Output Voltage for 5- Level Inverter with New Switching Strategy (M=0.8)

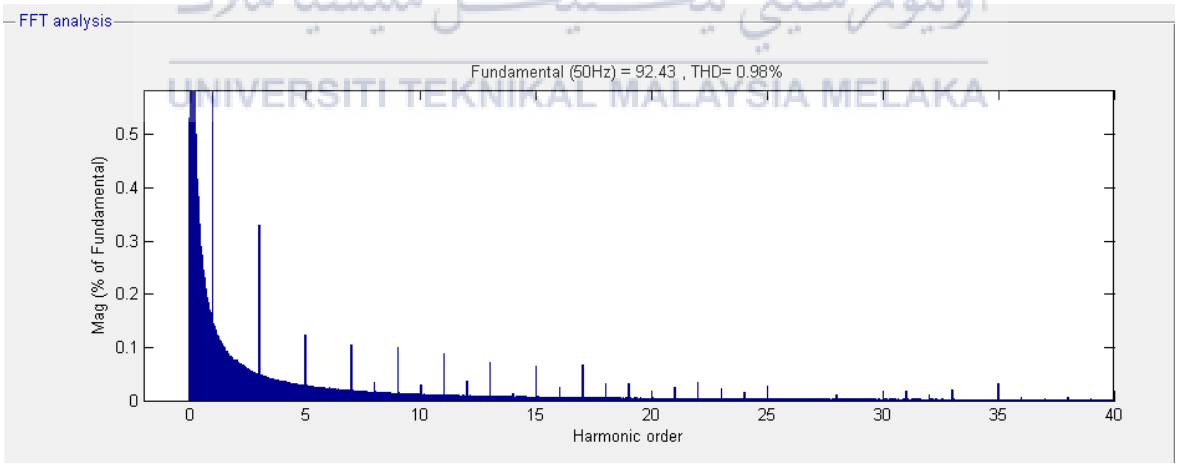

Figure 4.22: The THD of Five- Level CHMI with New Switching Strategy (M=0.8)

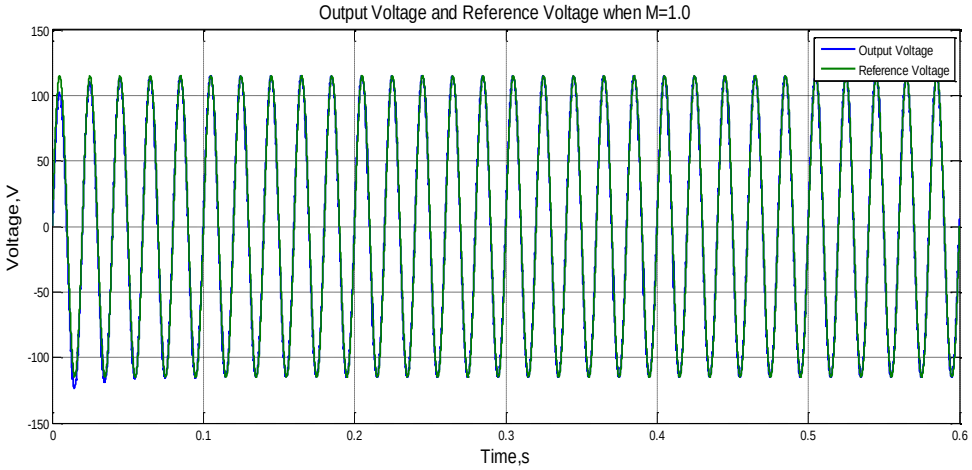

Figure 4.23: Output Voltage for 5- Level Inverter with New Switching Strategy (M=1.0)

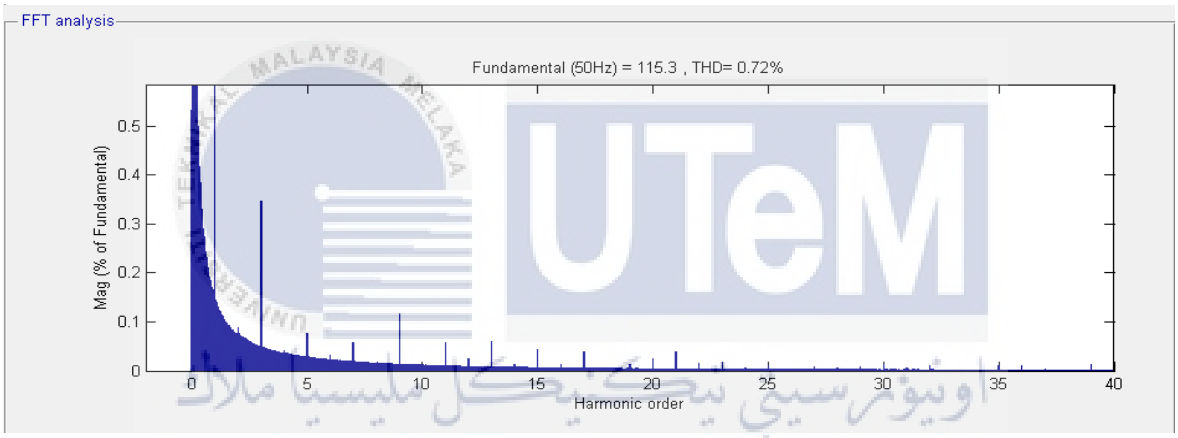

Figure 4.24: THD of 5- Level CHMI using new switching strategy (M=1.0)

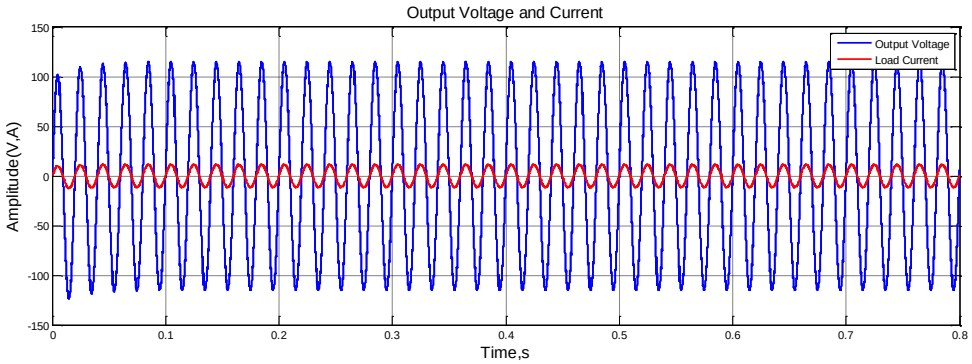

Figure 4.25: Output Voltage and Load Current of Five- Level CHMI using Proposed Switching Strategy

4.3 Closed- Loop Five- Level CHMI using the Proposed Switching Strategy

A modified PID controller is used as to correct the output voltage of the five- level CHMI. Figure 4.26 and 4.27 show the output voltage of the inverter when the load is varied without the PID Controller. The load is 20Ω at t=0s and changed to 15Ω at t=0.2s and 10Ω at t=0.4s. It can be observed that the output voltage does decreases when the load is increased. Therefore, to make the inverter operates normally when the load is varied, a modified PID controller is needed.

As shown in Figure 4.28 and 4.29, the output voltage of five- level CHMI under the control of a PID controller shows perfect sinusoidal waveform. It does not change when the load is varied. Although the output voltage waveform shows a minor delay in time, but it does not affect the power factor of the inverter. This can be proved by the output voltage and load current versus time graph as shown in Figure 4.30. The output voltage and load current are still in phase.

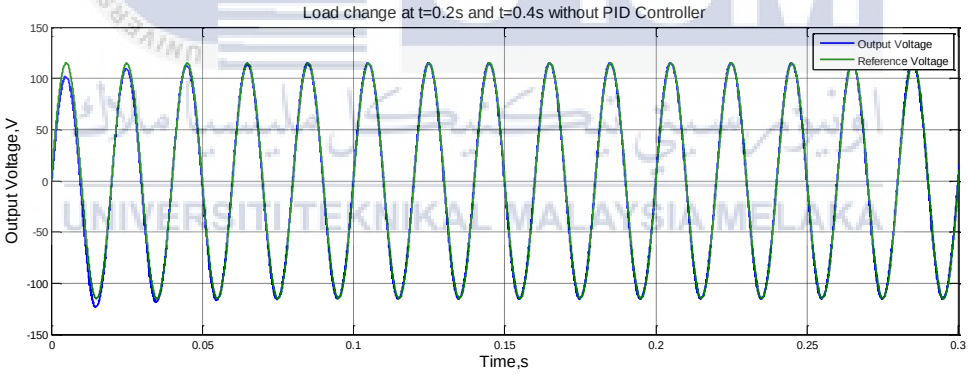

Figure 4.26: The output voltage when load is varied over time (t=0.0 to 0.3s)

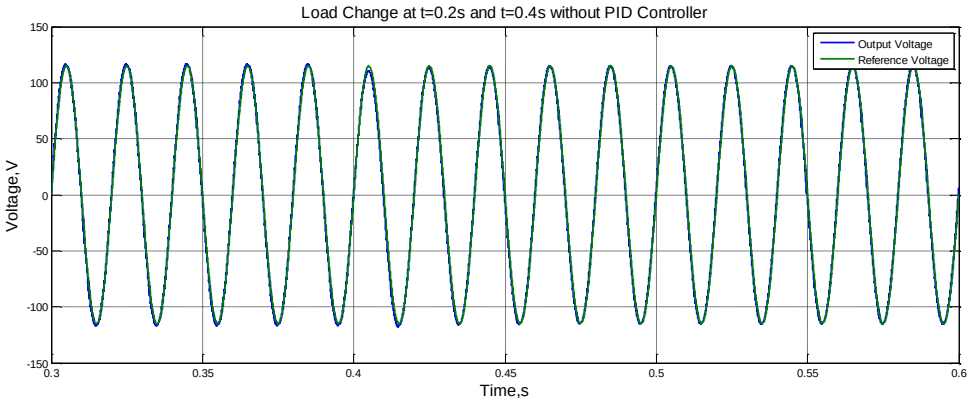

Figure 4.27: The output voltage when load is varied over time (t=0.3 to 0.6s)

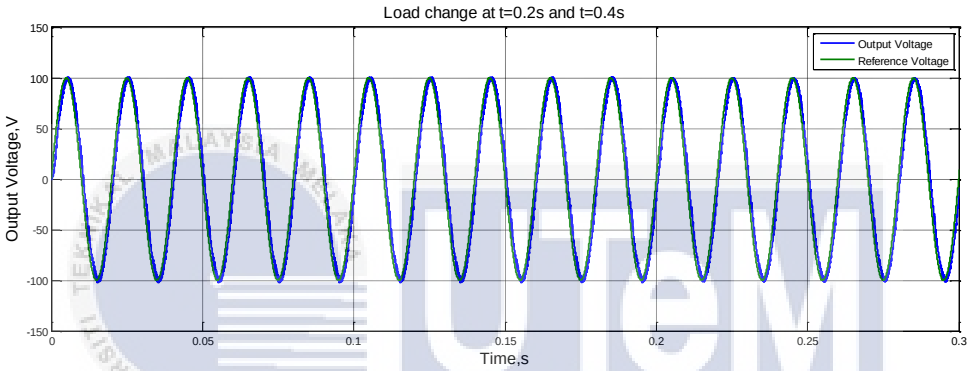

Figure 4.28: The output voltage when load is varied, t=0.0 to 0.3s (PID Controller is used)

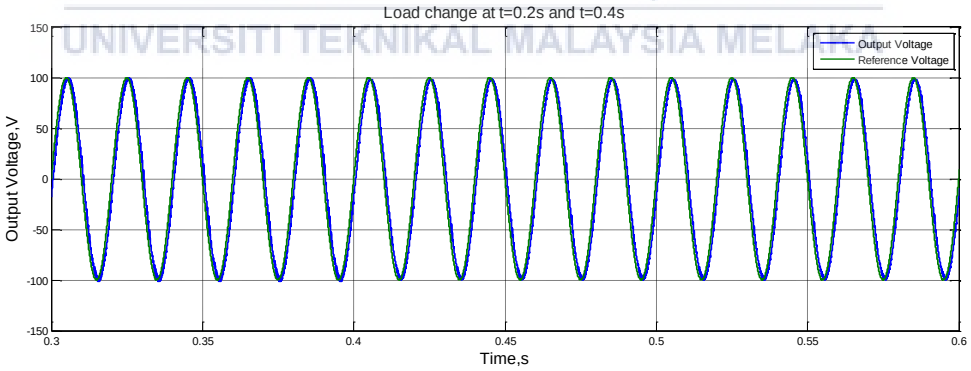

Figure 4.29: The output voltage when load is varied, t=0.3 to 0.6s (PID Controller is used)

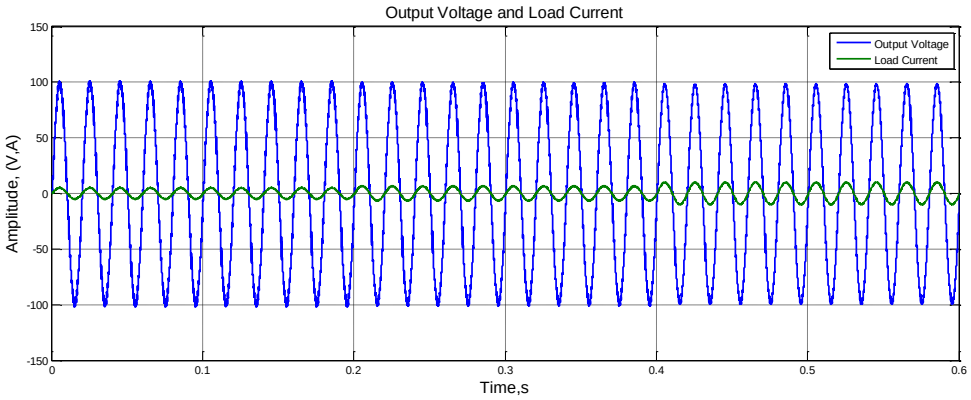

Figure 4.30: Output Voltage and Load Current of 5- Level CHMI with PID Controller

4.4 Conclusion

By comparing the THD value of both inverters, the THD for five- level CHMI is much lower than of Two- Level inverter. Thus, the proposed switching strategy is designed based on five- level CHMI.

After the proposed switching strategy is applied onto five- level CHMI, the THD measurement had shown an even better result. The new THD is now 0.72% which is 0.18% reduction compared to the conventional switching strategy.

Besides, a modified PID controller had also been designed to produce a better performance of five- level CHMI. The modified PID controller can correct the output voltage of the inverter when there is a load variation.

In a conclusion, simulation results of both Two- Level Inverter and Five- Level CHMI had been obtained. The newly proposed switching strategy had been validated using MATLAB Simulink simulation. As been observed in the obtained results, simulation and theoretical parts are in a great agreement which confirm the theoretical studies in Chapter 2.

CHAPTER 5

ANALYSIS AND DISCUSSION OF RESULTS

5.1 Introduction

As shown in Chapter 4, simulation results show great agreement with the theories shown in Chapter 2. The objectives of this paper are successfully met.

5.2 Analysis of the Results

Two- Level inverter and Five- Level CHMI are compared and the results are tabulated in Table 5.1. The total harmonic distortion of conventional inverter is 7.28% which is 6.38% larger than of five level CHMI which shows 0.90% THD. Since five- level CHMI shows better THD and the output waveform is better than Two- Level Inverter, thus the new switching strategy had been proposed based on five level CHMI.

Table 5.1: Comparison between 2- Level Inverter and 5- Level Inverter

Inverter Level	**Conventional Inverter (2-Level)**	**Multilevel Inverter (5-Level)**
Total Harmonic Distortion (THD), %	7.28	0.90
Power Factor (PF)	≈ 1	≈ 1

The existing switching strategy for five level CHMI and the proposed switching strategy are compared and the results are tabulated as in Figure 5.2. The THD of the existing switching strategy which needs four triangular carrier signals is 0.90% which is larger than of the proposed switching strategy which shows 0.72% THD.

Table 5.2: Comparison between Switching Strategies

Switching Strategy	Existing Switching Strategy (4 carriers signals)	Proposed Switching Strategy (1 carrier signal)
Total Harmonic Distortion (THD), %	0.90	0.72
Power Factor (PF)	≈ 1	≈ 1

Both switching strategies show satisfying power factor (PF) which is nearly 1. PF can be calculated using the equation as below:

$$PF = \cos \theta \tag{5.1}$$

Θ is the angle between the load current and output voltage. The larger the PF, the higher the utility of power in a circuit. Therefore, to lower the losses in a device, low PF is more preferable.

5.3 Significance and Implication of the Findings

One of the objectives of this paper which is designing a new switching strategy for five- level cascaded H- Bridge multilevel inverter is achieved.

The newly proposed switching strategy needs only one triangular carrier signal and one sinusoidal reference signal. It reduces the existing switching strategies' complexity and ease the implementation of it in simulation. Not only that, the proposed switching strategy shows a better output THD compared to the existing strategy.

Besides, the instantaneous voltage error from the comparison between the output voltage, V_o and the desired voltage is fed into a PID controller. The controller improves V_o by reducing the instantaneous voltage error between the reference and the actual voltage. This is to ensure V_o to be in nearly sinusoidal waveform which is a perfect alternating current (AC) waveform.

CHAPTER 6

CONCLUSION AND RECOMMENDATION

6.1 Conclusion

A study on total harmonic distortion and output voltage of Five- Level Cascaded H-Bridge Multilevel Inverter (CHMI) has been done in this paper. In each section, detailed techniques and ideas used to implement the Five- Level CHMI have been discussed.

This paper discussed the three types of multilevel inverter topologies which are CHMI, Diode- Clamped and Flying Capacitors. The CHMI topology has been chosen since it uses least number of components compared to the other two. Besides that, SPWM is chosen to implement into the CHMI topology for this paper. The existence of harmonics in the output voltage of a CHMI leads to inefficient of the system performance. Thus, SPWM is used to remove harmonics.

This paper suggests that the Five- Level CHMI is better than conventional inverter in terms of total harmonic distortion and output voltage. This suggestion is supported by simulation of the Five- Level CHMI done by using MATLAB. Results obtained validated the better harmonics by using Five- Level CHMI.

This paper also proposed a new switching scheme which needs only one triangular carrier signals for a five- level CHMI. The new switching strategy also shows a better total harmonic distortion (THD) which is lesser than of the existing switching strategy.

6.2 Recommendation

There are several recommendations can be proposed for future work:

i. Designing a better filter to eliminate the harmonics and get a better sine wave output signal with smaller THD.
ii. Implementing a higher number of output voltage levels topology to get a better output waveform with smaller THD.
iii. Designing switching pattern for three phase multilevel inverter.

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