DESIGN AND DEVELOPMENT OF AN ULTRA-LOW POWER CMOS VOLTAGE REGULATOR

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Supervisor's Name : Dr WONG YAN CHIEW

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For my lovely mother and father

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ABSTRACT

The Low Dropout Voltage Regulator (LDO) is widely used in the industry for wide range of applications such as smart phones, tablets, wearables. These LDOs are usually demanded to be ultra-low quiescent current. Low current consumption in LDO is favouring longevity of the battery life, such LDO become part of the powering solution for IoT devices that needed long sustain battery life at all times. The objectives of this work are focusing on realization of low current consumption that gives high power efficiency low dropout voltage regulator. The design of ultra-low power LDO in this work utilises the simple topology which comprising a bandgap reference, error amplifier, a feedback-voltage divider and a pass device. The design specification for current consumption of the LDO design is in micro ampere and the operating temperature of the LDO design is between -40 degrees Celsius to 125 degrees Celsius for the input range from 1.6 V to 5V. The LDO is designed and developed in Silterra 130nm technology by using Synopsys design tool and the performance of the LDO is analysed.

ABSTRAK

Low Dropout Voltage Regulator (LDO) digunakan secara meluas dalam industri untuk pelbagai aplikasi seperti telefon pintar, tablet dan sebagainya. LDOs biasanya diperlukan dengan penggunaan arus yang sangat rendah. LDO yang memerlukan arus yang rendah adalah memihak umur panjang hayat bateri, LDO tersebut boleh dijadikan salah satu penyelesaian untuk aplikasi IOT yang perlu lama mengekalkan hayat bateri pada setiap masa. Objektif kerja ini memberi tumpuan kepada merealisasikan penggunaan arus rendah di LDO untuk memberikan kuasa tinggi kecekapan bagi LDO. Reka bentuk LDO di kerja ini mengaplikasikan topologi yang ringkas dan mudah. Topologi ini mengandungi *bandgap reference*, *error amplifier, feedback-voltage divider* dan *pass device.* Spesifikasi reka bentuk LDO tersebut adalah berada di mikro ampere dan suhu operasi reka bentuk LDO adalah antara -40 darjah Celsius hingga 125 darjah Celsius untuk kemasukan volt daripada 1.6 V untuk 5V. LDO tersebut dicipta dalam teknologi 130nm Silterra dengan menggunakan Synopsys dan prestasi LDO tersebut dianalisiskan.

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LDO	Low Dropout Voltage Regulator
PMOS	P-type Metal-Oxide-Semiconductor
IoT	Internet of Things
SoC	System on Chip
PTAT	Proportional to absolute temperature
CTAT	Complementary to absolute temperature
DC	Direct Current
GBW	Gain-Bandwidth product
NMOS	N-type Metal-Oxide Semiconductor
PMOS	P-type Metal-Oxide Semiconductor
DRC	Design Rule Check
LVS	Layout Versus Schematic
PSRR	Power Supply Rejection Ratio
SR	Slew Rate

GLOSSARY

ERROR SIGNAL	A voltage whose magnitude is proportional to the difference between an actual and desired position
INPUT COMMON MODE RANGE	The average voltage of the inverting and non-inverting input

CHAPTER I

INTRODUCTION

1.1 PROJECT BACKGROUND

Power management for Internet of Things (IoT) devices is a challenging task. With the new data from Juniper Research reveals that the number of IoT devices will triple to over 38 billion units by 2020, the power solution for incoming wave of IoT devices in the future is becoming critical. IoT devices are always power-hungry as they require long sustain battery life to operate. It is almost impossible to have them wired and plugged in to power supply all the time as they are meant to work wirelessly. Therefore, to address this problem, scientists, and researchers study on the power solution for IoT devices such as utilizing ambient energy source and working on different battery technologies[1].

An ultra-low power low-dropout voltage regulator (LDO) can be part of the solution for power hungry IoT devices. It is a common block in power management system to regulate input voltage to a fix, steady and clean output

voltage and prevent potential damage caused by fluctuated voltage as well as overloading A LDO is designed to be high power efficiency to prolong battery life for IoT devices. It is expected to consume less current and drains less power from the battery to achieve longevity in the battery life.

1.2 PROBLEM STATEMENT

The power solution for IoT devices become significantly important especially the feature of the device drains battery very fast. This leads to the needs of frequent replacement of the battery in the device. The use of rechargeable battery seems to be a good option to avoid frequent replacement of battery but it has its own limitation as well. The rechargeable battery usually exhausts after a few hundred charge cycles and it will need a replacement eventually. Therefore, a low power LDO is designed. It consumes less current and prolong battery life in a way that less power is drain from the battery for the functionality of the LDO. However, a LDO requires low quiescent current in realizing a low power LDO design. This cannot be achieved with a conventional LDO due to the high quiescent current in conventional LDO. Moreover, the performance of the LDO must be compromised for a low quiescent current. The low quiescent deteriorates the driving capability of the pass device and causes poor performance of the LDO during changing of output load. Any buffer or driver that is added in front of the pass device will increase the driving force at the gate of the pass device but at the same time, it consumes quiescent current in the LDO. Due to this matter, the power consumption of the LDO is increased and leading to poor efficiency of the LDO [2].

1.3 OBJECTIVE

The main objectives of this project are:

I. Identify the key design parameters in low power CMOS LDO regulator design

II. To propose a new design methodology for high efficient low power CMOS LDO regulator

III. To design and develop the high efficiency low CMOS LDO regulator

IV. To verify the proposed methodology theoretically and analytically through modelling

1.4 SCOPE OF PROJECT

The design of the proposed LDO circuit is consisting of a bandgap reference, error amplifier and a pass device. A low power LDO topology is investigated and utilized in this proposed work to achieve low quiescent current and leading to high power efficiency design of LDO. The design considerations of each building blocks in the LDO circuit is considered to realize an ultra-low power LDO design. The LDO is designed and simulated using Synopsys tool. The LDO design will be for the use of device level in an IoT device. Finally, the design is completed until layout design that is ready for fabrication.

1.5 THESIS STRUCTURE

The dissertation is organized as follows:

I. Chapter I Introduction

This chapter presents the background study, problem statement, objectives as well as the scope of the study. The introduction of this project provides an overview of the proposed work.

II. Chapter II Literature Review

This chapter presents the architecture and working principle of low-dropout voltage regulator (LDO). Furthermore, a discussion on various low-dropout voltage regulator topologies from various research papers, the design consideration of LDO and bench marking will be included in this chapter.

III. Chapter III Methodology

The full design flow of analogue design and the analogue design rules are presented in this chapter. The design specification of this project is also presented in this chapter.

IV. Chapter IV The LDO Design

This chapter presents the schematic, layout of the proposed work and the detail working on how to design the LDO. This chapter is consisting the design specification. The final LDO design with all the parameters is also displayed in this chapter. At the end of this chapter, the layout design of the final LDO design is presented.

V. Chapter V Result and Discussion

This chapter will present the simulation analysis and discussion. The analysis and discussion is involving the bandgap reference, error. The bandgap reference simulation will verify the operating temperature followed by error amplifier simulation that verify the open loop frequency response of the error amplifier. The final LDO simulation is analysed for its steady state analysis and dynamic state analysis as well as high frequency analysis. The discussion is about the result achieved. amplifier and the final LDO design.

VI. Chapter VI Conclusion

This chapter summarizes the findings from overall results and discussion of the project. The future recommendation is also presented at the end of this chapter.

CHAPTER II

LITERATURE REVIEW

2.1 INTRODUCTION

This chapter presents an overview of the low-dropout voltage regulator (LDO). It also includes the architecture and working principle of a conventional low-dropout voltage regulator (LDO) and a review of various low-dropout voltage regulator topologies. The design consideration and bench marking of LDO will be presented in the following sections of this chapter.

2.2 LOW DROPOUT VOLTAGE REGULATOR

Low-dropout voltage regulator (LDO) is a type of linear voltage regulator and like any other voltage regulator, it regulates input voltage to give a fix, steady and clean output voltage. It is different from other linear voltage regulator in term of its drop-out voltage. LDO has low-dropout voltage which typically lower than 1V while

the drop-out voltage means the minimum differential voltage between the output and input at the instance it stops to regulate [3]. In other words, the low dropout voltage can be understood as the low input to output difference. When the difference of input and output is low, a lower value of minimum input voltage is required by the LDO to provide the fixed amount of output voltage Thus, the low drop-out nature of LDO is said to be appropriate for portable devices as the input supply voltage of portable devices will not be high [4].

LDO can be categorized as low power LDO or high power LDO. These two types of LDO are different in terms of their output current. Low power LDO are those consuming low current within themselves when no load is applied. This type of current is known as quiescent current. It is one of the parameter to refer as to compare how low power is the LDO. Most portable applications require low power LDOs because the battery supply is limited unlike power supply from the socket. Low power and low quiescent current flow is highly demand in portable electronics industry for long battery life and increased battery efficiency. On the other hand, high power LDO consumes higher current which typically greater than 1A. It is commonly used in industrial and automotive applications.

2.3 ARCHITECTURE AND WORKING PRINCIPLE OF LDO

The basic blocks of a conventional LDO include the bandgap, error amplifier, pass device of PMOS, a resistive feedback network which made up of two feedback resistors R1 and R2, a decoupled capacitor C_{out} with a parasitic resistor R_{esr} as shown in Figure 2.1.

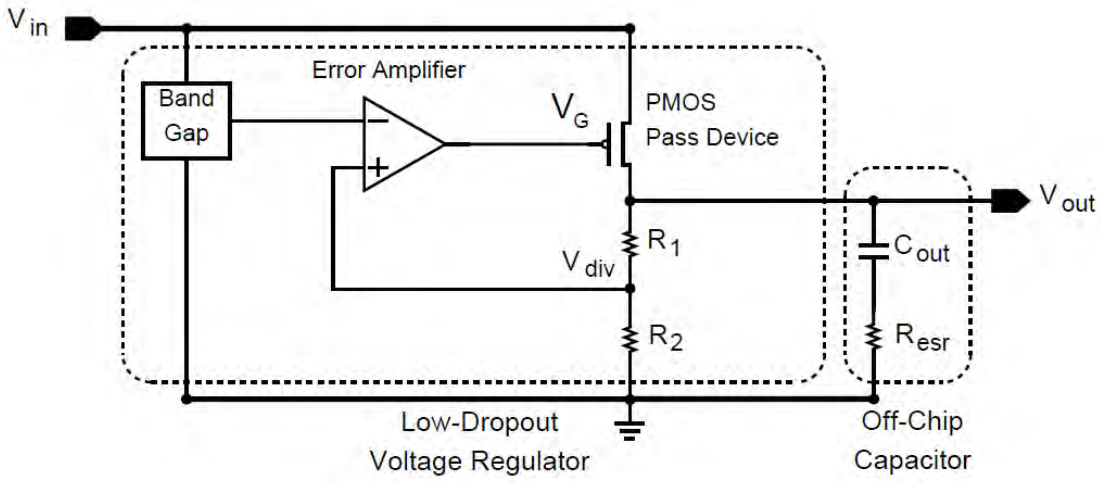

Figure 2.1 Conventional LDO

A LDO needs a voltage reference to operate. The voltage reference is used to compare with the scale down voltage to produce fix and steady required regulated voltage. The bandgap plays an important role in establishing the voltage reference for LDO. Since both bandgap and LDO have the same function of providing fix and steady output voltage, therefore it is of utmost importance to differentiate these two components. A LDO is required to provide steady current and voltage to numbers of blocks while a bandgap must be able to provide steady voltage only to a single block like in a LDO.

The error amplifier in the LDO compares the bandgap reference and the scaled down output voltage, it also controls the current flow through the pass device to meet the output requirement. Pass device is a PMOS with common source connection that places between input and output voltage. It is an important part of the LDO and occupied almost half of the LDO design area in the chip. This device is huge because it bears a big responsibility to drive the current flow to the load. Feedback resistors R1 and R2 are a voltage divider that scale down the output voltage to a suitable value for error amplifier to compare with bandgap reference. The scaled down voltage is a negative feedback to the positive terminal of the error amplifier while the bandgap feds to the negative terminal of the amplifier[5]. Lastly, a large off-chip capacitor is needed at the output of the LDO to improve the stability. [3], [6]