ANALYSE OF PROCESS PARAMETER VARIATION IN GRAPHENE FIELD-EFFECT TRANSISTOR (GFET) DEVICE USING L9 OA TAGUCHI METHOD

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DECLARATION

"I declare that this thesis entitle "Analyse of Process Parameter Variation In Graphene Field-Effect Transistor (GFET) Device Using L9 OA Taguchi Method" is the result on my own research except as cited with the references. The thesis has been accepted for any degree and is not concurrently submitted in candidature of any other degree."

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SUPERVISOR VERIFICATION

I hereby declare that I have read this report and in my opinion this report is sufficient in terms of scope and quality for the award of Bachelor of Electronic Engineering (Computer Engineering).

Signature :.....

Supervisor's Name : DR. FAIZIYATI SALEH-DAIN

Date : 2/6/2017.

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Dedicated to my beloved family especially my parents, supervisor, lecturers and all my friends who helping me whether directly or indirectly.

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ABSTRACT

This project is about analyse of process parameter variation in Graphene Field-Effect Transistor (GFET) device using L_9 OA Taguchi Method. The simulation process is done by using Silvaco TCAD tools and the statistical modeling is analyzed by using L_9 orthogonal array (OA) of Taguchi method. In this research, there are four process parameter that be investigated which halo implant dose, halo implant energy, S/D implant dose and S/D implant energy. L_9 OA Taguchi method is used to analyse the process parameters and noise factor to identify the optimum value of threshold voltage (V_{TH}), drive current (I_{ON}) and current state ratio (I_{ON}/I_{OFF}). The aims of this project are to design GFET device by using ATHENA module, to analyze the electrical characteristics of GFET by using ATLAS module and to optimize the process parameter variation of GFET using Taguchi method. The value of threshold voltage (V_{TH}), drive current (I_{ON}) and current state ratio (I_{ON}/I_{OFF}) are compared with before and after optimization. In addition, the value of current state ratio (I_{ON}/I_{OFF}) also be compared with previous research. This research is proved that the value after optimization is better than before optimization and current state ratio (I_{ON}/I_{OFF}) of this research is higher compared to previous research.

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ABSTRAK

Projek ini adalah mengenai analisis variasi proses parameter di dalam *Graphene Field-Effect Transistor (GFET)* peranti menggunakan *L9 OA* Kaedah Taguchi. Proses simulasi dilakukan dengan menggunakan alat *SILVACO TCAD* dan pemodelan statistik menggunakan *L9 OA* kaedah *Taguchi*. Dalam kertas ini, terdapat empat proses parameter yang dikaji iaitu halo implant dos, halo implant tenaga, S/D implant dos dan S/D implant tenaga. *L9 OA* kaedah Taguchi digunakan untuk menganalisis proses parameter untuk mengenal pasti nilai optimum ambang voltan *(V_{TH}), drive current (I_{ON})* dan current-state ratio (I_{ON}/I_{OFF}). Matlamat projek ini adalah untuk mereka bentuk peranti GFET dengan menggunakan modul *ATHENA*, menganalisis ciri-ciri elektrik dengan menggunakan modul *ATLAS* dan mengoptimumkan proses parameter dengan menggunakan kaedah Taguchi. Nilai V_{TH}, I_{ON} dan nisbah I_{ON}/I_{OFF} dibandingkan dengan sebulam dan selepas proses pengoptimum. Di samping itu, nilai nisbah I_{ON}/I_{OFF} dibandingkan dengan kajian penyelidikan yang lepas. Kajian ini membuktikan bahawa nilai selepas pengoptimum adalah lebih baik daripada sebelum pengoptimum dan nisbah I_{ON}/I_{OFF} kajian ini lebih tinggi berbanding dengan kajian penyelidikan sebelum ini.

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LIST OF ABBREVIATIONS

CMOS	-	Complementary Metal Oxide Semiconductor
MOSFET	-	Metal Oxide Semiconductor Field Effect Transistor
Si MOSFET	-	Silicon Metal Oxide Semiconductor Field Effect Transistor
GFET	-	Graphene Field Effect Transistor
TCAD	-	Technology Computer Aided Design
OA	-	Orthogonal Array
CVD	-	Chemical Vapor Deposition
FET	-	Field Effect Transistor
S/N	-	Signal-to-noise ratio
ITRS	-	International Technology Roadmap for Semiconductors
Bi-graphene	-	Bilayer Grapheme
I-V	-	Device Current-Voltage Characteristics
MOS	-	Metal-Oxide Semiconductor
S/D	-	Source/Drain

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LIST OF SYMBOLS

˚C	-	Celsius
2D	-	2-Dimensional
eV	-	Electron-volt
I_D	-	Drain Current
I_{OFF}	-	Off-state Current or Leakage Current
I_{ON}	-	On-state Current or Drive Current
k	-	Boltzmann constant
Lg	-	Gate Length
n	-	Free electron concentration
Ni	-	Nickel
Nm	-	Nano-meter
s	-	Second
Si	-	Silicon
SiC	-	Silicon Carbide
SiO_2	-	Silicon Dioxide
V_D	-	Drain Voltage
V_{DS}	-	Drain to Source Voltage
V_G	-	Gate Voltage
V_{GS}	-	Gate to Source Voltage
V_{TH}	-	Threshold Voltage
µm	-	Micro-meter
WSi_2	-	Tungsten Silicide
I_{ON}/I_{OFF}	-	Current State Ratio

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CHAPTER 1

INTRODUCTION

1.1 Background

In the past recent years, the microelectronic industry has decreased the transistor feature size scaling which 10µm to approximately 30nm. Apart from that, silicon(Si) bipolar also changed to p-channel metal oxidesemiconductor (MOS) and then evaluate to n-channel MOS and stop to complementary MOS (CMOS) planar transistor. Unfortunately, the industry also had faced challenges in scaling the transistor size into 10nm. However, this challenges need to be overcome by identifying other material that suitable to replace Si transistor in the future [1]. Another limitation that come across is the physical limits of the transistor [2]. The development of CMOS scaling in recent years is defined as Moore's Law. Figure 1.1 shown evolution of transistor according to Moore's Law [3].

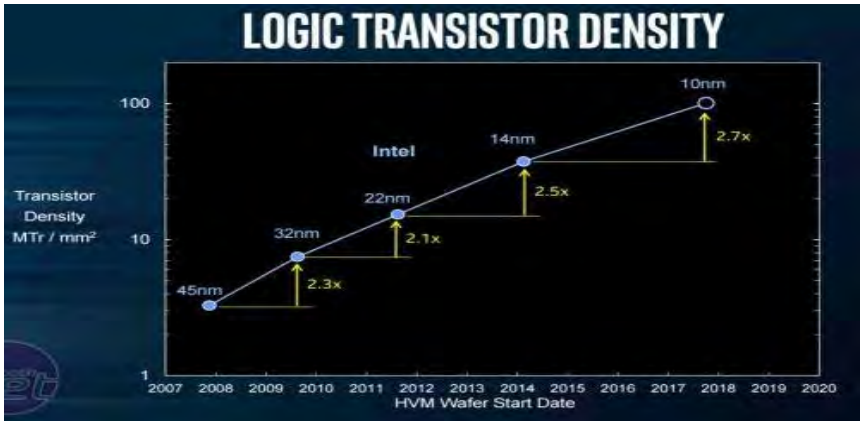

Figure 1.1 : Moore's Law in evolution of a billion transistor in recent years.

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Scaling theory is based on the simple rules of the transistor design which need in increase of circuit speed and density. Therefore, with the improvement on circuit performance and density, a complicated functionallity can be construct into a single chip. This can give benefit in reducing cost of fabrication [3]. Moore's Law state that the component density and performance of integrated circuits will be double in every two years. The integrated circuits and scaling based on Moore's Law is said as "the cheap way to do electronics". The rate of improvement to overcome the limitation of CMOS will be change again and that means that Moore's Law is still have more further. The limitations of the scaling are parasitic resistance and capacitance. This limitation is assumed as negligible by scaling theory. This limitation was accepted in the past 40 years but are not valid anymore for futher implementation in the next years. Moore's law is not a physical law but it is a law about economics [1].

Therefore, to overcome the limitation there are a research regarding to identify a new device structure and alternative material. A few nanoelectronics device have been choosen to replace MOSFET device. For example silicon nanowire (SiNW), carbon nanotubes (CNT), III-V compound materials such as gallium arsenide (GaAs) and germanium (Ge) and last but not least is graphene. As this reseacrh continued, the graphene had final be choose as the most suitable material that can replace Si MOSFET [4]. Graphene is type of material that produce as high quality material with simple procedure and has cheap cost. Graphene has a large number of its material parameters such as mechanical stiffness, strength and elasticity, very high electrical and thermal conductivity [5]. A further explanation regarding to this material will be explain further in literature review part of this report.

This project is about a simulation process of MOSFET-like graphene field-effect transistor (GFET) by using a technology computer aided design (TCAD) tools software. In this SILVACO TCAD tools software, the material of graphene does not still exist in its library therefore the polysilicon is set as a graphene with change the properties of polysilicon into graphene properties. The structure of GFET is design in ATHENA module and its electrical characteristics is define by using ATLAS module. Bilayer

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graphene is used in MOSFET-like GFET device due to its potential in one of the solution to open the band gap in graphene material. Taguchi method is utilize to optimize the process parameter on threshold voltage (Vth), drive current (I_{ON}) and current state ratio (I_{ON}/I_{OFF}) of the device. Analysis by using Taguchi method is done to identify which the process parameter that give the most impact on device performance. L9 Orthogonal Array (OA) of Taguchi Method is use for the statistical approach. The comparison is made up with previous research, before and after optimization.

1.2 Objectives of This Project

The main goal of this research is to analyse of process of parameter variation in Graphene field-effect transistor (GFET) device using L9 Orthogonal Array (OA) Taguchi method. The objectives are specific:

(i) To design MOSFET-like Graphene Field-Effect Transistor (GFET) by using ATHENA module in SILVACO TCAD tool.

(ii) To analyze the electrical characteristics of GFET by using ATLAS module.

(iii) To optimize the process parameter variation of MOSFET-like GFET using Taguchi method.

1.3 Problem Statement

Moore's law mentioned that the number of transistor in a chip will double every two years. For the past few years, researchers had identified for a new alternative to replace the existing silicon. There were showed a rapid growth between the developer to perform a better devices [3]. The variation of the development of transistor were changed aggressively in other to full fill the requirement for world industry and to define the limitation of Moore's law. It had been invented for low cost and sustain with high performance. The device had faced the limitation by using Si transistor due to the

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parasitic resistance and capacitance which are generally assumed negligible [1]. A new device structure and alternative material is needed to overcome this limitation. Hence, among the new material that been choose, graphene appeared as the most suitable material that can replaced Si MOSFET [5].

1.4 Scope of Project

This project execution is based on simulation and program development. Simulation of Graphene field-effect transistor (GFET) device will be conducted by using a ATHENA module in SILVACO's TCAD tool. Meanwhile, the simulation of electrical characteristics will be implemented by using an ATLAS module in SILVACO's TCAD simulation tool. This tool will be used to simulate and design device structures. Other than that, this project is focused on the application of Taguchi method to obtain the optimum solution for GFET device in order to verify the predicted optimal design.

1.5 Report Structure

This thesis consist of five chapters which contain of the introduction, literature review, methodology, result and discussion and for the last chapter is conclusion and recomendation of the project. Chapter 1 is about the introduction of the project. In this chapter, the background and specific intruction regarding to this project is explained. Apart from that, in this Chapter 1 the objectives of the project are state with the problem statement and also the scope of the project.

In Chapter 2, the real explaination regarding to this project is explain further with including the previous reseacrh done. The structure of the MOSFET-like GFET is discussed in this chapter with the analyse parameter by using Taguchi method. The methodologies of the project is explain in Chapter 3. Therefore, all the steps and flow toward solving the problem in such a specific method is used to design and develop the

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MOSFET-like GFET structure is explain further. Apart from that, the method that be used to analyse the parameter of the MOSFET-like GFET also is included in this chapter.

Next, for the Chapter 4 all the expected result from this project is describe here. Hence, the performance also be justified to make sure it meets the objectives of the reseacrh. Finally, Chapter 5 will concludes for the whole research progress of the project with the recommendation.

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