# ANALYZE THE PERFORMANCE OF 16NM DOUBLE GATE FINFET DEVICE USING SILVACO TCAD TOOL

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This Report Is Submitted In Partial Fulfillment Of Requirements For The Bachelor Degree of Electronic Engineering (Computer Engineering) With Honours

Faculty of Electronic Engineering and Computer Engineering
Universiti Teknikal Malaysia Melaka

May 2017

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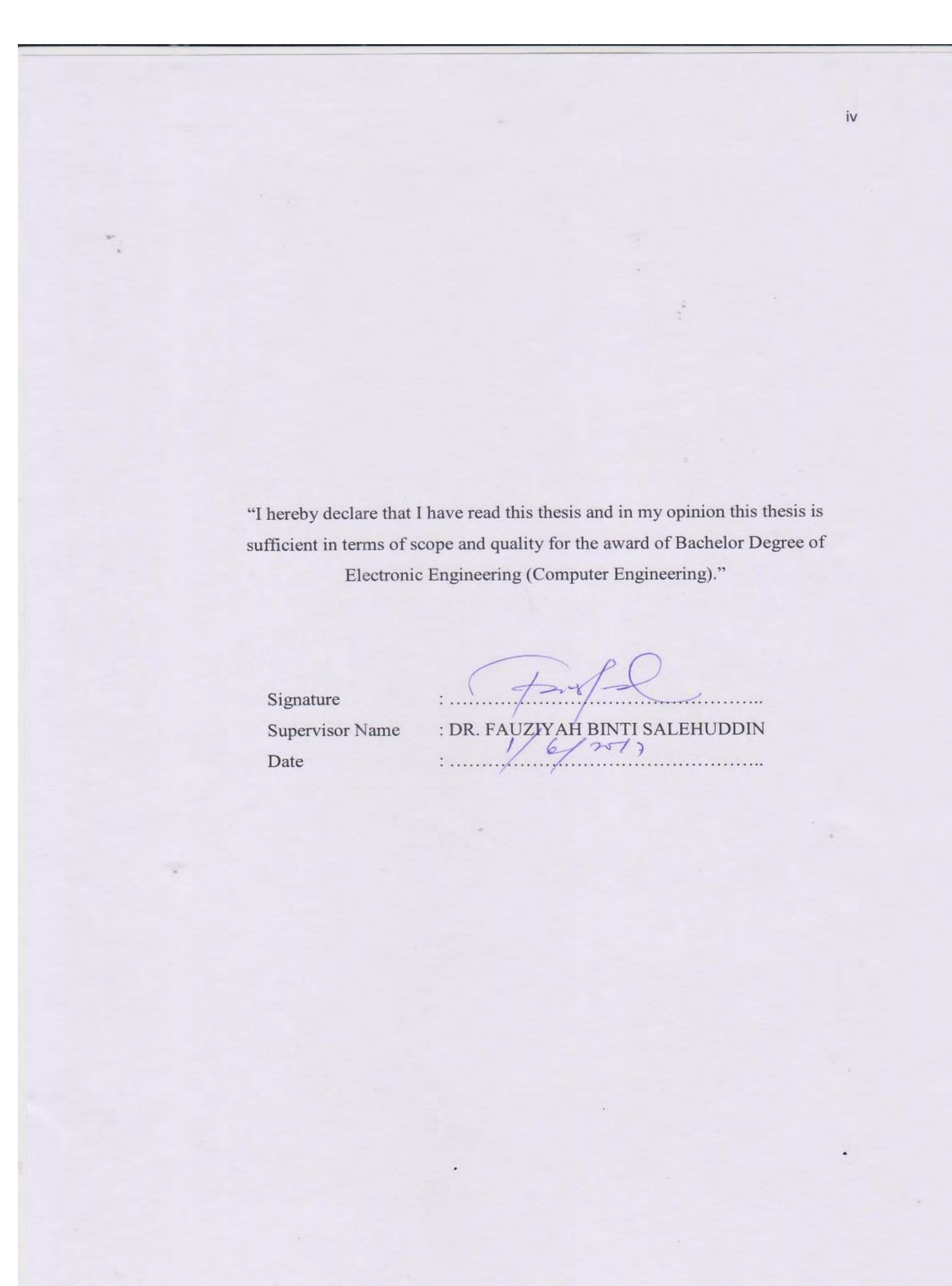



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# CHAPTER 1

# INTRODUCTION

This project used Silvaco Software and design and fabrication of MOSFET will be done using Silvaco's ATHENA software while device simulation (characterization) will be done by using ATLAS software. First part of the report will elaborate more on the project background. This chapter also mention on the problem statement, objective, and scope of the project.

## 1.1 Background

The electronic devices have grown dramatically and rapidly in line with the performance of the devices. The development of the modern electronic devices began since 1925 where the first solid-state transistor was built up which is metal-oxide-semiconductor field-effect-transistor or MOSFET. MOSFET is widely used for analog and digital circuits for example inverters, multiplexer, logic gate and etc. Then, the analog and digital circuits are combines to form integrated circuit (IC) that have been widely used either in low-power devices or high-power devices for example smart phones, laptops, sensors and etc. which is commonly used for human application. In daily life, portable devices are needed because it is easy to use, and more effective than

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wired devices. An example of a portable device that can be seen commonly is the portable charger. It make easy to charge smart phone during travelling and reduce the electricity cost. The performances of these devices are very good and meet the requirements of today.

Figure 1.1 **:** The trend of increasing the number of microprocessor transistor through the year 1971 to 2011 according to the Moore's Law as guidance.

The fabrication simulation process will be done by using technology computer-aided design (TCAD) simulator, consisting of a process simulator, ATHENA and device simulator, ATLAS. In this simulation, the fundamentals of metal oxide semiconductor chip fabrication will be discussed, and the major steps of the process flow will be examined. This simulation shows that there are very strong links between the fabrication process and the device performance. The major challenge in designing the MOSFET device is reducing the short channel effect due to the size of the transistor is shrinking every year. Short channel effects are also known as SCEs may contribute on high leakage current ($I_{OFF}$) which can make transistor experience power losses even in 'OFF'

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condition. There is another factor of SCEs which was known as drain induced barrier lowering (DIBL). DIBL will cause the threshold voltage to decrease when the drain voltage increases thus increasing the sub-threshold slope (SS). This effect will actually contribute on the increment of leakage current ($I_{OFF}$).

Multi gate FET in fully depleted mode activity permits superior control over short channel effect rather than one gate fully depleted FET. This is due to close coupling of capacitor of multiple gates to transistor channel area from different direction. Basic of electrostatic activity of multi gate FET is alike. Control of gate become strong as number of gate increase such as single to double to triple gate to all around gate FET as virtue of raised coupling. Double gate FET could be assumed as improved form of fully depleted SOI device with extremely narrow buried oxide "as thick as gate oxide". Next, only body is highly doped with electrically connect to gate. As, there has no capacitive voltage distribution betwixt upper and lower gate, that is both gate control substrate jointly, gate to body coupling is precise and sub threshold swing is 55 mV/dec for ideal device. Additionally, "short channel effect" (SCE) control is extremely fine as virtue of narrow fully depleted substrate and gate is shield of drain electrostatic from either side. Because of multiple gates, now transistor can scale down to smaller gate length for identical body (and "oxide thickness"). As multiple gates and thin substrate are enough to reduce SCE, so substrate kept undoped. Which enhance channel charge carrier movement since it improved mobility due to less ionized impurity scattering and smaller vertical electrostatics. Additionally, undoped substrate is highly protected from discrete doping fluctuations effect. In triple gate and all around gate FETs device, crystal orientation effect can plays significant part, as charge carrier arise along different orientation.

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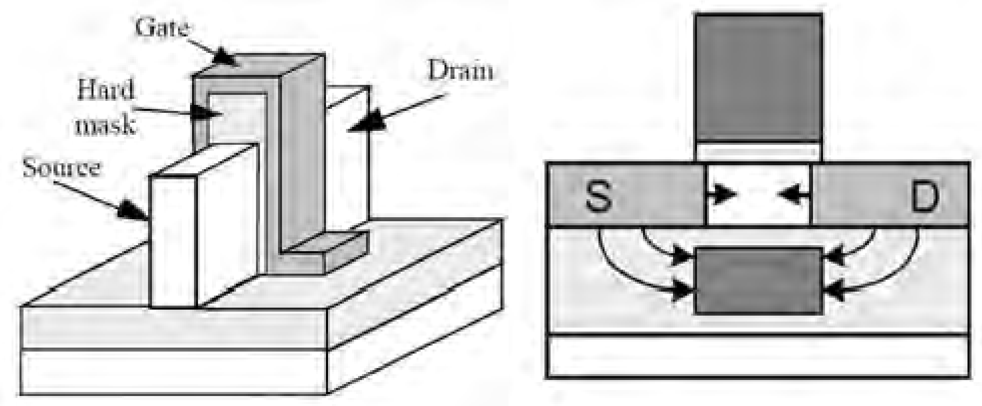


Figure 1.2 **:** Double gate FinFETs in 2D and 3D

The aid of TCAD tools was used and the researchers can explore the next transistor concept without do the real fabrication process to test the feasibility feature of transistors. It shortens the product development time. This research work will focus on the simulation and characterization of 16nm Double Gate FinFET by using Silvaco TCAD Tools

## 1.2 Problem Statement

The size of integrated devices such as PC mobiles are reducing day by day with multiple operations, all of these is happening because of the scaling down the size of MOSFETs which is the main component in memory, processors and so on [1]. As we scale down the MOSFETs to the nanometer regime the short channel effects arise which degrades the system performance and reliability. Therefore, FinFET will be designed in 16nm technology. The performance of the transistor must be improves to continue the Moore‟s Law [2]. Miniaturization of transistor through scaling process may degrade the performance of the devices. Meaning that, the reduction of channel length into the nanometer regime can reduce the key device parameters of a transistor such as carrier mobility and transconductance. Therefore, alternative structure such as Double Gate FinFET is believed to solve the scaling problems especially on the device short channel performance and scalability of nanoscale.

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## 1.3 Objectives of Study

The main goal of this research is to obtain the physical and electrical properties of FinFet Double-gate MOSFET device and also to design, analyze and optimize the devices according to the International Technology Roadmap Semiconductor (ITRS). Specifically, the objectives of study are:

i) To analyze the performance characteristic of a FinFET device.
ii) To design 16nm Double-Gate FinFET by using Silvaco TCAD tools.

## 1.4 Scope of Study

This project studied the design and optimization of Double Gate FinFET. Several scopes of work have been determined to provide guidelines for research limitations. This research project is based on the simulation and programming development. This scope of this project is to design 16nm Double-Gate FinFET device and analyze the performance using Silvaco TCAD tools. Design and fabrication of silicon MOSFET will be done using Silvaco's ATHENA software while device simulation (characterization) will be done by using ATLAS software. After the initial fabrication simulation, several experiments of designing FinFET Double-Gate MOSFET device will be carried out by altering several input process parameters. From the collected data, optimization of the input process parameters is implemented by using appropriate statistical analysis techniques. Each of every fabrication step and the order of fabrication steps are very important to ensure a proper FinFET Double-Gate MOSFET device is fabricated. Other than that, there is also some MOSFET characteristics that need to be studied in order to obtain the desired threshold voltage level ($V_{TH}$), drive current ($I_{ON}$), leakage current ($I_{OFF}$), and sub-threshold swing (SS).

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## 1.5 Report Structure

This thesis is a combination of five chapters that contain the introduction, literature review, methodology, result and discussion and the last chapter is conclusion and recommendation of the project.

Chapter 1 is an introduction to the project. The first chapter provides an introduction for this project. This includes the background, problem statement, objectives, and scopes. The second chapter contains literature review, theory and information about MOSFET, Double Gate FinFET, fabrication, and other relevant researches conducted by research institutes and universities around the world.

Chapter 3 will explain about the project methodologies of the project. This chapter will show the steps and flow for problem solving in such a specific method used to design and develop the MOSFET structure, also it also introduces the two modules of TCAD tool simulators, which is ATHENA and ATLAS module. Chapters 3 also discuss the step by step explanations for the development of the Double Gate FinFET device using Deckbuild and fabrication process using ATHENA. The characterization and optimization of Double Gate FinFET device will be discussed in detail in Chapter 4.

Chapter 4 shows the results that obtained from the process simulation of the device structure using the ATLAS tools. The data and results are then analyzed and optimized by using appropriate statistical modeling in this chapter. Analyses from threshold voltage, drive current, leakage current and subthreshold swing characteristics are also discussed throughout this chapter. Finally, Chapter 5 concludes the whole research and proposes the future progress for the project.

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# CHAPTER 2

# LITERATURE REVIEW

This chapter will discuss briefly about the theory and research from other researchers related to the project. The issue of short channel effect is discussed and several solutions involving advanced fabrication technique are performed.

## 2.1 Introduction

New applications and semiconductor devices have been proposed to suppress the prediction scaling of Moore‟s Law [3]. By downsizing the dimension of MOSFET, more transistors can be fabricated on each silicon wafer. Unfortunately, scaling down the size of MOSFET led to the limitations of a MOSFET. The limitation of MOSFET will be discussed further in the next section. Therefore, alternative method is needed to continue the scaling process. It is not possible if the functionality of new transistor is succeed, this transistor will trigger a phenomenon in electronic device industry and become a “next transistor”. The focus of the research is Double Gate FinFET.

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## 2.2 Shrinking Technology of MOSFET

Sixty years since the MOSFET was invented. During these years, integrated circuit (IC) has growth dynamically due to the scaling of MOSFET. In another meaning, scaling had been a fundamental driving force in MOSFET circuits[6]. Today, the scales of transistor reach into nanometer regime. It is reported in the article referenced[7] that in a single processor, there were billion numbers of transistors is packed for example Intel‟s processor, core i7 Extreme Edition. When size of MOSFET is shrinking, the distance between source and drain (channel length) is shortened. Therefore, the performance of the devices is improved. However, this phenomenon led to several issues that cause difficulties on fabrication process of semiconductor devices.

## 2.3 Scaling Issues

The growth of nanotechnology performance drives the scaling of transistor to the nanometer scale. Gate oxide thickness, tox and voltage supply is reduced for dynamic improvement in transistor performance and cost per function of transistors. From the theory of scaling, the higher the level of transistor miniaturization, the higher the packing density, the faster the speed as well as low power consumption. As MOSFET dimension is approaching beyond micrometer scale entering the nanometer scale regime (<100nm), there are some significant obstacle that must be look due to high gate leakage, high power dissipation and quantum well effects to achieved the desired performance [11] as shown in Figure 2.1.

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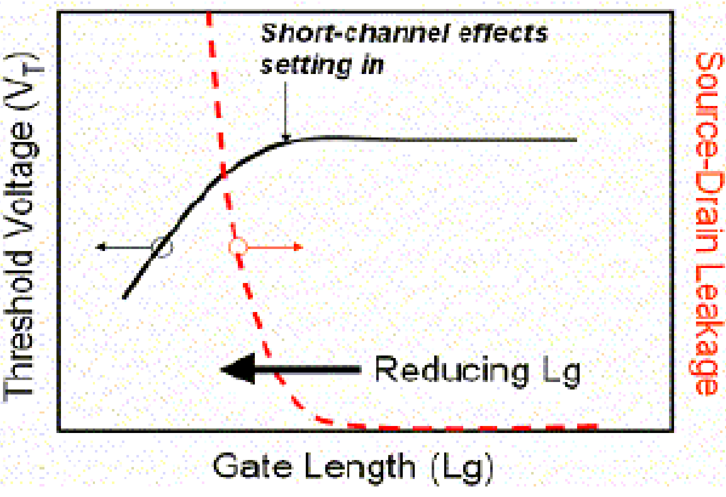


Figure 2.1: A plot of device gate length, is the function of VT and S-D Leakage.

Therefore, to extend the Moore's Law, innovation of device structure and modifications on fabrication process need to be discovered by the researchers. In addition, the rate of advancement in device performance can be preserve as well as overcoming the arise phenomenon known as "short channel effect" to inhibit the next progress in shrinking the transistor[12].

## 2.4 Short Channel Effects

MOSFET device is considered to be in short channel effects when there are some sharing of the electrical charge between the gate, source and drain. As the dimensions of the transistors shrunk and the channel length, L is reduced to increase both the operation speed and the number of components per chip, the ability of the gate electrode to control the potential distribution and flow of the channel region is also reduce. The source and drain junctions create depletion regions that penetrate the channel region from both sides of the gate, thus shortening the effective channel length [13]. According to [14], the gate oxide thickness and the gate-controlled junction or depletion depth in the silicon must be

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reduce in proportion to L (Gate Length). The Short Channel Effect (SCEs) effect the device and the performance of the circuit in many ways.

In particular, four different short-channel effects can be distinguished:

i) Drain-induced barrier lowering

ii) Punch-through

iii) Velocity saturation

iv) Hot electrons

### 2.4.1 Off-State Leakage Current ($I_{OFF}$)

In CMOS digital circuits this drive current is defined as the drain current of a MOS transistor with gate and drain connected to the supply voltage VDD, and source and bulk grounded. It is often referred to as "on-state current'" or simply "on-current" $I_{ON}$. The channel leakage current is defined as the drain current with drain connected to the supply voltage $V_{DD}$ and gate, source, and bulk grounded. It is often referred to as "off-state current" or simply "off-current" $I_{OFF}$. $I_{OFF}$ is one of the most essential device characteristics directly related to SCEs[15]. The stand-by power of a chip is determined by the combined $I_{OFF}$ of all the transistors, and it has to be minimized to integrate millions of transistors together. When designing a transistor, not only $I_{ON}$, but also $I_{OFF}$ should be optimized. The circuit delay, determined by $I_{ON}$, improves with constant E-field scaling.

On the other hand, $I_{OFF}$, which is mainly due to diffusion current, degrades (increases) with decreasing feature sizes. $I_{OFF}$ is one of the critical parameters that determines the scalability of a given technology. Other parameters such as $V_{TH}$ roll-off and DIBL indirectly contributes to the increment of the off-state leakage current. There is an inherent correlation between the drive and leakage currents which means that neither of them can be set completely independently from the other. This means if the drive current is increased by reducing the threshold voltage, the leakage current will

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usually become higher, too. Therefore, for the drive current optimizations performed in this work the leakage current will be kept below a certain limit while maximizing the drive current. The drive and leakage currents depend on several properties, namely the device geometry and the used materials, the contact resistances, the supply voltage, the temperature, and the doping profile.

### 2.4.2 Threshold Voltage Roll-Off ($V_{TH}$)

The threshold voltage is the minimum gate-to-source voltage differential that is needed to create a conducting path between the sources and drain terminals. The decrease of threshold voltage with decrease in gate length is a well-known short channel effect called the "threshold voltage roll-off". As the channel of the device is reduced to nano-scale region, the charge distribution in the channel is influenced by the field originating from the source/drain. When the threshold voltage decrease too much, the off-state leakage current become too large and the channel length is not acceptable. The critical geometry parameters which determine device short-channel behaviours spatially threshold voltage roll-off are gate length, fin thickness, fin height, oxide thickness and channel doping. Figure 2.2 illustrated the $V_{TH}$ vs. Gate Length.

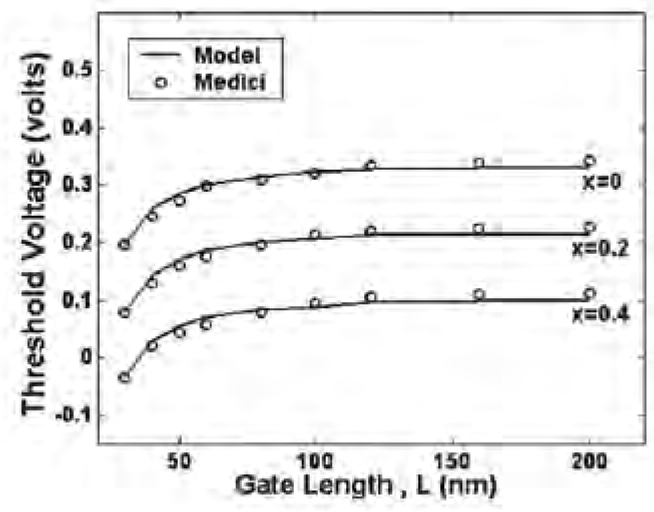


Figure 2.2: Threshold Voltage ($V_{TH}$) vs. Gate Length (L)

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### 2.4.3 Leakage Current

The problem when shrunken transistors to the point where the channel lengths are so short, that a significant amount of current leaks through the source-drain channel $I_{OFF}$, even when the transistor switch is in the off position. As temperature increased, the sub-threshold leakage increases exponentially because of a drop in the threshold voltage. Current also leaks from the base node through the oxide and channel and into the underlying substrate. Process geometries have shrunk even further, another leakage effect is band-to-band tunneling where the source/drain junctions reverse bias to allow electrons to tunnel their way into the substrate. All three sources of leakage have become a huge problem, and the process technology is working to come up with new materials and transistor designs that reduce the leakage. To reduce these unwanted current, several things can be done. $I_{OFF}$ can be reduced by increasing the threshold voltage. $I_{JUNC}$ can be reduced by low damage junction engineering while $I_{GATE}$ can be reduced by increasing the gate oxide thickness. Each technique to reduced unwanted current can cause other short channel effect, so the designer must scale appropriately to get an optimized device.

### 2.4.4 Sub-threshold Current

Weak inversion or subthreshold current between source and drain in MOSFET occur when the gate voltage, $V_{GS}$ is below threshold voltage, $V_{TH}$. Weak inversion current typically dominates the off-state leakage current, $I_{OFF}$ due to low $V_{TH}$[17]. As voltages has been scaled down with transistor size, the subthreshold conduction has become a bigger factor. Based on the research by, the subtreshold drain current increase as channel length decrease due to the leakage. The research also shows that the subthreshold leakage could be reduce by decreasing the effective gate oxide thickness. Figure 2.4 show the example of Subthreshold Slope (SS) vs. Gate Length (Lg).

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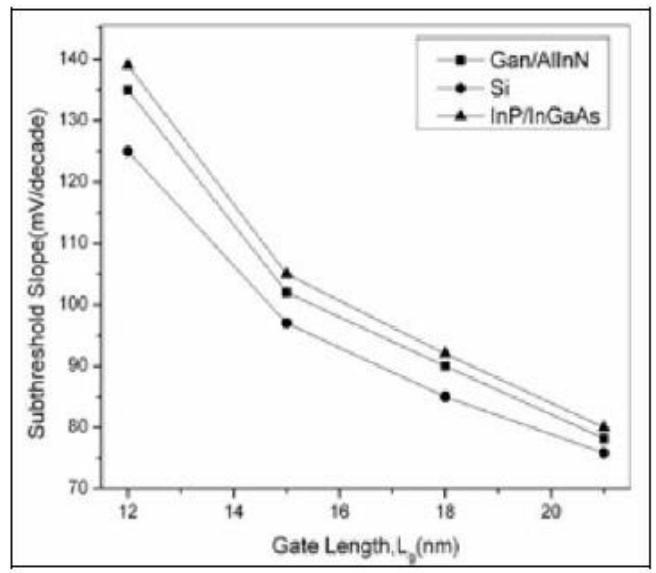


Figure 2.4: Example of Subthreshold Slope (SS) vs. Gate Length (Lg)

## 2.5 Multi-gate Structure : The FinFET Technology

Multi-gate structures had become compromising building blocks structure for an advance technology node of MOSFET. Multigate devices or knows as Multiple gate field-effect transistor (FET) is a structure that have more than one gate in a MOSFET[18]. Various type of multiple FET has been proposed by the CMOS innovator to boost the development of MOSFET ancestry. They were classified based on the number of gates and device architecture either planar or non-planar. Non-planar technology use metal gates while non-planar use the oxide with minimal variation in oxide thickness[19]. Examples of multi-gate MOSFET are double gate, triple gate and cylindrical gate all around (GAA) MOSFET.

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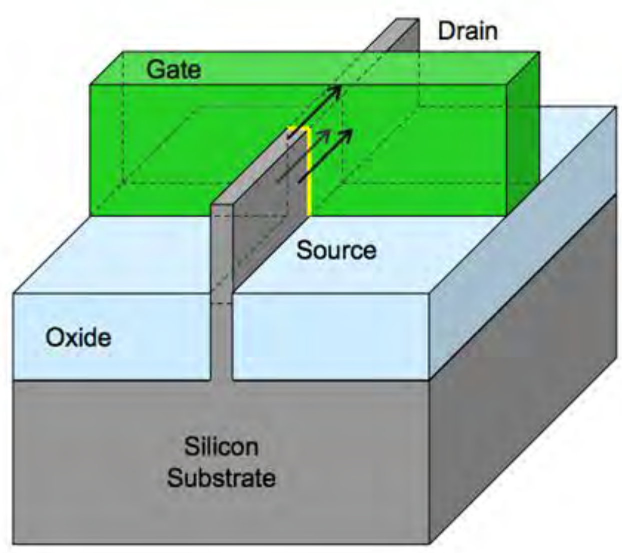


Figure 2.5: The structure of quasi-planar FinFET where gate cover the conducting channel between source and drain in perpendicular direction. Silicon substrate is used as base in this design of FinFET.

FinFET structure had ability to improve the subthreshold performance by overlapping top and side of gate electric fields at the corner of. It also suppresses the corner effect. In addition, corner effect can be reduced by make an oval shape at the corner. As shown in figure 2.5, Tri-gate FinFET was fabricated by wrapping around the 'fin' (channel) by three sides of gate [22]. Therefore, the length of channel has potential to be scaled down in order to continue the growth of Moore's Law. Previous novel has demonstrated the simulation by reducing the width of channel, as a results, short channel effect can be suppressed.

### 2.5.1 FinFET Fin Body Variations

FinFETs employ a fin-shaped body perpendicular to the wafer surface to carry the current. The fin is surrounded by the front and back gates or by a single gate and is made very thin to geometrically restrict the short channel effect. This structural characteristic ensures that the FinFET maintains the proper width, height, and quantity

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of fins in order to operate effectively. Based on research conducted by the fin body thickness (Tsi) of the FinFET has a substantial effect on the device leakage, threshold voltage, and on-current variations. The dimensions of the fin determines the effective channel length and gate width of the device been used. FinFETs comes from the constant fin height constraint the width of the FinFET device can be defined as :

$$W = 2Hfin + Tfin$$

where Hfin and Tfin are the fin height and thickness respectively.

The fin shape also has a considerable impact on leakage performance. Based on the research conducted by, the fin could be rectangular, trapezoidal or even triangular. Controlling the shape provide an effective way to increase the FinFET performance. The narrower the fin shape, the lower the leakage current in expense of drive current trade off. However, the fin shape design only possible in 3D design and due to the perspective limitations of the 2D design, the fin shape is neglected is 2D design. Figure 2.6 show the 2D vs. 3D design of FinFET.

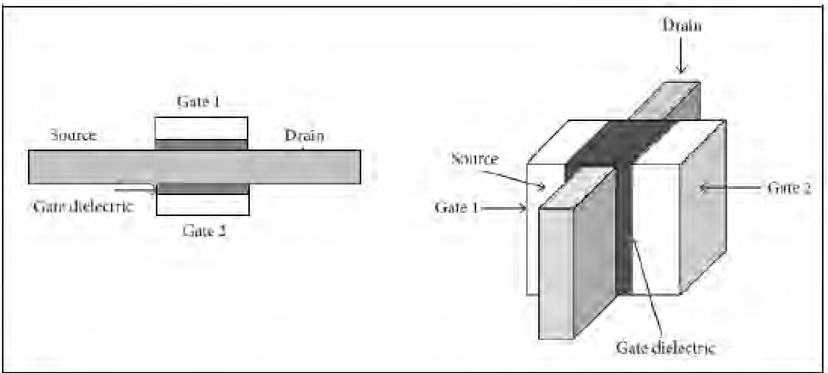


Figure 2.6: 2D vs. 3D design of FinFET

### 2.5.2 Effect of Fin-Height on Double Gate FinFET

The mobility was enhanced in devices with taller fins due to increased tensile stress. However, as gate length $L_G$ decreases, Ion for devices with tall fins becomes worse, probably due to a high parasitic resistance Rp. Furthermore, $V_{TH}$ variation increased with increasing Hfin due to rough etching of the fin sidewall. Process

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technologies for reducing Rp and etching technology that yields smooth precise profiles are essential to exploit the high performance of tall FinFETs. Mobility was enhanced in the tall-fin devices due to increased tensile stress. However, as $L_G$ was decreased, $I_{ON}$ became worse with taller fins, probably due to a high Rsp. It can be considered that both high mobility and suppressed next are crucial for achieving a higher Ion in the short-channel regime. It was also confirmed that the $V_{TH}$ variation increased with increasing Hfin due to rough etching of the fin sidewalls. Therefore, the bulk-FinFET, carefully fabricated by the novel process integration technology, may be a promising solution for low-cost SoC applications in the near future.

## 2.6 High-K Dielectric Material

The smaller MOSFET device requires an increased capacitance gate dielectric to control the short channel effects. This can be achieved by reducing the gate oxide thickness (EOT). But, the reduction of EOT leads to the increase of gate leakage which eventually decreases the drive current ($I_{ON}$). For below 2nm thickness, the leakage is unacceptably high when $SiO_2$ is used as a gate dielectric material. Therefore, the high-K dielectrics have been widely used as a gate dielectric material to replace the $SiO_2$ in current MOSFET's technologies due to their high dielectric constants. The dielectric layers with higher electrical permittivity are used in thicker films to reduce the leakage current and improve upon the reliability of the gate dielectric layer with electrical thickness equal to ultra-thin $SiO_2$ layer.

However, replacing the $SiO_2$ with a material having a different dielectric constant is not as simple as it may seem. The material bulk and interface properties must be comparable to those of silicone dioxide, which are remarkably good. For instance, thermodynamic stability with respect to silicon, stability under thermal conditions relevant to microelectronic fabrication, low diffusion coefficients, and thermal expansion match are quite critical. With these objectives in mind, recent research on high-k dielectrics has primarily focused on metal oxides and their silicates.

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## 2.7 Performance of Double Gate Over Single Gate

In this technology the transistor with a gate controlled bulk current using either an n-type or p-type substratefor the complementary transistor types are used. Such Double Gate MOSFETs rely on majority carrier flow through the bulk of the source drain silicon passage. The carrier concentration in the central part of this passage, called 'slit' is contrilled by the potentials of two gates (G1 and G2). In other words, change of the bias of the gate junctions result in variations of penetration of the depletion layers into substrate and modulate resistance of the channel.

As per the International Technology Roadmap for Semiconductor (ITRS), the gate length technology will scale down 16-nm by 2015. Single metal gate MOSFETs fails to meet the perpetual growing requirements. There are some potential solutions to overcome the limitations of transistors scaling such as initiation of promising structures, which improve gate controllability onthe channel. Therefore, multiple gate MOSFET shave evolved as the leading contenders to replace the planar single gate MOSFET, namely vertical MOSFET, multigates such as FinFET, double gate, tri-gate, omega gate, surrounding gate-all-around (GAA) where as new materials are carbon nano tube, high-k dielectric, strain silicon and metal gate. In particular, attention is keyed on multiple-gate MOSFETs because of their low body-effect coefficient and steep sub-threshold slope. Figure 2.7 show the different between single gate and double gate structure.

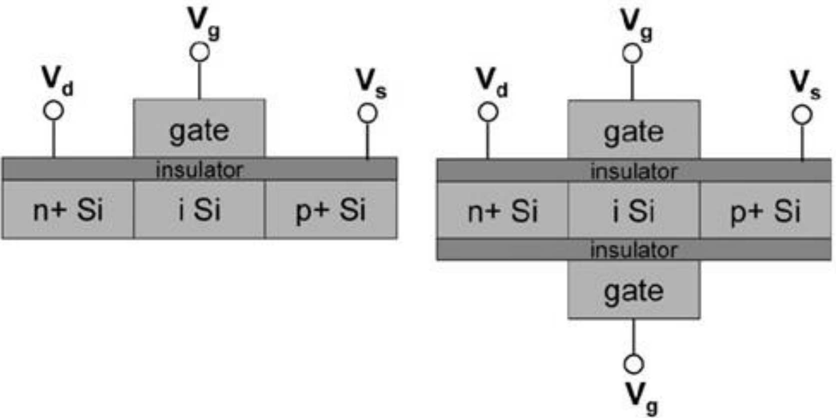


Figure 2.7: Single Gate and and Double Gate

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## 2.8 SUMMARY

As the MOSFET devices continue to downscale with improved device performance and lower power, challenges rises for designers and manufacturers to keep pace with the technological trend. This thesis focused on the issues related to the process variations in the CMOS technology. The aim of this research has been to analyse the impact of the process variations and find ways to minimize the effects.

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# CHAPTER 3

# METHODOLOGY

This chapter discusses the methodology that is used in this project. The next section will discuss the experiments and analysis of results in order to investigate the device performance. A comparison between single gate and double gate performance is also addressed.

## 3.1 Introduction

This chapter focuses on the FinFET transistor simulation design which is done by using Silvaco TCAD tools, that is ATHENA and ATLAS. Simulation of the device fabrication is done by ATHENA module while the simulation of the electrical characteristic is done by ATLAS module. Therefore, the performance of the device can be measured accurately and precisely before go to the actual fabrication process. The information use to design the FinFET are done by reviewing through white papers, technical papers, conference's proceedings, product data sheets, web pages, thesis, publications and also groups of the project. The process flow of the project as the Figure 3.1 must be follow to complete the project.

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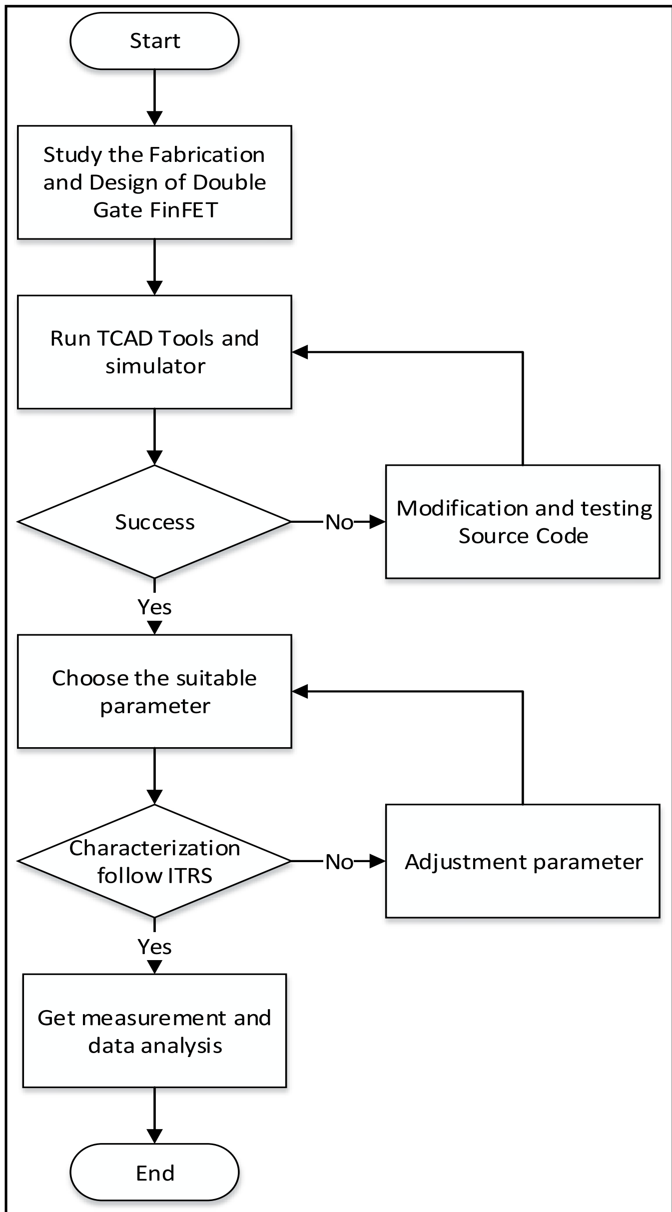


Figure 3.1: Process flow of the project

The explanation on identification of process parameter and analysis of data which involve the optimization approach are also covered in their respective Chapter 4.

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