HARMONIC MINIMIZATION OF A SINGLE PHASE CASCADED H-BRIDGE MULTILEVEL INVERTER

MUHAMMAD SYAHIR AFIF BIN ABDUL RAHMAN

BACHELOR OF ELECTRICAL ENGINEERING
(INDUSTRIAL POWER)

UNIVERSITI TEKNIKAL MALAYSIA MELAKA

DECLARATION

I declare that this thesis entitled "**HARMONICS MINIMIZATION OF A SINGLE PHASE CASCADED H-BRIDGE MULTILEVEL INVERTER**" is the result of my own research except as cited in the references.

Signature: .....

Name : Muhammad Syahir Afif Bin Abdul Rahman

Date : 15 June 2017

APPROVAL

I hereby declare that I have read through this thesis and found that is comply the partial fulfillment for awarding the degree of Bachelor of Electrical Engineering (Industrial Power)

Signature : ……..…….....

Name : Prof. Madya. Ir. Dr. Rosli Bin Omar

Date : 15 June 2017

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ABSTRACT

This project represent the research of harmonic minimization of a single phase cascaded H-bridge multilevel inverter (CHB-MLI). Multilevel inverter is used to combine a desired single or three-phase voltage waveform and also to minimize the harmonics in the electrical system. This project use cascaded H-bridge (CHB) topology due to least number of components use, output voltage level are doubled, and easy to controllled compared with diode clamp (DC) and flying capacitor (FC) topology. This research use three and five levels cascaded H-bridge multilevel inverter based on Newton-Raphson technique controller by using MATLAB/SIMULINK in order to reduce the harmonic in electrical system. The value of total harmonic distortion (THD) has been obtained based on the simulation design of three and five levels CHB-MLI.

Next, prototypes of single phase three and five level CHB-MLI based on Newton-Raphson technique controller using DSPTMS320F2812 has been analyzed. The parameter based on simulation has been used in order to analyze the proposed prototypes of CHB-MLI. The source codes has been created and embedded into DSPTMS320F2812 in order to operate the prototypes of CHB-MLI. The modulation index that has been used in this research were 0.84 for optimization and 0.68 for non-optimization. Based on this research, the output voltage of total harmonic distortion (THD_V) and output current of total harmonic distortion (THDi) content in the CHB-MLI has been analyzed. The performance of the proposed system was compared between the simulation and experimental results for optimization and non-optimization technique. Furthermore, the simulation and experimental results demonstrate which one of the proposed CHB-MLI has better performance in minimizing the harmonics contents. The waveforms of output voltage and current were smooth and low harmonic contents which suitable to be used in photovoltaic (PV) application.

ABSTRAK

Projek ini membentangkan kajian tentang pengurangan harmonik satu fasa penyongsang bertingkat cascaded H-bridge (CHB-MLI). Penyongsang bertingkat digunakan untuk menggabungkan satu atau tiga fasa gelombang voltan yang dikehendaki dan juga untuk mengurangkan harmonik dalam sistem elektrik. Projek ini menggunakan cascaded H-bridge (CHB) kerana bilangan komponen yang digunakan adalah sedikit, tahap voltan output adalah dua kali ganda, dan mudah untuk dikawal berbanding kapasitor terbang (FC) dan diod diapit (DC) topologi. Kajian ini menggunakan tiga dan lima tingkat penongsang bertingkat cascaded H-bridge berdasarkan kawalan teknik Newton-Raphson dengan menggunakan MATLAB/SIMULINK bertujuan untuk mengurangkan harmonik dalam sistem elektrik. Nilai jumlah herotan harmonic (THD) telah diperolehi berdasarkan reka bentuk simulasi tiga dan lima tingkat CHB-MLI.

Seterusnya, prototaip satu fasa tiga dan lima tingkat CHB-MLI berdasarkan kawalan Newton-Raphson teknik menggunakan DSPTMS320F2812 telah dianalisis. Parameter berdasarkan simulasi telah digunakan bertujuan untuk menganalisis prototaip CHB-MLI. Kod sumber telah dicipta dan ditanam ke dalam DSPTMS320F2812 untuk menjalankan prototaip CHB-MLI. Indeks modulasi yang telah digunakan dalam kajian ini ialah 0.84 untuk pengoptimuman dan 0.68 untuk bukan pengoptimuman Berdasarkan kajian ini, voltan keluaran jumlah herotan harmonik (THD_v) dan arus keluaran jumlah herotan harmonik (THDi) dalam CHB-MLI telah dianalisis. Prestasi sistem yang dicadangkan telah dibandingkan antara simulasi dan keputusan eksperimen untuk teknik pengoptimuman dan bukan pengoptimuman. Tambahan pula, keputusan simulasi dan eksperimen menunjukkan CHB-MLI yang dicadangkan yang mana satu mempunyai prestasi yang lebih baik dalam mengurangkan kandungan harmonik. Bentuk gelombang voltan dan arus keluaran adalah licin dan rendah kandungan harmonik yang sesuai untuk digunakan dalam aplikasi photovoltaic (PV).

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CHAPTER 1

INTRODUCTION

1.1 Project Background

In this chapter, a single-phase Cascaded H-bridge Multilevel Inverter (CHB-MLI) has been used to alternating current (AC) voltage waveform of the inverter output. For the ordinary inverter, the process of energy conversion is to convert Direct Current (DC) to Alternating Current (AC) [1]. The function of inverter is opposite the function of rectifier. The upgrade of inverter that nowadays used is called multilevel inverters. Multilevel inverter have more advantages compared to ordinary inverter. Multilevel inverters was invented with many levels that show the highest level give the best output. The main function for the multilevel inverter is to combine the desired output voltage waveform from several steps of voltage. There are three types of multilevel inverters topology that commonly used such as Cascaded H-Bridge Multilevel Inverter (CHB-MLI), Diode Clamp Multilevel Inverters (DC-MLI), and Flying Capacitor Multilevel Inverters (FC-MLI). This project use CHB-MLI in order to reduce harmonic because it easy to control and also the output voltages level are doubled the number of sources.

In this project, Cascaded H-bridge multilevel inverter (CHB-MLI) has been used to provide a sinusoidal output voltage. In single phase CHB-MLI, it uses several H-bridge inverters connected in series which each phase is connected to single dc source. Each level generates three voltage outputs which are positive, negative and zero [2]. The inverter will remain ON when two switches with the opposite positions will remain ON. When all the inverters switch ON or OFF, the inverter will turn OFF. Based on the Figure 1, when the S1 and S4 is ON, the inverter will ON. Same with when S2 and S3 is ON, inverter will ON. Inverter will OFF when S1, S2, S3 and S4 is ON or OFF.

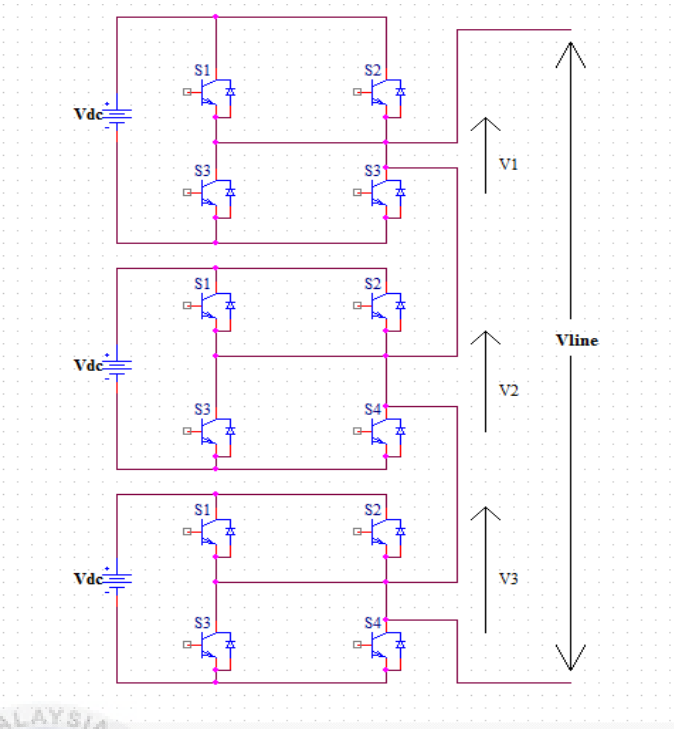

Figure 1.1: Single phase Cascaded H-bridge Multilevel Inverter

1.2 Problem Statement

Cascaded H-bridge multilevel inverter (CHB-MLI) is based on the series connection of the power cell and several H-bridge inverters to provide a sinusoidal output voltage. The main problem that always occurs in power electronics device is the harmonic content. In order to minimize the harmonic distortion, the switching angle has been used in the CHB-MLI for controlling the output voltage and current [3]. The major target is to decrease the total harmonic distortion (THD) in electronic devices. THD is the summation of all harmonic components of the voltage or current waveform that measured in a percentage. The higher the percentage of output voltage THD, the higher distortion that is present on the mains signal [4].

There are some control technique methods frequently used which are pulse width modulation (PWM), selective harmonic elimination (SHE), space vector pulse width modulation (SVPWM), and sinusoidal pulse width modulation (SPWM). The types of controllers cannot totally remove the harmonics because they cannot be applied in multilevel inverter with differing DC voltages. Thus, Newton-Raphson technique controller is the most suitable control technique in order to reduce the harmonic using CHB-MLI.

1.3 Objectives

The objective of this project are:

1) To study types of multilevel inverter topologies that mainly used to minimize harmonic distortion.
2) To investigate the harmonic minimization of optimization and non-optimization three-level and five-level single-phase Cascaded H-bridge Multilevel Inverter (CHB-MLI) by using MATLAB/SIMULINK.
3) To analyse a prototype of a single phase cascaded H-bridge multilevel inverter (CHB-MLI) based on Newton Raphson technique controller using DSP TMS320F2812.
4) To compare the differences of THD between simulation and hardware of three level and five level CHB-MLI.

1.4 Project Scope

Based on this research, there are three main types of multilevel inverter topologies which are Neutral Point Clamped (NPC), Flying Capacitor (FC) and Cascaded H-bridge (CHB). The main focus in this project is to simulate the proposed model and also to analyse the THD content of a single phase cascaded H-bridge multilevel inverter (CHB-MLI). Next, this project scope is also to analyse a prototype of a single phase CHB-MLI based on Newton Raphson technique controller using DSP TMS320F2812. The parameter from simulation will be used to analyze a prototype of a single phase cascaded H-bridge using DSP TMS320F2812 and the coding will be created using C++ programming. The proposed coding will be embedded with DSP TMS320F2812 in order to carry out the inverter.

1.5 Expected Project Outcome

In this study, this project propose is to minimize harmonic using three phase and five level cascaded H-bridge multilevel inverter (CHB-MLI) prototype based on simulation circuit design. Meanwhile, the prototype of a single phase CHB-MLI has been used in order to analyse the THD value. The comparison of THD between three level and five level CHB-MLI has been done to know which output level of multilevel inverter is better to reduce the harmonics.

CHAPTER 2

LITREATURE REVIEW

2.1 Introduction

In this study, a single phase cascaded H-bridge multilevel inverter (CHB-MLI) has been used to produce alternating current (AC) voltage waveform of the inverter output. There are three types of multilevel inverter topologies which are Diode Clamp (DC), Flying Capacitor (FC), and Cascaded H-Bridge (CHB) multilevel inverter. There are three types of inverter output waveform that commonly utilized which are square wave, modified sine wave and sine wave. Therefore, this study is to minimize the harmonic of a single phase cascaded H-bridge multilevel inverter by analysing its regulated output voltage.

2.2 The Concept of Inverter

Inverter are a device or electronic component which is provides AC load voltage from a DC voltage source. There are many types of semi-conductor switching that can be used to control the operation of the inverter such as bipolar junction transistor (BJT), metal oxide semiconductor field effect transistor (MOSFET), insulated-gate bipolar transistor (IGBT) and gate turn off thyristor (GTO). A single phase inverter usually contain two or four switches that consist in half-bridge or full-bridge topologies [1].

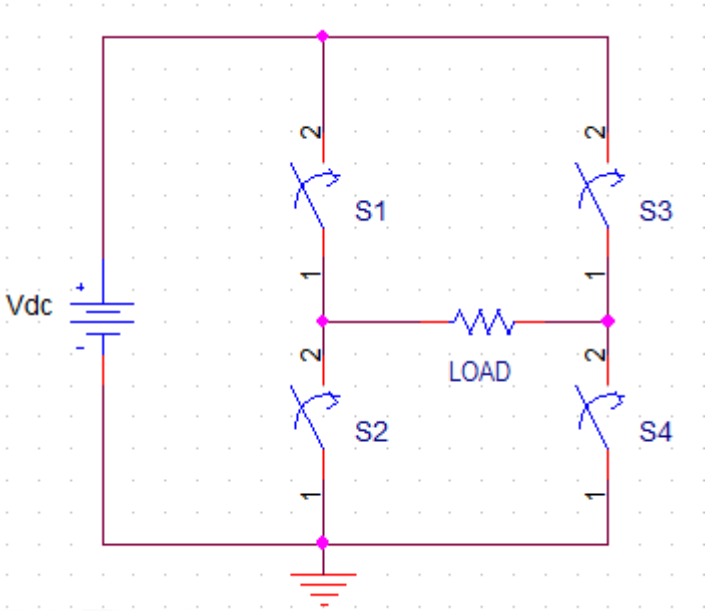

Figure 2.1: Basic connection of cascaded H-bridge inverter

Based on figure 2.1, the voltage source supply is a DC source which is 240Vdc. The purpose of DC/AC power inverter is to convert the DC power supplied to AC power supplied which is usually operate at frequency from 50Hz to 60Hz. Each switches has its own function which is to turn ON or to turn OFF the inverter.

In order to reduce the harmonic, pulse-width modulation (PWM) methods can be used which is the process of adjusting the width of the pulses directly proportional to small control signal. The higher the voltage control, the more extensive the producing pulse become [5]. The primary objective in PWM scheme which is to calculate the converter switch ON times and create low frequency target of output voltage current. The secondary objective is to identify the most productive way of organizing the switching processes to reduce unnecessary harmonic distortion, switching losses, or any other specified performance criterion [6].

2.2.1 Types of Inverter Output Waveform

There are three types of inverter output waveform that commonly used which are square wave, modified sine wave, and sine wave. Firstly, the square wave usually be the output waveform for the AC load voltage of the inverter as shown in the figure 2.2. The only advantages of square wave are can work with ordinary light bulb and the cost used is cheap. The square wave attempt to cause many problems for motors which is increase the motor power loss and caused reduction of efficiency in the motor [7]. Therefore, the square waveform has a very high harmonic content that form noise in electronic device particularly in audio device such as microphone or speaker [8].

The modified sine wave or also known as quasi-sine wave that show the enhancement over the square wave as shown in figure 2.2. The modified sine wave is quite similar to a square wave because it has "stepping" looks but different in the shape that more relates to the sine wave [8]. The quasi-sine wave have high power efficiency, and actually are suitable used for running some types of motors and incandescent lighting. The peak output voltage varies with the battery voltage is the main problems or disadvantages of quasi-sine wave which can produce harmonic [9].

Sine wave can be created by clarify more switching schemes and added circuitry that cause the cycle divided into smaller segments and creating a stepped voltage function that approximately looks like sine wave. Sine wave is a sinusoidal waveform as in figure 2.2 which is a better wave compared to square wave and modified sine wave. The advantages of sine wave is it has a very low harmonic distortion and high power efficiency. By using pulse width modulation (PWM) approached, the voltage and current pulses of varying width was created. The changing period of the pulse has the same result as a differing voltage magnitude. Therefore, pulse width modulation (PWM) definitely show a signal of changing magnitude. Thus, the harmonic content is minimize due to modification of square wave to sine wave using PWM approach. [8],[10]

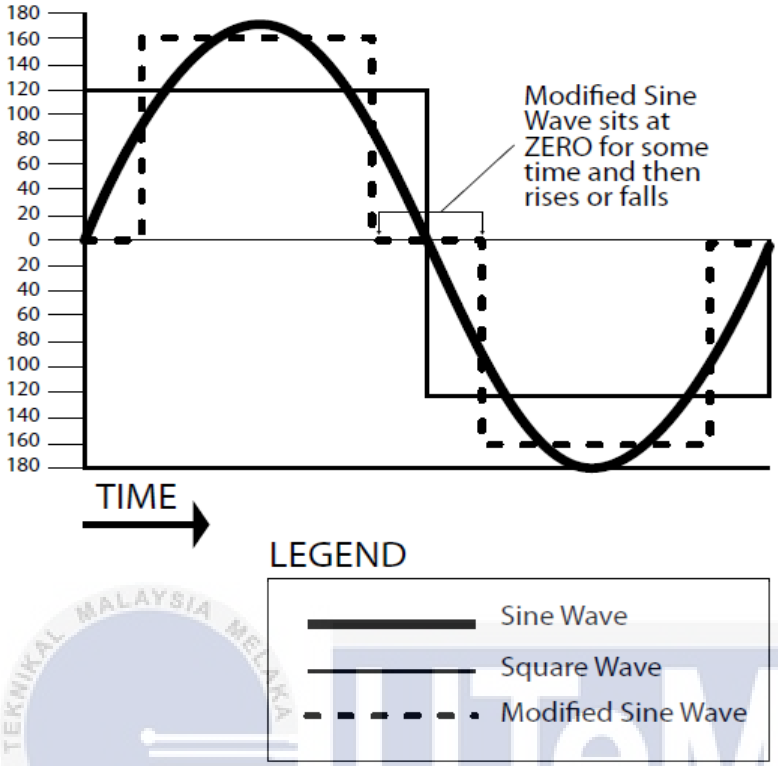

Figure 2.2: Inverter output waveforms [10]

2.3 The Concept of Multilevel Inverter

Multilevel inverter mainly apply to combine a desired single or three-phase voltage waveform. By combining a few dc voltage sources, the desired multi-staircase output voltage can be acquired. There are three types of multilevel inverter topologies that commonly used nowadays which are neutral point clamp (NPC) or diode clamp (DC), cascaded H-bridge (CH), and flying capacitor (FCs). Cascaded H-bridge multilevel inverter has the higher output voltage and power levels (13.8k, 30MVA) compared to the other two topologies. Furthermore, cascaded multilevel inverter also has higher dependability due to its modular topology [11].

2.3.1 Neutral Point Clamp Multilevel Inverter

The neutral point clamped topology or also known as diode clamped topology has it main advantage which is it requires a single DC source, and contributes better execution. This NPC topology disadvantages is when the level 'n' increase, the number of clamping diodes will increases [12]. Thus, the NPC topology is generally utilized for three-level inverter as shown in Figure 2.3. Based on the table 2.1, it display about the switching state for three-level neutral point clamped (NPC) multilevel inverter. The output voltage will become +0.5Vdc if the S1 and S2 at ON condition and another two switches which are S3 and S4 at OFF condition. There are no output voltage will came out if S2 and S3 at ON condition. To get –0.5Vdc output voltage, S3 and S4 at ON condition.

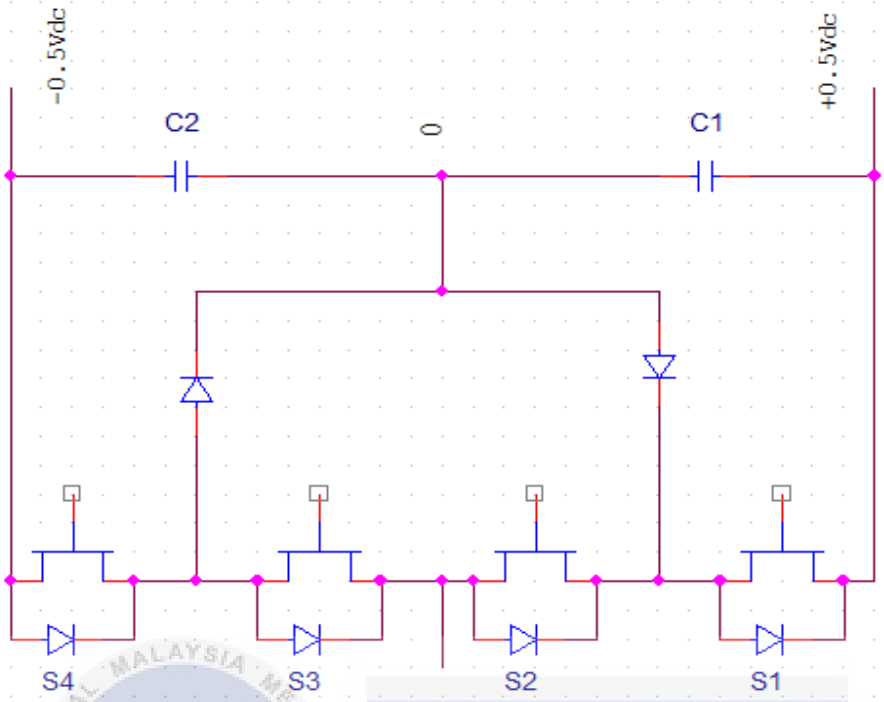

Figure 2.3: Three -level Neutral Point Clamped topology

S1	S2	S3	S4	V_o
1	1	0	0	+0.5Vdc
0	1	1	0	0
0	0	1	1	-0.5Vdc

Table 2.1: Table of switching state for three-level NPC topology

2.3.2 Flying Capacitor Multilevel Inverter

Flying capacitor topology also known as capacitor clamped topology which the voltage clipping is finished by utilizing capacitors floating with respect to the earth potential. Phase redundancies are available in order to balancing capacitors voltage levels. There is one main disadvantages for this topology which is it needs a large number of bulky capacitors that prevent the industrial use of this topology [12]. Flying capacitor topology generally utilized for 3-levels inverter as shown in figure 2.4. Table 2.2 show the switching state for 3-levels flying capacitor (FC) multilevel inverter.

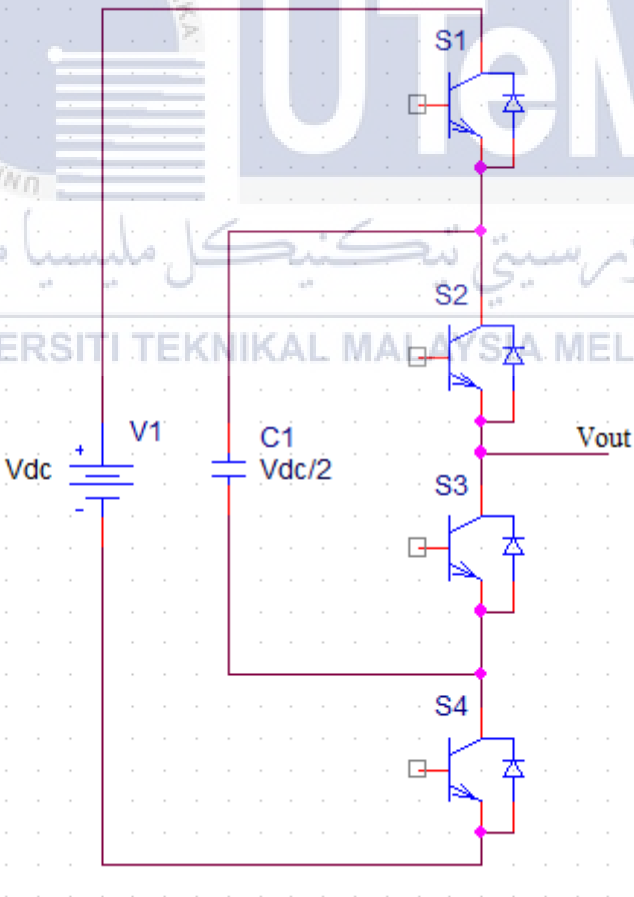

Figure 2.4: Three-level Flying Capacitor multilevel inverter

S1	S2	S3	S4	V_o
1	0	1	0	+0.5Vdc
0	1	1	0	0
0	1	0	1	-0.5Vdc

Table 2.2: Table of switching state for three-level FC multilevel inverter

2.3.3 Cascaded H-Bridge Multilevel Inverter

In cascaded H-bridge (CHB) topology, the H-bridges are cascaded in each phase. Thus, in order to get the output voltage waveform become more sinusoidal, the H-bridges should increase in each phase. There are many advantages of this topology compared to the other two topologies which are use least number of components, output voltage level are doubled, and easy to control. The main disadvantage of this topology is there must be a separate DC source for each H-bridge. The number of level which commonly used for this topology are 3-levels, 5-levels and 7-levels cascaded H-bridges. The higher the number of level used will produce lower content of harmonic distortion. The figure 2.5 show five-levels cascaded H-bridge multilevel inverter that contain 8 switching device to control.[2],[12] Table 2.3 show the switching state for five-level cascaded H-bridge multilevel inverter. There are five voltage output that can we get which are 0Vdc, +Vdc, +2Vdc, -Vdc and -2Vdc. The switching state as shown in table 2.3 should be apply to achieve all these five voltage output. The higher the level utilized, the higher the outputs voltage that will achieve.

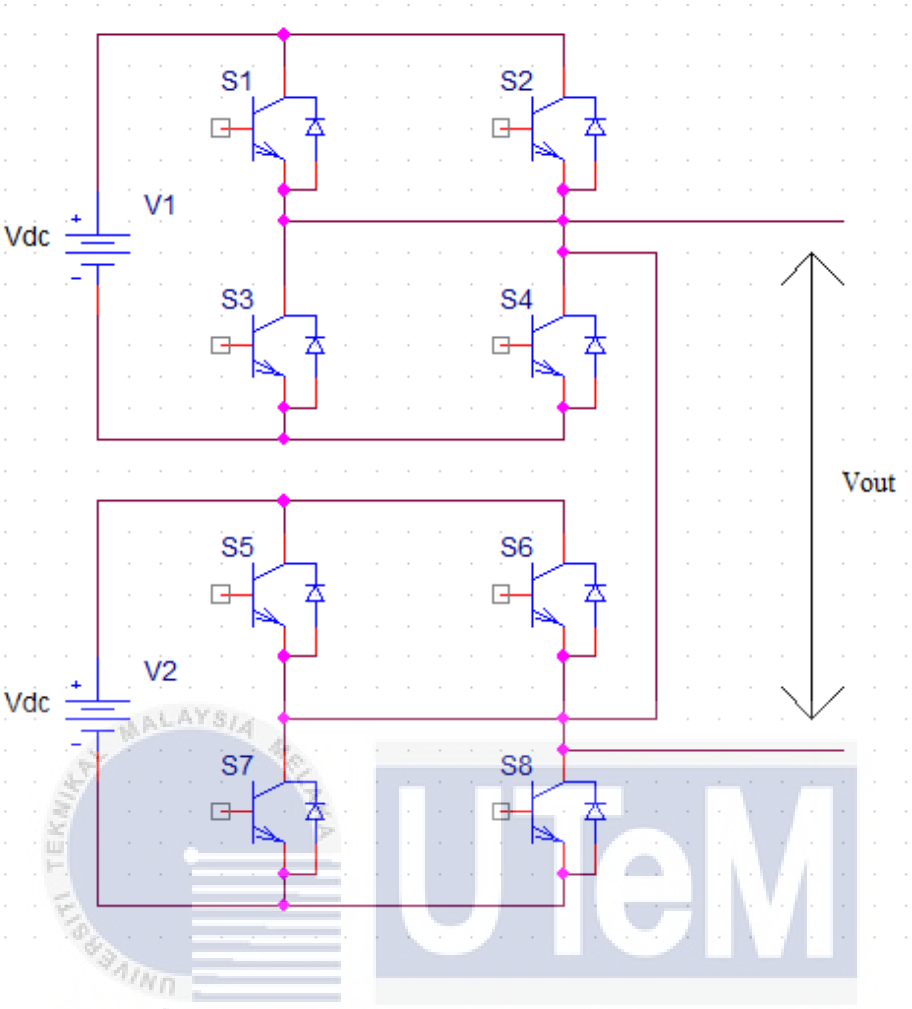

Figure 2.5: Five-level Cascaded H-Bridge multilevel inverter

Voltage (V_o)	S1	S2	S3	S4	S5	S6	S7	S8
0	0	1	0	1	1	0	1	0
+Vdc	1	0	0	1	0	1	0	1
+2Vdc	1	1	0	0	1	1	0	0
-Vdc	0	1	0	1	0	0	1	0
-2Vdc	0	0	1	1	0	0	1	1

Table 2.3: Table of switching state for five-level CHB multilevel inverter

2.4 Description of Harmonics

In electronic devices, the main problem that always occur which disturb the power quality of the electronic devices known as harmonic content. Harmonics can be defined as a sinusoidal component of a periodic wave which an integral multiple of the fundamental frequency which means the frequency of the harmonic are dissimilar, rely on the fundamental frequency [13]. Hence, if the fundamental frequency is 50 Hz, the frequency for the second harmonic will be 2×50 Hz or 100 Hz. The harmonic will continue increasing due to increasing of the harmonic order. Figure 2.5 represent the divided fundamental and harmonic waveforms that occur in an electronic device.

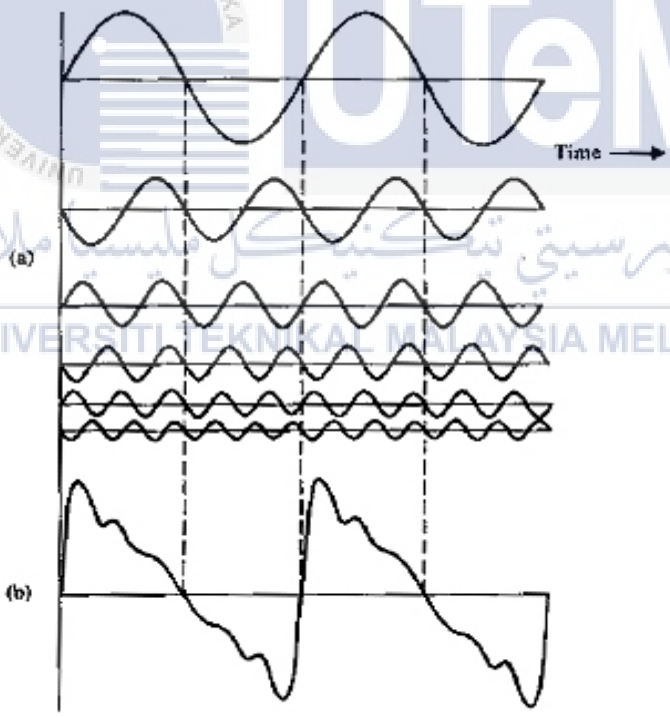

Figure 2.6: Divided fundamental and harmonic waveforms

2.4.1 Effect of Harmonics Distortion

Harmonic distortion will occur due to a source from a non-linear loads that implanted in the AC power motor or devices network. There are some effect of the harmonics distortion that will disturb the power quality of electronic devices one of it is increase the current in power systems which produces higher temperatures in the system. Besides that, the higher the frequency of harmonics can extremely shorten the life of electronic equipment and cause destruction to power systems. [4]

2.4.2 Harmonic Fundamental Equation

Harmonic can be determine from a non-linear loads supply voltage or current. The easier way to measure the harmonic is by finding non-linear loads current, I(t) as given in Equation (2.1):

$$I(t) = \sum_{n=1}^{\infty} I_x \sin(2\pi f x t + \Theta) \quad (2.1)$$

The total RMS and harmonic current can be measured by using Equation (2.2):

$$I = \sqrt[2]{\frac{1}{T}\int_0^T i(t)dt} \quad (2.2)$$

$$I_{\text{harmonic}} = \sqrt{\sum_{x=2}^{\infty} I_x^2}$$

Where, I_x is the fundamental current which used to calculate total harmonic current.

2.5 Control Techniques for Multilevel Inverter

There are many types of control techniques that can be applied for multilevel inverters such as Sinusoidal Pulse width Modulation (SPWM), Space Vector PWM (SVPWM), Selective Harmonic Elimination PWM (SHE-PWM) and Newton-Raphson technique that used to control and determine switching angles to obtain the wanted output voltage and removing the unwanted harmonics [14]. Each of these control techniques have their own advantages and methods of implementation to achieved the output voltage and reducing the harmonics.

2.5.1 Sinusoidal Pulse Width Modulation

One of the control technique that have been evolved to reduce the harmonic distortion which is classical SPWM with triangular carriers. In order to achieve the generation of desired output voltage, the desired reference waveform or also known as modulating signal have been compared with a high frequency triangular carrier wave. The modulating signal is the ratio of sinusoid of amplitude, Am and the amplitude of triangular carrier, Ac or also known as modulation index, m = Am/Ac. The amplitude of the applied output voltage can be controlled by controlling the modulation index. The fundamental wave can exceed the triangle wave by keeping m<1. If m>1, the carrier and the signal will not intersect. Therefore, the modulation index should less than 1 in order to smooth the sinusoidal PWM process.[15],[16]

2.5.2 Space Vector Pulse Width Modulation

Space vector PWM also one of the control technique that can be applied for multilevel inverters. This technique produce less harmonic content, and effective usage of DC bus compared with other modulation techniques. The output voltage and current used to the phases of an AC motor generates less harmonic and gives higher efficient use of supply voltage compared to SPWM control technique. SVPWM technique commonly used in three-phase source inverters because the six power semiconductor switches that shape the output have been used in this control technique. There are some advantages of SVPWM controller such as has better usage of DC-link, has lower current ripple, and digital signal processing (DSP) can be interfaced and executed easily. [17],[18]

2.5.3 Selective Harmonic Elimination Pulse Width Modulation

Selective harmonic PWM technique is presently utilized to combine an output waveform of multilevel inverters and commonly applied in three level inverter circuit. This technique can achieve three state of output voltage waveform which is zero, positive and negative. The amplitude of the output waveform can be control by adjusting the modulation index, m. The disadvantages of this control technique is the solution is a little bit complex because its condition has less degree of freedom [19]. The major concept of this controller technique is based on determining the switching angles of harmonic orders to remove and in achieve the Fourier series expansion of output voltage. The output voltage Fourier expansion using this controller technique can be written as Equation (2.3),

$$V(\omega t) = \frac{4}{n\pi} \sum_{n=1}^{\infty} [V1\cos(n\theta 1) + V2\cos(n\theta 2) + \dots] \quad (2.3)$$

2.5.4 Newton-Raphson Technique

The major function of Newton-Raphson (NR) technique controller are to compute the stepped switches angle and also to measure THD value. Besides that, this controller method also used to control the fundamental output voltage and to reduce the harmonics. Based on this controller technique, the switching angles can be calculated to generate the required fundamental voltage, V_1 [20]. The required fundamental voltage can be calculated using Equation (2.4):

$$V_1 = MI\ (4SVdc/\pi) \quad (2.4)$$

Where, Vdc is the magnitude voltage of each dc source, S is the number of dc source or H-bridges cells, and MI is the modulation index. Fourier transformation equation will be used if there is any non-sinusoidal periodic waveform occur. The Fourier transformation equation can be represent as Equation (2.5):

$$F(x) = A_0 + \sum_{n=1}^{\infty}(An\cos n\omega t + Bn\sin n\omega t) \quad (2.5)$$

The Newton-Raphson technique is suitable used to solved non- linear equation in order to calculate the initial switching angle of single phase or three phase multilevel inverter. The formula used to obtain the initial switching angle by applying Newton-Raphson method as indicated in Equation (2.6):

$$\alpha_i = i\,\frac{90}{K+0.6} \quad (2.6)$$

Where, i = 1, 2, 3, 4, 5….K, α_i is the initial value of switching angle, and K is the constant. The switching angle will be measured in degree unit. [21]

2.6 The Concept of DSPTMS320F2812

A Digital Signal Processing (DSP) is a particular device that manipulate digital data that are measured by signal sensor using the normal mathematical operations. The main function of DSP is to interface software and hardware in order to get the waveform of the output prototype [22]. This device is suitable used to run a single phase CHB-MLI by embedded the suitable source code programming. Based on portfolio of Texas Instruments, DSP has been divided by three major device families such as C2000, C5000 and C6000. The C6000 series has the highest performance compared to the other two series. The application fields that usually be applied for C6000 series are image processing, audio, multimedia server, and base station for wireless communication. For the C5000 series, the main focus is for mobile systems where it has a very efficient power consumption per MIPS.

For the C2000 series, it is suitable for real time control applications such as to control or run a multilevel inverter. There are three types of DSP in C2000 series that commonly used such as DSPTMS320F2810, DSPTMS320F2811 and DSPTMS320F2812. The better performance among these three types is DSPTMS320F2812 because it can support the highest bit of instruction where the higher performance produce greater integration [23]. The DSPTMS320F2812 suitable to run a multilevel inverter in order to minimize the harmonic where the DSP-based control circuit with RL loads should connect to multilevel inverter and a DC source where the output waveform will displayed using oscilloscope and the fluke meter utilized to measure percentage of THD in the system.

2.7 Summary of the Review

A literature review about multilevel inverters was included in this chapter to improve the understanding about this project objectives. The types of multilevel inverter has been include in this chapter to compare which topology is better. Based on this project, a single phase cascaded H-bridge multilevel inverter has been used to minimize the harmonic by applying several control techniques. Besides that, the concept of hardware component also has been presented in this chapter.

CHAPTER 3

RESEARCH METHODOLOGY

3.1 Introduction of the Methods Utilized

This chapter explain about the methodology for this project. The methodology begins with designing the simulation of three level and five level single phase cascaded H-Bridge multilevel inverter (CHB-MLI) by using MATLAB/SIMULINK. The basic CHB-MLI circuit consist of direct current (DC) voltage source, H-bridge including switches and diodes, and load. Based on the previous researcher, at least three voltage levels are needed for a multilevel inverter [24].

The analysis and study about the proposed prototypes of three level and five level single phase cascaded multilevel inverter (CHB-MLI) has been done in order to compare which one has lower total harmonic distortion (THD). The prototypes has been analyze based on Newton-Raphson technique controller using DSP TMS320F2812. The parameter of the prototypes has been take from the simulation. The proposed coding of the prototypes for the three level and five level CHB-MLI is also created and then will be embedded in DSP TMS320F2812. Finally, the proposed method will be evaluated through simulation and experimental results.

3.2 Flow Chart of the project

The flow chart of the project has been developed as shown in figure 3.1. Firstly, the selection of final year project topic is done which is a research about harmonic minimization of a single phase cascaded H-bridge multilevel inverter. After the topic was selected, the project objectives must be understood in advance before doing a further step. Therefore, in order to increase the understanding about this project objectives, the literature review of the project must be done. This project main focus is how to reduce harmonic reduction by using a single phase cascaded H-bridge multilevel inverter based on the output voltage level selected. Thus, the simulation design based on MATLAB/SIMULINK has been done in order to get the results. By using MATLAB/SIMULINK software, there are four design has been done which are optimization single phase of CHB-MLI for 3-level, optimization single phase of CHB-MLI for 5-level, a non-optimization single phase of CHB-MLI for 3-level, and a non-optimization single phase of CHB-MLI for 5-level. Besides that, the study about Newton Rapshon controller technique also has been done in order to apply the technique during analysing the hardware. Then, after finish the simulation design, the hardware has been analyse to get the harmonics content and THD values. The experiment on the proposed hardware has been done in order to compare the results. Finally, discussion and conclusion of the results has been done to demonstrate the overall understanding about this research.

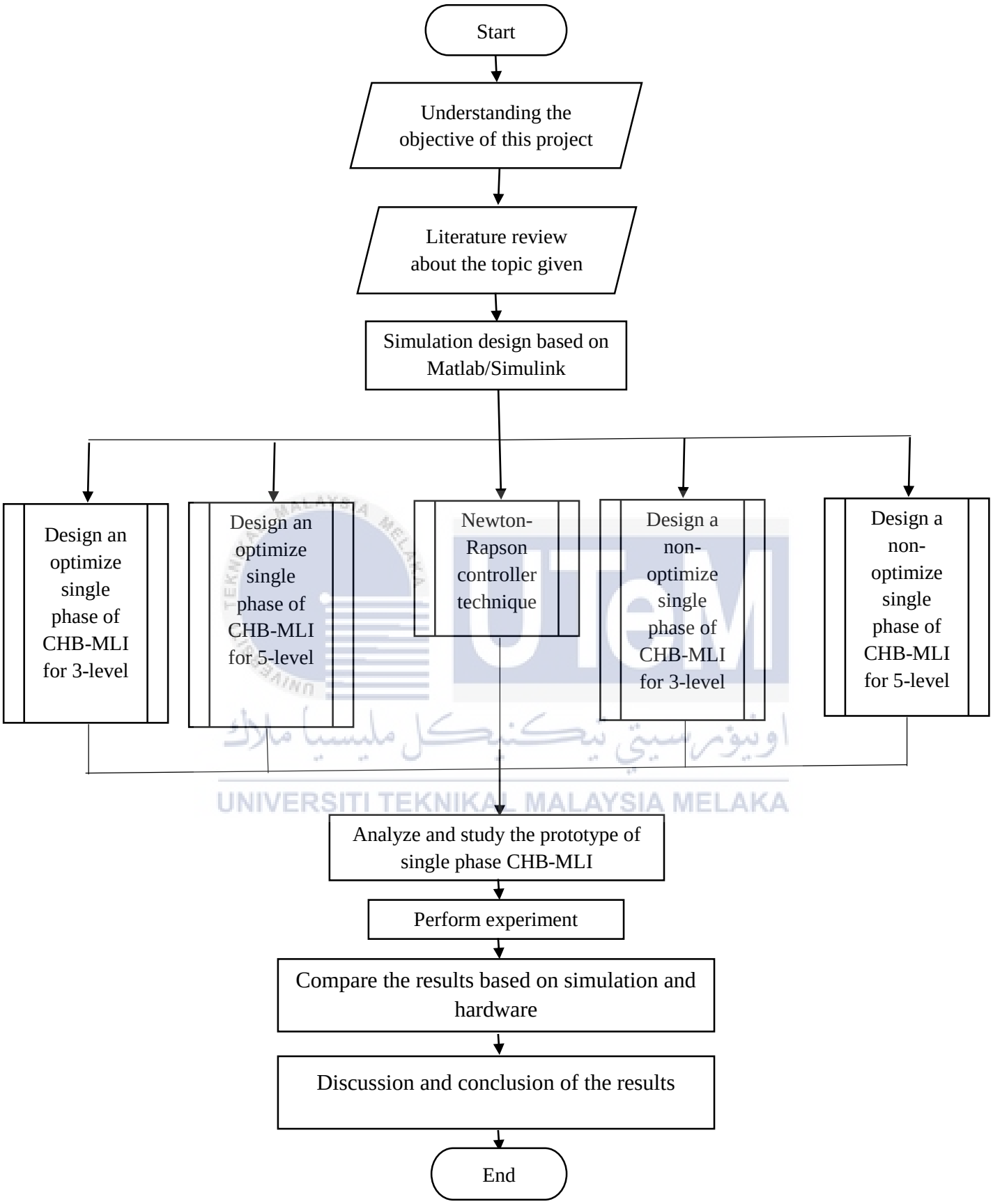

Figure 3.1: Flow Chart of the project

3.3 Discussion on selected design using MATLAB/SIMULINK

3.3.1 Simulation of Optimization three-levels cascaded H-bridge multilevel inverter by using MATLAB/SIMULINK

Based on this simulation design represent in Figure 3.2, an optimize single phase of three-levels CHB-MLI has been designed by using MATLAB/SIMULINK which is the modulation index (MI) for this design is 0.84. This proposed model utilize 50Hz of fundamental frequency to simulate the system. The maximum frequency for this model is 2500Hz. In this simulation, the supply used is direct current (DC) voltage source where the amount of supply used is 100V. Besides that, the SIMULINK model also consists of pulse generator block, one unit of single phase CHB-MLI, ideal voltage measurement, ideal current measurement, and RLC loads. The values of the loads utilized in this simulation circuit are R = 100Ω, L = 35mH and C = 70μF. Four ideal switch has been used in this simulation circuit which act as switching scheme to convert direct current (DC) to alternating current (AC) waveform.

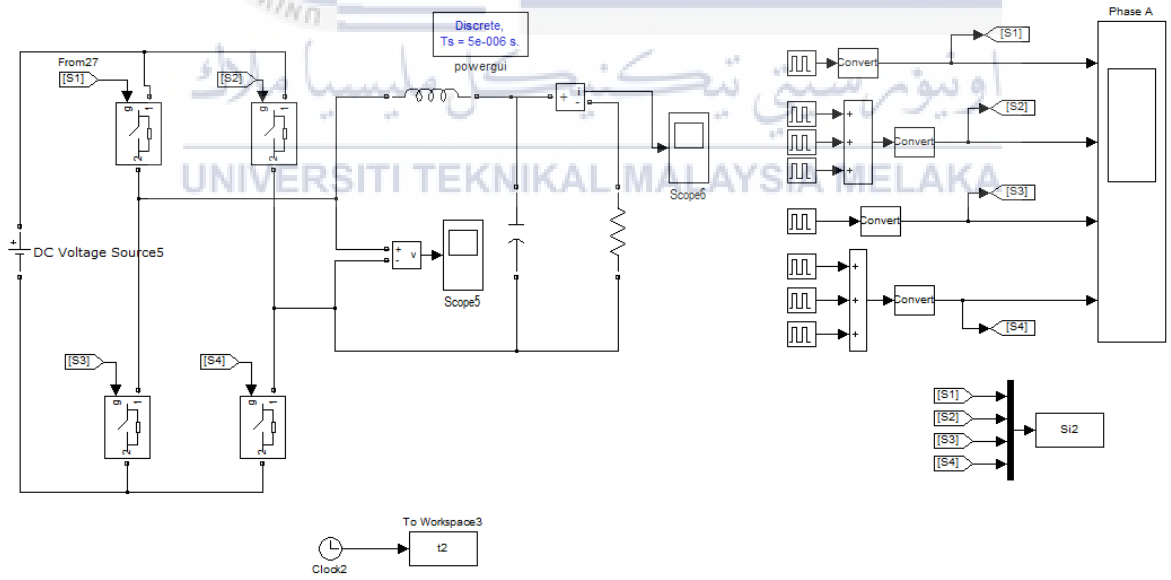

Figure 3.2: Modeling of optimize single phase three-level cascaded H-bridge multilevel inverter by using MATLAB/SIMULINK

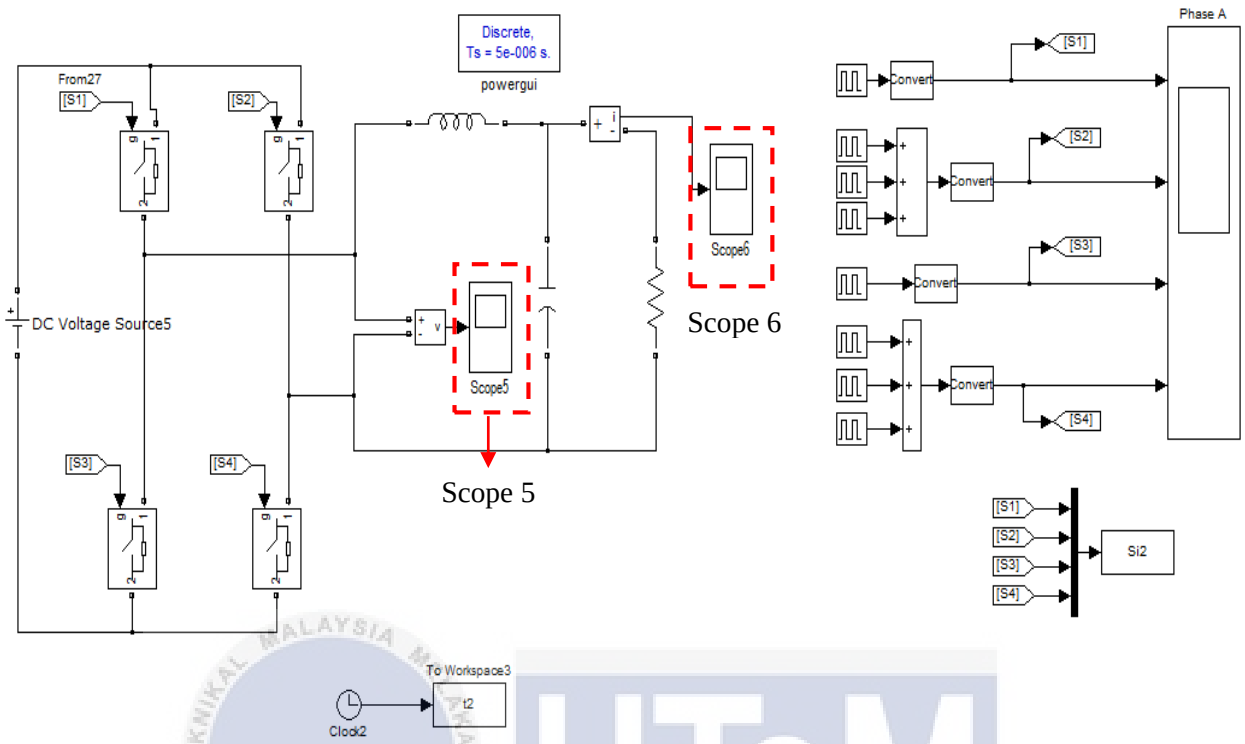

Figure 3.3: Scope for three-level cascaded H-bridge multilevel inverter by using MATLAB/SIMULINK

Based on Figure 3.3, the red dotted box represent the scope for three-level cascaded H-bridge multilevel inverter CHB-MLI by using MATLAB/SIMULINK where the scope 5 used to display the output waveform for phase voltage and the scope 6 used to display the output waveform for phase current. The voltage and current output waveform represents the magnitude and direction of voltage and current that flow in the simulation circuit.

3.3.2 The proposed Switching Scheme for three-levels cascaded H-bridge multilevel inverter

Based on the figure 3.4 shows that a single phase three-levels cascaded H-bridge multilevel inverter where the type of switching used for this simulation circuit is an ideal switch. This simulation circuit consist of four ideal switches which is upper switching where each switches have its own waveform. The ideal switch block does not suitable to a specific physical device because the ideal switch does not have conduction loss. For the ideal switches, $R_{on} = 0\Omega$ where there will be no power loss during activation and deactivation of the switches. For the practical switches, the value of R_{on} is based on the value of voltage rating and switching type. The gate signal used to completely control the ideal switch where the ideal switch block will turn on due to the existing of positive signal at the gate input. The ideal switch will turn off when the gate input does not receive any signal or the gate signal is equal to 0 [25]. The Ideal Switch block also consist of a series Rs-Cs snubber circuit which connected to ideal switch in parallel.

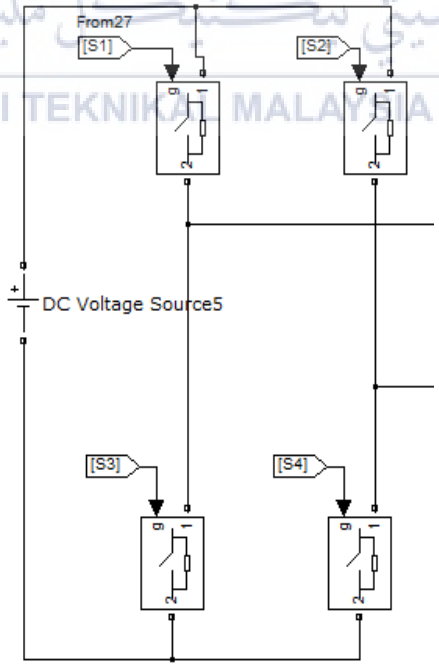

Figure 3.4: Switching design for a three-level CHB-MLI by using MATLAB/SIMULINK

3.3.3 The Switching Block design for three-levels cascaded H-bridge multilevel inverter by using MATLAB/SIMULINK

The switching for simulation design for three-level cascaded H-bridge multilevel inverter has been done as shown in Figure 3.5 where the waveform for the switching can be obtain from the phase A in the red dotted box. The waveform for the switches was produce by the pulse generator blocks where the direct current (DC) will be convert to alternating current (AC). Thus, the waveform for each switch will be formed where each switch have different waveform.

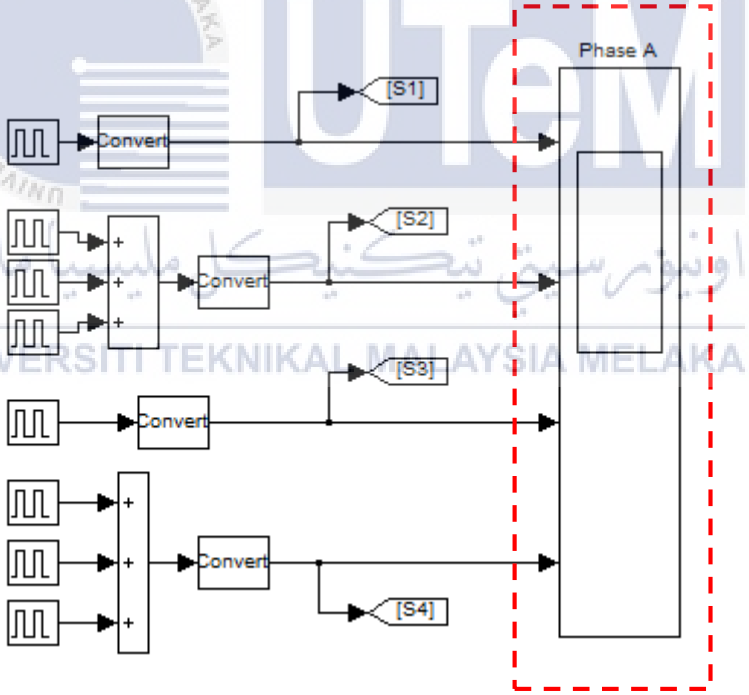

Figure 3.5: Pulse generator block connected to switching signal in three level CHB-MLI by using MATLAB/SIMULINK

3.3.4 Simulation of Optimization five-levels cascaded H-bridge multilevel inverter by using MATLAB/SIMULINK

A simulation circuit of optimization single phase five-level cascaded H-bridge multilevel inverter (CHB-MLI) has been designed by using MATLAB/SIMULINK as shown in Figure 3.7 where the modulation index (MI) for this simulation circuit is rated at 0.84. This proposed model utilize 50Hz of fundamental frequency to simulate the system and the maximum frequency for this model is 2500Hz. In this simulation, two voltage supply has been used which is direct current (DC) voltage source where the amount of supply used is 100V. Besides that, the SIMULINK model also consists of pulse generator block, two units of single phase CHB-MLI, ideal voltage measurement, ideal current measurement, and R, L and C as loads. The values of the loads used in this simulation circuit are R = 100Ω L = 35mH, and C = 70µF. Eight ideal switch has been used in this simulation circuit which act as switching scheme to convert direct current (DC) to alternating current (AC) waveform.

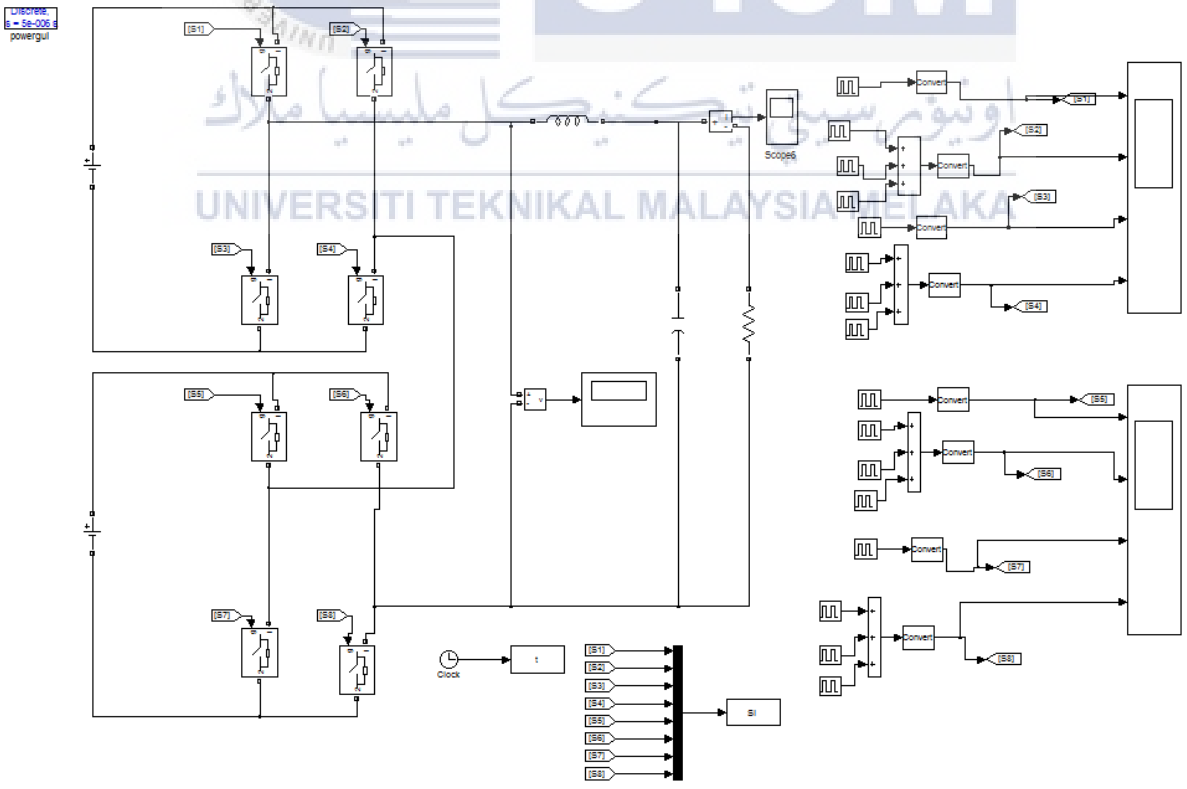

Figure 3.6: Five-level cascaded H-bridge multilevel inverter design using MATLAB/SIMULINK

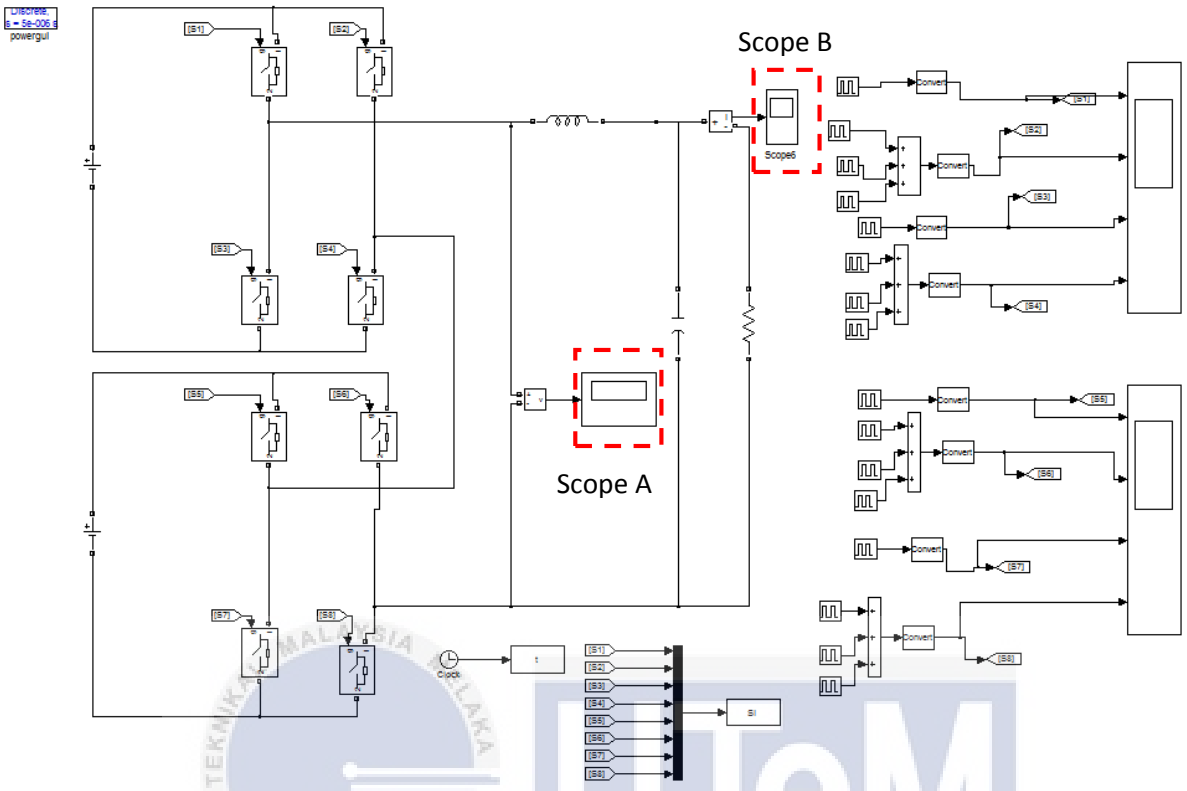

Figure 3.7: Scope for five-level cascaded H-bridge multilevel inverter by using MATLAB/SIMULINK

The red dotted box in Figure 3.8 represent the scope for five-level cascaded H-bridge multilevel inverter (CHB-MLI) by using MATLAB/SIMULINK where the scope A is used to display the output waveform phase voltage and scope B used to display the output waveform of phase current. The voltage and current output waveform represents the magnitude and direction of voltage and current that flow in the simulation circuit.

3.3.5 The proposed Switching Scheme for five-levels cascaded H-bridge multilevel inverter

Figure 3.9 shows that a single phase five-levels cascaded H-bridge multilevel inverter where the type of switching used for this simulation circuit is an ideal switch. This simulation circuit consist of eight ideal switches where S1, S2, S3 and S4 are upper switching and S5, S6, S7, and S8 are lower switching. The ideal switch was selected for this simulation because power loss can be neglected.

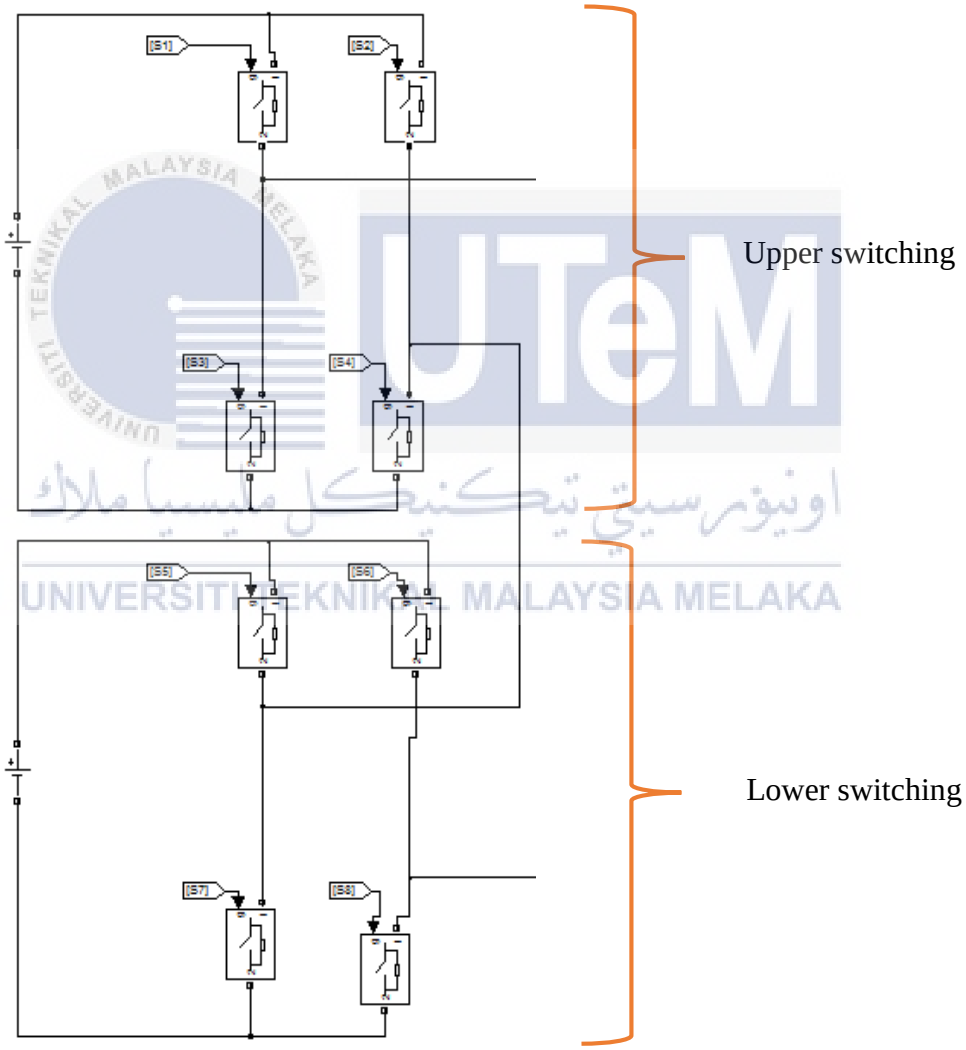

Figure 3.8: Switching design for a three-level CHB-MLI by using MATLAB/SIMULINK

3.3.6 The Switching Block design for five-levels cascaded H-bridge multilevel inverter by using MATLAB/SIMULINK

Figure 3.9 represent the switching for simulation design of three-level cascaded H-bridge multilevel inverter where the waveform for the switching can be obtain from the scope in the red dotted box. There are two units of single phase switching for this simulation where the upper switching contain the waveform for the switch S1, S2, S3 and S4 while the lower switching consist of switch S5, S6, S7, and S8. The waveform for the switches was produce by the pulse generator blocks where the direct current (DC) will be convert to alternating current (AC). Thus, the waveform for each switch will be formed where each switch have different waveform.

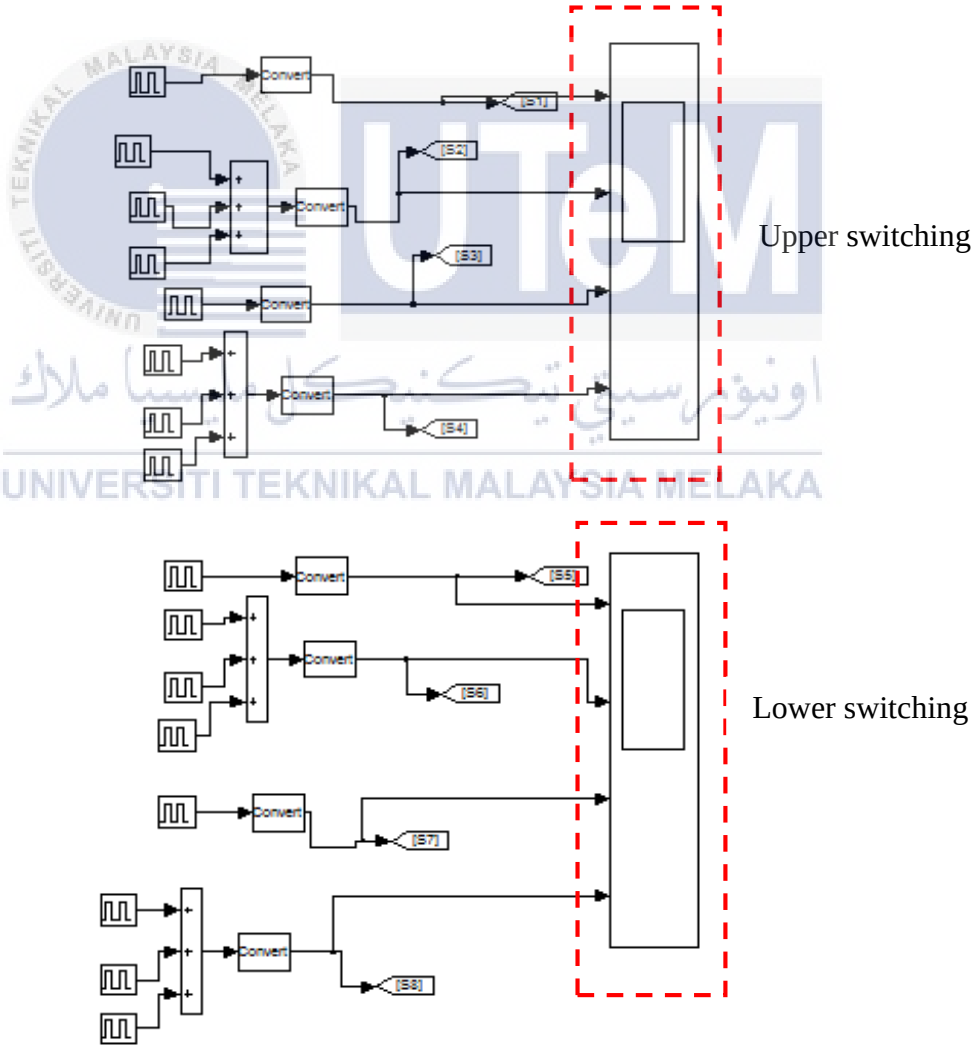

Figure 3.9: Pulse generator block connected to switching signal in five level CHB-MLI by using MATLAB/SIMULINK

3.3.7 Simulation of Non-Optimization three-levels cascaded H-bridge multilevel inverter by using MATLAB/SIMULINK

Based on the simulation circuit displayed in Figure 3.11, a non-optimization single phase cascaded H-bridge multilevel inverter (CHB-MLI) has been designed by using MATLAB/SIMULINK where the modulation index is 0.68. This proposed model utilize 50Hz of fundamental frequency to simulate the system. The maximum frequency for this model is 2500Hz. In this simulation, the supply used is direct current (DC) voltage source where the amount of supply used is 100V. This simulation circuit use RLC connected loads where the values of the loads are R = 100Ω, L = 35mH, and C = 70μF.

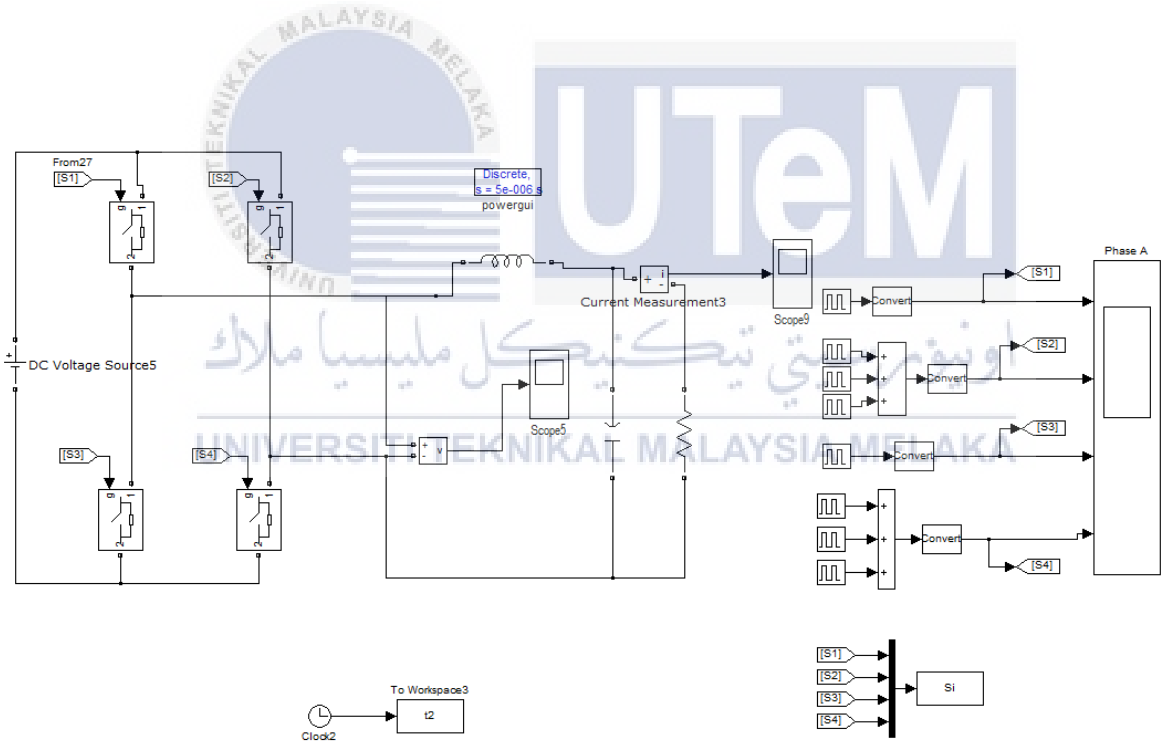

Figure 3.10: Modeling of non-optimize single phase three-level cascaded H-bridge multilevel inverter by using MATLAB/SIMULINK

3.3.8 Simulation of Non-Optimization five-levels cascaded H-bridge multilevel inverter by using MATLAB/SIMULINK

Figure 3.12 represent the simulation circuit of a non-optimization single phase cascaded H-bridge multilevel inverter (CHB-MLI) that has been design by using MATLAB/SIMULINK where the modulation index of this simulation circuit is 0.68. This proposed model utilize 50Hz of fundamental frequency to simulate the system and the maximum frequency for this model is 2500Hz. In this simulation circuit, two voltage supply has been used is direct current (DC) voltage source where the amount of supply used is 100V. This simulation circuit use RLC connected loads where the values of the loads are R = 100Ω, L = 35mH, and C = 70μF.

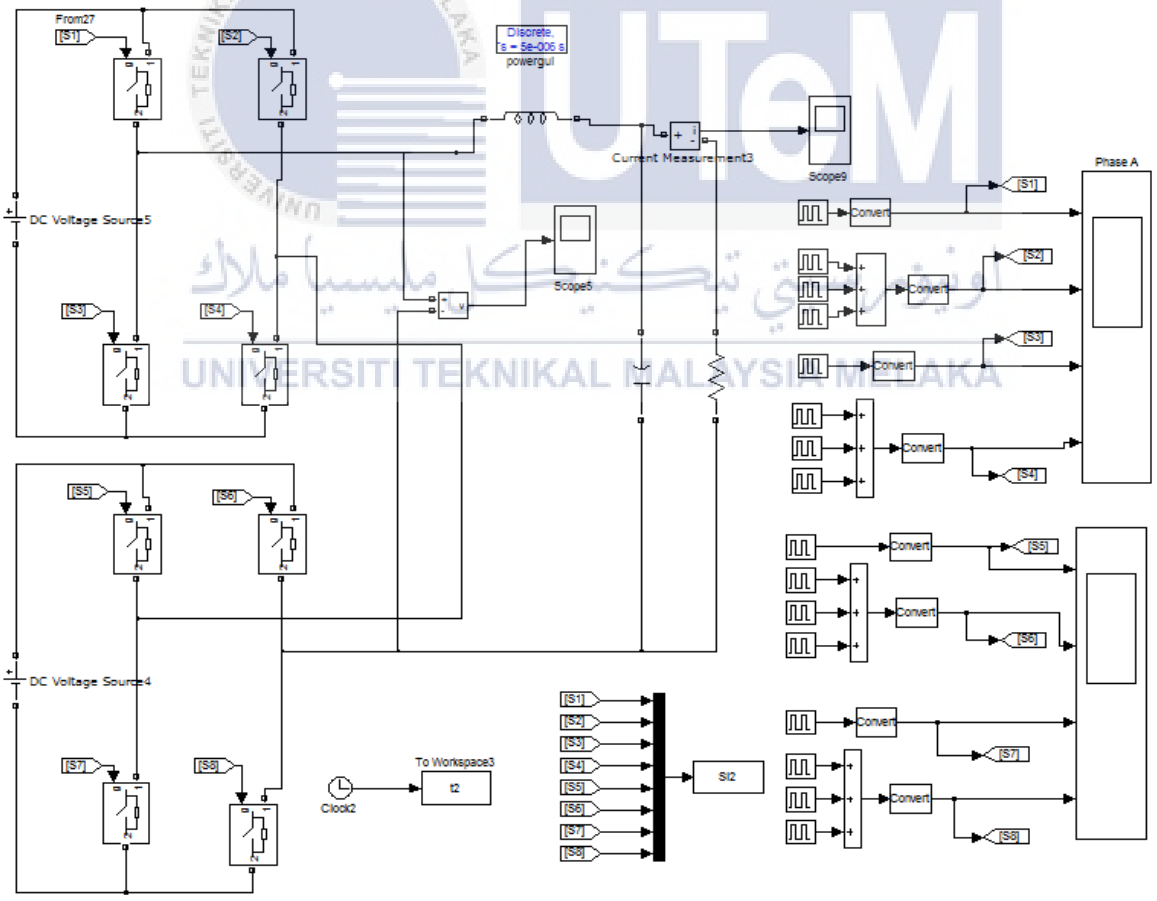

Figure 3.11: Modeling of non-optimization single phase five-level cascaded H-bridge multilevel inverter by using MATLAB/SIMULINK

3.4 Mathematical Technique of Switching by using Newton-Raphson

The values for two switching angles which are Θ_1 and Θ_2 can be obtain by solving the transcendental equations where a modulation index formula has been used to acquire suitable modulation index values, MI. Equation (3.1) show the formula to calculate the suitable modulation index values.

$$MI = V_1/2(4Vdc/\pi) \quad (3.1)$$

The switching angle that can be obtain is until Θ_8. The switching angles, Θ_3 until Θ_8 can be obtain based on the calculation by using Θ_1 and Θ_2. The procedure of detecting attributes and configuration of a system is called optimization. For the 5-level multilevel inverter, only one harmonic will be eliminated which is the 3rd harmonics was chosen to be evacuated [26].

Therefore, the Newton-Raphson technique has been used in order to solve the transcendental equations and to determine the switching angle. The harmonic equations can be expressed as:

$$\cos(\Theta_1) + \cos(\Theta_2) = 2(MI) \quad (3.2)$$

$$\cos(3\Theta_1) + \cos(3\Theta_1) = 0 \quad (3.3)$$

By using the following trigonometric identities:

$$\cos(3\Theta) = 4\cos^3(\Theta) - 3\cos(\Theta) \quad (3.4)$$

Equation (3.4), (3.5), and (3.6) were changed into polynomials harmonic equations.

Assume the variable as follow,

$$X_1 = \cos(\Theta_1) \quad (3.5)$$

$$X_2 = \cos(\Theta_2) \quad (3.6)$$

Substitute (3.5) and (3.6) into (3.2) and (3.3) and these equations were achieved,

$$X_1 + X_2 = 2(MI) \tag{3.7}$$

$$(4X_1^3 - 3X_1) + (4X_2^3 - 3X_2) = 0 \tag{3.8}$$

By solving (3.7) and (3.8), the polynomial function equation were achieved,

$$F(x) = X_2^2 - X_2 + s \tag{3.9}$$

By referring to iteration method, the values of X_1 and X_2 were calculated in order to obtain the values of switching angle for Θ_1 and Θ_2. Then, the switching angle values for Θ_3 until Θ_8 were achieved by substituting the values of angle Θ_1 and Θ_2 into these equations,

$$\Theta_3 = \pi - \Theta_2 \tag{3.10}$$

$$\Theta_4 = \pi - \Theta_1 \tag{3.11}$$

$$\Theta_5 = 2\pi - \Theta_4 \tag{3.12}$$

$$\Theta_6 = 2\pi - \Theta_3 \tag{3.13}$$

$$\Theta_7 = 2\pi - \Theta_2 \tag{3.14}$$

$$\Theta_8 = 2\pi - \Theta_1 \tag{3.15}$$

These switching angle has been used in 5-level cascaded H-bridge multilevel inverter which are the switches consist of S1, S2, S3, S4, S5, S6, S7, and S8. The values of switching angle for MI = 0.68 and MI = 0.84 that has been calculated using Newton-Raphson technique can be summarized in Table 3.1.

Modulation index, MI	MI = 0.68	MI = 0.84
Θ_1	8.77°	17.06°
Θ_2	68.16°	43.53°
Θ_3	111.84°	136.47°
Θ_4	171.23°	162.94°
Θ_5	188.77°	197.06°
Θ_6	248.16°	223.53°
Θ_7	291.84°	316.47°
Θ_8	351.23°	342.94°

Table 3.1: The values of switching angles based on modulation index

The mathematical technique of switching by using Newton-Raphson for three-level cascaded H-bridge multilevel inverter (CHB-MLI) is same as five-level CHB-MLI which is by solving those transcendental equations. But the different between these two circuits is three-level CHB-MLI only consist of four switches and four switching angle which are S1, S2, S3, S4 and Θ_1, Θ_2, Θ_3, Θ_4 respectively. Therefore, the calculation to get the switching angle is less complex compared to five-level CHB-MLI circuit.

3.5 Discussion on the Proposed Hardware Design

3.5.1 Gate Drive for IGBT Switching

Gate drive for inverter was utilized for switching the IGBT where the development of gate drive consist of optocoupler HCPLA3120. Figure 3.12 represent the design of gate drive connected with CHB-MLI. The purpose of using optocoupler HCPLA3120 is to interface the signal from DSP as low power voltage side to high voltage side. Meanwhile, it is a high-current output IGBT gate drive. The rating current and voltage supplied by the optocoupler that ideally suitable for precisely driving IGBTs is up to 1200V/100A. Based on this research, the IGBT from Infineon IHW30N90T has been utilized with built up gate drive where this gate drive can receive +3.3 volts input signal from DSP and sent it with isolated $\pm 15V$ to drive the IGBT that was connected to 60 volts DC. The other components that were utilized in this gate drive are DC-DC power supply +5V / $\pm 15V$, gate drive IC, resistors with different value which are 180Ω, 1kΩ, and 10 Ω, boost transformer, and connecters.

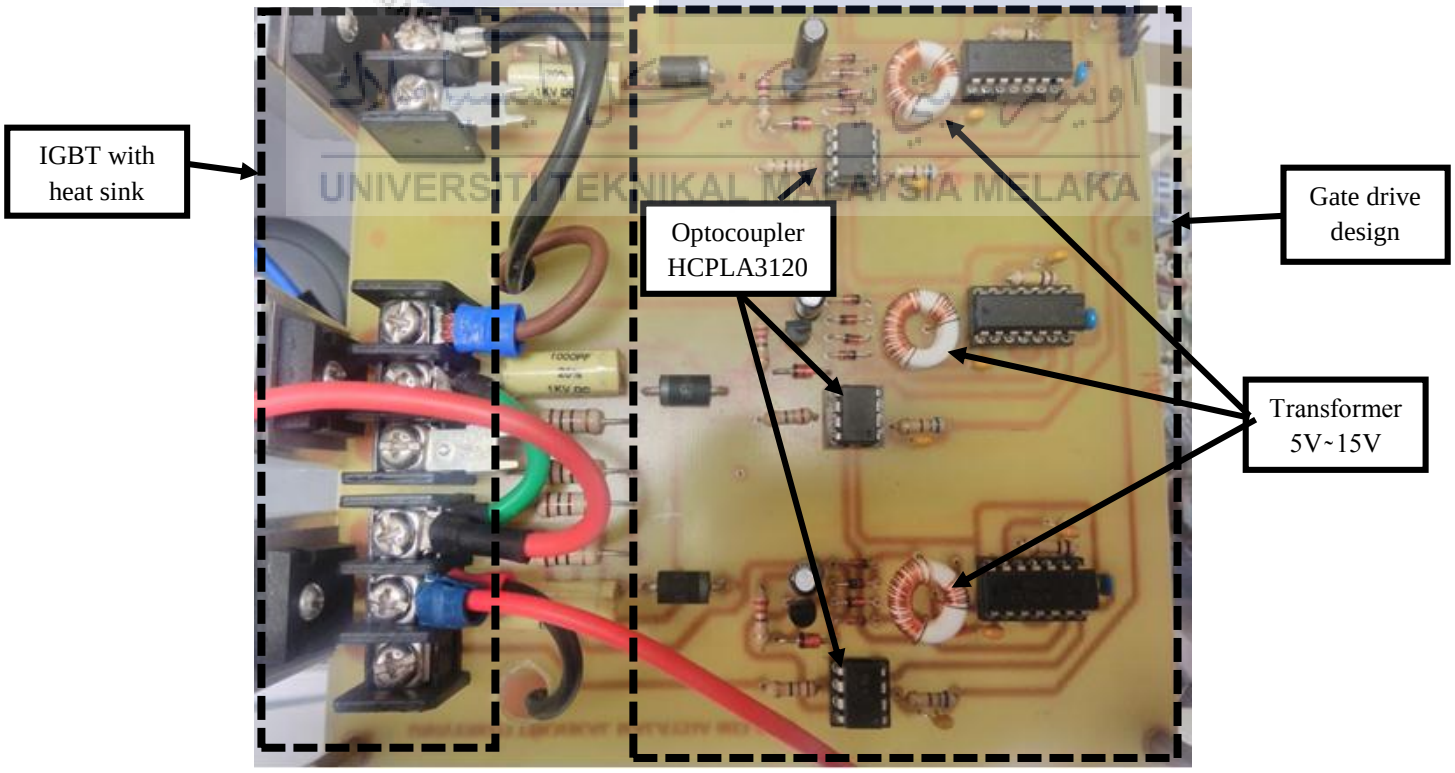

Figure 3.12: The prototype of gate drive connected with CHB-MLI

3.5.2 The Hardware for Single Phase Three Level and Five CHB-MLI

The design of the three-level CHB-MLI contain of 12 parts of semiconductor switching which are IGBTs – IHW30N90T with snubber circuits, 4 transformers coil (5V-15V), and 4 pieces optocoupler HCPLA3120 as represent in Figure 3.13. For the five-level CHB-MLI, the circuit consist of 24 parts of semiconductor switching, 8 transformer coil (5V-15V), and 8 pieces of optocupler HCPLA3120 as shown in Figure 3.14. The IGBT capable to operate the switching frequency up to 100 kHz and the current that will be supply was 60A at 25°C while the current will drop to 30A when the temperature at 100°C. The DC voltage that IGBT can operate was at 600 Volts DC and the breakdown voltage will be at 900 Volts DC.

There are terminals contain in IGBT which are gate (G), collector (C), and emitter (E). The voltage form IGBT was produce from gate drives circuits where the important condition to select the IGBT was the voltage of the IGBT from collector to emitter ($+V_{CE}$). The advantage of applying IGBT in these circuits was the switching sequence of the voltage across the IGBT similar to DC voltage source. Thus, the inverter enable to operate higher current capacity due to the IGBT has the ability in conducting frequency switching. Additionally, the higher the frequency capability, hence the higher the switching frequency. Low switching frequency will be suitable utilize in five-level CHB-MLI because the output current that has been produce contain less harmonic.

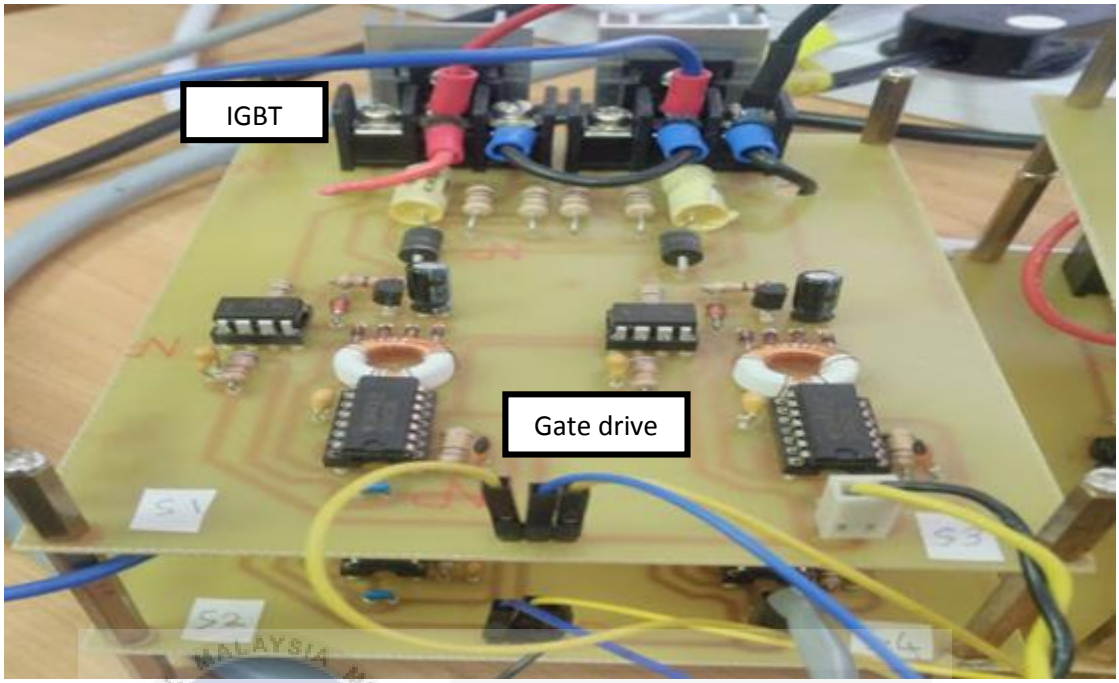

Figure 3.13: The design of a single phase three-level CHB-MLI

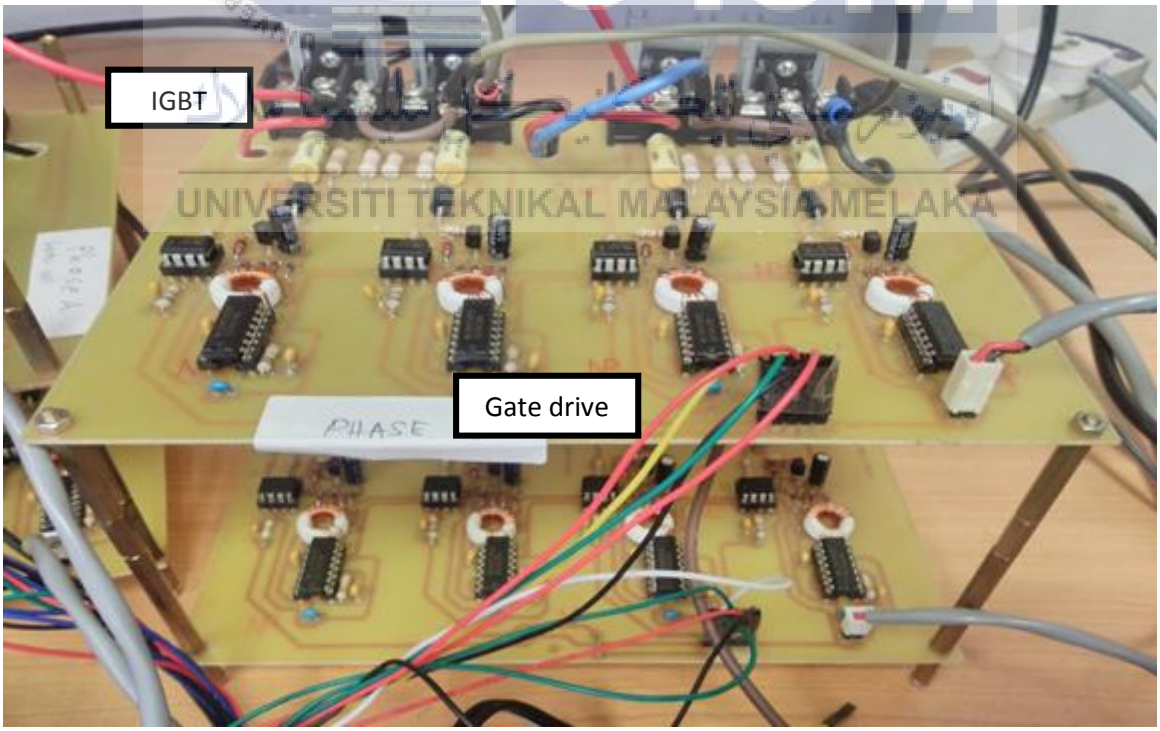

Figure 3.14: The design of a single phase five-level CHB-MLI

3.5.3 Hardware Utilization Based on Digital Signal Processor (DSP)

Figure 3.15 illustrate the Digital Signal Processor (DSP) TMS320F2812 which the frequency used in this hardware was 150MHz. The DSP TMS320F2812 consists of control system, time sampling, and analogue to digital conversion (ADC). Based on this research, the main function of using DSP TMS320F2812 was as a tool in order to get the output of the proposed prototypes. The coding based on Newton-Raphson has been developed then coded and stored in the DSP. The parameter from simulation will be used to develop a prototype of a single phase cascaded H-bridge using DSP TMS320F2812 and the coding will be created using C++ programming. The proposed coding will be embedded with DSP TMS320F2812 in order to carry out the inverter.

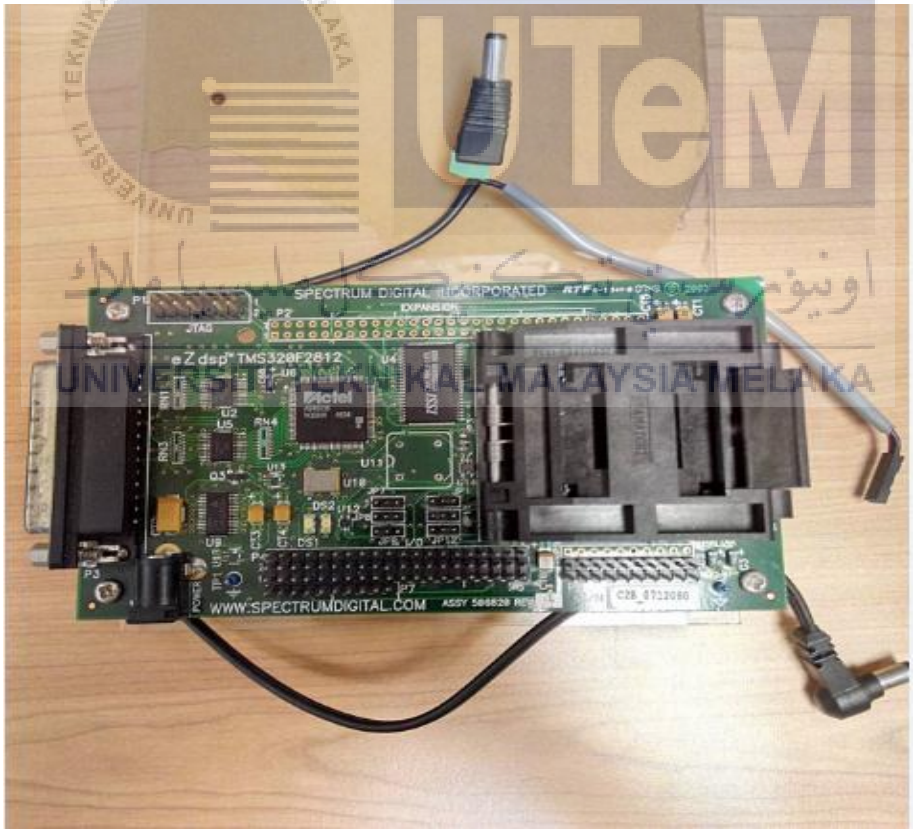

Figure 3.15: Digital Signal Processor (DSP) TMS320F2812

3.5.4 Experimental Prototype Circuits of Three and Five Level CHB-MLI

The experimental prototype circuits for three and five level has been designed as represent in Figure 3.16 and Figure 3.17 respectively. The hardware connection of the three and five level CHB-MLI has been analyze to compare the performance between these two types of multilevel inverter based on the total harmonic distortion (THD), output voltage, and output current. The hardware that has been used in order to complete this experiment such as DC supply source, single phase five-and three level of CHB-MLI with DSP-based control circuit and connected RL loads, oscilloscope and a personal computer (PC).

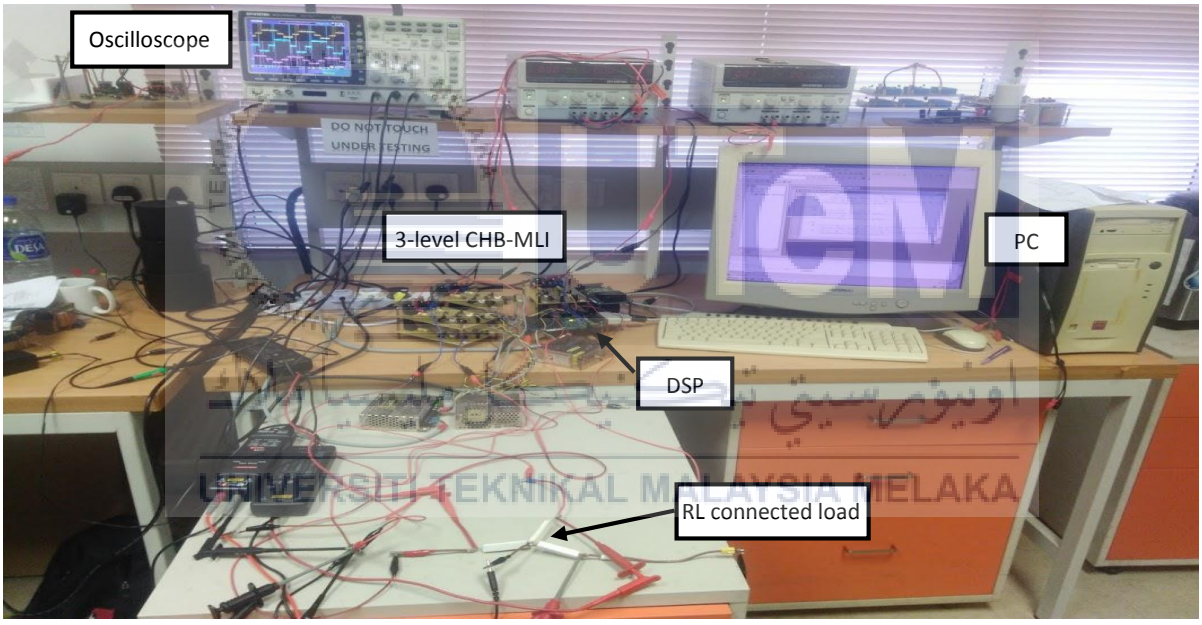

Figure 3.16: Set up of experimental prototype circuit of for three level CHB-MLI

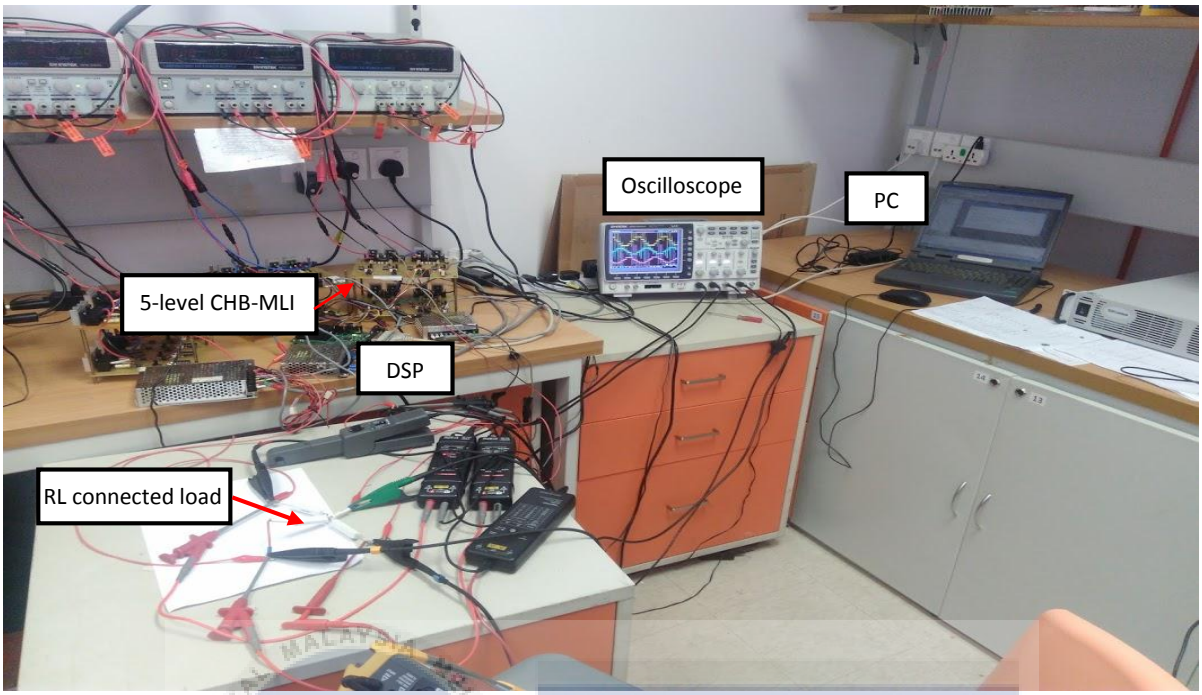

Figure 3.17: Set up of experimental prototype circuit for five level CHB-MLI

3.6 Summary of the Method Use

Based on this chapter, the research methodology has been discussed to fulfill and obtain the objectives of the thesis. Firstly, the single phase three and five level CHB-MLI has been design by using MATLAB/SIMULINK. Besides that, the circuit for optimization and non-optimization of a single phase three and five level CHB-MLI also has been design. Then, the parameters based on proposed simulation has been used in order to analyze the proposed hardware using DSPTMS320F2812. Newton-Raphson controller technique has been applied for this hardware where the proposed source code will be embedded in DSPTMS320F2812. Finally, the experiment has been done for the three and five level CHB-MLI hardware.

CHAPTER 4

RESULTS AND DISCUSSION

4.1 Introduction to Project Results

This chapter will describes the results of the simulation and analysis the hardware prototype that has been proposed which are three-level and five-level cascaded H-bridge multilevel inverter (CHB-MLI). The simulation results for three level and five level CHB-MLI were obtain by using the proposed method which is Newton-Raphson technique. The simulation results has been achieved by using MATLAB/SIMULINK where the parameters for the simulation circuits will be used to analyze prototypes of three-level and five-level CHB-MLI. Then, the experimental setup has been perform in order to obtain the results of the proposed prototypes. The proposed source code for three-level and five-level CHB-MLI has been used in these prototypes where the coding will be embedded into DSP TMS320F2812 platform which used to operate the prototypes of CHB-MLI. The results for the simulation circuits and hardware of three-level and five-level CHB-MLI will be discussed and compared.

4.2 Simulation of a Single Phase CHB-MLI for Five and Three level

The proposed simulation design of single phase CHB-MLI for three-level and five-level as shown in Figure 3.2, Figure 3.6, Figure 3.10, and Figure 3.11 were simulated by using MATLAB/SIMULINK. There are two values of MI was used for three and five levels CHB-MLI which are 0.84 and 0.68. The different value of MI will affect the percentage of THD in the simulation circuit. The value of MI for optimization was 0.84 while the value of MI for

non-optimization was 0.68. In order to execute the simulation of three and five levels CHB-MLI, Newton-Raphson technique has been used for both types of CHB-MLI. By using Newton-Raphson technique, the switching angles were calculated to obtain the value of timing diagram of switches pulses for upper and lower switching of three and five levels CHB-MLI. The calculation of switching angle for optimization of three and five levels CHB-MLI is accurate where the harmonic contents for voltage and current can be minimize. Meanwhile, the calculation for non-optimization of CHB-MLI was inaccurate which the harmonic contents produced much higher.

4.2.1 Simulation Results for Optimization of a Single Phase Three-Level CHB-MLI design with MI = 0.84

Based on this simulation, the duration of time to operate the simulation was 0.02s for each cycle. The value of MI = 0.84 and the switching angles has been calculated in order to simulate the three level CHB-MLI. The switching angles has been calculate using Newton-Raphson technique where the switching angles $\Theta_1 = 17.06°$ and $\Theta_2 = 43.53°$. These switching angles has been used to simulate the switches of CHB-MLI.

Figure 4.1 represent the switching waveforms for each switch which are S1, S2, S3, and S4. The different switching angle from each switch produce the different switching waveform that will cause the inverter to operate. The waveform of the switch has been determine by applied the switching angle control. In this simulation, the switching angle has been used to obtain waveform period and phase delay then has been applied in the pulse generator block. This switching waveform is better compared to non-optimize waveform because optimize circuit produce less THD and harmonics content compared to non-optimize circuit.

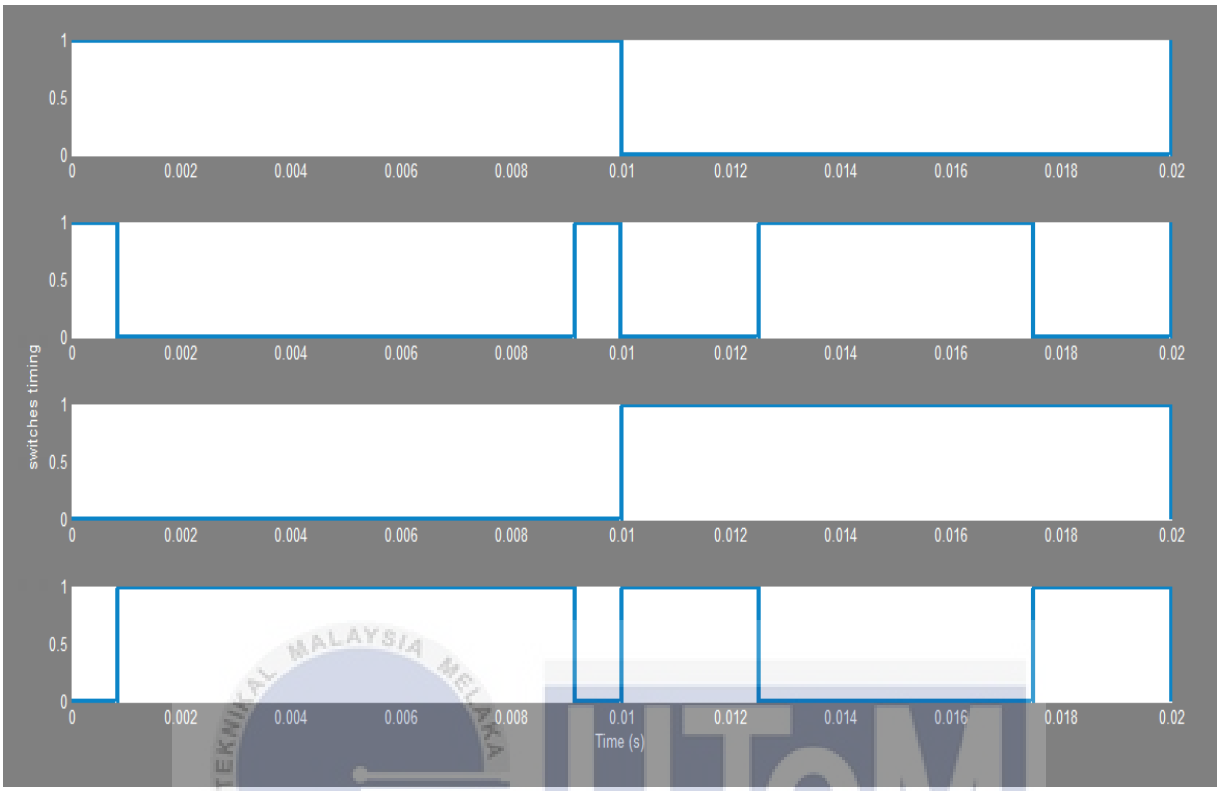

Figure 4.1: Switching waveform for optimization three-level CHB-MLI with MI = 0.84 for $\Theta_1 = 17.06°$ and $\Theta_2 = 43.53°$

The output voltage waveform of single phase three level CHB-MLI that has been obtain in this simulation as illustrate in Figure 4.2. The smooth output voltage waveform of the CHB-MLI come from the accurate calculation of switching angles. Figure 4.3 display the harmonic spectrum of optimization voltage output waveform for three level CHB-MLI. Based on the harmonic spectrum, the percentage of THD can be obtain which the value is equal to 35.55%. The harmonic contents in the simulation was refer to the value of THD obtain.

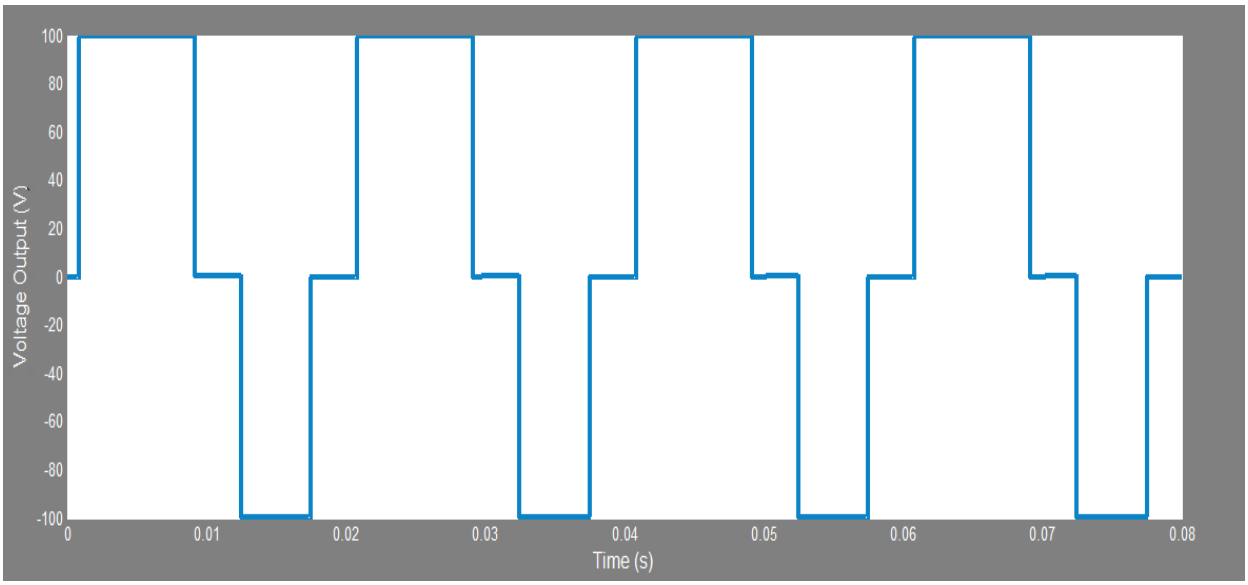

Figure 4.2: Output voltage waveform of optimization single phase three level CHB-MLI with MI = 0.84

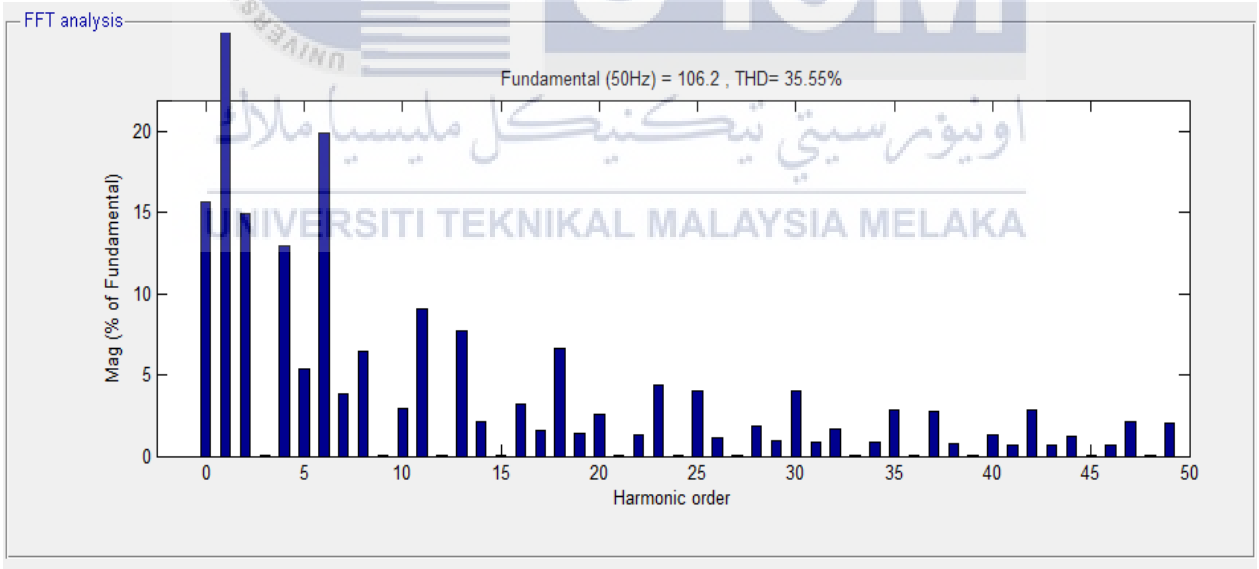

Figure 4.3: Harmonic spectrum for voltage output waveform of optimization three level CHB-MLI with MI = 0.84

Figure 4.4 represent the result of optimization for the current output waveform of three level CHB-MLI. The smooth output current waveform of the CHB-MLI can be obtain from the accurate calculation of switching angles. Figure 4.5 illustrate the harmonic spectrum of optimization voltage output waveform for three level CHB-MLI. Based on the harmonic spectrum, the percentage of THD can be obtain which the value is equal to 11.49%. The harmonic contents in the simulation was refer to the value of THD obtain.

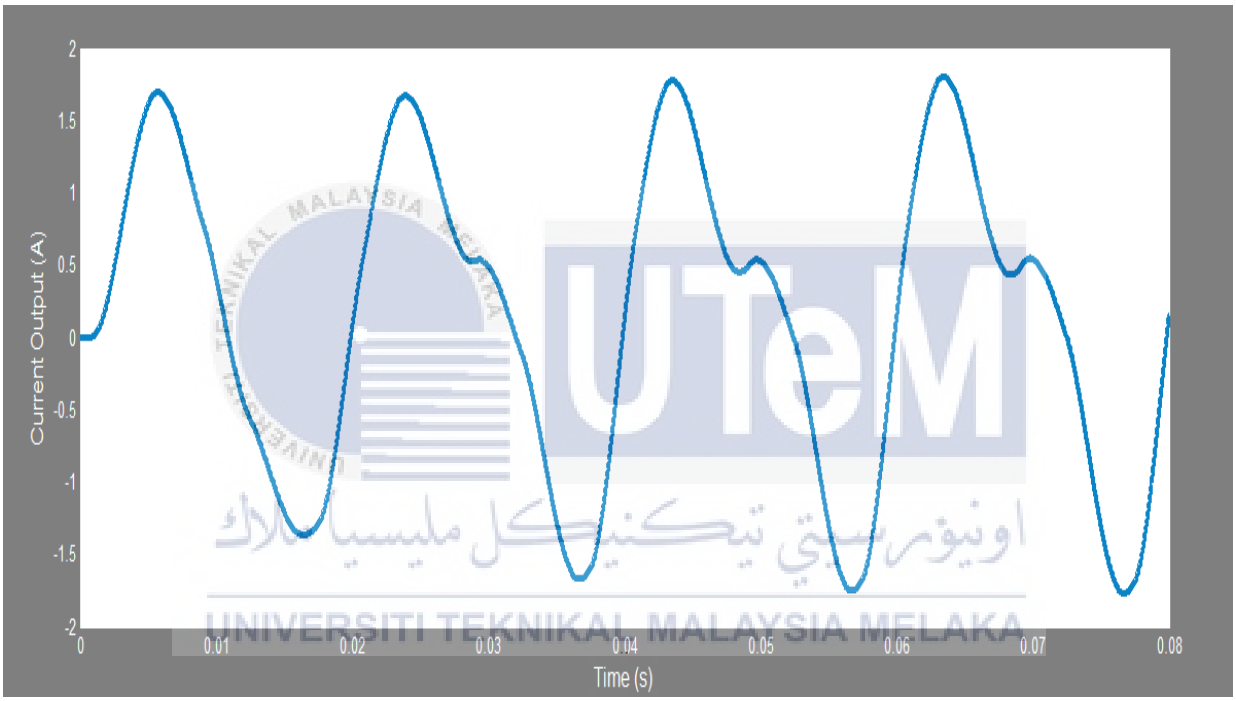

Figure 4.4: Output current waveform of optimization single phase three level CHB-MLI with MI = 0.84

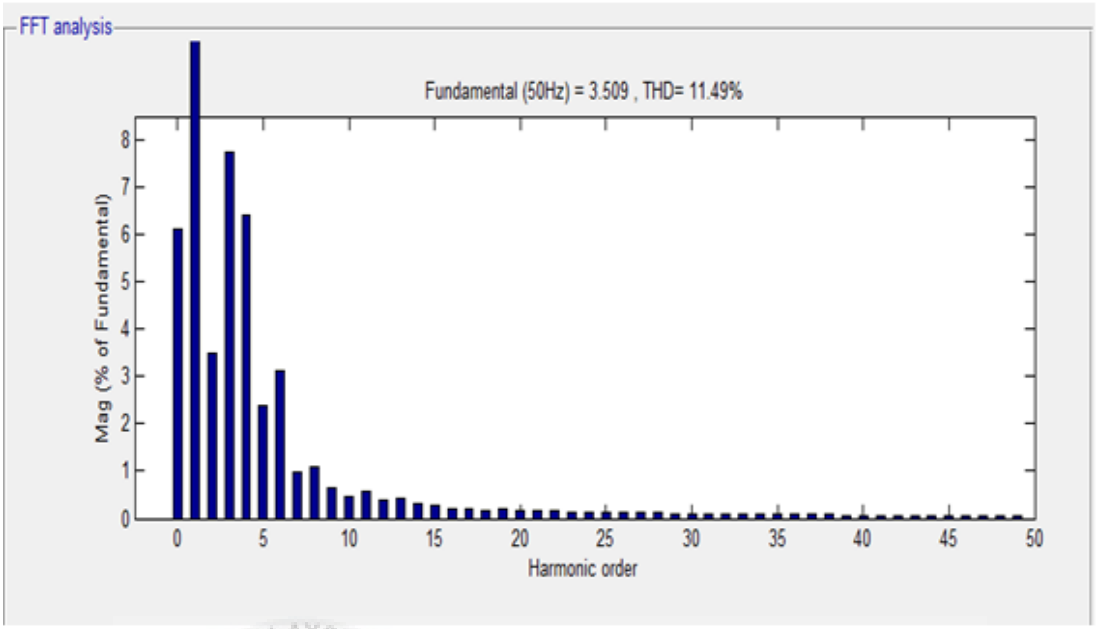

Figure 4.5: Harmonic spectrum for current output waveform of optimization three level CHB-MLI with MI = 0.84

4.2.2 Simulation Results for Non-Optimization of a Single Phase Three-Level CHB-MLI design with MI = 0.68

Figure 4.6 illustrate the switching waveform for non-optimization three level CHB-MLI where there are four switches which are S1, S2, S3, and S4 has been used in this simulation circuit. Each switch produce different waveform in order to operate the simulation circuit. The switching angle should be obtain by using mathematical technique of switching where the switching angle has been used to calculate the value of phase delay and period for each switches. The switching angles that has been utilized in this simulation based on the mathematical calculation are $\Theta_1 = 8.77°$ and $\Theta_2 = 68.16°$. The phase delay and period for each switches has been used as the parameter for pulse generator in the simulation circuit. The phase delay and period for this simulation circuit are based on the value of the modulation index used where the modulation index for this simulation circuit is lower compared to optimization simulation circuit.

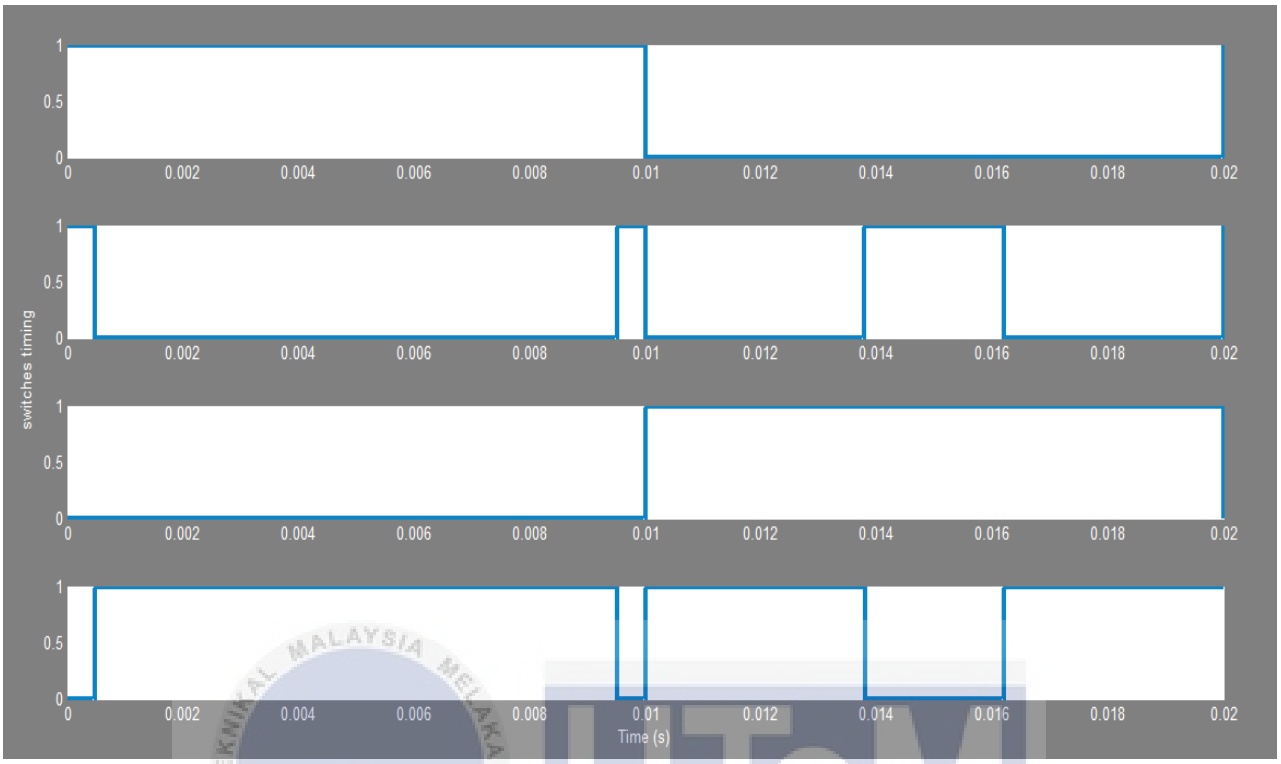

Figure 4.6: Switching waveform for non-optimization three-level CHB-MLI with MI = 0.68 for $\Theta_1 = 8.77°$ and $\Theta_2 = 68.16°$

The non-optimization three level CHB-MLI has been simulated at MI = 0.68 and the switching angles $\Theta_1 = 8.77°$ and $\Theta 2 = 68.16°$ has been used. This simulation use the duration of time equal to 0.02s for each cycle. Figure 4.7 and Figure 4.8 show the output voltage waveform of non-optimization three level CHB-MLI and harmonic spectrum for voltage output waveform respectively. Based on the harmonic spectrum, the percentage of THD can be obtain which the value is equal to 48.62%. The harmonic contents in the simulation was refer to the value of THD obtain.

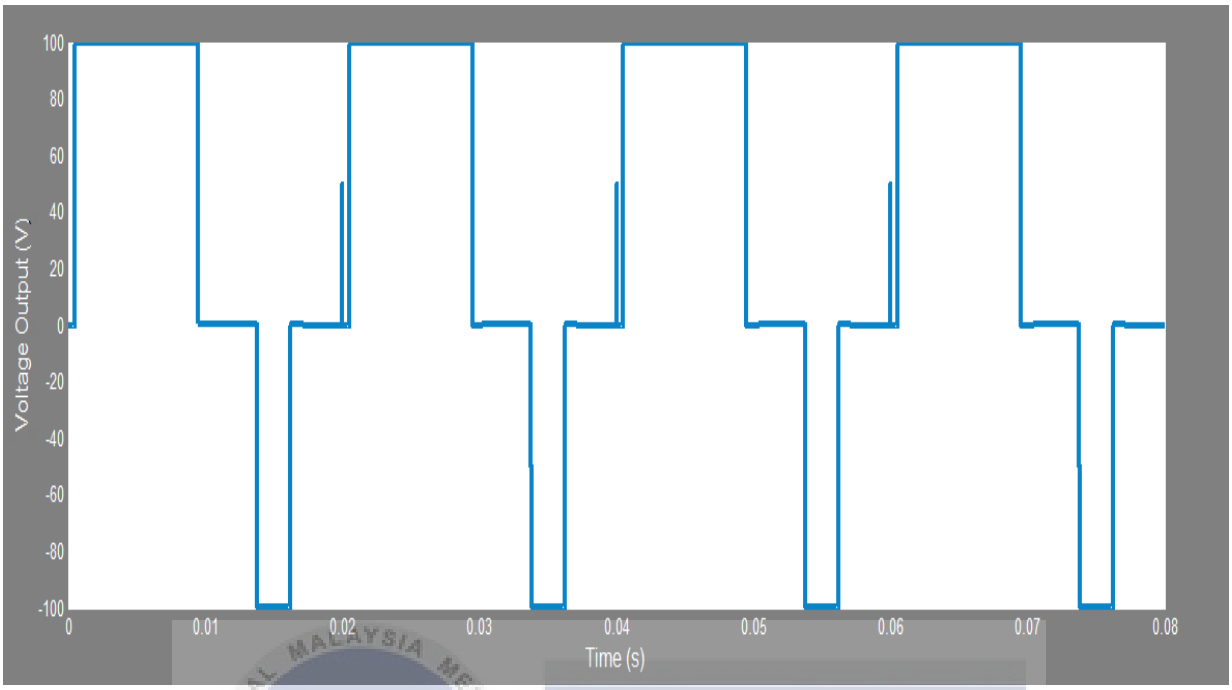

Figure 4.7: Output voltage waveform of non-optimization three level CHB-MLI with MI =0.68

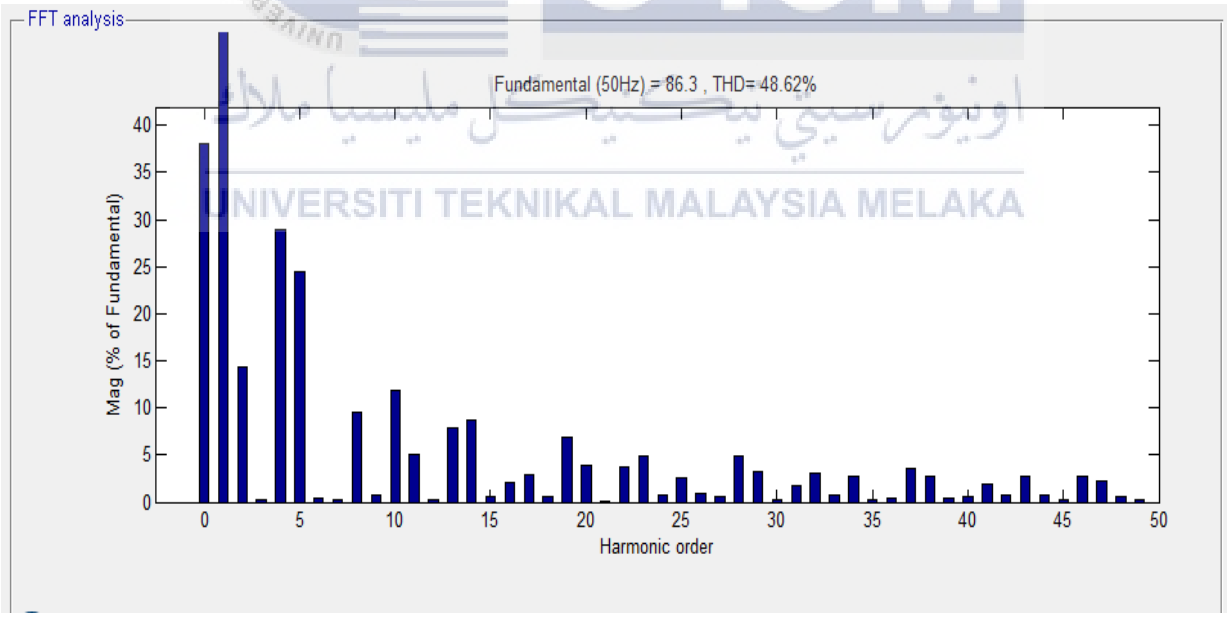

Figure 4.8: Harmonic spectrum for voltage output waveform non-optimization three level CHB-MLI with MI = 0.68

The current output waveform for non-optimization three level CHB-MLI can be obtain as display in Figure 4.9. The non-optimization output current waveform of the CHB-MLI not very smooth due to inaccurate calculation of switching angles. Figure 4.10 represent the harmonic spectrum of non-optimization current output waveform of CHB-MLI with THD values equivalent 13.40%. The THD value is higher compared to optimization three-level CHB-MLI as shown in Figure 4.5.

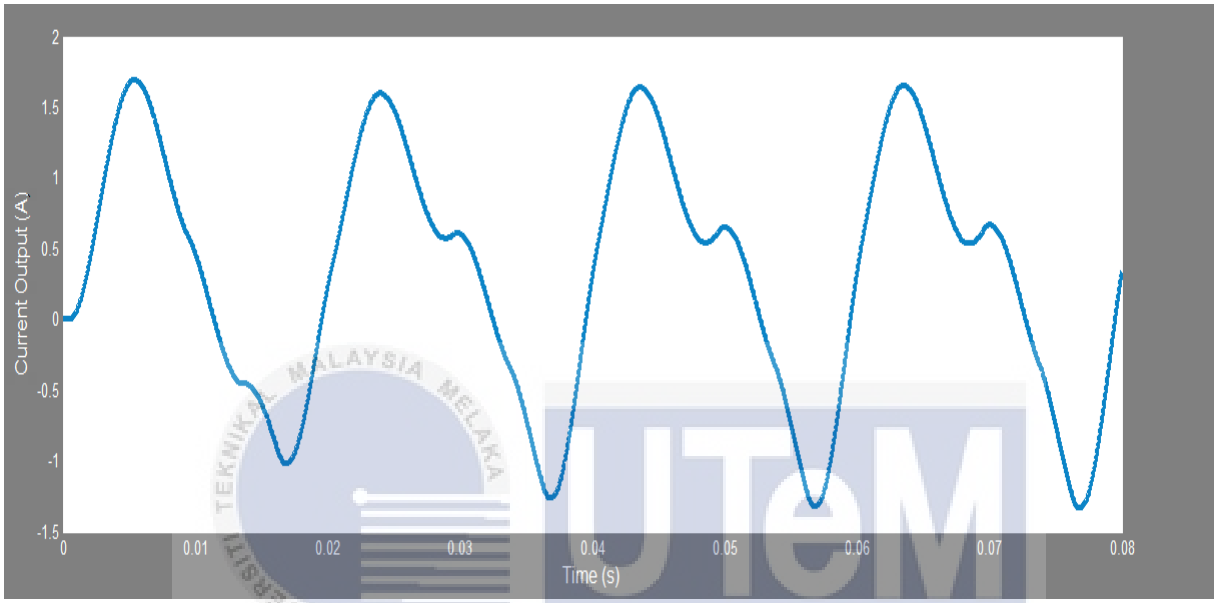

Figure 4.9: Output current waveform of non-optimization three level CHB-MLI with MI =0.68

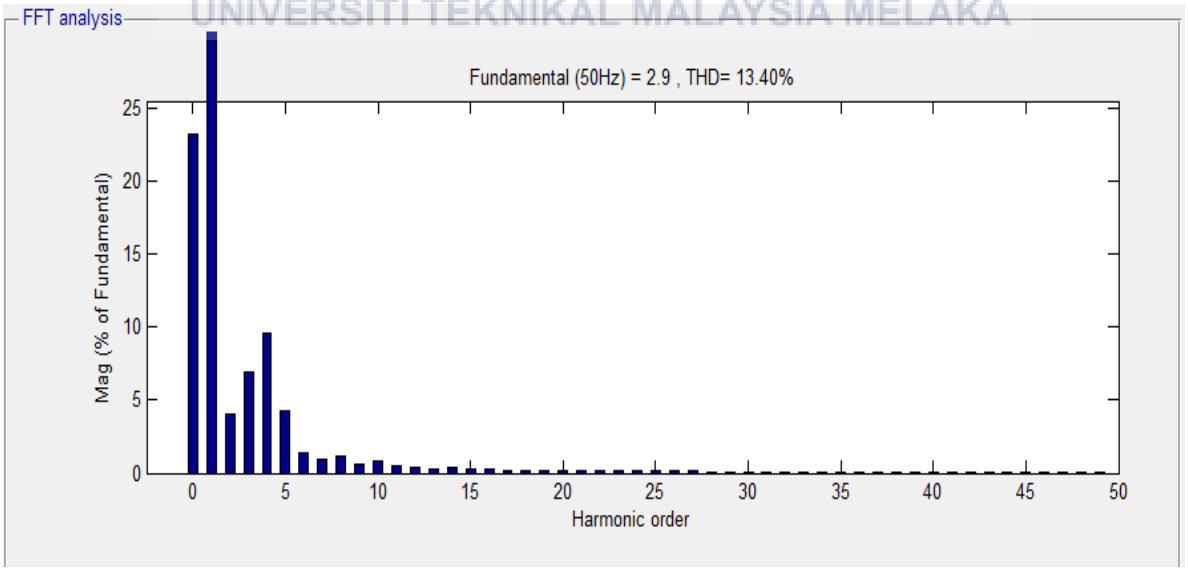

Figure 4.10: Harmonic spectrum for current output waveform non-optimization three level CHB-MLI with MI = 0.68

4.2.3 Simulation Results for Optimization of a Single Phase Five-Level CHB-MLI design with MI = 0.84

Figure 4.11(a) and Figure 4.11(b) represent the switching waveforms for each switch where the Figure 4.11(a) show the waveform for the S1, S2, S3 and S4 while the Figure 4.11(b) show the waveform for the S5, S6, S7, S8. The different waveform from each switch cause the cascaded H-bridge multilevel inverter to operate. By obtaining the switching angle using mathematical technique of switching, the parameter for the pulse generator block which are phase delay and period also has been obtain. The switching angles $\Theta_1 = 17.06°$ and $\Theta_2 = 43.53°$ has been utilized in order to simulate the CHB-MLI.

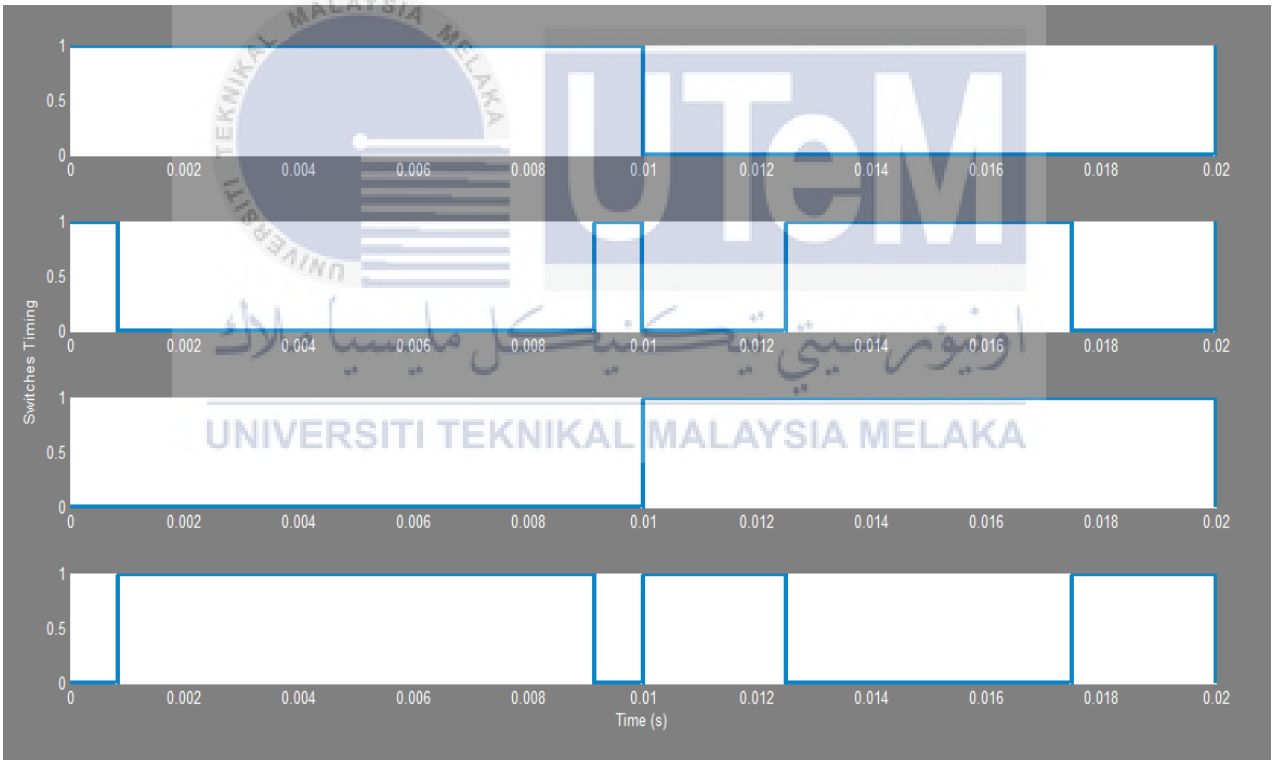

Figure 4.11(a): Upper switching waveform for optimization five-level CHB-MLI with MI = 0.84 for $\Theta_1 = 17.06°$ and $\Theta_2 = 43.53°$

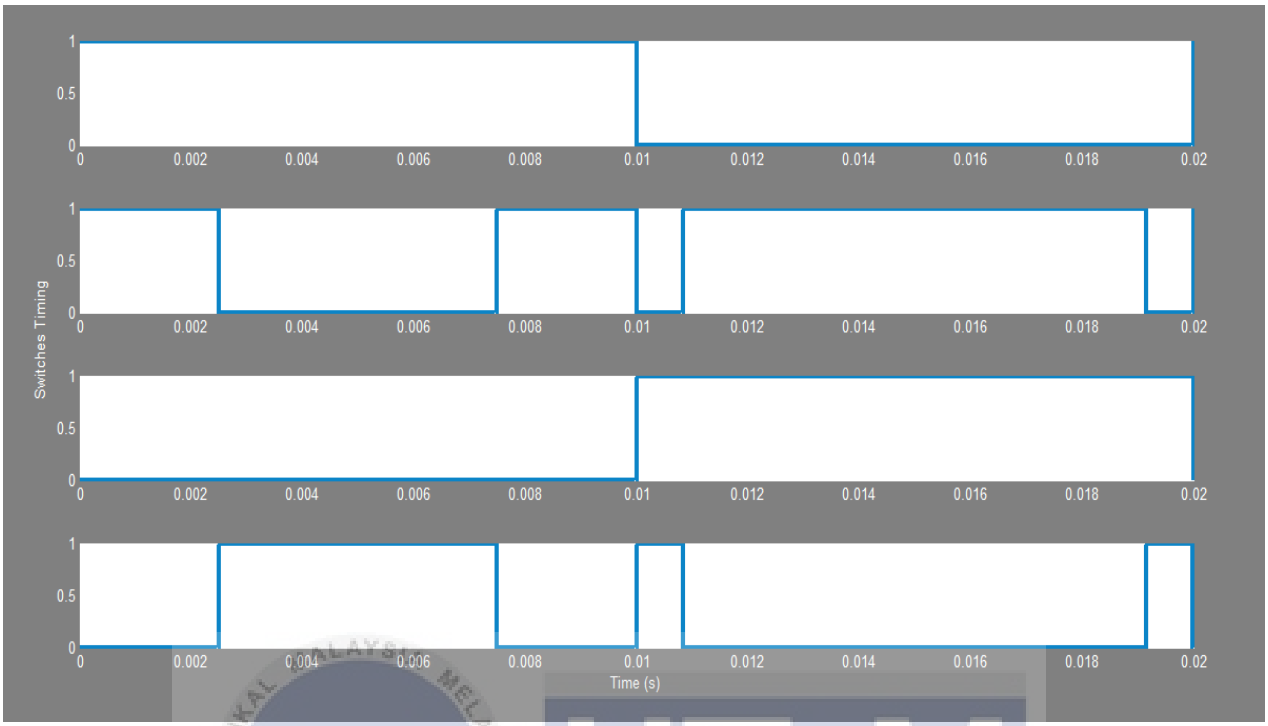

Figure 4.11(b): Lower switching waveform for optimization five-level CHB-MLI with MI = 0.84 for $\Theta_1 = 17.06°$ and $\Theta_2 = 43.53°$

Figure 4.12 represent the output voltage waveform of single phase five level CHB-MLI that has been obtain in this simulation. The accurate calculation of switching angle produce smooth output waveform of the CHB-MLI. Figure 4.13 display the harmonic spectrum of optimization voltage output waveform for five level CHB-MLI. Based on the harmonic spectrum, the percentage of THD can be obtain which the value is equal to 16.86%. The harmonic contents in the simulation was refer to the value of THD obtain.

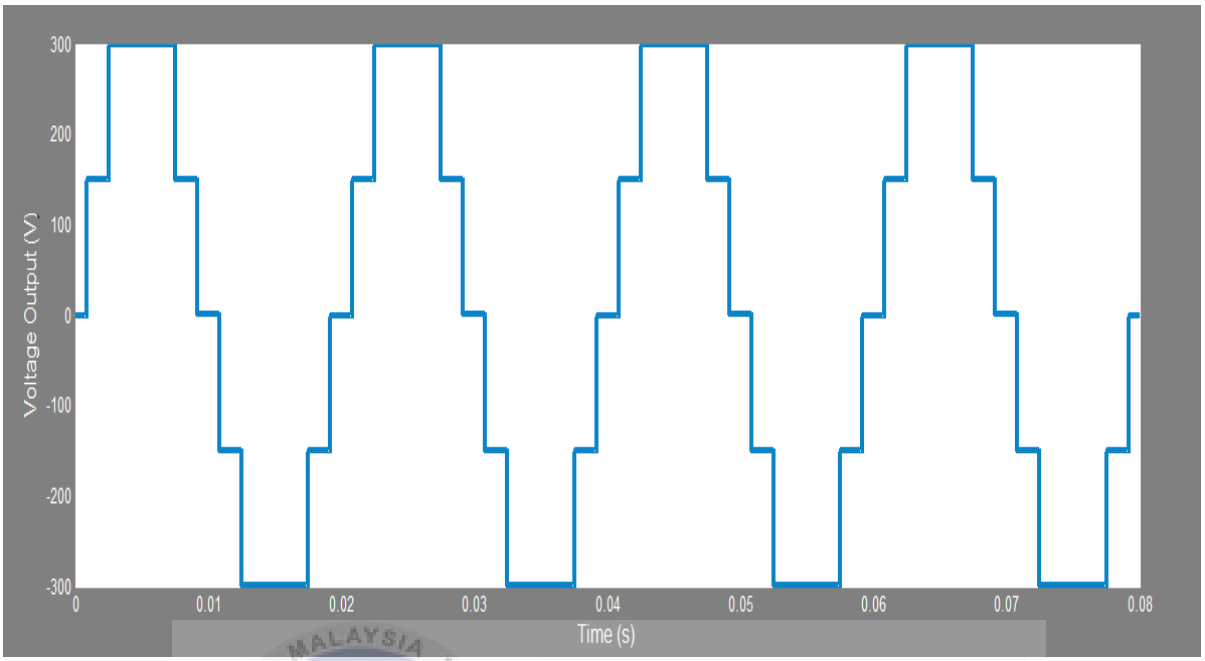

Figure 4.12: Output voltage waveform of optimization five level CHB-MLI with MI = 0.84

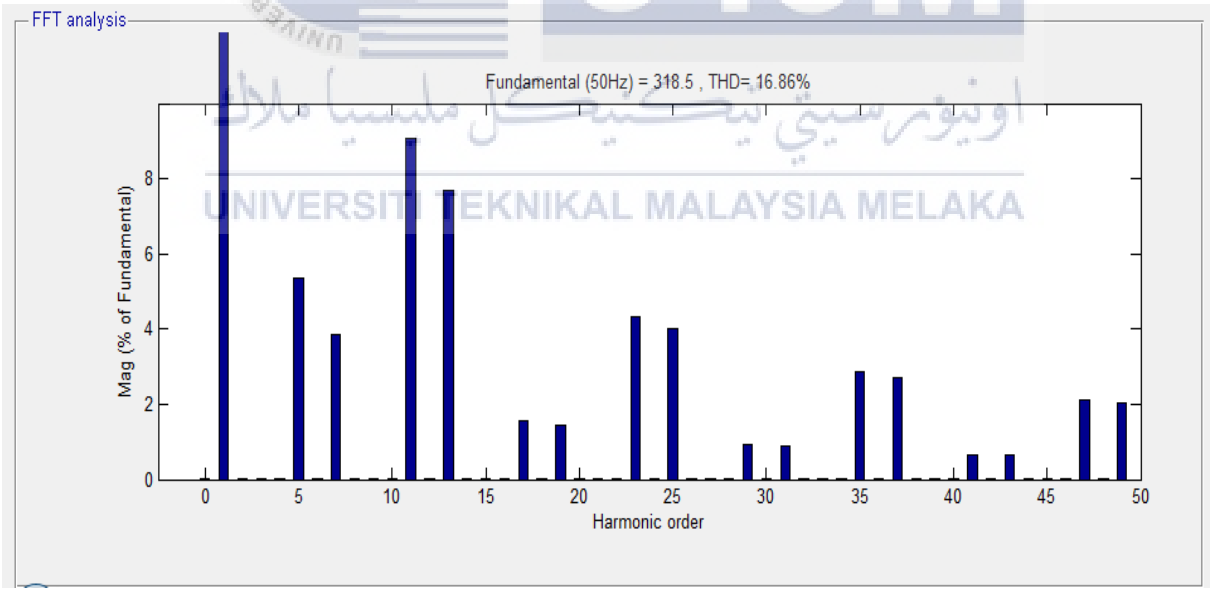

Figure 4.13: Harmonic spectrum of optimization voltage output waveform for five level CHB-MLI with MI = 0.84

Figure 4.14 illustrate the result of optimization for the current output waveform of five level CHB-MLI. The smooth output current waveform of the CHB-MLI can be obtain from the accurate calculation of switching angles. Figure 4.15 display the harmonic spectrum of optimization current output waveform for five level CHB-MLI. The percentage of THD can be obtain via the harmonic spectrum where the value of the THD is equal to 2.53%. The harmonic contents in the simulation was refer to the value of THD obtain.

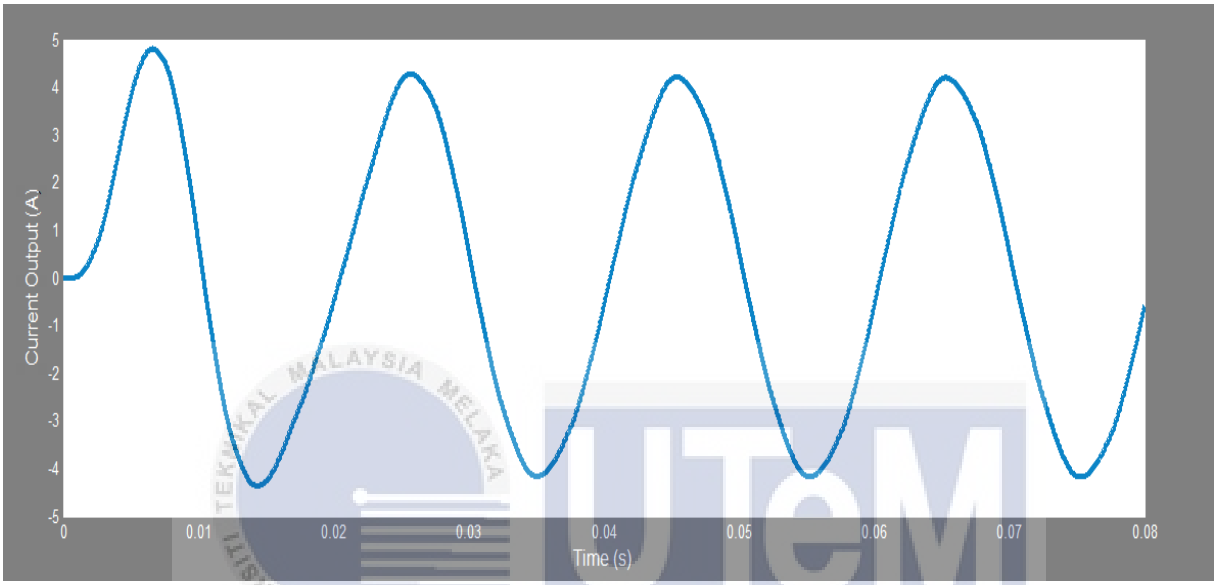

Figure 4.14: Output current waveform of optimization five level CHB-MLI with MI = 0.84

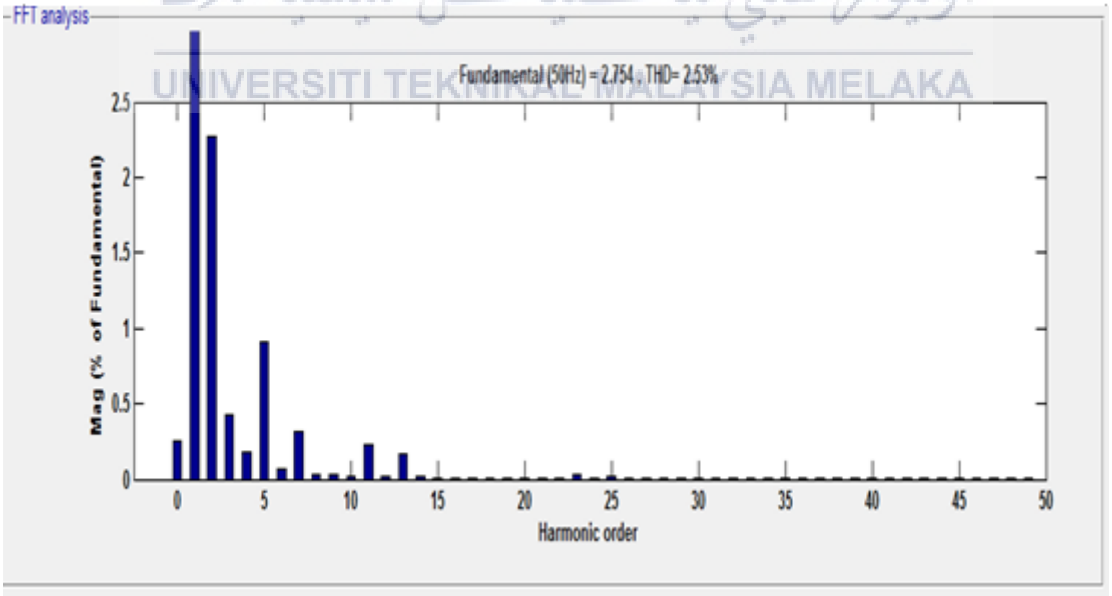

Figure 4.15: Harmonic spectrum of optimization current output waveform for five level CHB-MLI with MI = 0.84

4.2.4 Simulation Results for Non-Optimization of a Single Phase Five-Level CHB-MLI design with MI = 0.68

Figure 4.16(a) and Figure 4.16(b) represent the switching waveform for non-optimization five level CHB-MLI where there are eight switches which are S1, S2, S3, S4 for upper switching and S5, S6, S7, S8 for lower switching has been used in this simulation circuit. Each switch produce different waveform in order to operate the simulation circuit. There are two part of switching waveform in this simulation circuit which are waveform for upper switching and lower switching where the waveform for upper switching. The switching angles Θ_1 = 8.77° and Θ2 = 68.16° has been used in this simulation where the switching angles has been obtain using mathematical switching equation.

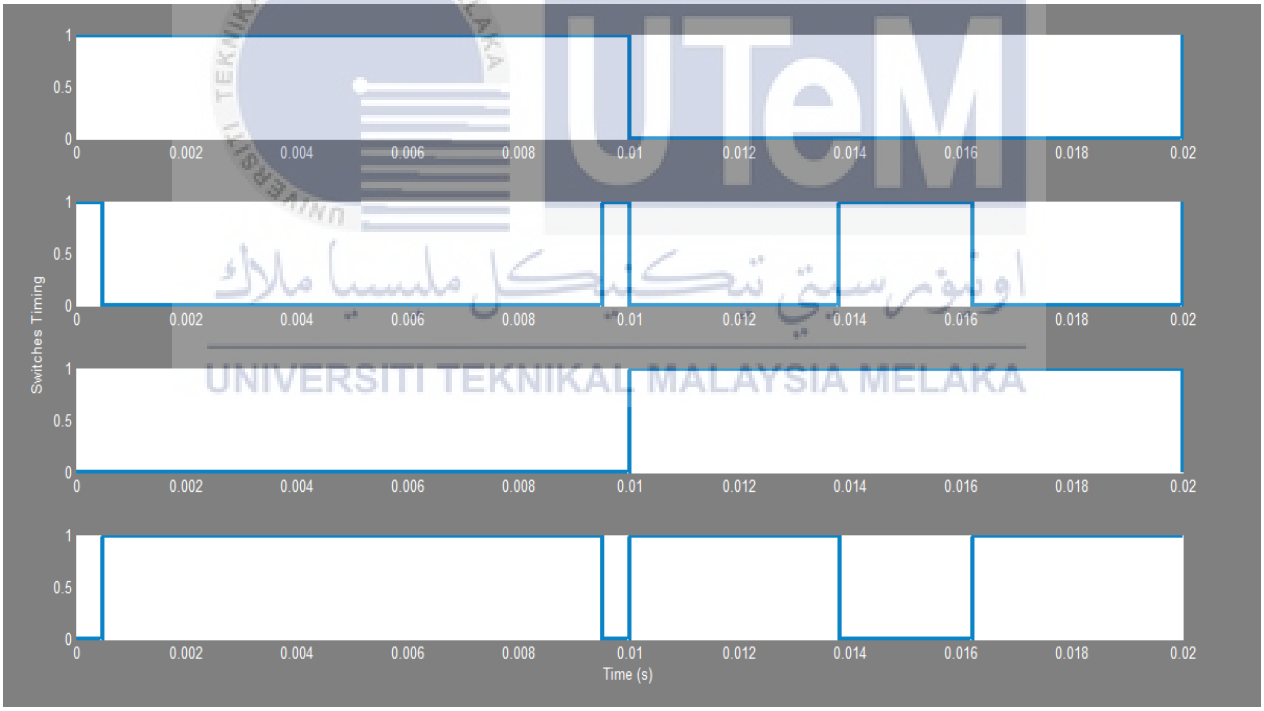

Figure 4.16(a): Upper switching waveform for non-optimization five-level CHB-MLI with MI = 0.68 for Θ_1 = 8.77° and Θ2 = 68.16°

Figure 4.16(b): Lower switching waveform for non-optimization five-level CHB-MLI with MI =0.68

The non-optimization five level CHB-MLI has been simulated at MI = 0.68 and the switching angles Θ_1 = 8.77° and $\Theta 2$ = 68.16° has been used. This simulation use the duration of time equal to 0.02s for each cycle. Figure 4.17 and Figure 4.18 represents the output voltage waveform of non-optimization three level CHB-MLI and harmonic spectrum for voltage output waveform respectively. Based on the harmonic spectrum, the percentage of THD can be obtain which the value is equal to 29.53%. The harmonic contents in the simulation was refer to the value of THD obtain.

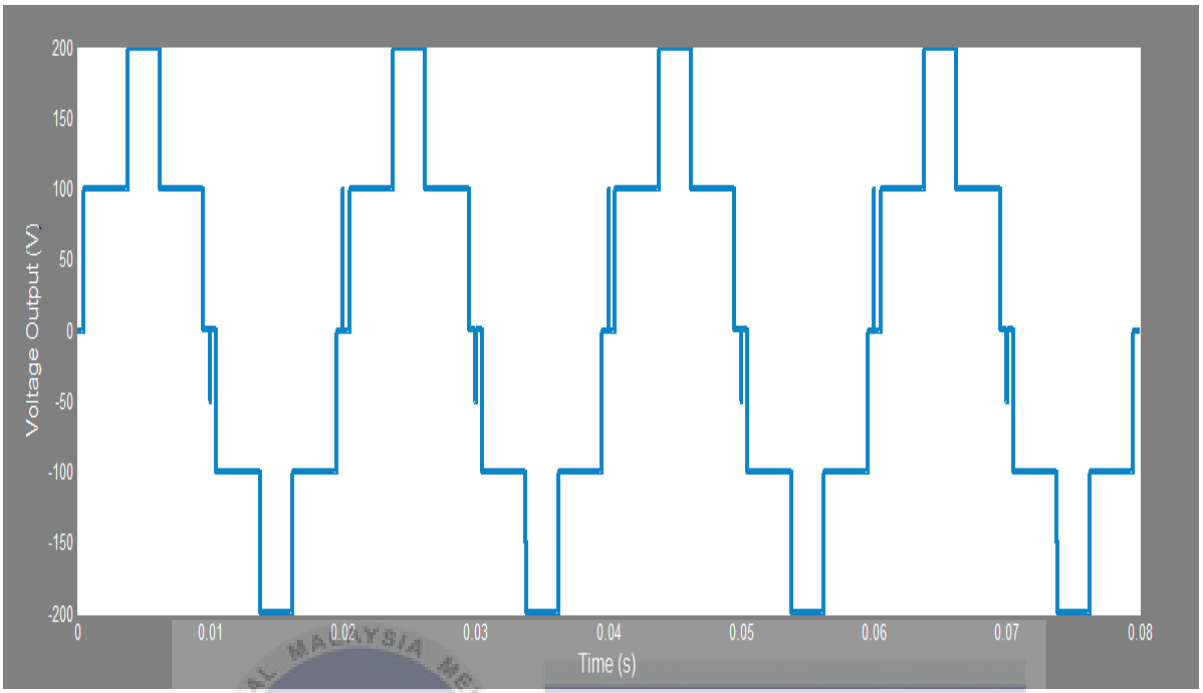

Figure 4.17: Output voltage waveform of non-optimization five level CHB-MLI with MI = 0.68

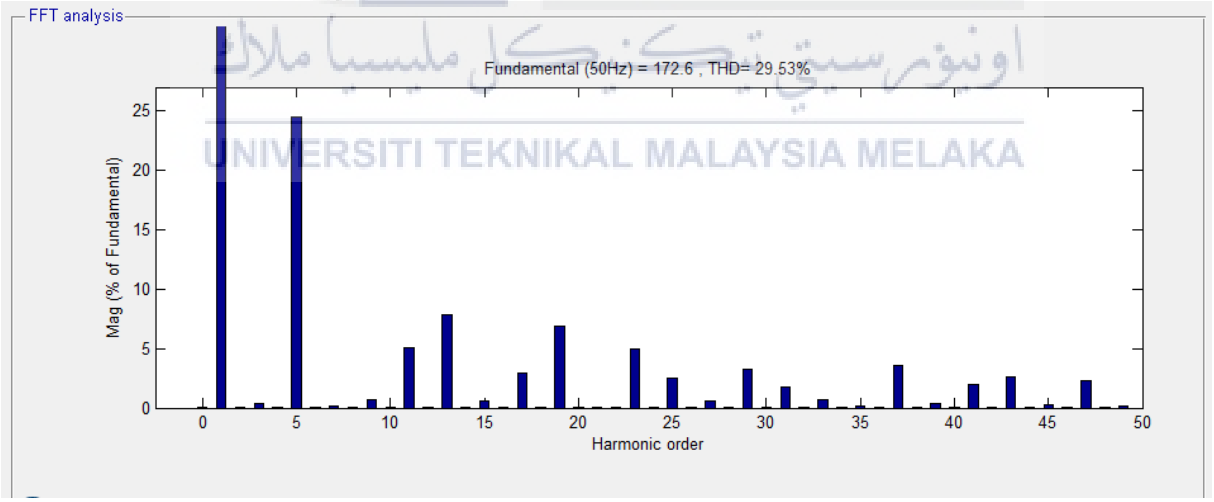

Figure 4.18: Harmonic spectrum of non-optimization voltage output waveform for five level CHB-MLI with MI = 0.68

Figure 4.19 illustrate the result of non-optimization for the current output waveform of five level CHB-MLI. The non-optimization output current waveform of the CHB-MLI not very smooth due to inaccurate calculation of switching angles. Figure 4.20 display the harmonic spectrum of optimization current output waveform for five level CHB-MLI. The percentage of THD can be obtain based on the harmonic spectrum where the value of the THD is equal to 6.48%. The harmonic contents in the simulation was refer to the value of THD obtain.

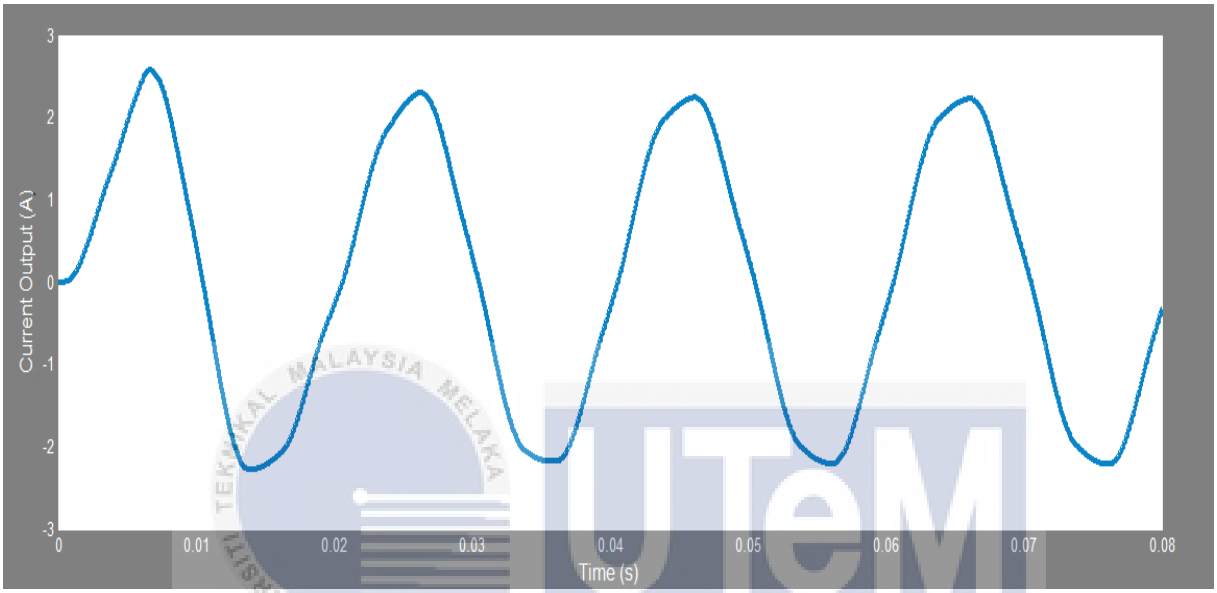

Figure 4.19: Output current waveform of non-optimization five level CHB-MLI with MI = 0.68

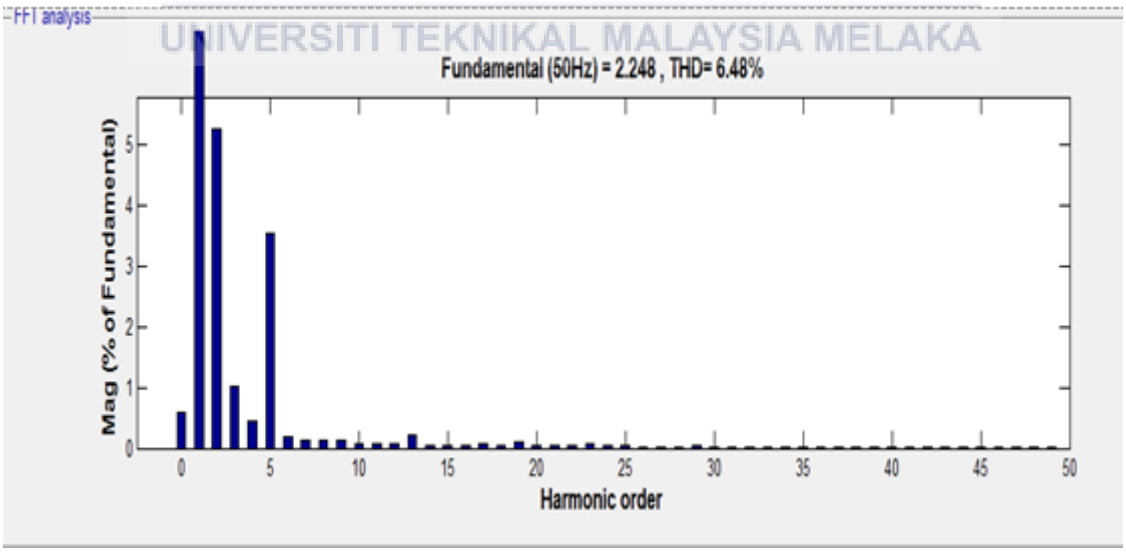

Figure 4.20: Harmonic spectrum of non-optimization output current waveform for five level CHB-MLI with MI = 0.68

4.3 Experimental Hardware Results of a Single Phase Three-level CHB-MLI with Different Value of MI

The experimental of the proposed hardware has been done in order to validate the performance for both multilevel inverters which are three and five level CHB-MLI. The function of proposed CHB-MLI interface with DSPTMS320F2812 was to obtain the waveform of the output prototype of three and five level CHB-MLI where the outputs are voltage output and current output. The switching signal has been produced by using DSPTMS320F2812 target board. Thus, the DSPTMS320F2812 was an important hardware in order to operate the CHB-MLI.

The source codes programming has been produced for three and five level CHB-MLI where the source codes was created based on Newton-Raphson technique. The production of source codes have two types which are optimization and non-optimization of three and five level CHB-MLI. The proposed source codes has been embedded into DSPTMS320F2812 which act as the switching scheme for the CHB-MLI. Hence, the source codes based on Newton-Raphson technique has been integrated by using DSPTMS320F2812 in order to operate the three and five level CHB-MLI.

The proposed CHB-MLI utilized the DC power supply because the main function of the inverter was to convert the DC source to AC source. Based on this experimental, the MI that has been used are 0.84 for optimization and 0.68 for non-optimization. The switching frequency which used to execute the experiment was 1 kHz. The value of DC voltage that has been supply for the CHB-MLI was 150V and the value of connected loads were R = 100kΩ and L = 5mH. This experiment used 2 milliseconds as one period which is equal to one cycle.

4.3.1 Experimental Results for Optimization Single Phase Three-level CHB-MLI with (MI = 0.84)

The switching operation for the optimization of three-level CHB-MLI with MI = 0.84 has been described by using source code as shown in Appendix (I). The switching angles that has been used to operate this CHB-MLI was $\Theta_1 = 17.06°$ and $\Theta_2 = 43.53°$. The source code then has been embedded into DSPTMS320F2812 in order to operate the CHB-MLI. The switching waveform for optimization three- level CHB-MLI at $\Theta_1 = 17.06°$ and $\Theta_2 = 43.53°$ was as illustrate in Figure 4.21.

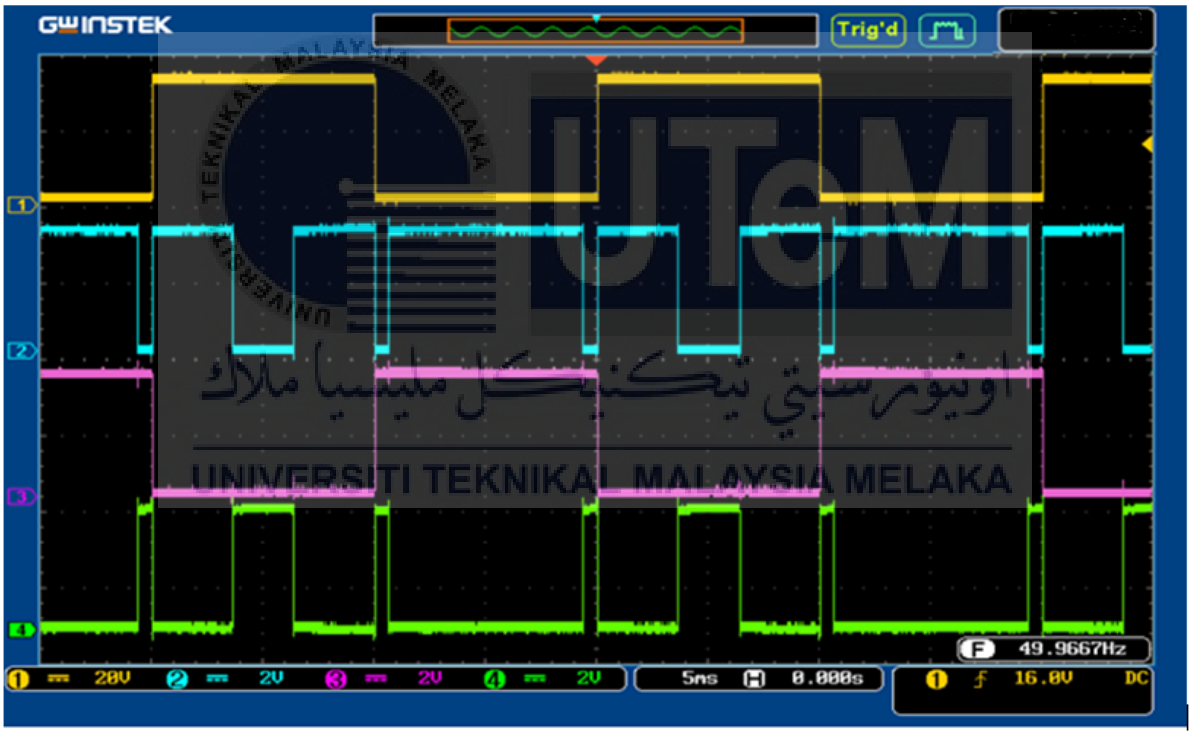

Figure 4.21: Switching waveform for optimization three- level CHB-MLI with MI = 0.84 at $\Theta_1 = 17.06°$ and $\Theta_2 = 43.53°$

The output voltage waveform for optimization of three-level CHB-MLI was as represent in Figure 4.22. The voltage waveform was smoother compared to non-optimization three-level CHB-MLI but less smooth compared to five level CHB-MLI. Hence, the value of THD can be obtain via the harmonic spectrum of voltage output waveform for optimization three-level CHB-MLI where the value of THD was equal to 32.4% as shown in Figure 4.23.

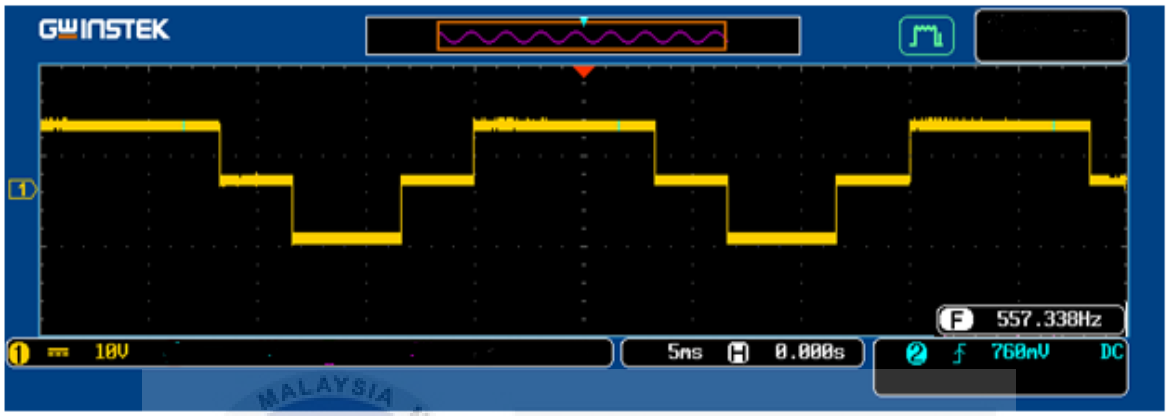

Figure 4.22: Output voltage waveform for optimization of three-level CHB-MLI

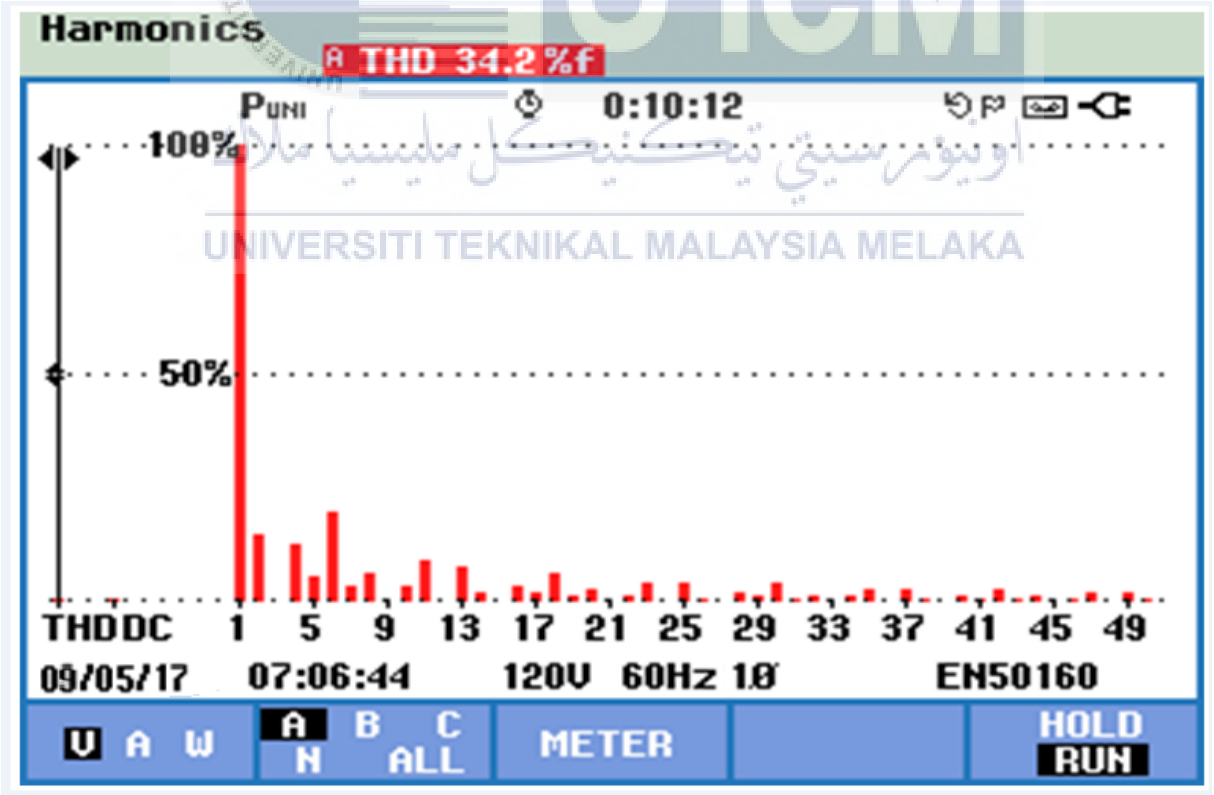

Figure 4.23: Harmonic spectrum of voltage output waveform for optimization of three-level CHB-MLI

Figure 4.24 represent the current output waveform for optimization of three-level CHB-MLI where the waveform was smoother compared to non-optimization three-level CHB-MLI but less smooth compared to five-level CHB-MLI. The harmonic spectrum of the current output waveform for optimization of three-level CHB-MLI was as display in Figure 4.25. The value of THD for the output current can be achieved from the harmonic spectrum where the value of THD was 11.8%.

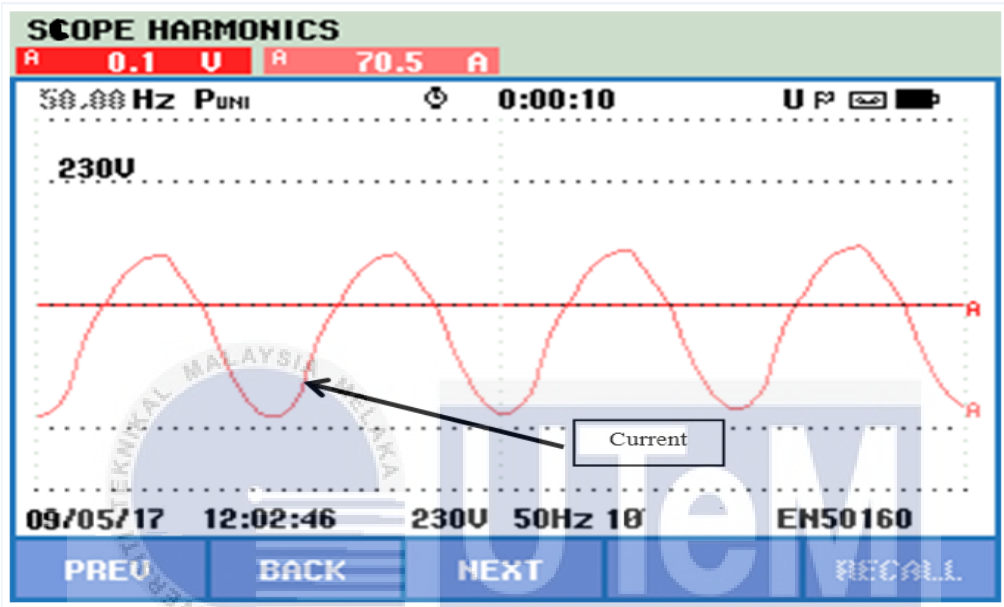

Figure 4.24: Current output waveform for optimization of three-level CHB-MLI

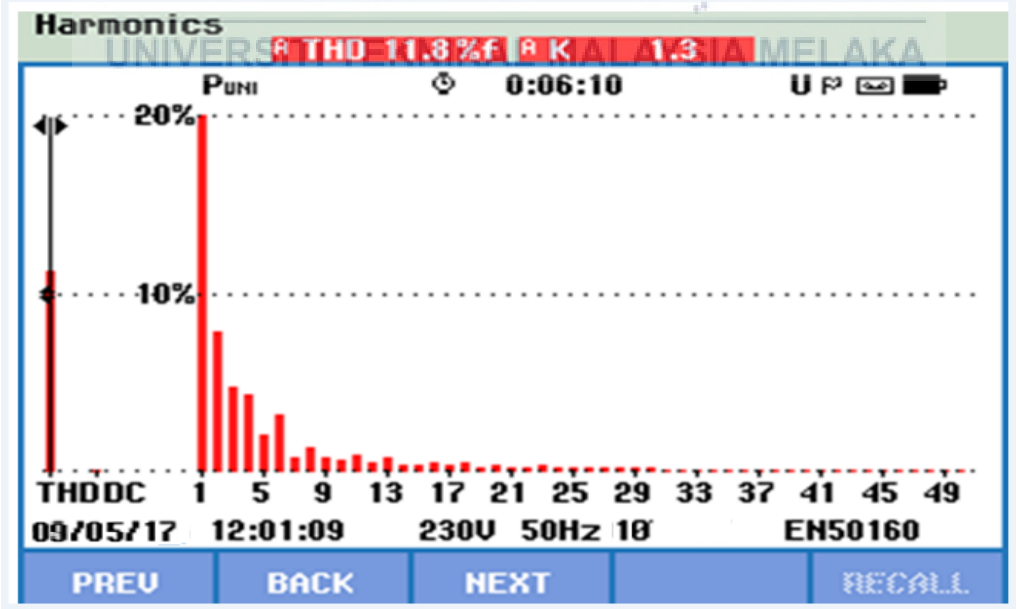

Figure 4.25: Harmonic spectrum of the current output waveform for optimization of three-level CHB-MLI

4.3.2 Experimental Results for Non-Optimization Single Phase Three-level CHB-MLI with (MI = 0.68)

The switching operation for the optimization of three-level CHB-MLI with MI = 0.68 has been described by using source code as shown in Appendix (II). The switching angles that has been used to operate this CHB-MLI was Θ1 = 8.77° and Θ2 = 68.16°. The source code then has been embedded into DSPTMS320F2812 in order to operate the CHB-MLI. The switching waveform for optimization three- level CHB-MLI at Θ1 = 8.77° and Θ2 = 68.16° was as illustrate in Figure 4.26.

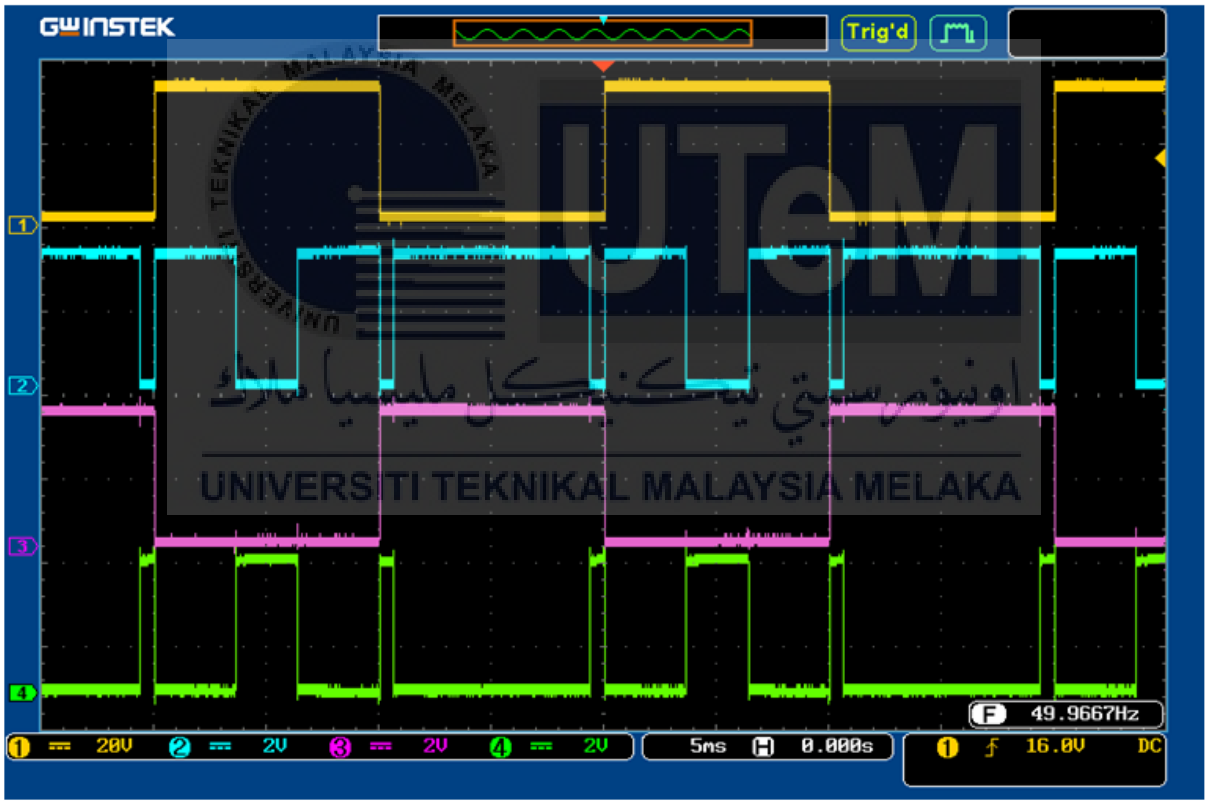

Figure 4.26: Switching waveform for non-optimization three- level CHB-MLI with MI = 0.68 at Θ1 = 8.77° and Θ2 = 68.16°

The output voltage waveform for non-optimization of three-level CHB-MLI was as shown in Figure 4.27. The voltage waveform was less smooth compared to optimization three-level CHB-MLI and five level CHB-MLI. Therefore, the value of THD can be achieved via the harmonic spectrum of voltage output waveform for non-optimization three-level CHB-MLI where the value of THD was equal to 48.4% as shown in Figure 4.28.

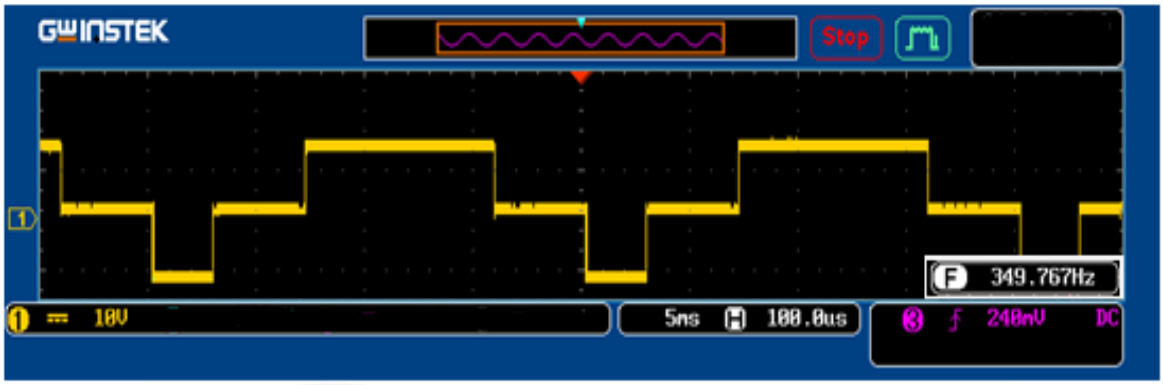

Figure 4.27: Output voltage waveform for non-optimization of three-level CHB-MLI

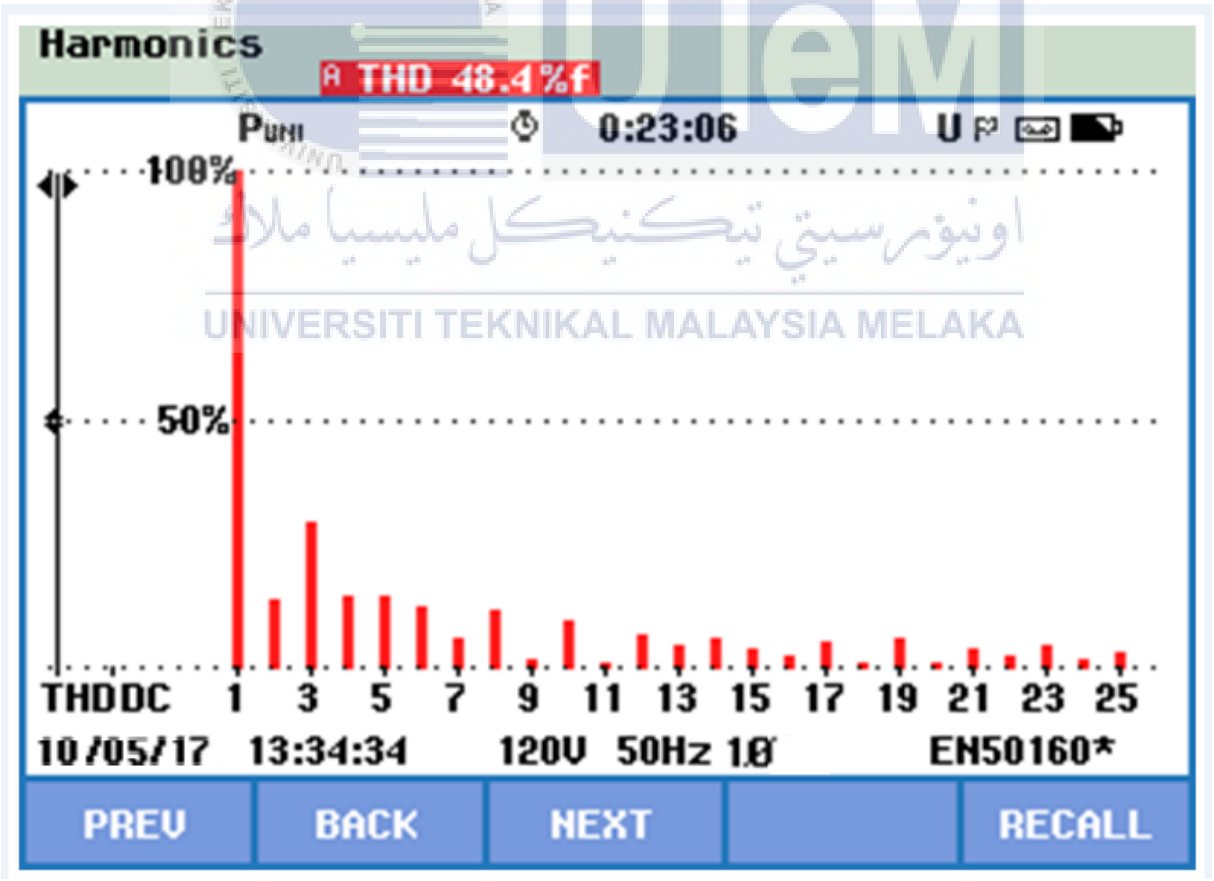

Figure 4.28: Harmonic spectrum of voltage output waveform for non-optimization three-level CHB-MLI

Figure 4.29 represent the current output waveform for non-optimization of three-level CHB-MLI where the waveform was less smooth compared to optimization of three-level CHB-MLI and five-level CHB-MLI. The harmonic spectrum of the current output waveform for non-optimization of three-level CHB-MLI was as display in Figure 4.25. The value of THD for the output current can be achieved from the harmonic spectrum where the value of THD was 13.3%.

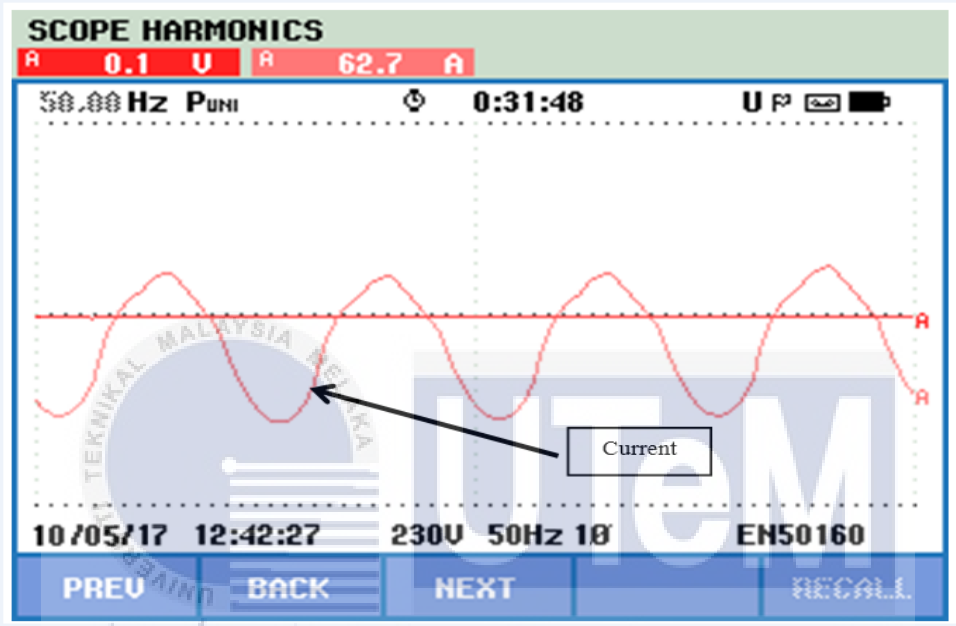

Figure 4.29: Current output waveform for non-optimization of three-level CHB-MLI

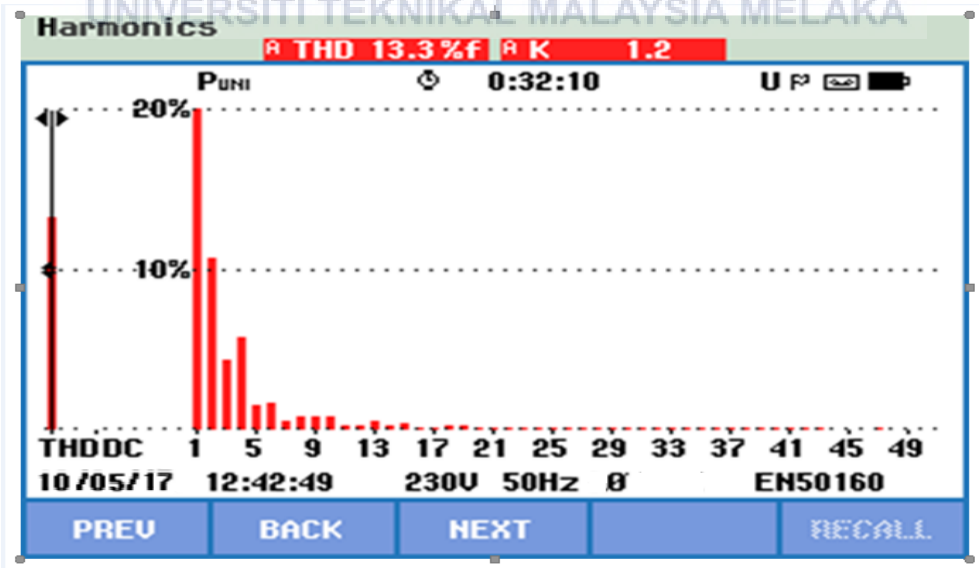

Figure 4.30: Harmonic spectrum of the current output waveform for non-optimization of three-level CHB-MLI

4.3.3 Experimental Results for Optimization Single Phase Five-Level CHB-MLI with (MI = 0.84)

The switching operation for the optimization of five-level CHB-MLI with MI = 0.84 has been defined by using source code as shown in Appendix (III). The switching angles that has been used to operate this CHB-MLI was $\Theta_1 = 17.06°$ and $\Theta_2 = 43.53°$. The source code then has been stored into DSPTMS320F2812 in order to operate the CHB-MLI. There are two parts of switching which are upper switching and lower switching The switching waveform for optimization five-level CHB-MLI at $\Theta_1 = 17.06°$ and $\Theta_2 = 43.53°$ as represent in Figure 4.31(a) and Figure 4.31(b).

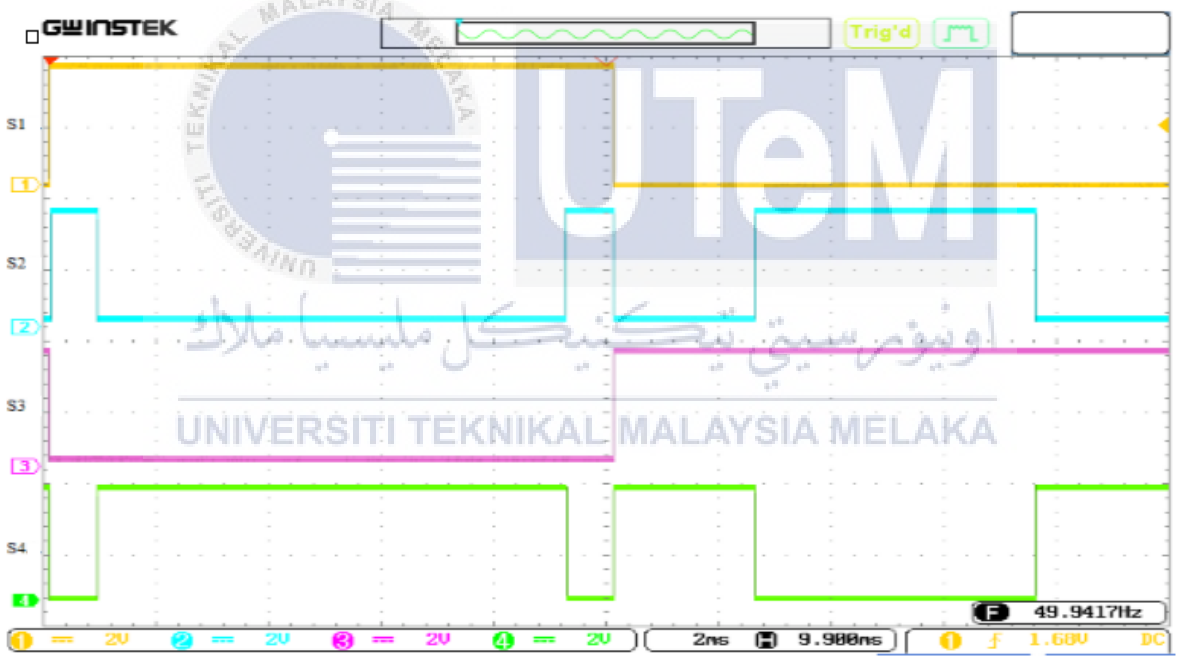

Figure 4.31(a): Upper switching waveform for optimization of five-level CHB-MLI with MI = 0.84 at $\Theta_1 = 17.06°$ and $\Theta_2 = 43.53°$

Figure 4.31(b): Lower switching waveform for optimization of five-level CHB-MLI with MI = 0.84 at Θ_1 = 17.06° and Θ_2 = 43.53°

The output voltage waveform for optimization of five-level CHB-MLI was as shown in Figure 4.32. The voltage output waveform was very smooth compared to non-optimization five-level CHB-MLI because of the accurate calculation of switching angles. Therefore, the value of THD can be obtain via the harmonic spectrum of voltage output waveform for optimization five-level CHB-MLI where the value of THD was equal to 15.6% as shown in Figure 4.33.

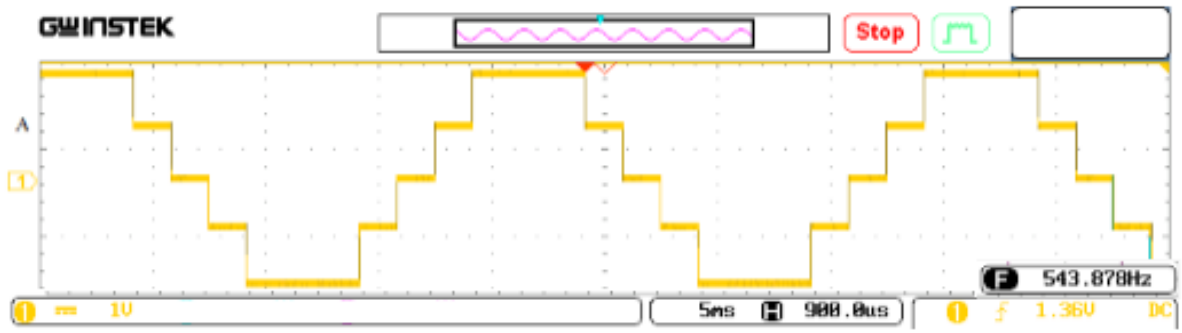

Figure 4.32: Output voltage waveform for optimization of five-level CHB-MLI

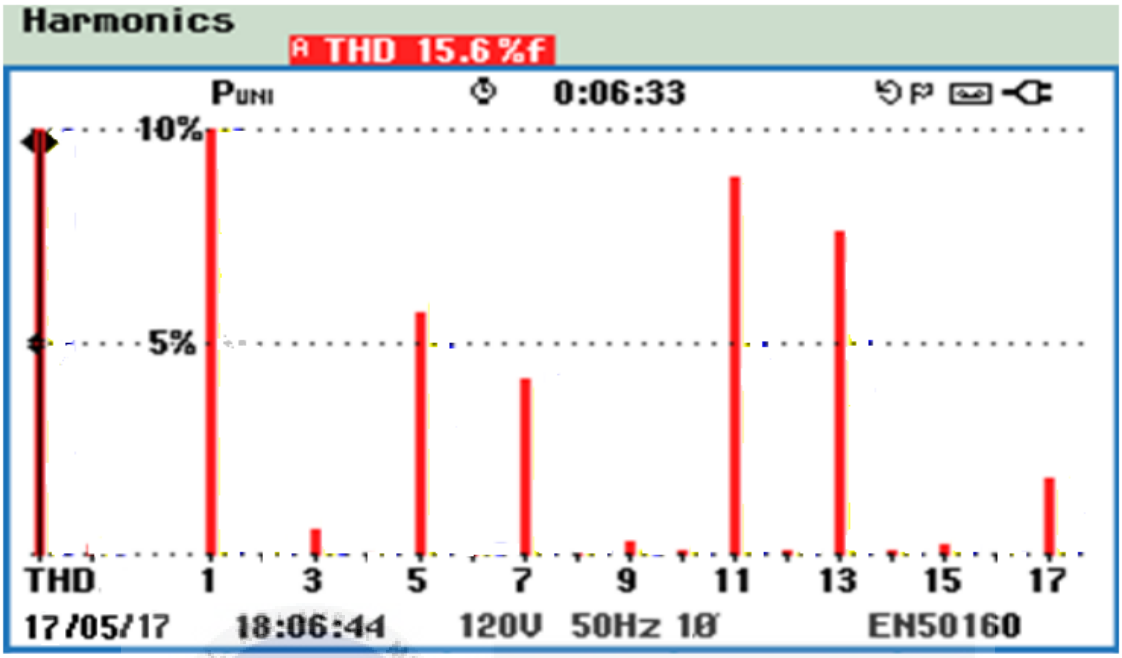

Figure 4.33: Harmonic spectrum of voltage output waveform for optimization five-level CHB-MLI

The current and voltage output waveform for optimization of five-level CHB-MLI were illustrated in Figure 4.34 where the current and voltage output waveform was very smooth compared to non-optimization five-level CHB-MLI due to the accurate calculation of switching angles. The harmonic spectrum of the current output waveform for optimization of five-level CHB-MLI was as represent in Figure 4.35. The value of THD for the output current can be obtained from the harmonic spectrum where the value of THD was 3.9%.

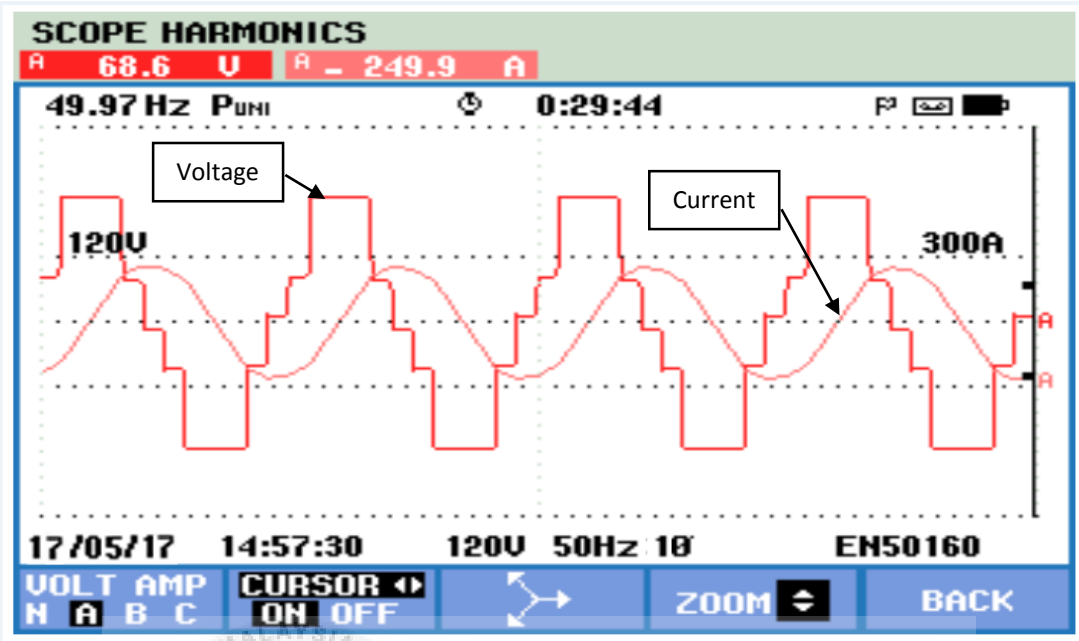

Figure 4.34: Current and voltage output waveform for optimization of five-level CHB-MLI

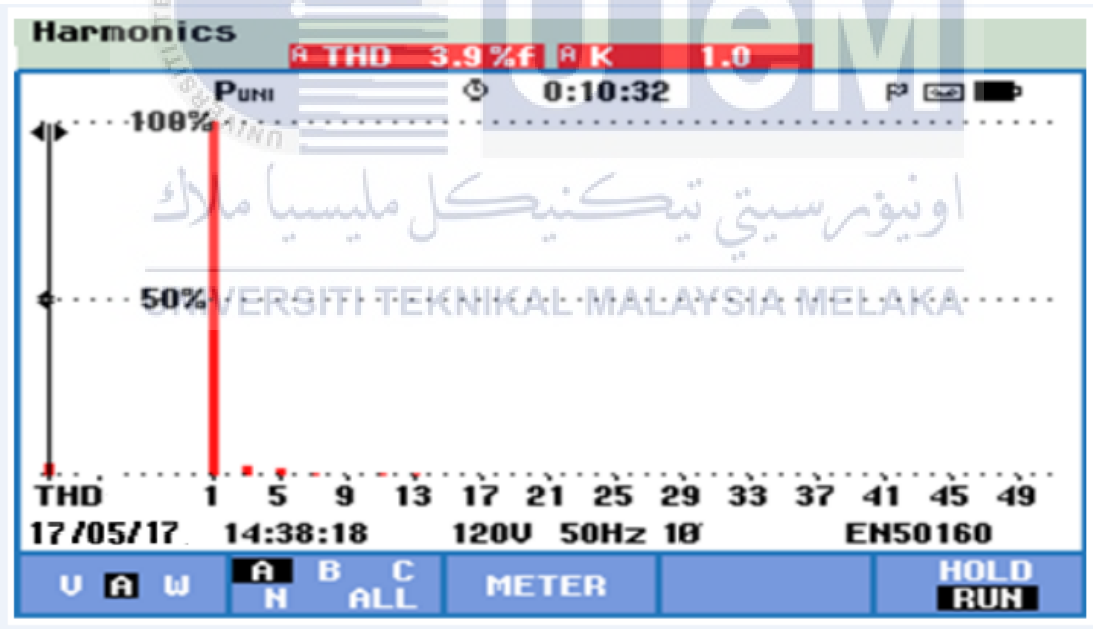

Figure 4.35: Harmonic spectrum of the current output waveform for optimization of five-level CHB-MLI

4.3.4 Experimental Results for Non-Optimization Single Phase Five-Level CHB-MLI with (MI = 0.68)

The switching operation for the non-optimization of five-level CHB-MLI with MI = 0.68 has been defined by using source code as shown in Appendix (IV). The switching angles that has been used to operate this CHB-MLI was Θ1 = 8.77° and Θ2 = 68.16°. The source code then has been stored into DSPTMS320F2812 in order to operate the CHB-MLI. There are two parts of switching which are upper switching and lower switching The switching waveform for non-optimization five-level CHB-MLI at Θ1 = 8.77° and Θ2 = 68.16° as represent in Figure 4.36(a) and Figure 4.36(b).

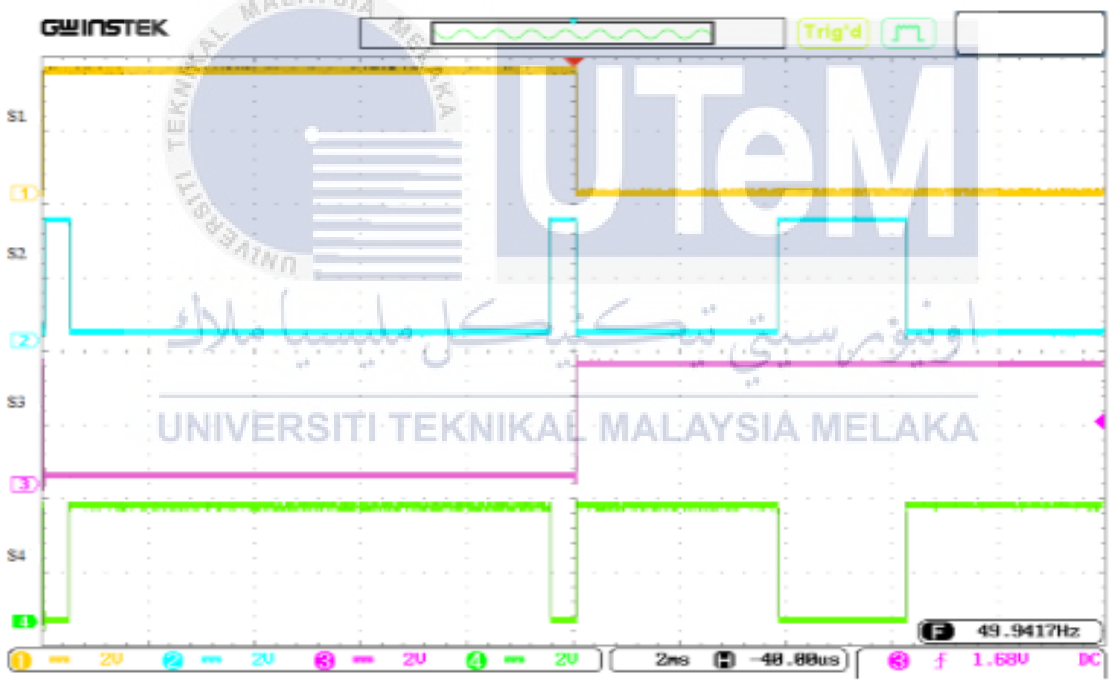

Figure 4.36(a): Upper switching waveform for non-optimization of five-level CHB-MLI with MI = 0.68 at Θ_1 = 8.77° and Θ_2 = 68.16°

Figure 4.36(b): Lower switching waveform for non-optimization of five-level CHB-MLI with MI = 0.68 at Θ_1 = 8.77° and Θ_2 = 68.16°

The output voltage waveform for non-optimization of five-level CHB-MLI was as illustrated in Figure 4.37. The voltage output waveform was less smooth compared to optimization five-level CHB-MLI because of the inaccurate calculation of the switching angles. Thus, the value of THD can be acquired form the harmonic spectrum of voltage output waveform for non-optimization five-level CHB-MLI where the value of THD was equal to 28.5% as shown in Figure 4.38.

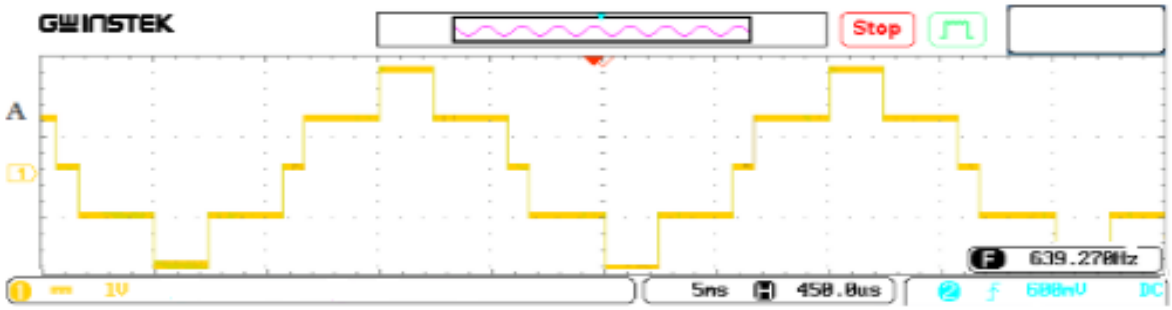

Figure 4.37: Output voltage waveform for non-optimization of five-level CHB-MLI

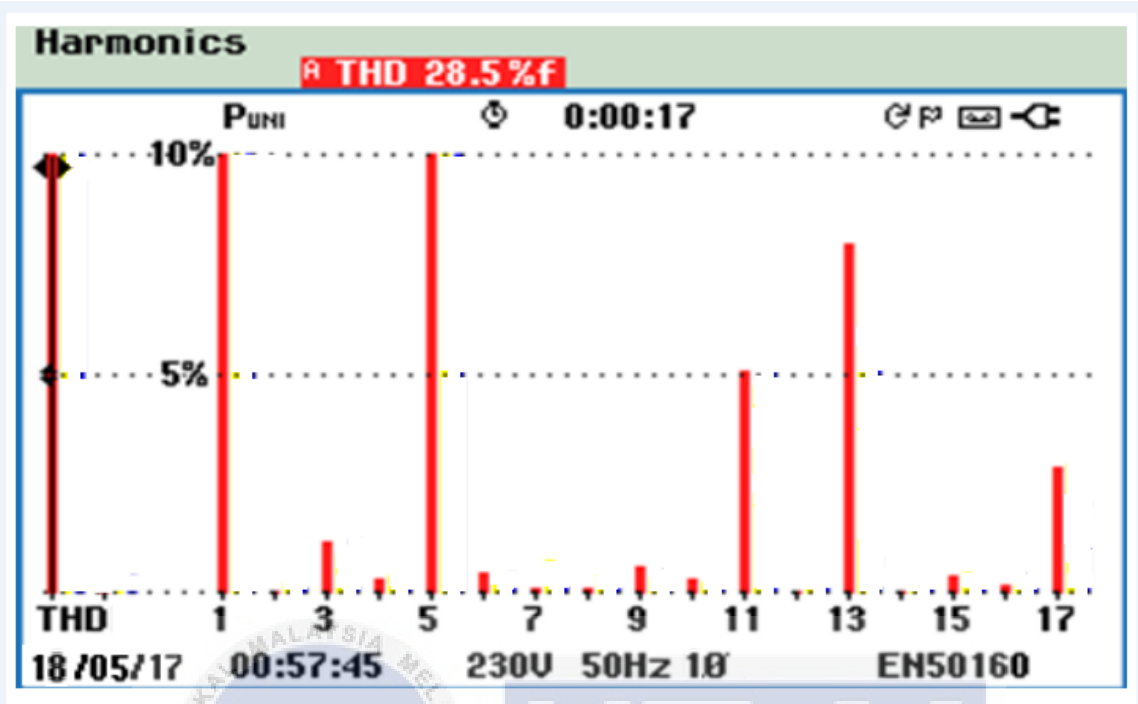

Figure 4.38: Harmonic spectrum of voltage output waveform for non-optimization five-level CHB-MLI

The current and voltage output waveform for non-optimization of five-level CHB-MLI were demonstrate in Figure 4.39 where the current and voltage output waveform was less smooth compared to optimization five-level CHB-MLI due to the inaccurate calculation of the switching angles. The harmonic spectrum of the current output waveform for non-optimization of five-level CHB-MLI was as represent in Figure 4.40. The value of THD for the output current can be attained from the harmonic spectrum where the value of THD was 6.6%.

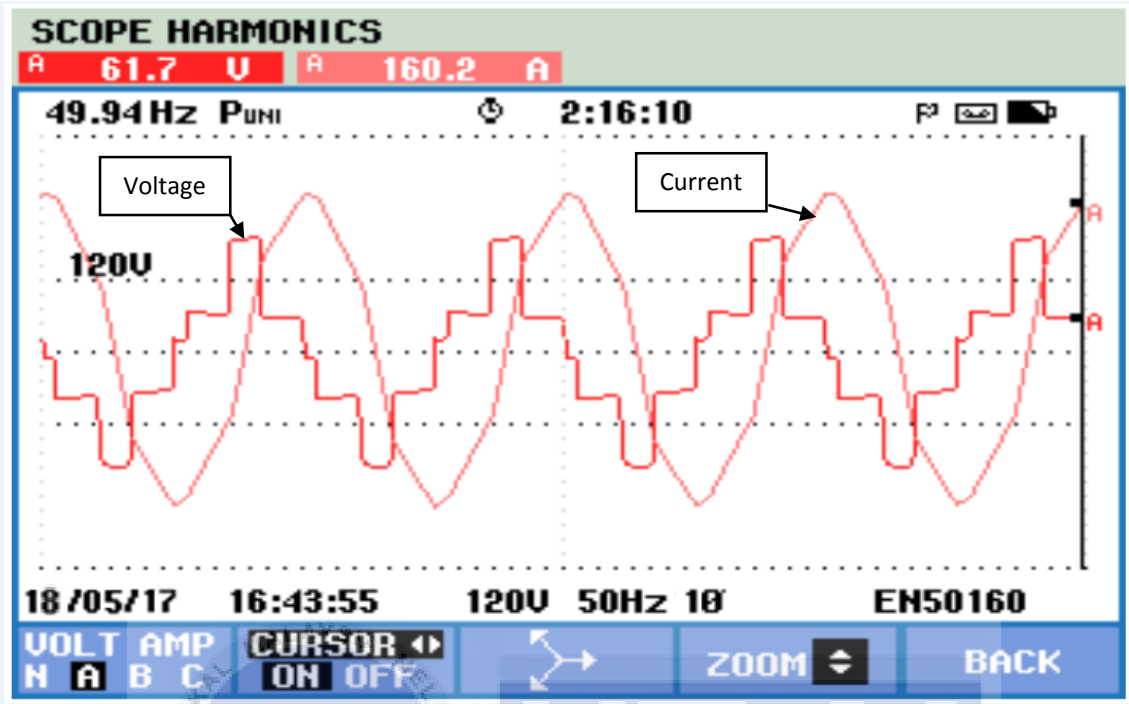

Figure 4.39: Current and voltage output waveform for non-optimization of five-level CHB-MLI

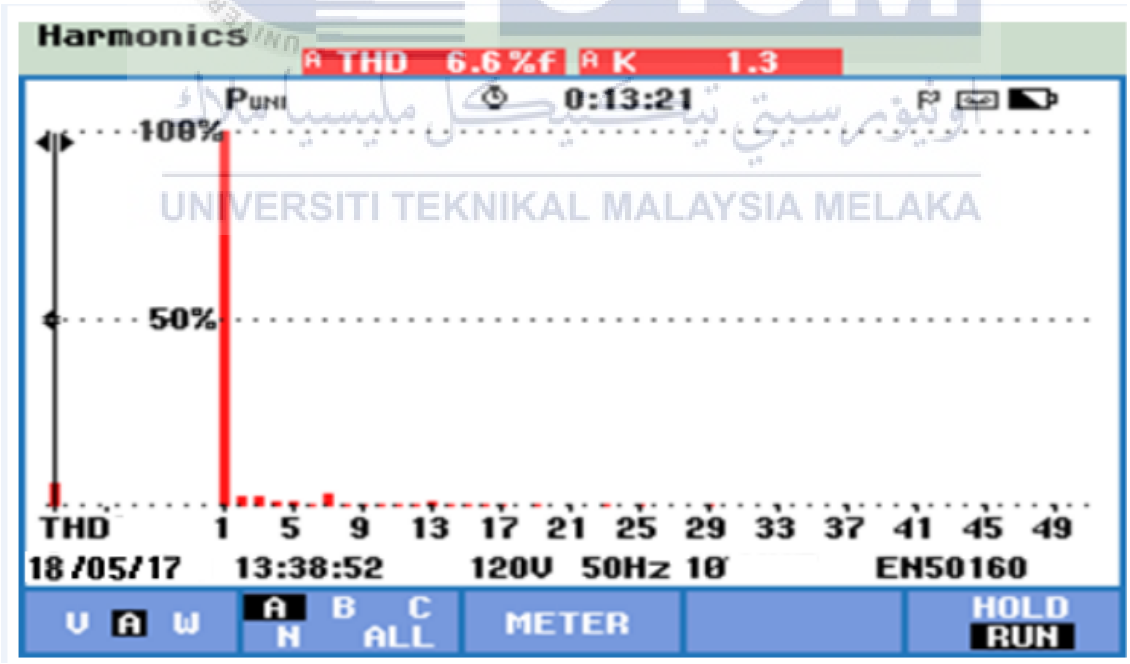

Figure 4.40: Harmonic spectrum of the current output waveform for non-optimization of five-level CHB-MLI

4.4 Performance Comparison of Simulation and Experimental Results of Three and Five level CHB-MLI with Difference Value of MI

Table 4.1 represent the performance comparison between simulation and experimental results of three and five level CHB-MLI with different value of MI. Based on the results shown in the Table 4.1, the simulation and experimental results of THD_V and THD_i are quite similar. Therefore, the value of THD that has been obtain from simulation and experimental can be used to compare the performance of the proposed CHB-MLI. Based on this research, the highest performance among the proposed CHB-MLI was optimization of single phase five-level CHB-MLI with MI = 0.84.

Results	Simulation Results		Hardware Results	
CHB-MLI	3-level	5-level	3-level	5-level
THD_V (%) (MI = 0.84)	35.55	16.86	32.4	15.6
THD_i (%) (MI = 0.84)	11.49	2.53	11.8	3.9
THD_V (%) (MI = 0.68)	48.62	29.53	48.4	28.5
THD_i (%) (MI = 0.68)	13.40	6.48	13.3	6.6

Table 4.1: Performance comparison of simulation and experimental results of three and five level CHB-MLI with different value of MI

4.5 Summary of the Results

The analysis of simulations and experimental has been done successfully in this chapter. The study of the simulation design of three and five level CHB-MLI by using MATLAB/SIMULINK has been done in order to obtain the results for this project. Besides that, the concept of Newton-Raphson technique also has been applied in this research in order to get the switching angles. Then, the parameters based on the simulation design has been used in the hardware prototypes of three and five level CHB-MLI. The coding based on Newton-Raphson technique has been embedded into DSPTMS320F2812 and the coding will integrate by the DSPTMS320F2812 in order to operate the proposed prototypes of CHB-MLI. Therefore, the experimental results were obtained based experiment that has been done. The performance of the proposed CHB-MLI has been certified based on the output voltage, output current, and the value of the THD.

CHAPTER 5

CONCLUSION AND RECOMMENDATION

5.1 Conclusion

As the conclusion, the main focus for this project to minimize harmonic of a single phase cascaded H-bridge multilevel inverter had achieved based on the experimental and simulation results. Three and five level CHB-MLI was successfully designed and obtain the results from the simulation by using MATLAB/SIMULINK. Both prototypes of three and five level CHB-MLI has been analyze based on the parameters from the simulation where the value for the modulation index (MI) that has been used in these research were 0.84 for optimization and 0.68 for non-optimization. Newton-Raphson technique controller has been used in order to perform both simulation and hardware for three and five level CHB-MLI. The Newton-Raphson technique angle calculation for optimization and non-optimization three and five level CHB-MLI has been described clearly in chapter 3.

Based on the results achieved in chapter 4, the simulation and experimental results demonstrate that the higher level of the multilevel inverter will create lower harmonics contents where the harmonics contents will be determined by the value of the THD. Thus, the lower the value of THD, the lower the harmonic contents of the CHB-MLI. The THD for the output voltage and current represent the harmonics contents in electrical power system which the performance of CHB-MLI will be better if both harmonics contents in voltage and current were low.

5.2 Recommendation

Total harmonic distortion (THD) of single phase three and five level CHB-MLI has been compared and the highest performance among the proposed CHB-MLI was optimization of a single phase five-level CHB-MLI. The accurate calculation of switching angles cause the optimization five-level CHB-MLI has the highest performance among the others proposed CHB-MLI where the value of MI used was 0.84. Next, the simulation and experimental results has been done in order to strengthen the statement about the comparison of performance of three and five level CHB-MLI. The value of total harmonic distortion of voltage (THD_V) and total harmonic distortion (THD_i) has been obtain for the proposed CHB-MLI in the simulation and experimental results.

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APPENDIX

I – SOURCE CODE Optimization Three-Level CHB-MLI (MI=0.84)

```
#include "DSP281x_Device.h"     // DSP281x Headerfile Include File
#include "DSP281x_Examples.h"   // DSP281x Examples Include File
void Gpio_select(void);
// Prototype statements for functions found within this file.
interrupt void cpu_timer0_isr(void);


unsigned int i1, k1;

void main(void)
{
        Gpio_select();          // Setup the GPIO Multiplex Registers

  InitSysCtrl();

  DINT;

  InitPieCtrl();

// Disable CPU interrupts and clear all CPU interrupt flags:
  IER = 0x0000;
  IFR = 0x0000;

  InitPieVectTable();

// Interrupts that are used in this example are re-mapped to
// ISR functions found within this file.
  EALLOW;  // This is needed to write to EALLOW protected registers
  PieVectTable.TINT0 = &cpu_timer0_isr;
  EDIS;    // This is needed to disable write to EALLOW protected registers


  InitCpuTimers();   // For this example, only initialize the Cpu Timers

// Configure CPU-Timer 0 to interrupt every second:
// 100MHz CPU Freq, 20 usec Period (in uSeconds)
  ConfigCpuTimer(&CpuTimer0, 150, 10);
  StartCpuTimer0();

// Step 5. User specific code, enable interrupts:
```

```
// Enable CPU INT1 which is connected to CPU-Timer 0:
   IER |= M_INT1;

// Enable TINT0 in the PIE: Group 1 interrupt 7
   PieCtrlRegs.PIEIER1.bit.INTx7 = 1;

// Enable global Interrupts and higher priority real-time debug events:
   EINT;   // Enable Global interrupt INTM
   ERTM;   // Enable Global realtime interrupt DBGM

// Step 6. IDLE loop. Just sit and loop forever (optional):
    for(;;);

}

interrupt void cpu_timer0_isr(void)
{
   CpuTimer0.InterruptCount++;
          i1 = CpuTimer0.InterruptCount-1;
   PieCtrlRegs.PIEACK.all = PIEACK_GROUP1;


    S1
    if (i1<=1000) {GpioDataRegs.GPBDAT.bit.GPIOB8=1;}

    if (i1>1000)  {GpioDataRegs.GPBDAT.bit.GPIOB8=0;}

   S2
   if ((i1>84 && i1<916 || i1>1000) && i1<11250||(i1>1750 && i1<=2000))
       {GpioDataRegs.GPADAT.bit.GPIOA1=0;}
          if ((i1>=1 && i1<=84)||(i1>=916 && i1<=1000)||(i1>=1250 && i1<=1750))
             {GpioDataRegs.GPADAT.bit.GPIOA1=1;}

    S3
    if   (i1<=1000)
       {GpioDataRegs.GPADAT.bit.GPIOA2=0;}
          if   (i1>1000) // S3
             {GpioDataRegs.GPADAT.bit.GPIOA2=1;}

    S4
    if ((i1<84)||(i1>916 &&i1<=1000)||(i1>1250 && i1<=1750))
       {GpioDataRegs.GPADAT.bit.GPIOA3=0;}
          if ((i1>=84 && i1<=916)||(i1>1000 && i1<=1250)||(i1>1750 && i1<=2000))
             {GpioDataRegs.GPADAT.bit.GPIOA3=1;}  //S4

          if (CpuTimer0.InterruptCount>=2001)
            {CpuTimer0.InterruptCount=0;

}
```

```
void Gpio_select(void)
{
        EALLOW;
        GpioMuxRegs.GPAMUX.all = 0x0000;      //        choosing PORTA Pin's AS I/O
   GpioMuxRegs.GPBMUX.all = 0x0000;   //        choosing PORTB Pin's AS I/O

   GpioMuxRegs.GPADIR.all = 0xFFFF;   // A7-A0 output
   GpioMuxRegs.GPBDIR.all = 0xFFFF;   // B7-B0 output

 //   GpioDataRegs.GPADAT.bit.GPIOA13=1;
//    GpioDataRegs.GPADAT.bit.GPIOA9 =1;

   EDIS;
}
```

II – SOURCE CODE Non-Optimization Three-Level CHB-MLI (MI=0.68)


```
#include "DSP281x_Device.h"     // DSP281x Headerfile Include File
#include "DSP281x_Examples.h"   // DSP281x Examples Include File
void Gpio_select(void);
// Prototype statements for functions found within this file.
interrupt void cpu_timer0_isr(void);
unsigned int i1, k1;

void main(void)
{

        Gpio_select();          // Setup the GPIO Multiplex Registers



interrupt void cpu_timer0_isr(void)
{
  CpuTimer0.InterruptCount++;
        i1 = CpuTimer0.InterruptCount-1;
  PieCtrlRegs.PIEACK.all = PIEACK_GROUP1;


   S1
   if (i1<=1000) {GpioDataRegs.GPBDAT.bit.GPIOB8=1;}

   if (i1>1000)  {GpioDataRegs.GPBDAT.bit.GPIOB8=0;}

   S2
  if ((i1>49 && i1<952 || i1>1000) && i1<1379||(i1>1622 && i1<=2000))
```

```
      {GpioDataRegs.GPADAT.bit.GPIOA1=0;}
        if ((i1>=1 && i1<=49)||(i1>=952 && i1<=1000)||(i1>=1379 && i1<=1622))
          {GpioDataRegs.GPADAT.bit.GPIOA1=1;}

   S3
   if   (i1<=1000)
      {GpioDataRegs.GPADAT.bit.GPIOA2=0;}
        if   (i1>1000) // S3
          {GpioDataRegs.GPADAT.bit.GPIOA2=1;}

  S4
   if ((i1<49)||(i1>952 &&i1<=1000)||(i1>1380 && i1<=1622))
      {GpioDataRegs.GPADAT.bit.GPIOA3=0;}
        if ((i1>=49 && i1<=952)||(i1>1000 && i1<=1380)||(i1>1622 && i1<=2000))
          {GpioDataRegs.GPADAT.bit.GPIOA3=1;}  //S4


        if (CpuTimer0.InterruptCount>=2001)
          {CpuTimer0.InterruptCount=0;}

}

void Gpio_select(void)
{
        EALLOW;
        GpioMuxRegs.GPAMUX.all = 0x0000;      //        choosing PORTA Pin's AS I/O
   GpioMuxRegs.GPBMUX.all = 0x0000;   //        choosing PORTB Pin's AS I/O

   GpioMuxRegs.GPADIR.all = 0xFFFF;   // A7-A0 output
   GpioMuxRegs.GPBDIR.all = 0xFFFF;   // B7-B0 output

 //   GpioDataRegs.GPADAT.bit.GPIOA13=1;
//    GpioDataRegs.GPADAT.bit.GPIOA9 =1;

   EDIS;
}
```

III - SOURCE CODE Optimization Five-Level CHB-MLI (MI=0.84)

```
#include "DSP281x_Device.h"     // DSP281x Headerfile Include File
#include "DSP281x_Examples.h"   // DSP281x Examples Include File
void Gpio_select(void);
// Prototype statements for functions found within this file.
interrupt void cpu_timer0_isr(void);


unsigned int i1, k1;

void main(void)
{

        Gpio_select();          // Setup the GPIO Multiplex Registers

  InitSysCtrl();

  DINT;

  InitPieCtrl();

  IER = 0x0000;
  IFR = 0x0000;

  InitPieVectTable();

// Interrupts that are used in this example are re-mapped to
// ISR functions found within this file.
  EALLOW;  // This is needed to write to EALLOW protected registers
  PieVectTable.TINT0 = &cpu_timer0_isr;
  EDIS;    // This is needed to disable write to EALLOW protected registers

  InitCpuTimers();   // For this example, only initialize the Cpu Timers

// Configure CPU-Timer 0 to interrupt every second:
// 100MHz CPU Freq, 20 usec Period (in uSeconds)
  ConfigCpuTimer(&CpuTimer0, 150, 10);
  StartCpuTimer0();

  IER |= M_INT1;

// Enable TINT0 in the PIE: Group 1 interrupt 7
  PieCtrlRegs.PIEIER1.bit.INTx7 = 1;

// Enable global Interrupts and higher priority real-time debug events:
  EINT;   // Enable Global interrupt INTM
  ERTM;   // Enable Global realtime interrupt DBGM
```

```
   for(;;);

}

interrupt void cpu_timer0_isr(void)
{
  CpuTimer0.InterruptCount++;
        i1 = CpuTimer0.InterruptCount-1;
  PieCtrlRegs.PIEACK.all = PIEACK_GROUP1;


 S1
   if (i1<=1000) {GpioDataRegs.GPBDAT.bit.GPIOB8=1;}

   if (i1>1000)  {GpioDataRegs.GPBDAT.bit.GPIOB8=0;}

 S2
  if ((i1>84 && i1<916 || i1>1000) && i1<11250||(i1>1750 && i1<=2000))
      {GpioDataRegs.GPADAT.bit.GPIOA1=0;}
        if ((i1>=1 && i1<=84)||(i1>=916 && i1<=1000)||(i1>=1250 && i1<=1750))
{GpioDataRegs.GPADAT.bit.GPIOA1=1;}

 S3
   if   (i1<=1000)
      {GpioDataRegs.GPADAT.bit.GPIOA2=0;}
        if   (i1>1000) // S3
           {GpioDataRegs.GPADAT.bit.GPIOA2=1;}

 S4
  if ((i1<84)||(i1>916 &&i1<=1000)||(i1>1250 && i1<=1750))
      {GpioDataRegs.GPADAT.bit.GPIOA3=0;}
        if ((i1>=84 && i1<=916)||(i1>1000 && i1<=1250)||(i1>1750 && i1<=2000))
           {GpioDataRegs.GPADAT.bit.GPIOA3=1;}  //S4

 S5
  if (i1<=1000) {GpioDataRegs.GPADAT.bit.GPIOA4=1;}

  if (i1>1000)  {GpioDataRegs.GPADAT.bit.GPIOA4=0;}

 S6
   if ((i1>250 && i1<750 || i1>1000) && i1<1083||(i1>1916 && i1<=2000))
      {GpioDataRegs.GPADAT.bit.GPIOA5=0;}
   if((i1>=1 && i1<=250)||(i1>=750 && i1<=1000)||(i1>=1083 && i1<=1916))
           {GpioDataRegs.GPADAT.bit.GPIOA5=1;}// S6

  S7
   if (i1<1000)
      {GpioDataRegs.GPADAT.bit.GPIOA6=0;}
        if   (i1>=1000)
```

```
                {GpioDataRegs.GPADAT.bit.GPIOA6=1;}    // S7

  S8
    if ((i1<250)||(i1>750 && i1<=1000)||(i1>1083 && i1<=1916))
       {GpioDataRegs.GPADAT.bit.GPIOA7=0;}
    if ((i1>=250 && i1<=750)||(i1>1000 && i1<=1083)||(i1>1916 && i1<=2000))
           {GpioDataRegs.GPADAT.bit.GPIOA7=1;}    // S8
if (CpuTimer0.InterruptCount>=2001)
           {CpuTimer0.InterruptCount=0;

}

void Gpio_select(void)
{
        EALLOW;
        GpioMuxRegs.GPAMUX.all = 0x0000;      //        choosing PORTA Pin's AS I/O
 GpioMuxRegs.GPBMUX.all = 0x0000;   //          choosing PORTB Pin's AS I/O

   GpioMuxRegs.GPADIR.all = 0xFFFF;   // A7-A0 output
   GpioMuxRegs.GPBDIR.all = 0xFFFF;   // B7-B0 output

//   GpioDataRegs.GPADAT.bit.GPIOA13=1;
//    GpioDataRegs.GPADAT.bit.GPIOA9 =1;

   EDIS;
}
```

IV - SOURCE CODE Non-Optimization Five-Level CHB-MLI (MI=0.68)


```
#include "DSP281x_Device.h"     // DSP281x Headerfile Include File
#include "DSP281x_Examples.h"   // DSP281x Examples Include File
void Gpio_select(void);
// Prototype statements for functions found within this file.
interrupt void cpu_timer0_isr(void);


unsigned int i1, k1;

void main(void)
{

        Gpio_select();          // Setup the GPIO Multiplex Registers



interrupt void cpu_timer0_isr(void)
{
```

```
 CpuTimer0.InterruptCount++;
        i1 = CpuTimer0.InterruptCount-1;
 PieCtrlRegs.PIEACK.all = PIEACK_GROUP1;


 S1
  if (i1<=1000) {GpioDataRegs.GPBDAT.bit.GPIOB8=1;}

  if (i1>1000)  {GpioDataRegs.GPBDAT.bit.GPIOB8=0;}

 S2
if ((i1>49 && i1<952 || i1>1000) && i1<1379||(i1>1622 && i1<=2000))
      {GpioDataRegs.GPADAT.bit.GPIOA1=0;}
         if ((i1>=1 && i1<=49)||(i1>=952 && i1<=1000)||(i1>=1379 && i1<=1622))
            {GpioDataRegs.GPADAT.bit.GPIOA1=1;}

 S3
  if   (i1<=1000)
     {GpioDataRegs.GPADAT.bit.GPIOA2=0;}
        if   (i1>1000) // S3
           {GpioDataRegs.GPADAT.bit.GPIOA2=1;}

 S4
  if ((i1<49)||(i1>952 &&i1<=1000)||(i1>1380 && i1<=1622))
     {GpioDataRegs.GPADAT.bit.GPIOA3=0;}
        if ((i1>=49 && i1<=952)||(i1>1000 && i1<=1380)||(i1>1622 && i1<=2000))
           {GpioDataRegs.GPADAT.bit.GPIOA3=1;}  //S4

 S5
  if (i1<=1000) {GpioDataRegs.GPADAT.bit.GPIOA4=1;}

  if (i1>1000)  {GpioDataRegs.GPADAT.bit.GPIOA4=0;}

 S6
  if ((i1>380 && i1<622 || i1>1002) && i1<1048||(i1>1952 && i1<=2000))
     {GpioDataRegs.GPADAT.bit.GPIOA5=0;}
  if((i1>=1 && i1<=380)||(i1>=622 && i1<=1002)||(i1>=1048 && i1<=1952))
           {GpioDataRegs.GPADAT.bit.GPIOA5=1;}// S6

 S7
  if (i1<1000)
     {GpioDataRegs.GPADAT.bit.GPIOA6=0;}
        if   (i1>=1000)
                {GpioDataRegs.GPADAT.bit.GPIOA6=1;}    // S7

 S8
  if ((i1<378)||(i1>622 && i1<=1000)||(i1>1049 && i1<=1951))
     {GpioDataRegs.GPADAT.bit.GPIOA7=0;}
  if ((i1>=378 && i1<=622)||(i1>1000 && i1<=1049)||(i1>1951 && i1<=2000))
           {GpioDataRegs.GPADAT.bit.GPIOA7=1;}    // S8
```

```
        if (CpuTimer0.InterruptCount>=2001)
          {CpuTimer0.InterruptCount=0;}


}

void Gpio_select(void)
{
        EALLOW;

GpioMuxRegs.GPAMUX.all = 0x0000;      //        choosing PORTA Pin's AS I/O
   GpioMuxRegs.GPBMUX.all = 0x0000;   //        choosing PORTB Pin's AS I/O

   GpioMuxRegs.GPADIR.all = 0xFFFF;   // A7-A0 output
   GpioMuxRegs.GPBDIR.all = 0xFFFF;   // B7-B0 output

 //   GpioDataRegs.GPADAT.bit.GPIOA13=1;
//    GpioDataRegs.GPADAT.bit.GPIOA9 =1;

   EDIS;
}
```