# OPTIMIZATION AND DEVELOPMENT OF A LOW POWER MICROCONTROLLER FOR IOT APPLICATION

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*Dedicated to my beloved family members and friends, your love and support are the strength that carry me on.*

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## ABSTRACT

Internet of Things (IoT) devices are soon to be a huge enhancement of microcontroller technology. The IoT demands minimal power consumption. Being able to have right features at the right power consumption will be critical. In this work, an example of IoT device - a fall detection system with data monitoring targeting elderly people has been developed. Rather than using a general purpose microcontroller, a specific application based system has been proposed. The mechanism of the falling behaviour has been modelled by a finite state machine. Trend of changes in accelerometer has been used as the input of the system. Clock gating technique has been applied in the design in order to reduce the power consumption of the developed system. Effectiveness of clock gating technique has also been evaluated. The highest reduction in power consumption achieved is 13.26%. Moreover, RAM module is added to the design in order to lower the uploading rate of IoT transmitter. Its impact to the finite state machine is studied as well as the effectiveness with clock gating technique. The uploading rate is reduced by 96.88%. The proposed design has been implemented using Synopsys tool in 0.13um Silterra process technology. By reducing the power consumption of the IoT devices, this could greatly prolong the battery powered lifetime of a sensor node. Benchmarking with the lowest compared microcontroller, STM32L051x6 is 1357% higher power consumption than this project design.

# ABSTRAK

Internet of Things (IoT) merupakan peranti yang tidak lama lagi akan menjadi peningkatan besar teknologi mikropengawal. IoT menuntut penggunaan kuasa yang minimum. Merekaan IC yang mempunyai ciri-ciri yang dikehendaki dengan mempuyai penggunaan kuasa yang tepat akan menjadi kritikal. Dalam projek ini, satu contoh peranti IOT - sistem pengesanan jatuh dengan pemantauan data mensasarkan orang tua telah dibangunkan. Selain daripada menggunakan tujuan mikropengawal umum, sistem yang berdasarkan aplikasi khusus telah dicadangkan. Mekanisme tingkah laku yang jatuh telah dimodelkan dalam finite state machine. Trend perubahan dalam meter pecutan telah digunakan sebagai input sistem. Teknik clock gating telah digunakan dalam reka bentuk untuk mengurangkan penggunaan kuasa sistem yang direka. Keberkesanan teknik clock gating juga telah dinilai. Pengurangan tertinggi dalam penggunaan kuasa dicapai adalah 13.26%. Selain itu, modul RAM telah ditambah dalam reka bentuk untuk mengurangkan kadar muat naik IOT isyarat pemancar. Kesannya kepada finite state machine telah dikaji serta keberkesanan dengan teknik clock gating. Kadar memuat naik dikurangkan sebanyak 96.88%. Reka bentuk yang dicadangkan itu telah dilaksanakan dengan menggunakan alat-alatan Synopsys dalam teknologi proses Silterra 0.13um. Dengan mengurangkan penggunaan kuasa peranti IOT, ini akan memanjangkan jangka hayat bateri berkuasa daripada nod sensor. Penandaarasan dengan pengawal mikro rendah dibandingkan, STM32L051x6 adalah penggunaan kuasa 1357% lebih tinggi daripada reka bentuk projek ini.

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# LIST OF ABBREVIATIONS

| | |
|---|---|
| IoT | Internet of Things |
| RTL | Register Transfer Level |
| IC | Integrated Circuit |
| DC | Design Compiler |
| VCS | Verification Compiler Simulator |
| ICC | Integrated Circuit Compiler |
| SIP | Silicon Intellectual Property |

# CHAPTER 1

# INTRODUCTION

In this chapter, explanation of the details is done regarding the project *optimization and development of a low power microcontroller for IoT applications*. This chapter includes project background, problem statement, objectives, scope of project and chapter organization.

## 1.1 Project Overview

IoT is the new enhancement or application of microcontroller technology. Forecasting in the year of 2020, everything from home cities will have IoT devices installed at surroundings. Huge number of IoT devices are expected, power consumption will be the essential consideration in designing microcontroller. The main objective of this project is to achieve the power consumption of microwatts in simulation design of the microcontroller for IoT application. Clock gating technique will be implemented to reduce the power consumption of the microcontroller. The simulation design will be conducted in Synopsys platform with Verilog language and no hardware prototype will be produced. The result of this project is the design system that can achieve a low power consumption in microwatts.

## 1.2 Problem Statements

According to the prediction of Cisco Internet Business Solution Group (IBSG) that in the year of 2020, there would be a total number of 50 billion of IoT devices connected worldwide[1]. Assuming the power consumption of one device consume 1 W of power and total of 50 billion of devices will consume a total of 50 GW. Moreover,

IoT devices most likely using battery as their power source. Due to the convenient and miniature size of the IoT devices, the battery size would be small as well. Thus, the battery lifespan will be considerably short. To overcome this battery problem, a low power consumption of microcontroller is needed for IoT applications. One of solution in designing a low power consumption microcontroller is by implementing a technique called “clock gating”. This clock gating technique will reduce the power consumption of the devices. It is implemented while designing the RTL for the microcontroller embedded system.

## 1.3 Objectives

There are five objectives which need to be focused in this project and achieved at the end of it.

i. To develop a low power microcontroller specifically for IoT applications
ii. To optimize the power consumption of the microcontroller using Synopsys tool and clock gating technique
iii. To achieve a low power microcontroller embedded system design for IoT application.

## 1.4 Scope of Project

SIP also known as the Silicon Intellectual Property that is designed and developed by other sources. It will be the functional block used in this embedded system design project and optimize its interconnections. A low power embedded system design of IoT application will include a processor, SRAM, buses and interfaces. The result of this embedded system design will optimize the power consumption by using clock gating technique. The embedded system will be designed in Synopsys tools using Hardware Description Language (HDL), Verilog.

## 1.5 Chapter Organization

This thesis comprises of seven chapters:

Chapter 1 is explaining the introduction of the project. This comprises project background, objectives, problem statement, scopes of project, and chapter organization.

Chapter 2 is explaining the theory that is related to this project, AMBA, I2C, and clock gating technique.

Chapter 3 is the illustration of process flow of this project in detail explanation. This also includes the tools of Synopsys software that are used in this project.

Chapter 4 is the development process of finite state machine. It explain the model structure, flow chart and all development stages using VCS, DC and ICC tools.

Chapter 5 discuss about the power optimization clock gating technique. The effectiveness of the technique is analysed.

Chapter 6 is to study the impact of RAM module when added to the finite state machine. The effectiveness of clock gating technique to the RAM module is also discussed.

# CHAPTER 2

# LITERATURE REVIEW

In this chapter, books, journals, and article are being discussed in relation to this project. Advanced Microcontroller Bus Architecture (AMBA), I2C bus and clock gating technique are discussed in related to the project of developing low power microcontroller for IoT application.

## 2.1 AMBA

Advanced microcontroller bus architecture in short AMBA for ARM. AMBA define the specification for on-chip communication standard[2]. All embedded system design must be designed according to the AMBA standard.

AMBA ver 2.0 consists of three different buses:

i. Advanced High-performance Bus (AHB)
ii. Advanced System Bus (ASB)
iii. Advanced Peripheral Bus (APB)

AMBA ver 3.0 has only one type of protocol, AMBA Advanced eXtensible Interface (AXI)[3].

### 2.1.1 Terminology

The terms that describe the operation of Bus:

i. Bus cycle – it is a unit that represent one bus clock period. AHB and APB define bus clock period start from a rising edge to rising edge transitions. ASB define different which is from falling edge to falling edge transition.
ii. Bus transfer – it can be either a read or write operation of a data object. AHB and ASB may require one or more bus cycle and terminated by a completion command from the addressed slave. But APB always requires two bus cycle for a bus transfer operation.
iii. Burst operation – it is define as one or more data transaction been initiated by the bus master that consist of equal width of transaction to the increase of the address space region. But this burst operation only apply for AHB and ASB, not APB.

### 2.1.2 Advanced High-performance Bus (AHB)

AMBA AHB are design in to support high performance and high clock frequency. AHB do comes with some features:

i. Burst transfers
ii. Split transactions
iii. Single-cycle bus master handover
iv. Single-clock edge operation
v. Non-tristate implementation
vi. Wider data bus configurations (64/128 bits)

Most commonly applications of AHB is direct memory access (DMA) and digital signal processing (DSP).

AMBA AHB system design contains four components:

i. AHB master – the bus master that initiate read and write operation by issuing the address information and command.