ENERGY SCAVENGING FOR MOBILE AND WIRELESS DEVICES USING CMOS RECTIFIER CIRCUIT

TAN CHONG WEI

This Report Is Submitted In Partial Fulfilment of Requirements For The Bachelor Degree of Electronic Engineering (Telecommunication Electronic) with Honours

Faculty of Electronics and Computer Engineering
Universiti Teknikal Malaysia Melaka

June 2017

UNIVERSTI TEKNIKAL MALAYSIA MELAKA
FAKULTI KEJURUTERAAN ELEKTRONIK DAN KEJURUTERAAN KOMPUTER

BORANG PENGESAHAN STATUS LAPORAN
PROJEK SARJANA MUDA II

Tajuk Projek : ENERGY SCAVENGING FOR MOBILE AND WIRELESS DEVICES USING CMOS RECTIFIER CIRCUIT

Sesi Pengajian : 1 6 / 1 7

Saya TAN CHONG WEI

mengaku membenarkan Laporan Projek Sarjana Muda ini disimpan di Perpustakaan dengan syarat-syarat kegunaan seperti berikut:

1. Laporan adalah hakmilik Universiti Teknikal Malaysia Melaka.
2. Perpustakaan dibenarkan membuat salinan untuk tujuan pengajian sahaja.
3. Perpustakaan dibenarkan membuat salinan laporan ini sebagai bahan pertukaran antara institusi pengajian tinggi.
4. Sila tandakan (√) :

☐	**SULIT***	*(Mengandungi maklumat yang berdarjah keselamatan atau kepentingan Malaysia seperti yang termaktub di dalam AKTA RAHSIA RASMI 1972)
☐	**TERHAD****	**(Mengandungi maklumat terhad yang telah ditentukan oleh organisasi/badan di mana penyelidikan dijalankan)
☑	**TIDAK TERHAD**	

Disahkan oleh:

(TANDATANGAN PENULIS)

Tarikh: 01/06/2017

(COP DAN TANDATANGAN PENYELIA)

Tarikh: 01/06/2017

Dr. WONG YAN CHIEW
Pensyarah Kanan
Fakulti Kejuruteraan Elektronik & Kejuruteraan Komputer
Universiti Teknikal Malaysia Melaka (UTeM)
Hang Tuah Jaya
76100 Durian Tunggal, Melaka

"I admit that this report is the result of my own work except summaries and excerpts that each of them I have explained the source."

Signature : 

Student's Name : TAN CHONG WEI

Date : 2nd JUNE 2017

"I / we hereby declare that I have read this in my / our work is sufficient in scope and quality for the award of the Bachelor in Electronic Engineering (Telecommunication Electronic) with Honours."

Signature : 

Supervisor's Name : DR. WONG YAN CHIEW

Date : 2nd JUNE 2017

For my father and mother.

ACNOWLEDGEMENT

First and foremost, I would like to thanks all the lectures in University Teknikal Malaysia Melaka and Faculty of Electronic and Computer Engineering who have teach, instruct, train and educate me. Without them, I would never accomplish this work.

I would like to express my deepest gratitude to my project supervisor Dr Wong Yan Chiew for her generous guidance. Dr Wong is kind and responsible that she has always ensured my progress is done correctly. With her advice and help, the project could conduct successfully. Beside I would also like to thank Dr Wong for giving me an opportunity to conduct this project. Through this project, I have enhanced my knowledge and experience.

Special thanks to Miss Bee Shei Er and Mr. Chan Lisen. They have spent time with me to discuss about the energy scavenging system topics. They are willing to share their knowledge on related topic. I am much appreciated with the good relationship with them and all the collaboration has been built up.

Besides, another thank I would like to give to them who have evaluate my work. I appreciate all the suggestion they have provided. Moreover, I would like to thanks Mr Sreedharan Baskara Dass who has provided a technical support on my project. In addition, I would like to thank my classmate who has helped me directly and indirectly.

Last but not least, I express the most wholehearted gratitude to my family. Thanks to their spiritual support and encouragement. They have motivated me whenever I was tired or depressed.

ABSTRACT

The world is surrounded with billions of radio devices, therefore RF energy is easy available from the ambient environment. The RF energy scavenging system can be realised by converting the RF source to stable DC output where this could be done by a rectifier. However, most of the rectifier only able to achieve low power conversion efficiency due to high threshold voltage drops and low input sensitivity. In this project, a CMOS rectifier is designed in 130nm technology. It is designed for high sensitivity at input power of -20dBm and operating in 2.45 GHz. This project covered complete flow of IC design with Cadence Virtuoso custom design tools from schematic to layout. In the schematic design a cross-coupled rectifier has been designed. This topology has been proved that have reduce the threshold voltage to approximately 50% as compared to the conventional rectifier. The rectifier is cascaded into 5 stages so that to increase the output voltage to a usable level. Supporting circuit such as matching circuit has been constructed for the rectifier.so that it could receive RF energy from a RF port. Several parametric studies have been carried in this project, the parameter such as matching circuit component, transistor size and load resistor has been defined. These parameters provide the optimum performance of the rectifier. To ensure the rectifier could work properly, numerous simulation and data analysis is performed in this project. Transient response of the rectifier have been plotted, the rectifier shows a linear and stable output voltage and current. Next, the load capability of the rectifier has been determine by sourcing the current from the rectifier. The rectifier could draw out 1µA current at -10dBm input. The output current increased to 10µA as the input power increased to 0dBm. After that, a steady state analysis have been carried out to determine the steady state output voltage and output current. The rectifier have achieved output voltage at 1.742V and output current at 1.34µA. Besides, the rectifier has also achieved high power conversion efficiency at 68.26% at -20dBm. It has also achieved a high voltage gain at 88.91 at -20dBm too. Furthermore, the layout of the rectifier have been constructed, physical verification have been carried out.

ABSTRAK

Dunia ini dikelilingi dengan berbilion-bilion peranti radio, oleh itu tenaga RF mudah didapati daripada suasana persekitaran. Sistem mengumpul tenaga RF boleh dibina dengan menukar sumber RF kepada isyarat elektrik DC yang stabil. Ini boleh dilakukan oleh penerus. Walau bagaimanapun, kebanyakan penerus hanya mampu mencapai kecekapan penukaran kuasa yang rendah disebab oleh kejatuhan voltan ambang yang tinggi dan sensitiviti input yang rendah. Dalam projek ini, penerus CMOS dibina dengan teknologi 130nm. Ia direka untuk kepekaan yang tinggi pada kuasa input -20dBm dan beroperasi di 2.45 GHz. Projek ini termasuk reka bentuk IC yang lengkap dengan Cadence Virtuoso, bermula daripada skematik hingga susun atur IC. Dalam reka bentuk skematik penerus 'cross-coupled' telah direka. Topologi ini telah dibuktikan bahawa dapat mengurangkan voltan ambang kepada lebih kurang 50% berbanding kepada penerus konvensional. Penerus ini disebarkan kepada 5 peringkat supaya untuk meningkatkan voltan output ke tahap yang boleh digunakan. Litar sokongan seperti pemadanan galangan telah dibina untuk penerus. Oleh itu, ia boleh menerima tenaga RF dari port RF. Beberapa kajian parametrik telah dijalankan dalam projek ini, parameter seperti komponen pemadanan galangan, saiz transistor dan rintangan beban telah ditakrifkan. Parameter ini memberikan prestasi optimum penerus. Untuk memastikan penerus boleh berfungsi dengan baik, banyak simulasi dan analisis data dilakukan dalam projek ini. Sambutan fana penerus telah diplotkan, penerus menunjukkan voltan dan arus output adalah linear dan stabil. Seterusnya, keupayaan beban penerus telah ditakrifkan dengan mendapatkan arus daripada penerus. Penerus dapat menarik arus 1μA pada input -10dBm. Output arus meningkat kepada 10μA apabila kuasa input meningkat kepada 0dBm. Selepas itu, analisis 'periodic steady state' telah dijalankan untuk menentukan voltan output stabil dan arus output stabil. Penerus telah mencapai voltan keluaran di 1.742V dan arus output di 1.34μA. Selain itu, penerus juga telah mencapai kuasa tinggi kecekapan penukaran pada 68.26% pada -20dBm. Ia juga telah mencapai gandaan voltan yang tinggi pada 88.91 di -20dBm juga. Tambahan pula, susun atur penerus telah dibina, pengesahan fizikal telah dijalankan.

TABLE OF CONTENTS

LIST OF FIGURE

LIST OF TABLE

LIST OF ABBREVATIONS

RF	-	Radio Frequency
AC	-	Alternative Current
DC	-	Direct Current
IC	-	Integrated Circuit
LDO	-	Low-dropout regulator
CMOS	-	Complementary Metal-Oxide Semiconductor
MOSFET	-	Metal–oxide–semiconductor Field-effect Transistor
NMOS	-	N-type MOSFET
PMOS	-	P-type MOSFET
DRC	-	Design Rule Check
LVS	-	Layout Versus Schematic
PEX	-	Parasitic Extraction
PCE	-	Power Conversion Efficiency
SVC	-	Self Vth Cancellation
DTMOS	-	Dynamic Threshold-voltage MOSFET
LAN	-	Local Area Network
GSM	-	Global System for Mobile communication

CHAPTER 1

INTRODUCTION

1.1. Project Overview

RF energy has become one of the very common man-made energy source due to the highly usage of radio sources device such as mobile phones, television, WIFI devices etc. At the same time, the demand for battery free application like wireless sensor-based network is growing up. Compared to a self-powered system, a battery's life span is limited to a system. This could be a challenge to achieve the fast grows in the integrated circuit technology as described by Moore's law. Therefore, RF energy harvesting has become dominant to substitute a battery as the RF energy source is cheap and easy available. RF energy can be harvest with energy scavenging circuit. The circuit could extract the electrical energy from the ambient RF energy source and convert it into a stable DC voltage. One of the important blocks in the RF energy harvesting circuit is the rectifier circuit.

RF energy that could receive form the environment is usually low. It can be even worse when most of the mobile and wireless devices could receive RF signal with small gain antenna only. It could be a challenge for RF energy scavenging system to achieve high power conversion efficiency especially the threshold voltage of transistors in the rectifier circuit cause a major voltage drop. To solve the problem, a threshold cancellation method could be applied in the rectifier design. The threshold cancellation methods include bulk modulation technique and cross coupler rectifier topology. In addition a comparator based and control circuit based design can be applied in the rectifier to speed up the ON-OFF transition of transistor to prevent the reverse leakage current of transistor.

In this project, a CMOS rectifier will be implemented from schematic entry to simulation and the layout drawing with verification. The design of the rectifier will focus on the threshold cancellation and power conversion efficiency of the CMOS rectifier.

1.2. Problem Statement

As the emerging of Internet of things in the future, there will be billions of sensors, mobile devices and wireless devices would be needed to power up. However to power up those devices with battery is impractical. Therefore a RF energy scavenging system can be used as substitution for battery and provide power to the mobile and wireless devices. A CMOS rectifier is one of the important parts in the RF energy scavenging system which convert RF energy to stable DC supply.

To design a CMOS rectifier, the power conversion efficiency is the main consideration. The factor that affects the efficiency of the rectifier is the threshold voltage of diode. The RF energy that received by an antenna from the surrounding could only achieved in a low voltage. High threshold voltage cause major voltage drop, hence achieve low power conversion efficiency. The case can be even worse, if the rectifier is cascaded in multiple stage, the total threshold voltage drop could be higher. Zero V_{th} MOS or Schottky diode which have low threshold could use to solve the problem. However, Zero V_{th} MOS could result in high reverse leakage current while Schottky diodes are not supported in all CMOS technologies. Therefore a threshold cancellation technique needs to be proposed.

Although, there are several threshold voltage reduction techniques has been proposed by many researchers. However most of the topologies are facing a same problem, power conversion efficiency degraded due to reverse leakage current of transistor. Reverse leakage current could introduce during the non-switching state of a transistor. One of the factors that cause the reverse leakage current is the ON OFF transition of the rectifier is not fast enough this could cause a major power loss. Therefore a control technique need to be introduce to control the transition speed of the transistor in order to improve the forward current and eliminate the reverse leakage current.

1.3. Objective

The objectives of this project are:

- To identify the key parameters in CMOS rectifier
- To design a CMOS rectifier circuit with low threshold voltage
- To improve the power conversion efficiency of CMOS rectifier that could be applied on the RF harvesting circuit
- To verify the proposed methodology theoretically and analytically through modelling

1.4. Scope of Project

In this project, the CMOS rectifier would be done in 130nm CMOS technology. Schematic and layout of the CMOS rectifier would be designed and simulated in the Synopsys IC design software. The input signal for the CMOS rectifier would be 2.45GHz. It would able to be operating at input power as low as -20dBm. The input RF signal will be converted into higher DC voltage. The threshold voltage of the CMOS rectifier would be eliminated effectively and the CMOS rectifier would have better improvement on the power conversion efficiency as compared to conventional rectifier. In the end the output voltage rectifier should achieve a level that may be filtered by regulator in the energy scavenging system and finally usable for mobile and wireless devices.

1.5. Project Development

First and foremost, to design a CMOS rectifier, a research on previously proposed rectifier design has to be carried out. The fundamental theory of CMOS rectifier design and the existing topologies would be studied. Next, the specifications of the rectifier will be define, the specification are such as input power, input signal frequency, load resistor, W/L ratio and so on. After that, the design of the rectifier will be started with schematic design with Cadence Vituoso IC design software. The architecture of the circuit will be concern on the threshold voltage reduction. Besides, the schematic will be simulate to make sure the circuit is well functioning. Once the schematic have been finalized, the project will be continued with layout drawing. Design rule check (DRC), Layout Versus Schematic (LVS) and Parasitic Extraction (PEX) will be performed to ensure that the simulation result of layout is similar the schematic design.

1.6. Report Outline

Five chapters are written in this thesis. The information gathered from the research and investigation is presented in this thesis. Each description and detail for each chapter is explains below:

Chapter 1 – Introduction

This is the most important part in this thesis. In this chapter, general ideal of the CMOS rectifier design have been descripted. The aims of the project have been stated and the boundaries of this work have been discussed.

Chapter 2 – Literature Review

In this chapter, a generic knowledge of CMOS rectifier design and previous research of CMOS rectifier have been studied. The generic knowledge includes the conceptual framework and applies theory of CMOS rectifier. The conceptual framework is such as brief concept of RF energy scavenging. While applies theory are such as rectifier, voltage multiplier, power convention efficiency and characteristic of MOSFET. Besides, the previous researches on CMOS rectifier are focus on the threshold cancellation technique. The specification and validity of previous researches are discussed. The previous researches that have studied can be categories into three parts which are Bulk Modulation Technique, Cross Coupler Rectifier and Comparator Based & Control Circuit Based Rectifier.

Chapter 3 – Methodology

This chapter will provides detailed method and procedures of designing the CMOS rectifier. A flow chart of the CMOS rectifier design and development is shown. The design specifications are stated precisely in this chapter. The steps involved in the CMOS rectifier design include schematic design, design simulation, layout design, layout validation and post-simulation.

Chapter 4 – Rectifier Architecture

This chapter describes the general concept of the rectifier design. Several part in the schematic have been explained, such as threshold reduction by cross coupled technique, reverse current prevention by bulk terminal connection, voltage doubled by charging capacitor and voltage smoothing by smoothing capacitor. Beside, multiple stages cross-

coupled rectifier is introduced in this chapter too. Next, the supporting circuit for the rectifier is explained block by block. The blocks which included in the supporting circuit are the RF port, balun, L-matching circuit, rectifier and the output port.

Chapter 5 – Design Parameters

There is several parameter need to be defined in order to maximize the performance of the rectifier. In this chapter, the value of the capacitor and inductor in L-matching circuit is determined by s-parameter analysis. Next, the width and length of PMOS and NMOS are identified by parametric study. Beside, another parametric study is carried for load resistor.

Chapter 6 – Result and Analysis

This chapter is one of the important parts of this thesis. It describes the performance of the rectifier. The analysis that have been performed in this chapter including the transient response, load current analysis, steady state output voltage and current, power conversion efficiency and voltage gain. The transient response shows the output achieved at a stable DC. The load current analysis is to test the load capability of the transistor. Moreover, the steady state output voltage and current shows the maximum output voltage and the output current that the rectifier could achieve. In addition, the power conversion efficiency and voltage gain represent how much power the rectifier can conserve and how sensitive the rectifier could receive input power.

Chapter 7 – Conclusion and Recommendation

This is the last section of this thesis, it has presented a true reflection of the work. The finding and analysis for general project are concluded. The objectives of the project are sum up. The future development and implementation are suggested.

CHAPTER 2

LITERATURE REVIEW

2.1. Overview

This chapter includes the background theory to design a CMOS rectifier. First of all, a brief concept of RF Energy Scavenging is introduced. Next the basic concept of rectifier, voltage multiplier and power conversion efficiency are discussed. Furthermore, the generic concepts of MOSFET such as MOSFET structure, threshold voltage, I-V characteristics and body effect have been review. Besides, the previous researches of CMOS rectifier have been studied. These researches are focus on the threshold voltage cancelation technique such as Bulk modulation technique, cross-coupler rectifier and Comparator Based & Control Circuit Based Rectifier. Their specifications, operation, background theory and findings are described. Results of several topologies are compared.

2.2. RF Energy Scavenging

Energy scavenging is a process to collect certain form of energy such as solar energy, kinetic energy and RF energy and convert the energy in electrical energy. RF energy have becomes common energy source due to tremendous number of radio broadcasting. RF energy can be collected from ambient by receiving it with an antenna. RF energy can be broadcasted in several bands such as 900MHz, 1800MHz and 2.4GHz. Figure 2.1 shows a block diagram of RF Energy Scavenging system.

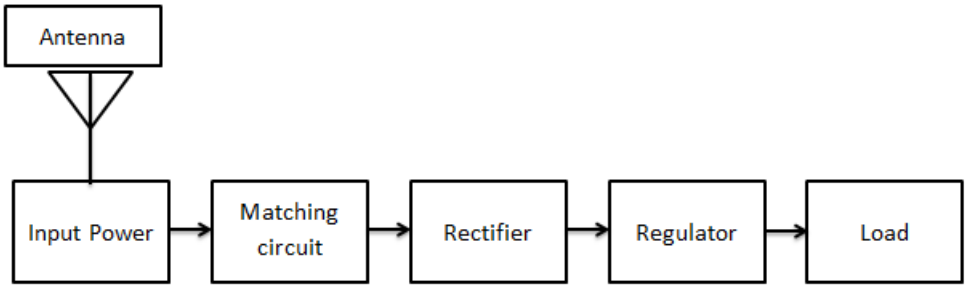


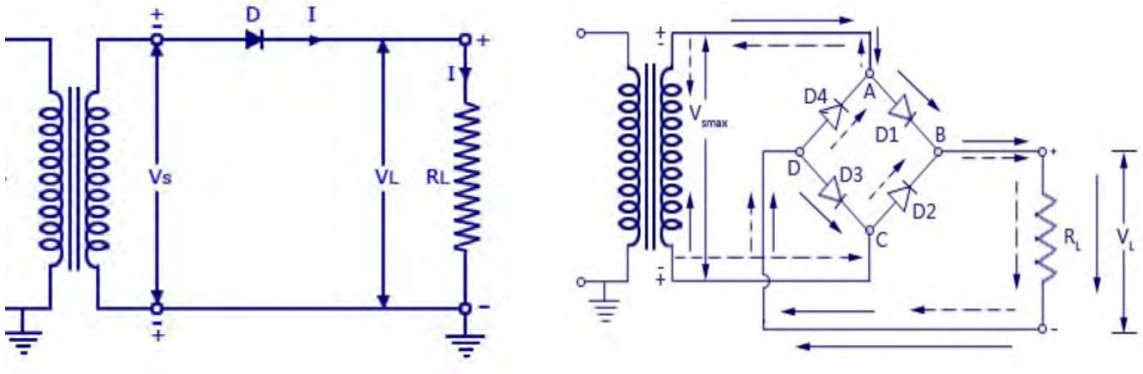
Figure 2.1 RF energy scavenging system

The antenna is use to receive the RF energy from the surrounding. The received RF energy is usually low. It could even lower if RF energy is received by a small gain antenna which is commonly used by mobile device. The received RF energy becomes the input power for the rectifier. Before the rectifier, a matching circuit is used to decrease the reflected power from the source into the rectifier circuit and this could prevent energy loss in the circuit. Next, the function of the rectifier circuit is to convert the RF input signal into stable DC signal. A regulator is use to provide a smooth and stable linear DC signal. A Low-dropout regulator (LDO) can be a suitable component in this part. LDO could regulate the output voltage to a useful level in order to address the power needs for applications. Lastly, the regulator connected to the load of related application, the destination where the power wants to deliver.

2.3. Rectifier

A rectifier is use to convert a signal from ac to dc, or usually convert a zero average value signal into a nonzero average signal. Diode is usually used to construct rectifier such as half-wave rectifier and full-wave rectifier. To receive low power RF energy, a Schottky Diode with low forward voltage drop can be used to perform RF-DC conversion. N-MOSFET and P-MOSFET can used to replace diode, especially the Schottky diode do not be supported in CMOS technology

The half wave rectifier makes use of only one half cycle of the input alternating current while a full wave rectifier is more efficient than a half wave rectifier. Figure 2.2 shows half wave rectifier and full wave rectifier



(a) (b)

Figure 2.2 (a) Half wave rectifier (b) Full wave rectifier

There are only 1 diode will be use to design a half- wave rectifier while full wave rectifier require 4 diodes. The only diode of half wave rectifier will turn 'on' during positive half cycle of signal and turn 'off' during the other cycle. For full wave rectifier, during any half cycle of the signal, two diodes will be turn 'on' while the other two will be turn 'off'.

In fact, there would be a forward voltage or threshold voltage drop for every forward bias diode. This would cause a major drop on dc level. It will perform very bad power convention efficiency especially for a low input power. Besides, the power convention efficiency is affected by the reverse leakage current too. High reverse leakage current means a high power lost.

There are two main reasons that cause the undesired reverse leakage current. Reverse leakage current occur most the time when the diode or MOSFET do not turn 'off' fast enough, current will flow in opposite direction during the transition of the state. Another reason that causes the reverse leakage current is the low threshold voltage of diode or MOSFET. Because of threshold voltage, it could efficiently block the current during the reverse bias. That is the reason for zero-Vth diode is not suitable to be used in the design of rectifier. However, as mention before high threshold voltage decrease the power conversion efficiency of the rectifier.

There are several CMOS rectifier have been proposed[1]–[9] . These rectifiers are proposed for RFID, Body Area Network and RF harvesting.

2.4. Voltage multiplier

Voltage multiplier is similar to the rectifier but it could convert the AC from low voltage to higher DC voltage. The voltage multiplier circuit consists of two important components, capacitor and diode. Figure 2.3 shows a simple construction of a voltage multiplier.

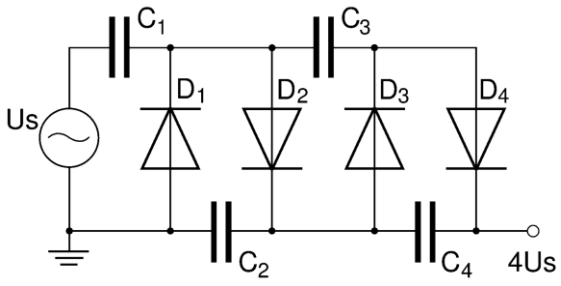


Figure 2.3 Voltage multiplier

The capacitors are act as energy-storage element while the diode is use to control the connection of voltage to the capacitor. In the first cycle of the signal, a capacitor C1 is connected to the supply would charge to that same voltage. In the second cycle, C2 will be charge to double of supply voltage. So as next following cycle, C3 and C4 will be charge to double of supply voltage too. The sum of voltages under C2 and C4 rise to 4 times of supply voltage. The voltage can be further increased by adding more capacitor and diode.

2.5. Power Conversion Efficiency (PCE)

Power conversion efficiency or PCE is a measure of the performance of a power conversion circuit such as RF to DC conversion. High PCE represent low power loss in the system. There are several reasons that could the power loss, such as thermal loss, mismatch load and leakage current. The PCE could be calculated as the ratio of delivered power to the load and the input power. The PCE, $\eta$is given that equation (2.1)

$$\eta = \frac{P_{load}}{P_{in}} \tag{2.1}$$

PCE is a quantitatively unitless value. For a rectifier, its performance can be defined by PCE too. The output power is calculated by measuring the average output dc voltage and dividing the square of this value by the load resistor. To achieve high PCE in a