



**DESIGN FOR IMPROVEMENT OF METROLOGY AND INSPECTION
OF INTEGRATED CIRCUIT FOR ACCURACY CHECK USING
SMARTSCOPE APPLICATION**

This report submitted in accordance with requirement of the University Teknikal
Malaysia Melaka (UTeM) for Bachelor Degree of Manufacturing Engineering
(Engineering Design)(Hons.)

by

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2017

DECLARATION

I hereby, declared this report entitled “Design for Improvement of Metrology and Inspection of Integrated Circuit for Accuracy Check Using Smartscope Application” is the results of my own research except as cited in reference.

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APPROVAL

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SESI PENGAJIAN: 2016/17 Semester 2

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ABSTRAK

Tujuan projek sarjana muda ini adalah untuk mereka bentuk lekapan semakan pemeriksaan yang boleh digunakan dalam proses ketepatan semakan. Lekapan ini direka sebagai bantuan dalam menjalankan mod automatik dalam proses ketepatan semakan. Dalam peringkat mereka bentuk konsep, terdapat beberapa konsep reka bentuk yang telah dicadangkan dan dihasilkan yang mesti mengikut kekangan reka bentuk yang telah ditetapkan. Kemudian, semua konsep reka bentuk menjalani kaedah Pugh untuk pemilihan konsep yang terbaik. Pemilihan dilakukan berdasarkan 10 kriteria yang ditetapkan untuk memenuhi keperluan pelanggan. Konsep reka bentuk terbaik adalah Konsep Reka Bentuk 1 (CD-1) yang memperoleh skor tertinggi sebanyak 5. Konsep tersebut kemudiannya menjalani pembangunan selanjutnya dengan analisis Failure Mode Effect Analysis (FMEA). Analisis ini telah menambahbaik konsep reka bentuk berdasarkan mod pontensi kegagalan yang dikesan. Selepas itu, konsep reka bentuk akhir dihasilkan. Reka bentuk itu kemudiannya dihantar untuk proses fabrikasi menggunakan kaedah percetakan 3D. Selepas prototaip difabrikasi, prototaip dibawa untuk pengesahan reka bentuk untuk mengesahkan fungsi prototaip. Fasa ini dijalankan menggunakan aplikasi SmartScope dimana proses ketepatan semakan dilakukan. Keputusan yang dihasilkan daripada proses ini membuktikan dan mengesahkan bahawa reka bentuk yang dihasilkan adalah berjaya.

ABSTRACT

The aim of this project is to design an inspection checking fixture that can be used in accuracy check process. The fixture is designed as an aid in conducting automatic mode of the process. In conceptual design stage, there are several proposed conceptual designs are generated which must follow design constraints that are set. Then, all of the conceptual designs underwent Pugh's Method for concept selection to come out with the best conceptual design. The selection is done based on 10 criteria that are set to meet customer's requirement. The best conceptual design goes to Conceptual Design 1 (CD-1) that obtained highest score of 5. The design underwent further development with Failure Mode Effects Analysis (FMEA). The analysis has improved the design based on potential failure mode that are detected. After that, the final design is generated. The design is then sent for fabrication process using 3D printing method. After the prototype is fabricated, the prototype went of design validation to verify the functionality of the prototype. This phase is conducted using SmartScope application which the real accuracy check process is performed. The results generated from this process proved the design is validated.

DEDICATION

This report is dedicated to my strong father, Alias bin Mamat
my late mother, Zainon Binti Husin
my brothers and sisters, Deen, Jaja, Amir, Azila and Hafiz
and my other loved ones and friends
for giving me continuous motivation, financial support, cooperation and understandings
Thank you all!

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LIST OF ABBREVIATIONS

CAD	-	Computer Aided Design
CATIA	-	Computer Aide Three-dimensional Interactive Application
CMM	-	Coordinate Measuring Machines
CNC	-	Computer Numerical Control
CD	-	Conceptual Design
FEA	-	Finite Element Analysis
FMEA	-	Failure Mode and Effects Analysis
IC	-	Integrated Circuit
IT	-	Information Technology
LED	-	Light-emitting Diode
MJP	-	Multi-Jet Printing
OGP	-	Optical Gaging Products
PM	-	Pugh Matrix
QVI	-	Quality Vision International
SOIC	-	Small Outline Integrated Circuit
TTL	-	Through the Lens

CHAPTER 1

INTRODUCTION

This chapter provides brief ideas about the research study of the project, which is divided into four major sections; background, problem statement, objectives and scope of the project.

1.1 Background

Semiconductor industry plays an important role in digital globalization era nowadays; the era which everything is at one's fingertips. This industry is facing many challenges to be confronted include reducing cost of designing and manufacturing Integrated Circuit (IC) without downgrading its quality, meeting production deadlines, minimizing time-to-market and time-to-volume, and maximizing profitability. Industry revolution has made electronic devices become essential in easing one's daily routine. High quality of ICs in these electronic devices are very crucial for the devices to be functional maximally. The failure of these ICs can lead to many fatalities especially when it involves automotive components. However, the high demand from the market forces this industry to massively produce the ICs which might affect its quality.

There are many methods used to control and maintain the quality of these ICs. Numerous inspection machines are invented to check and make sure the quality of the ICs meet the requirements. One of the machines are coordinate measuring machine (CMM) which a device for measuring the physical geometrical characteristics of any objects. For example, Optical Gaging Products (OGP), one of the world's leading multi-sensor metrology solutions provider, has created SmartScope Flash Systems which are high-accuracy metrology systems designed to measure any objects in automatic mode with a high quality, 12:1 zoom lens. These systems helps manufacturers across the world to improve the quality of their products in term of its metrology.

Results obtain from these systems are then used as references for inspection machine in the company by altering the machine settings to attain nearly similar results as the SmartScope Flash Systems. The process of checking metrology of the ICs is called accuracy check. Figure 1.1 shows the desired dimensions for accuracy check process. Therefore, the results from this process have to be very accurate as it might affect the machine performance.

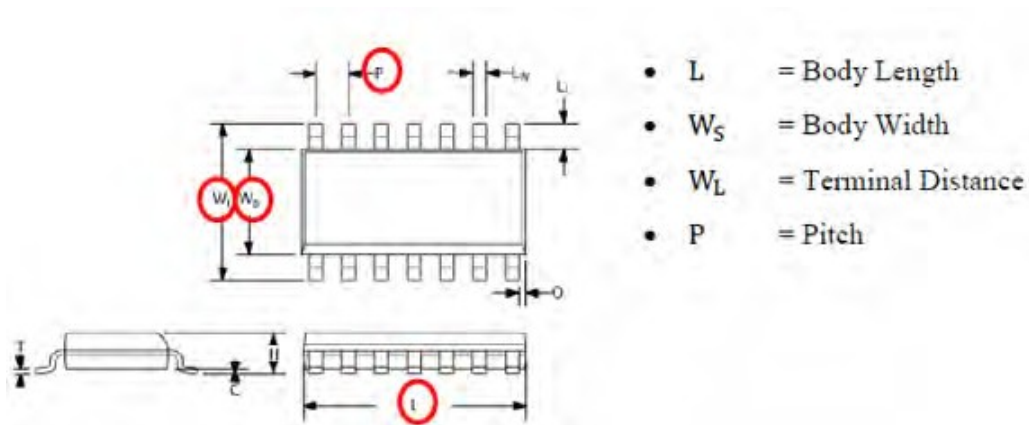


Figure 1.1: Dimensions for accuracy check process (Wikipedia, 2006)

Problem Statement

SmartScope Flash Systems is used to carry out accuracy check process by taking several IC samples from customers and measuring the desired dimensions of the ICs. In order to obtain most accurate results which will be used as reference by inspection machines, the orientation of ICs on the SmartScope must be in a correct position. However, current process of Accuracy Check is carried out manually which the ICs are placed on the SmartScope without any tooling aids to hold the ICs. This might cause misalignment of the ICs that will affect the reading of its dimensions.

The results from SmartScope will be compared with machine results. The fail results which both results from SmartScope and machine (NV Core software) are out of tolerance, will have to be rechecked and recalculated its dimensions again under SmartScope. The new readings might vary from the recent ones. This variation of results is now a problem to this process. Table 1.1 shows the comparison of both results with a tolerance of $\pm 20 \mu\text{m}$ and

correlation offset of -0.030 for minimum and maximum terminal distance, T_D of 20 Small Outline Integrated Circuit (SOIC) samples. The full result is attached in Appendices.

Table 1.1: Comparison of results from SmartScope and NV Core (Cohu Inc. 2016)

TD Min/Max	(+/- 20um / 0.020mm)			Correlation Offset TD Min			Correlation Offset TD Max: -0.030								
Comp	1			2			3			4			5		
	NVCore	Scope	Diff	NVCore	Scope	Diff	NVCore	Scope	Diff	NVCore	Scope	Diff	NVCore	Scope	Diff
TD Min	6.049	6.003	-0.046	6.028	6.008	-0.020	6.004	6.014	0.010	6.008	5.985	-0.023	6.011	6.011	0.000
TD Max	6.071	6.070	-0.001	6.053	6.054	0.001	6.023	6.025	0.002	6.045	6.055	0.010	6.036	6.026	-0.010
Comp	6			7			8			9			10		
	NVCore	Scope	Diff	NVCore	Scope	Diff	NVCore	Scope	Diff	NVCore	Scope	Diff	NVCore	Scope	Diff
TD Min	6.010	5.995	-0.015	6.008	5.998	-0.010	6.008	6.015	0.007	6.009	6.008	-0.001	6.009	6.008	-0.001
TD Max	6.034	6.051	0.017	6.024	6.035	0.011	6.039	6.026	-0.013	6.044	6.051	0.007	6.073	6.053	-0.020
Comp	11			12			13			14			15		
	NVCore	Scope	Diff	NVCore	Scope	Diff	NVCore	Scope	Diff	NVCore	Scope	Diff	NVCore	Scope	Diff
TD Min	6.011	6.008	-0.003	5.990	6.005	0.015	5.997	6.012	0.015	6.019	6.017	-0.002	6.020	6.027	0.007
TD Max	6.036	6.037	0.001	6.018	6.024	0.006	6.036	6.033	-0.003	6.048	6.044	-0.004	6.091	6.089	-0.002
Comp	16			17			18			19			20		
	NVCore	Scope	Diff	NVCore	Scope	Diff	NVCore	Scope	Diff	NVCore	Scope	Diff	NVCore	Scope	Diff
TD Min	6.017	6.005	-0.012	6.019	6.017	-0.002	5.979	5.980	0.001	6.017	6.015	-0.002	6.007	6.010	0.003
TD Max	6.028	6.025	-0.003	6.035	6.031	-0.004	6.004	6.005	0.001	6.041	6.024	-0.017	6.019	6.015	-0.004

Legend:
 Component missing
 Pass measurement
 Fail measurement

As the process of taking dimensions of SOIC is done manually, person-in-charge of this process has to readjust the orientation of the component using a holder, as SOIC is very small and sensitive, so that it fits perfectly inside the grid in SmartScope software called MeasureMind as shown in Figure 1.2. This manual handling process must be carried out carefully to avoid any damages happen to the components which might change the dimensions of component leads. Therefore, this tedious work consumes a lot of time which one component takes approximately about one hour to finish taking all the dimensions. Besides that, the productivity of the person-in-charge also decreases as the person has to spend a week to completely finish 40 samples in one project. If the components are missed while undergoing inspection in the machine, the person-in-charge has to take new samples and carry out accuracy check on the new samples.

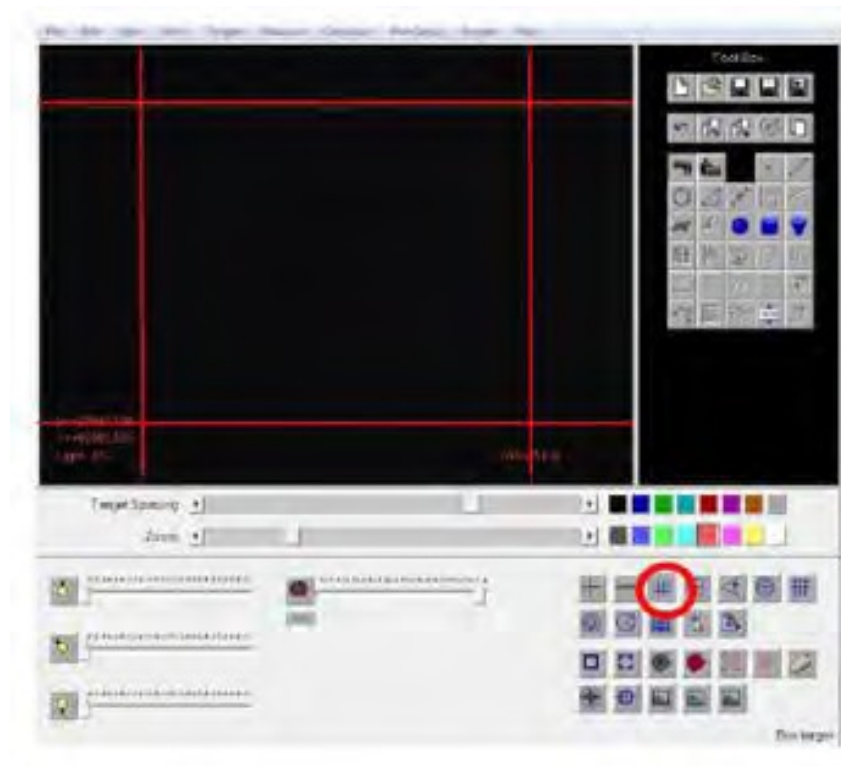


Figure 1.2: Grid feature in MeasureMind software (Cohu Inc., 2016)